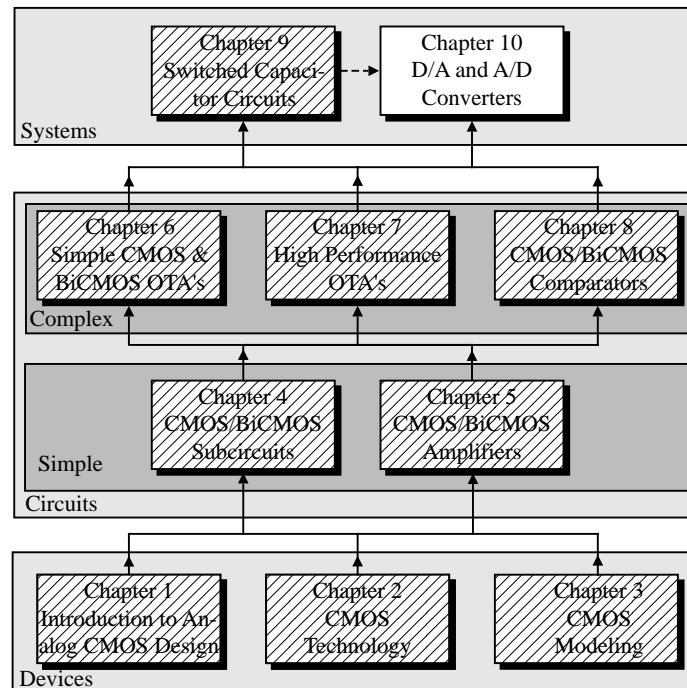


CHAPTER 10 – DIGITAL-ANALOG AND ANALOG-DIGITAL CONVERTERS

INTRODUCTION

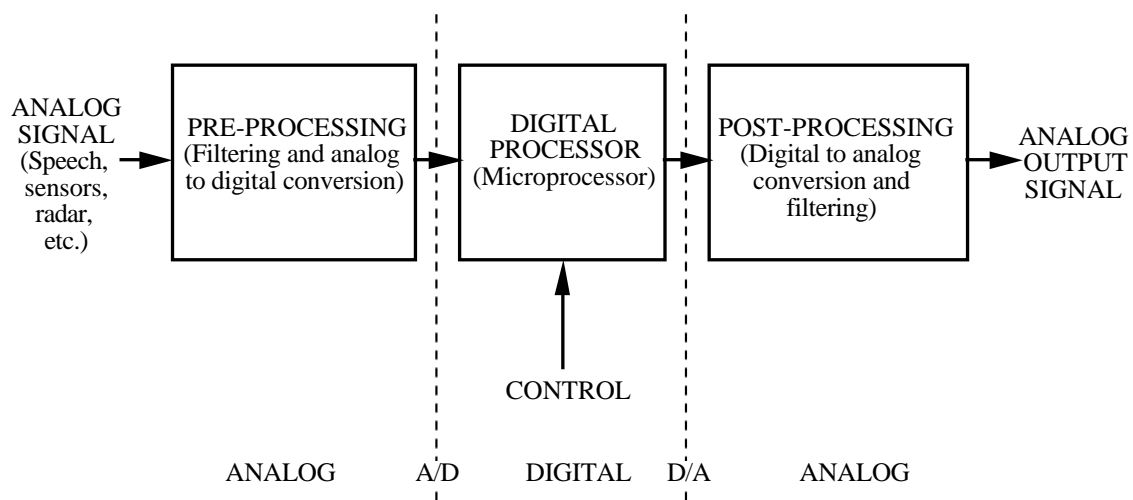
Organization



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Importance of Data Converters in Signal Processing



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Digital-Analog Converters

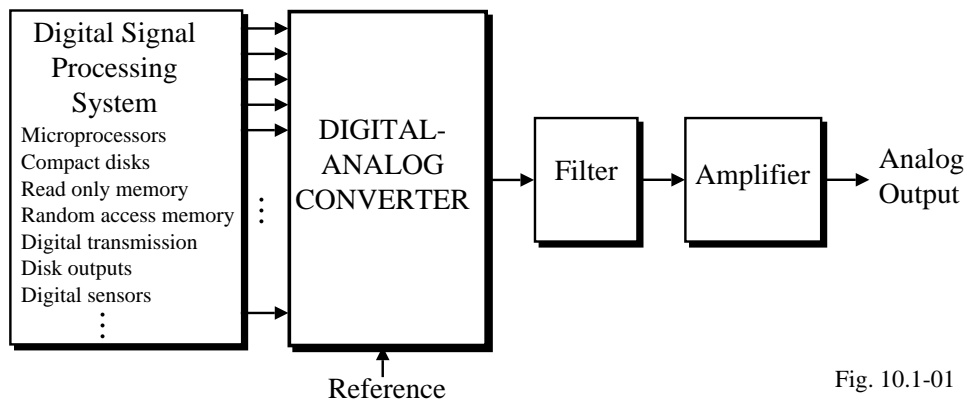
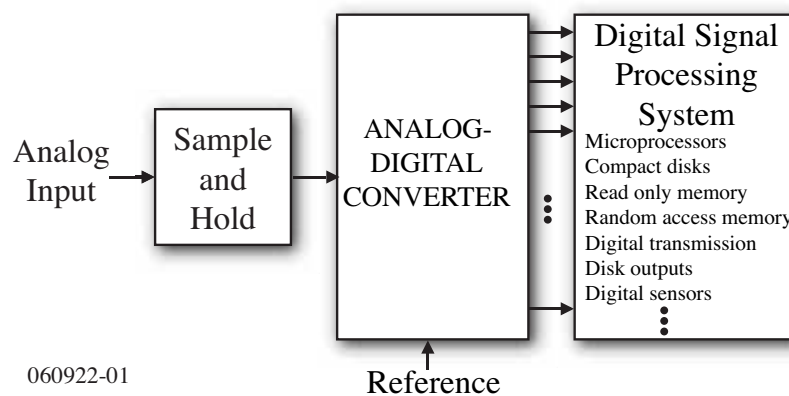


Fig. 10.1-01

Characteristics:

- Can be asynchronous or synchronous
- Primary active element is the op amp
- Conversion time can vary from fast (one clock period, T) to slow ($2^{\text{No. of bits}} \cdot T$)

Analog-Digital Converters



060922-01

Characteristics:

- Can only be synchronous (the analog signal must be sampled and held during conversion)
- Primary active element is the comparator
- Conversion time can vary from fast (one clock period, T) to slow ($2^{\text{No. of bits}} \cdot T$)

SECTION 10.1 - CHARACTERIZATION OF DIGITAL-ANALOG CONVERTERS

STATIC CHARACTERISTICS

Block Diagram of a Digital-Analog Converter

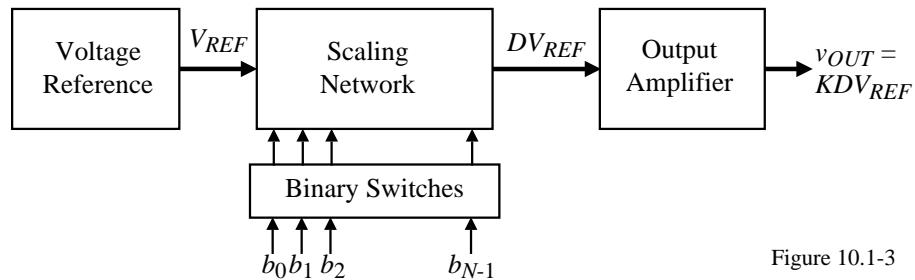


Figure 10.1-3

b_0 is the most significant bit (MSB)

The MSB is the bit that has the most (largest) influence on the analog output

b_{N-1} is the least significant bit (LSB)

The LSB is the bit that has the least (smallest) influence on the analog output

Input-Output Characteristics

Ideal input-output characteristics of a 3-bit DAC

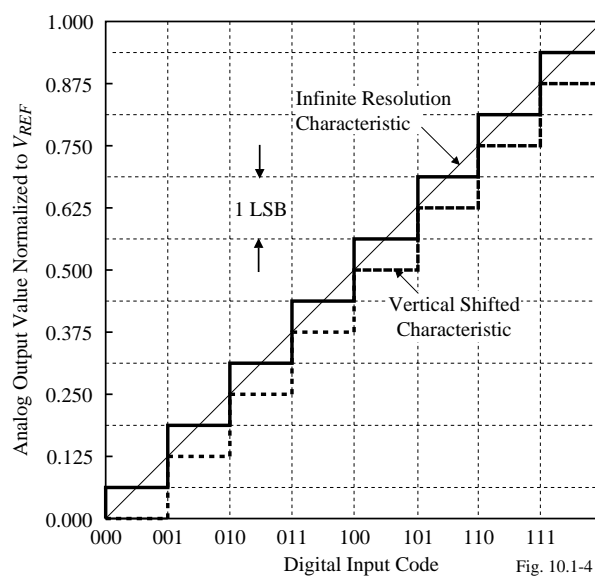


Fig. 10.1-4

Definitions

- *Resolution* of the DAC is equal to the number of bits in the applied digital input word.
- *The full scale (FS)*:

FS = Analog output when all bits are 1 - Analog output all bits are 0

$$FS = (V_{REF} - \frac{V_{REF}}{2^N}) - 0 = V_{REF} \left(1 - \frac{1}{2^N}\right)$$

- *Full scale range (FSR)* is defined as

FSR =

- *Quantization Noise* is the inherent uncertainty in digitizing an analog value with a finite resolution converter.

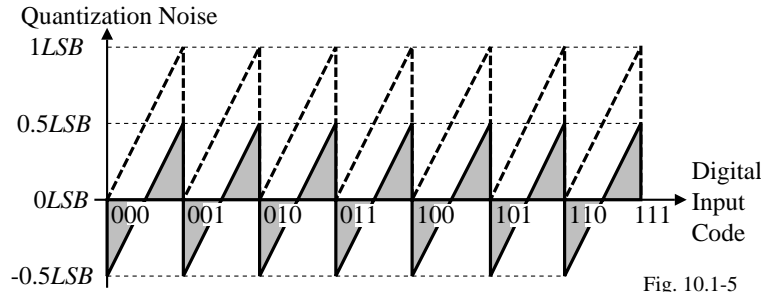


Fig. 10.1-5

More Definitions

- *Dynamic Range (DR)* of a DAC is the ratio of the FSR to the smallest difference that can be resolved (i.e. an LSB)

$$DR = \frac{FSR}{LSB \text{ change}} = \frac{FSR}{(FSR/2^N)} = 2^N$$

or in terms of decibels

$$DR(\text{dB}) = 6.02N \text{ (dB)}$$

- *Signal-to-noise ratio (SNR)* for the DAC is the ratio of the full scale value to the rms value of the quantization noise.

$$rms(\text{quantization noise}) = \sqrt{\frac{1}{T} \int_0^T LSB^2 \left(\frac{t}{T} - 0.5\right)^2 dt} = \frac{LSB}{\sqrt{12}} = \frac{FSR}{2^N \sqrt{12}}$$

$$\therefore SNR = \frac{v_{OUT}(rms)}{(FSR/\sqrt{12} \cdot 2^N)}$$

- *Maximum SNR (SNR_{max})* for a sinusoid is defined as

$$SNR_{max} = \frac{v_{OUTmax}(rms)}{(FSR/\sqrt{12} \cdot 2^N)} = \frac{FSR/(2\sqrt{2})}{FSR/(\sqrt{12} \cdot 2^N)} = \frac{\sqrt{6} \cdot 2^N}{2}$$

or in terms of decibels

$$SNR_{max}(\text{dB}) = 20 \log_{10} \left(\frac{\sqrt{6} \cdot 2^N}{2} \right) = 10 \log_{10}(6) + 20 \log_{10}(2^N) - 20 \log_{10}(2) = 1.76 + 6.02N \text{ dB}$$

Even More Definitions

- *Effective number of bits (ENOB)* can be defined from the above as

$$ENOB = \frac{SNR_{Actual} - 1.76}{6.02}$$

where SNR_{Actual} is the actual SNR of the converter.

Comment:

The DR is the amplitude range necessary to resolve N bits regardless of the amplitude of the output voltage.

However, when referenced to a given output analog signal amplitude, the DR required must include 1.76 dB more to account for the presence of quantization noise.

Thus, for a 10-bit DAC, the DR is 60.2 dB and for a full-scale, *rms* output voltage, the signal must be approximately 62 dB above whatever noise floor is present in the output of the DAC.

Accuracy Requirements of the i -th Bit

- The output of the i -th bit of the converter is expressed as:

$$\text{The output of the } i\text{-th bit} = \frac{V_{REF}}{2^{i+1}} \left(\frac{2^n}{2^n} \right) = 2^{n-i-1} \text{ LSBs}$$

- The uncertainty of each bit must be less than $\pm 0.5 \text{ LSB}$ (assuming all other bits are ideal. Must use $\pm 0.25 \text{ LSB}$ if each bit has a worst case error.)
- The accuracy of the i -th bit is equal to the uncertainty divided by the output giving:

$$\text{Accuracy of the } i\text{-th bit} = \frac{\pm 0.5 \text{ LSB}}{2^{n-i-1} \text{ LSB}} = \frac{1}{2^{n-i}} = \frac{100}{2^{n-i}} \%$$

Result: The highest accuracy requirement is always the MSB ($i = 1$).

The LSB bit only needs $\pm 50\%$ accuracy.

Example:

What is the accuracy requirement for each of the bits of a 10 bit converter?
Assuming all other bits are ideal, the accuracy requirement per bit is given below.

Bit Number	0	1	2	3	4	5	6	7	8	9
Accuracy %	0.098	0.195	0.391	0.781	1.563	3.125	6.25	12.5	25	50

(If all other bits are worst case, the numbers above must be divided by 2.)

Offset and Gain Errors

An *offset error* is a constant difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured at any vertical jump.

A *gain error* is the difference between the slope of the actual finite resolution and the ideal finite resolution characteristic measured at the right-most vertical jump.

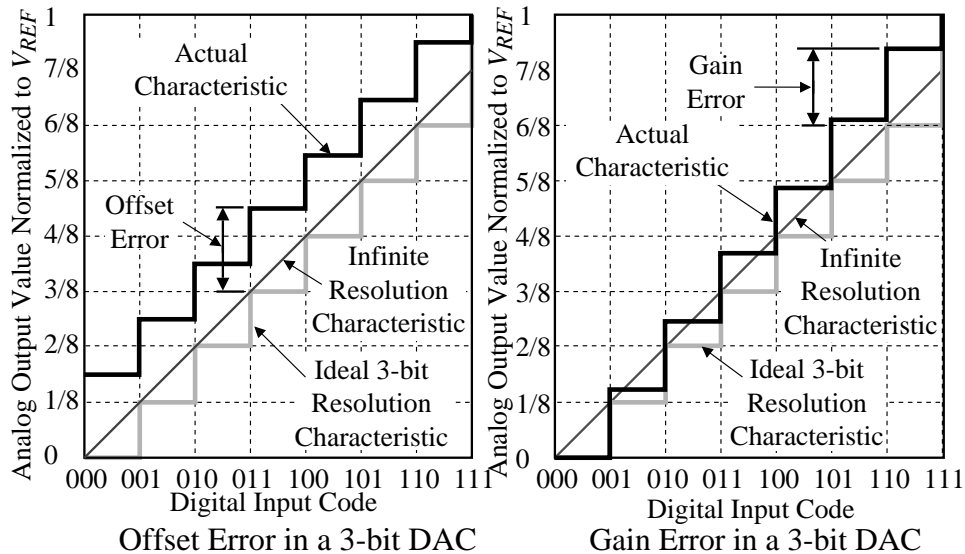


Fig. 10.1-6

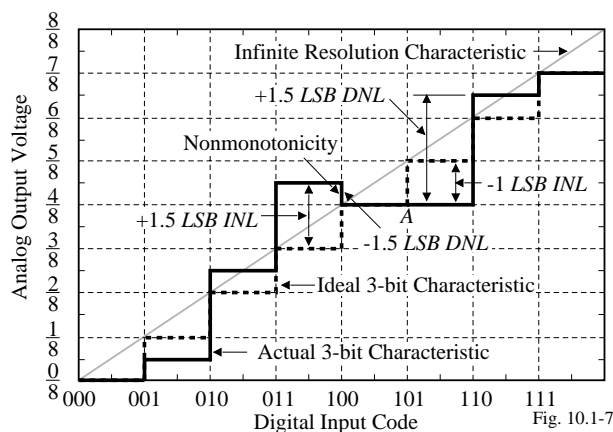
Integral and Differential Nonlinearity

- *Integral Nonlinearity (INL)* is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*).
- *Differential Nonlinearity (DNL)* is a measure of the separation between adjacent levels measured at each vertical jump (% or *LSB*).

$$DNL = V_{cx} - V_s = \left(\frac{V_{cx} - V_s}{V_s} \right) V_s = \left(\frac{V_{cx}}{V_s} - 1 \right) LSB_s$$

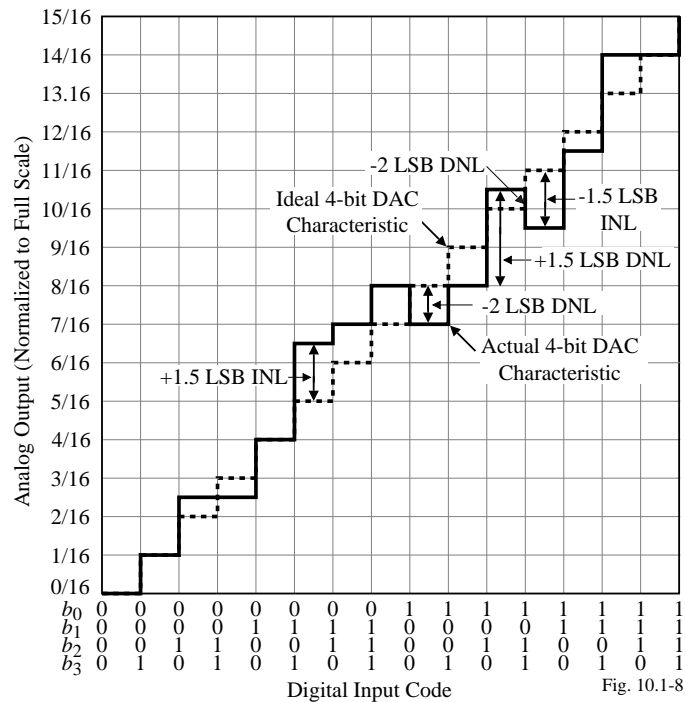
where V_{cx} is the actual voltage change on a bit-to-bit basis and V_s is the ideal *LSB* change of $(V_{FSR}/2^N)$

Example of a 3-bit DAC:



Example of INL and DNL of a Nonideal 4-Bit Dac

Find the $\pm INL$ and $\pm DNL$ for the 4-bit DAC shown.



DYNAMIC CHARACTERISTICS OF DIGITAL-ANALOG CONVERTERS

Dynamic characteristics include the influence of time.

Definitions

- *Conversion speed* is the time it takes for the DAC to provide an analog output when the digital input word is changed.

Factor that influence the conversion speed:

Parasitic capacitors (would like all nodes to be low impedance)

Op amp gainbandwidth

Op amp slew rate

- *Gain error* of an op amp is the difference between the desired and actual output voltage of the op amp (can have both a static and dynamic influence)

$$\text{Actual Gain} = \text{Ideal Gain} \times \left(\frac{\text{Loop Gain}}{1 + \text{Loop Gain}} \right)$$

$$\text{Gain error} = \frac{\text{Ideal Gain} - \text{Actual Gain}}{\text{Ideal Gain}} = \frac{1}{1 + \text{Loop Gain}}$$

Example of Influence of Op Amp Gain Error on DAC Performance

Assume that a DAC using an op amp in the inverting configuration with $C_1 = C_2$ and $A_{vd}(0) = 1000$. Find the largest resolution of the DAC if V_{REF} is 1V and assuming worst case conditions.

Solution

The loop gain of the inverting configuration is $LG = \frac{C_2}{C_1+C_2} A_{vd}(0) = 0.5 \cdot 1000 = 500$. The gain error is therefore $1/501 \approx 0.002$. The gain error should be less than the quantization noise of $\pm 0.5LSB$ which is expressed as

$$\text{Gain error} = \frac{1}{501} \approx 0.002 \leq \frac{V_{REF}}{2^{N+1}}$$

Therefore the largest value of N that satisfies this equation is $N = 7$.

Influence of the Op Amp Gainbandwidth

Single-pole response:

$$v_{out}(t) = A_{CL}[1 - e^{-\omega_H t}]v_{in}(t)$$

where

A_{CL} = closed-loop gain

$$\omega_H = GB \left(\frac{R_1}{R_1 + R_2} \right) \text{ or } GB \left(\frac{C_2}{C_1 + C_2} \right)$$

To avoid errors in DACs (and ADCs), $v_{out}(t)$ must be within $\pm 0.5LSB$ of the final value by the end of the conversion time.

Multiple-pole response:

Typically the response is underdamped like the following (see Appendix C of text).

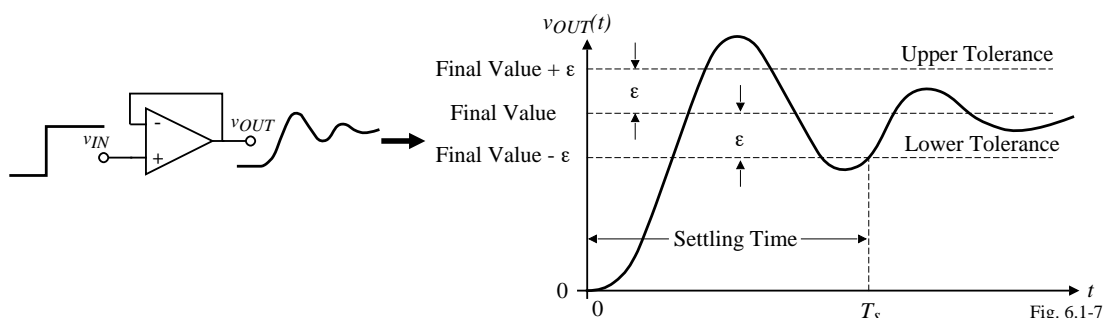


Fig. 6.1-7

Example of the Influence of GB and Settling Time on DAC Performance

Assume that a DAC uses a switched capacitor noninverting amplifier with $C_1 = C_2$ using an op amp with a dominant pole and $GB = 1\text{MHz}$. Find the conversion time of an 8-bit DAC if V_{REF} is 1V.

Solution

From the results in Sections 9.2 and 9.3 of the text, we know that

$$\omega_H = \left(\frac{C_2}{C_1 + C_2} \right) GB = (2\pi)(0.5)(10^6) = 3.141 \times 10^6$$

and $A_{CL} = 1$. Assume that the ideal output is equal to V_{REF} . Therefore the value of the output voltage which is 0.5LSB of V_{REF} is

$$1 - \frac{1}{2^{N+1}} = 1 - e^{-\omega_H T}$$

or

$$2^{N+1} = e^{\omega_H T}$$

Solving for T gives

$$T = \left(\frac{N+1}{\omega_H} \right) \ln(2) = 0.693 \left(\frac{N+1}{\omega_H} \right) = \left(\frac{9}{3.141} \right) 0.693 = 1.986 \mu\text{s}$$

TESTING OF DACs

Input-Output Test

Test setup:

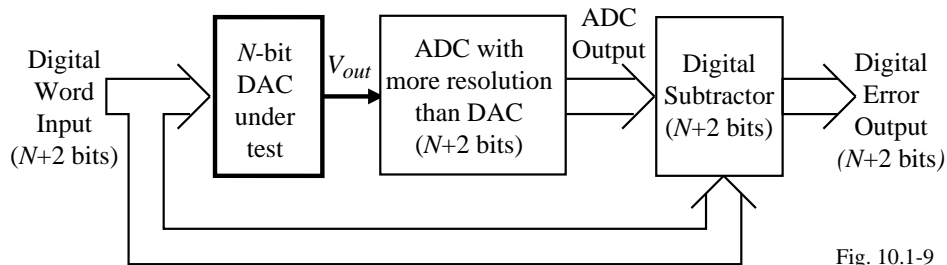


Fig. 10.1-9

Comments:

Sweep the digital input word from 000...0 to 111...1.

The ADC should have more resolution by at least 2 bits and be more accurate than the errors of the DAC

INL will show up in the output as the presence of 1's in any bit.

If there is a 1 in the Nth bit, the *INL* is greater than $\pm 0.5\text{LSB}$

DNL will show up as a change between each successive digital error output.

The bits which are greater than N in the digital error output can be used to resolve the errors to less than $\pm 0.5\text{LSB}$

Spectral Test

Test setup:

Comments:

Digital input pattern is selected to have a fundamental frequency which has a magnitude of at least $6N$ dB above its harmonics.

Length of the digital sequence determines the spectral purity of the fundamental frequency.

All nonlinearities of the DAC (i.e. *INL* and *DNL*) will cause harmonics of the fundamental frequency

The THD can be used to determine the SNR dB range between the magnitude of the fundamental and the THD. This SNR should be at least $6N$ dB to have an *INL* of less than $\pm 0.5LSB$ for an ENOB of N -bits.

Note that the noise contribution of V_{REF} must be less than the noise floor due to nonlinearities.

If the period of the digital pattern is increased, the frequency dependence of *INL* can be measured.

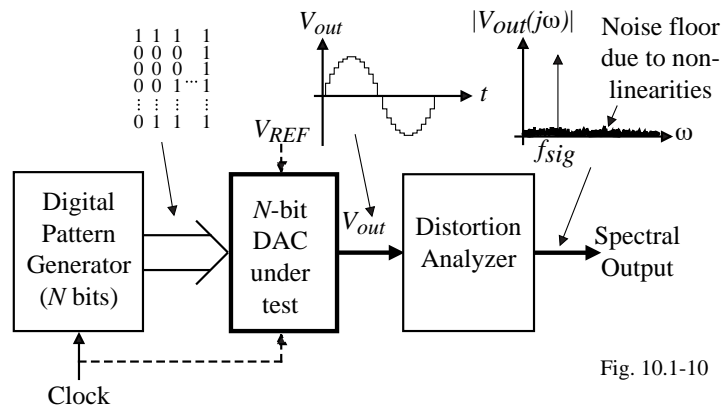


Fig. 10.1-10

SECTION 10.2 - PARALLEL DIGITAL-ANALOG CONVERTERS

Classification of Digital-Analog Converters

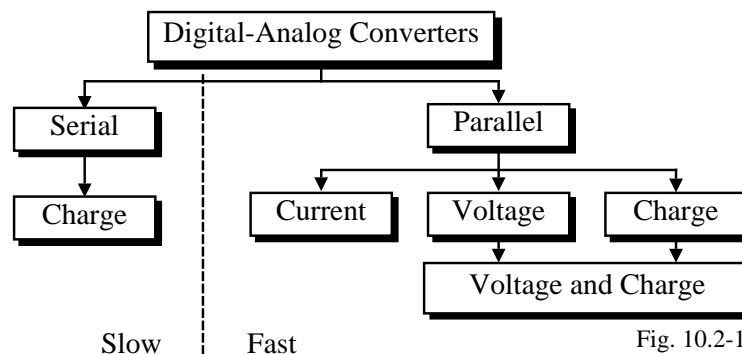


Fig. 10.2-1

CURRENT SCALING DIGITAL-ANALOG CONVERTERS

General Current Scaling DACs

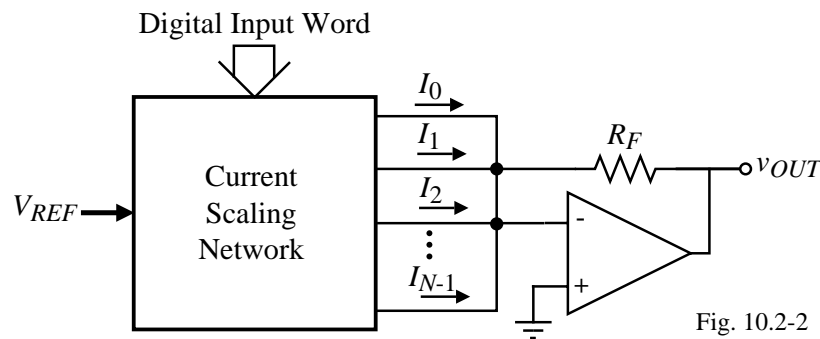


Fig. 10.2-2

The output voltage can be expressed as

$$V_{OUT} = -R_F(I_0 + I_1 + I_2 + \dots + I_{N-1})$$

where the currents I_0, I_1, I_2, \dots are binary weighted currents.

Binary-Weighted Resistor DAC

Circuit:

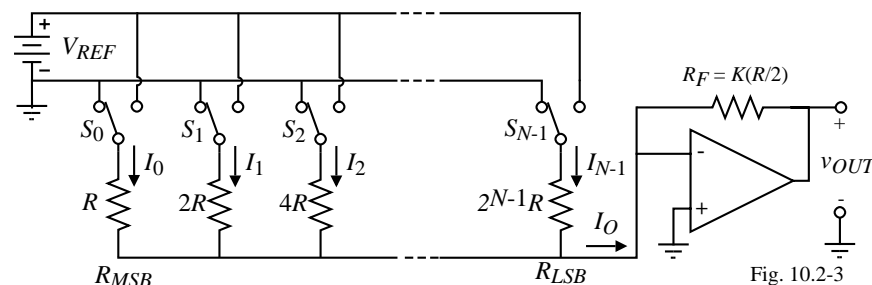


Fig. 10.2-3

Comments:

1.) R_F can be used to scale the gain of the DAC. If $R_F = KR/2$, then

$$v_{OUT} = -R_F I_O = \frac{-KR}{2} \left(\frac{b_0}{R} + \frac{b_1}{2R} + \frac{b_2}{4R} + \dots + \frac{b_{N-1}}{2^{N-1}R} \right) V_{REF} \Rightarrow v_{OUT} = -K \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \dots + \frac{b_{N-1}}{2^N} \right) V_{REF}$$

where b_i is 1 if switch S_i is connected to V_{REF} or 0 if switch S_i is connected to ground.

2.) Component spread value = $\frac{R_{MSB}}{R_{LSB}} = \frac{R}{2^{N-1}R} = \frac{1}{2^{N-1}}$

3.) Attributes:

Insensitive to parasitics \Rightarrow fast

Large component spread value

Trimming required for large values of N

Nonmonotonic

R-2R Ladder Implementation of the Binary Weighted Resistor DAC

Use of the R-2R concept to avoid large element spreads:

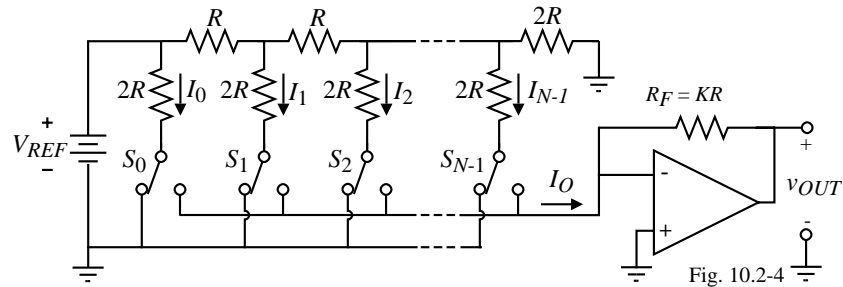


Fig. 10.2-4

How does the R-2R ladder work?

“The resistance seen to the right of any of the vertical $2R$ resistors is $2R$.”

Attributes:

- Not sensitive to parasitics

(currents through the resistors never change as S_i is varied)

- Small element spread. Resistors made from same unit ($2R$ consist of two in series or R consists of two in parallel)
- Not monotonic

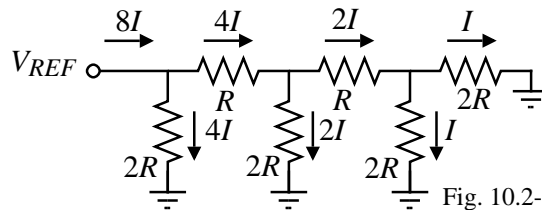


Fig. 10.2-4(2R-R)

Current Scaling Using Binary Weighted MOSFET Current Sinks

Circuit:

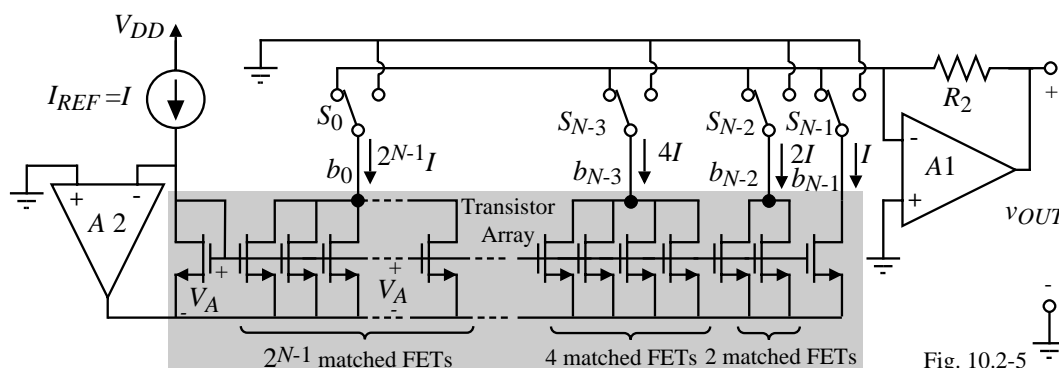


Fig. 10.2-5

Operation:

$$v_{OUT} = R_2(b_{N-1} \cdot I + b_{N-2} \cdot 2I + b_{N-3} \cdot 4I + \dots + b_0 \cdot 2^{N-1} \cdot I)$$

$$\text{If } I = I_{REF} = \frac{V_{REF}}{2^N R_2}, \text{ then } v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \dots + \frac{b_{N-3}}{2^{N-2}} + \frac{b_{N-2}}{2^{N-1}} + \frac{b_{N-1}}{2^N} \right) V_{REF}$$

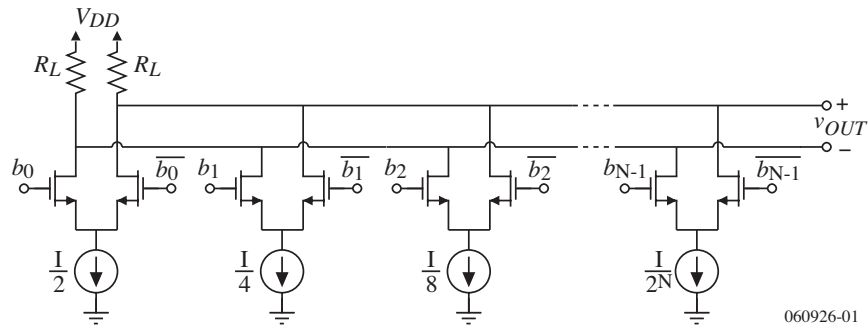
Attributes:

Fast (no floating nodes) and not monotonic

Accuracy of MSB greater than LSBs

High-Speed Current DACs

Current scaling DAC using current switches:



$$v_{OUT} = IR_L \left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \dots + \frac{b_{N-1}}{2^N} \right]$$

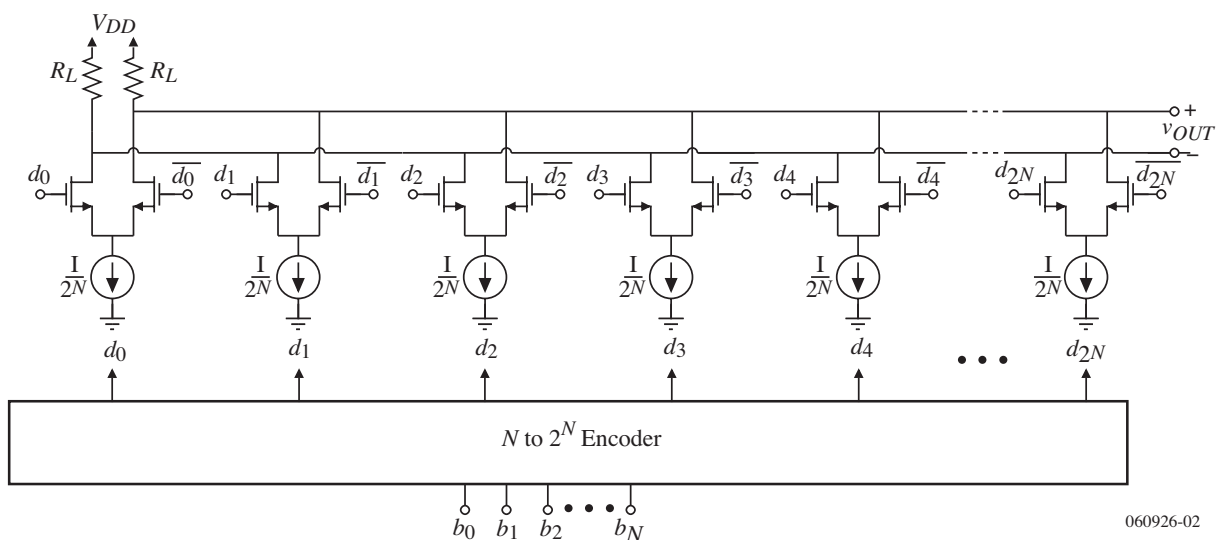
where

$$b_i = \begin{cases} +1 & \text{if the bit is 1} \\ -1 & \text{if the bit is 0} \end{cases}$$

A single-ended DAC can be obtained by replacing the left R_L by a short.

High-Speed, High-Accuracy Current Scaling DACs

The accuracy is increased by using the same value of current for each switch as shown.



For a 4 bit DAC, there would be 16 current switches.

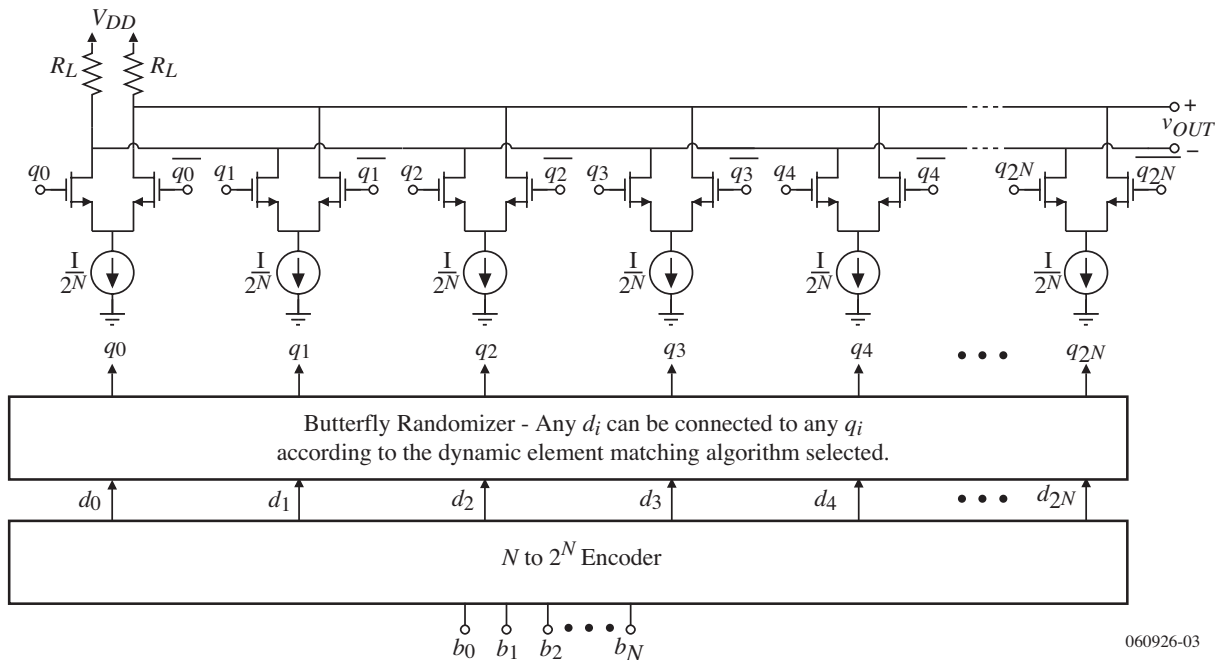
The MSB bit would switch 8 of the current switches to one side.

The next-MSB bit would switch 4 of the current switches to one side.

Etc.

Increasing the Accuracy of the Current Switching DAC

The accuracy of the previous DAC can be increased by using dynamic element matching techniques. This is illustrated below where a butterfly switching element allows the switch control bits, d_i , to be “randomly” connected to any of the current switches.



CMOS Analog Circuit Design

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VOLTAGE SCALING DIGITAL-ANALOG CONVERTERS

General Voltage Scaling Digital Analog Converter

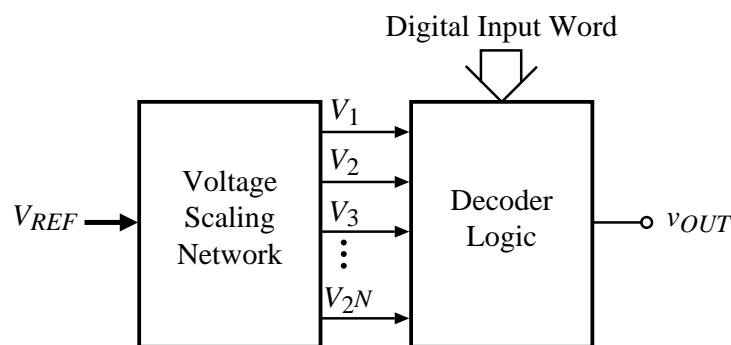


Fig. 10.2-6

Operation:

Creates all possible values of the analog output then uses a decoding network to determine which voltage to select based on the digital input word.

3-Bit Voltage Scaling Digital-Analog Converter

The voltage at any tap can be expressed as: $v_{OUT} = \frac{V_{REF}}{8} (n - 0.5) = \frac{V_{REF}}{16} (2n - 1)$

Attributes:

- Guaranteed monotonic
- Compatible with CMOS technology
- Large area if N is large
- Sensitive to parasitics
- Requires a buffer
- Large current can flow through the resistor string.

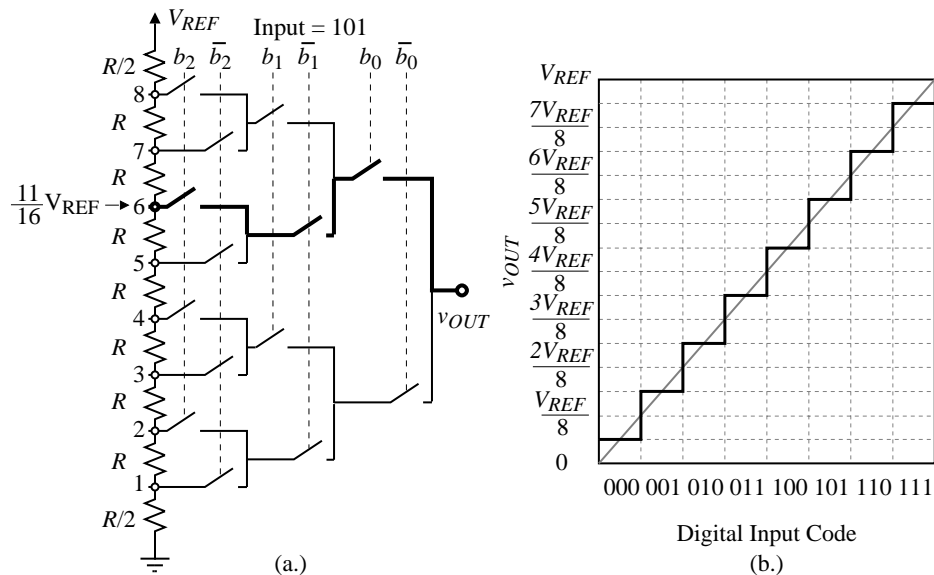


Figure 10.2-7 - (a.) Implementation of a 3-bit voltage scaling DAC. (b.) Input-output characteristics of Fig. 10.2-7(a.)

Alternate Realization of the 3-Bit Voltage Scaling DAC

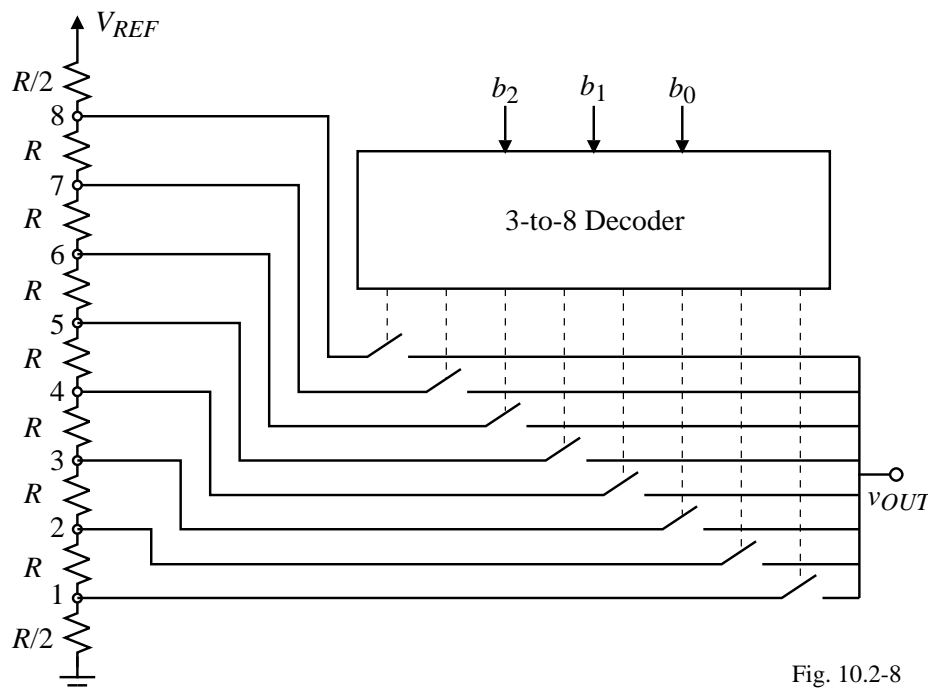


Fig. 10.2-8

INL and DNL of the Voltage Scaling DAC

Find an expression for the INL and DNL of the voltage scaling DAC using a worst-case approach. For an n -bit DAC, assume there are 2^n resistors between V_{REF} and ground and that the resistors are numbered from 1 to 2^n beginning with the resistor connected to V_{REF} and ending with the resistor connected to ground.

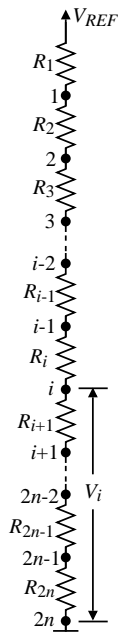


Fig. 10.2-085

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Integral Nonlinearity

The voltage at the i -th resistor from the top is,

$$v_i = \frac{(2^n - i)R}{(2^n - i)R + iR} V_{REF}$$

where there are i resistors above v_i and $2^n - i$ below.

For worst case, assume that $i = 2^{n-1}$ (midpoint).

Define $R_{max} = R + \Delta R$ and $R_{min} = R - \Delta R$.

The worst case INL is

$$INL = v_{2^{n-1}}(\text{actual}) - v_{2^{n-1}}(\text{ideal})$$

Therefore,

$$INL = \frac{2^{n-1}(R + \Delta R)V_{REF}}{2^{n-1}(R + \Delta R) + 2^{n-1}(R - \Delta R)} - \frac{V_{REF}}{2} = \frac{\Delta R}{2R} V_{REF}$$

$$INL = \frac{2^n}{2^n} \left(\frac{\Delta R}{2R} \right) V_{REF} = 2^{n-1} \left(\frac{\Delta R}{R} \right) \left(\frac{V_{REF}}{2^n} \right) = 2^{n-1} \left(\frac{\Delta R}{R} \right) LSBs$$

Differential Nonlinearity

The worst case DNL is

$$DNL = v_{step}(\text{act}) - v_{step}(\text{ideal})$$

Substituting the actual and ideal steps gives,

$$= \frac{(R + \Delta R)V_{REF}}{2^n R} - \frac{R V_{REF}}{2^n R}$$

$$= \left(\frac{R + \Delta R}{R} - \frac{R}{R} \right) \frac{V_{REF}}{2^n}$$

$$= \frac{\pm \Delta R}{R} \frac{V_{REF}}{2^n}$$

Therefore,

$$DNL = \frac{\pm \Delta R}{R} LSBs$$

Example 10.2-1 - Accuracy Requirements of a Voltage-Scaling digital-analog Converter

If the resistor string of a voltage scaling digital-analog converter is a $5 \mu\text{m}$ wide polysilicon strip having a relative accuracy of $\pm 1\%$, what is the largest number of bits that can be resolved and keep the worst case INL within ± 0.5 LSB? For this number of bits, what is the worst case DNL?

Solution

From the previous page, we can write that

$$2^{n-1} \left(\frac{\Delta R}{R} \right) = 2^{n-1} \left(\frac{1}{100} \right) \leq \frac{1}{2}$$

This inequality can be simplified

$$2^n \leq 100$$

which has a solution of $n = 6$.

The value of the DNL for $n = 6$ is found from the previous page as

$$DNL = \frac{\pm 1}{100} LSBs = \pm 0.01 LSBs$$

(This is the reason the resistor string is monotonic.)

CHARGE SCALING DIGITAL-ANALOG CONVERTERS

General Charge Scaling Digital-Analog Converter

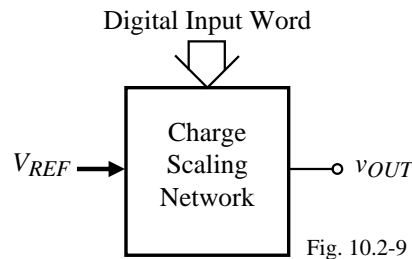


Fig. 10.2-9

General principle is to capacitively attenuate the reference voltage. Capacitive attenuation is simply:

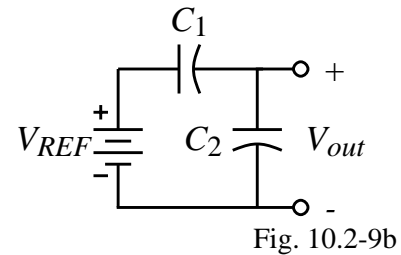


Fig. 10.2-9b

Calculate as if the capacitors were resistors. For example,

$$V_{out} = \frac{\frac{1}{C_2}}{\frac{1}{C_1} + \frac{1}{C_2}} V_{REF} = \frac{C_1}{C_1 + C_2} V_{REF}$$

Binary-Weighted, Charge Scaling DAC

Circuit:

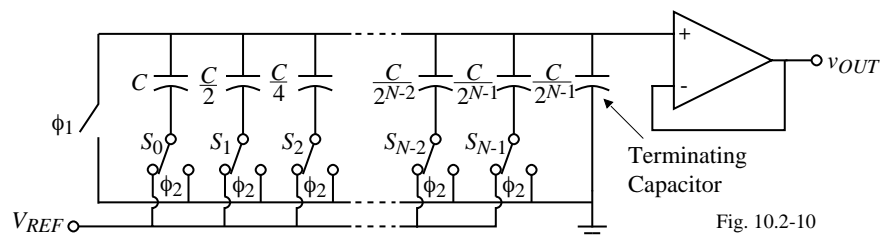


Fig. 10.2-10

Operation:

1.) All switches connected to ground during ϕ_1 .

2.) Switch S_i closes to V_{REF} if $b_i = 1$ or to ground if $b_i = 0$.

Equating the charge in the capacitors gives,

$$V_{REF} C_{eq} = V_{REF} \left(b_0 C + \frac{b_1 C}{2} + \frac{b_2 C}{2^2} + \dots + \frac{b_{N-1} C}{2^{N-1}} \right) = C_{tot} v_{OUT} = 2C v_{OUT}$$

which gives

$$v_{OUT} = [b_0 2^{-1} + b_1 2^{-2} + b_2 2^{-3} + \dots + b_{N-1} 2^{-N}] V_{REF}$$

Equivalent circuit of the binary-weighted, charge scaling DAC is:

Attributes:

- Accurate
- Sensitive to parasitics
- Not monotonic
- Charge feedthrough occurs at turn on of switches

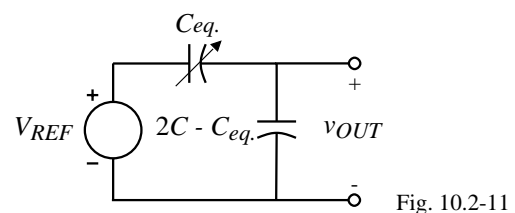


Fig. 10.2-11

Integral Nonlinearity of the Charge Scaling DAC

Again, we use a worst case approach. Assume an n -bit charge scaling DAC with the *MSB* capacitor of C and the *LSB* capacitor of $C/2^{n-1}$ and the capacitors have a tolerance of $\Delta C/C$.

The ideal output when the i -th capacitor only is connected to V_{REF} is

$$v_{OUT}(\text{ideal}) = \frac{C/2^{i-1}}{2C} V_{REF} = \frac{V_{REF}}{2^i} \left(\frac{2^n}{2^n} \right) = \frac{2^n}{2^i} \text{LSBs}$$

The maximum and minimum capacitance is $C_{max} = C + \Delta C$ and $C_{min} = C - \Delta C$. Therefore, the actual worst case output for the i -th capacitor is

$$v_{OUT}(\text{actual}) = \frac{(C \pm \Delta C)/2^{i-1}}{2C} V_{REF} = \frac{V_{REF}}{2^i} \pm \frac{\Delta C \cdot V_{REF}}{2^i C} = \frac{2^n}{2^i} \pm \frac{2^n \Delta C}{2^i C} \text{LSBs}$$

Now, the *INL* for the i -th bit is given as

$$INL(i) = v_{OUT}(\text{actual}) - v_{OUT}(\text{ideal}) = \frac{\pm 2^n \Delta C}{2^i C} = \frac{2^{n-i} \Delta C}{C} \text{LSBs}$$

Typically, the worst case value of i occurs for $i = 1$. Therefore, the worst case *INL* is

$$INL = \pm 2^{n-1} \frac{\Delta C}{C} \text{LSBs}$$

Differential Nonlinearity of the Charge Scaling DAC

The worst case *DNL* for the binary weighted capacitor array is found when the *MSB* changes. The output voltage of the binary weighted capacitor array can be written as

$$v_{OUT} = \frac{C_{eq.}}{(2C - C_{eq.}) + C_{eq.}} V_{REF}$$

where $C_{eq.}$ are capacitors whose bits are 1 and $(2C - C_{eq.})$ are capacitors whose bits are 0.

The worst case *DNL* can be expressed as

$$DNL = \frac{v_{\text{step}}(\text{worst case})}{v_{\text{step}}(\text{ideal})} - 1 = \frac{v_{OUT}(1000....) - v_{OUT}(0111....)}{LSB} - 1 \text{LSBs}$$

The worst case choice for the capacitors is to choose C_1 larger by ΔC and the remaining capacitors smaller by ΔC giving,

$$C_1 = C + \Delta C, C_2 = \frac{1}{2}(C - \Delta C), \dots, C_{n-1} = \frac{1}{2^{n-2}}(C - \Delta C), C_n = \frac{1}{2^{n-1}}(C - \Delta C), \text{ and } C_{term} = \frac{1}{2^{n-1}}(C - \Delta C)$$

Note that $\sum_{i=2}^n C_i + C_{term} = C_2 + C_3 + \dots + C_{n-1} + C_n + C_{term} = C - \Delta C$

Differential Nonlinearity of the Charge Scaling DAC - Continued

$$\therefore v_{OUT}(1000...) = \left(\frac{C+\Delta C}{(C+\Delta C)+(C-\Delta C)} \right) V_{REF} = \left(\frac{C+\Delta C}{2C} \right) V_{REF}$$

and

$$\begin{aligned} v_{OUT}(0111...) &= \left(\frac{(C-\Delta C) - C_{term}}{(C+\Delta C)+(C-\Delta C)} \right) V_{REF} = \frac{(C-\Delta C) - \frac{1}{2^{n-1}}(C-\Delta C)}{(C+\Delta C)+(C-\Delta C)} V_{REF} \\ &= \left(\frac{C-\Delta C}{2C} \right) \left(1 - \frac{2}{2^n} \right) V_{REF} \end{aligned}$$

$$\therefore \frac{v_{OUT}(1000...) - v_{OUT}(0111...)}{LSB} - 1 \text{ LSBs} = 2^n \left(\frac{C+\Delta C}{2C} \right) - 2^n \left(\frac{C-\Delta C}{2C} \right) \left(1 - \frac{2}{2^n} \right) - 1 = (2^n - 1) \frac{\Delta C}{C} \text{ LSBs}$$

Therefore,

$$DNL = (2^n - 1) \frac{\Delta C}{C} \text{ LSBs}$$

Example 10.2-2 - DNL and INL of a Binary Weighted Capacitor Array DAC

If the tolerance of the capacitors in an 8-bit, binary weighted, charge scaling DAC are $\pm 0.5\%$, find the worst case *INL* and *DNL*.

Solution

For the worst case *INL*, we get from above that

$$INL = (2^7)(\pm 0.005) = \pm 0.64 \text{ LSBs}$$

For the worst case *DNL*, we can write that

$$DNL = (2^8 - 1)(\pm 0.005) = \pm 1.275 \text{ LSBs}$$

Example 10.2-3 - Influence of Capacitor Ratio Accuracy on Number of Bits

Use the data shown to estimate the number of bits possible for a charge scaling DAC assuming a worst case approach for *INL* and that the worst conditions occur at the midscale (1 *MSB*).

Solution

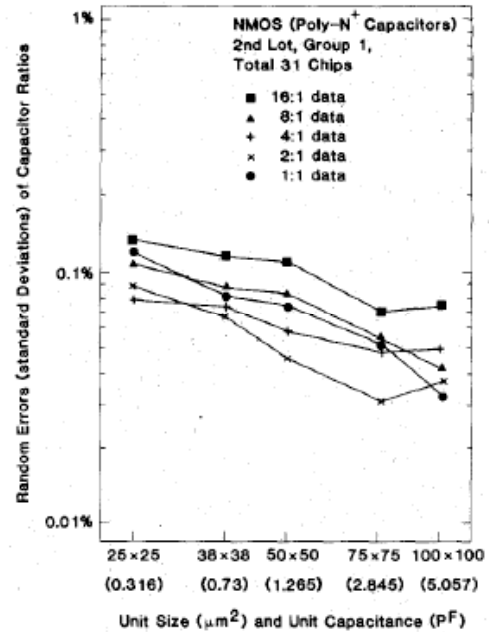
Assuming an *INL* of ± 0.5 *LSB*, we can write that

$$INL = \pm 2^{N-1} \frac{\Delta C}{C} \leq \pm \frac{1}{2} \rightarrow \left[\frac{\Delta C}{C} \right] = \frac{1}{2^N}$$

Let us assume a unit capacitor of $50 \mu\text{m}$ by $50 \mu\text{m}$ and a relative accuracy of approximately $\pm 0.1\%$. Solving for *N* in the above equation gives approximately 10 bits. However, the $\pm 0.1\%$ figure corresponds to ratios of 16:1 or 4 bits. In order to get a solution, we estimate the relative accuracy of capacitor ratios as

$$\frac{\Delta C}{C} \approx 0.001 + 0.0001N$$

Using this approximate relationship, a 9-bit digital-analog converter should be realizable.



Binary Weighted, Charge Amplifier DAC

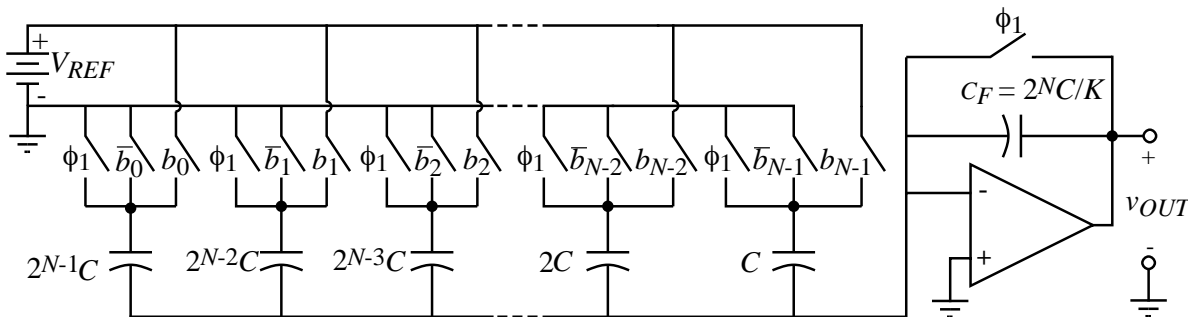


Fig. 10.2-12

Attributes:

- No floating nodes which implies insensitive to parasitics and fast
- No terminating capacitor required
- With the above configuration, charge feedthrough will be $\Delta V_{error} \approx -(C_{OL}/2CN)\Delta V$
- Can totally eliminate parasitics with parasitic-insensitive switched capacitor circuitry but not the charge feedthrough

Summary of the Parallel DAC Performance

DAC Type	Advantage	Disadvantage
Current Scaling	Fast, insensitive to switch parasitics	Large element spread, nonmonotonic
Voltage Scaling	Monotonic, equal resistors	Large area, sensitive to parasitic capacitance
Charge Scaling	Fast, good accuracy	Large element spread, nonmonotonic

SECTION 10.3 - EXTENDING THE RESOLUTION OF PARALLEL DIGITAL-ANALOG CONVERTERS

Background

Technique:

Divide the total resolution N into k smaller sub-DACs each with a resolution of $\frac{N}{k}$.

Result:

Smaller total area.

More resolution because of reduced largest to smallest component spread.

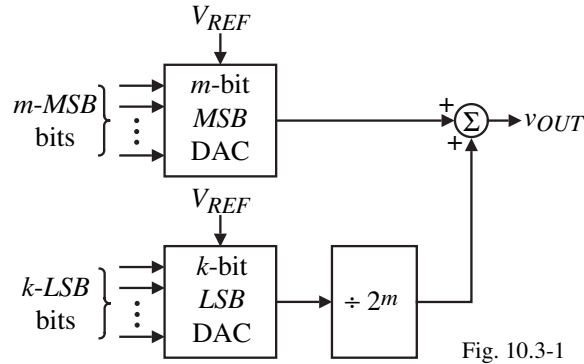
Approaches:

- Combination of similarly scaled subDACs
 - Divider approach (scale the analog output of the subDACs)
 - Subranging approach (scale the reference voltage of the subDACs)
- Combination of differently scaled subDACs

COMBINATION OF SIMILARLY SCALED SUBDACs

Analog Scaling - Divider Approach

Example of combining a m -bit and k -bit subDAC to form a $m+k$ -bit DAC.



$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{m-1}}{2^m} \right) V_{REF} + \left(\frac{1}{2^m} \right) \left(\frac{b_m}{2} + \frac{b_{m+1}}{4} + \cdots + \frac{b_{m+k-1}}{2^k} \right) V_{REF}$$

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{m-1}}{2^m} + \frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \cdots + \frac{b_{m+k-1}}{2^{m+k}} \right) V_{REF}$$

Example 10.3-1 - Illustration of the Influence of the Scaling Factor

Assume that $m = 2$ and $k = 2$ in Fig. 10.3-1 and find the transfer characteristic of this DAC if the scaling factor for the *LSB* DAC is $3/8$ instead of $1/4$. Assume that $V_{REF} = 1V$. What is the $\pm INL$ and $\pm DNL$ for this DAC? Is this DAC monotonic or not?

Solution

The ideal DAC output is given as

$$v_{OUT} = \frac{b_0}{2} + \frac{b_1}{4} + \frac{1}{4} \left(\frac{b_2}{2} + \frac{b_3}{4} \right) = \frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16}.$$

The actual DAC output can be written as

$$v_{OUT(act.)} = \frac{b_0}{2} + \frac{b_1}{4} + \frac{3b_2}{16} + \frac{3b_3}{32} = \frac{16b_0}{32} + \frac{8b_1}{32} + \frac{6b_2}{32} + \frac{3b_3}{32}$$

The results are tabulated in Table 10.3-1 for this example.

Example 10.3-1 - Continued

Table 10.3-1

Ideal and Actual Analog Output for the DAC in Ex. 10.3-1,

Input Digital Word	$v_{OUT}(\text{act.})$	v_{OUT}	$v_{OUT}(\text{act.}) - v_{OUT}$	Change in $v_{OUT}(\text{act.}) - v_{OUT}$
0000	0/32	0/32	0/32	-
0001	3/32	2/32	1/32	1/32
0010	6/32	4/32	2/32	1/32
0011	9/32	6/32	3/32	1/32
0100	8/32	8/32	0/32	-3/32
0101	11/32	10/32	1/32	1/32
0110	14/32	12/32	2/32	1/32
0111	17/32	14/32	3/32	1/32
1000	16/32	16/32	0/32	-3/32
1001	19/32	18/32	1/32	1/32
1010	22/32	20/32	2/32	1/32
1011	25/32	22/32	3/32	1/32
1100	24/32	24/32	0/32	-3/32
1101	27/32	26/32	1/32	1/32
1110	30/32	28/32	2/32	1/32
1111	33/32	30/32	3/32	1/32

Table 10.3-1 contains all the information we are seeking. An LSB for this example is $1/16$ or $2/32$. The fourth column gives the $+INL$ as $1.5LSB$ and the $-INL$ as $0LSB$. The fifth column gives the $+DNL$ as $-0.5LSB$ and the $-DNL$ as $-1.5LSB$. Because the $-DNL$ is greater than $-1LSB$, this DAC is not monotonic.

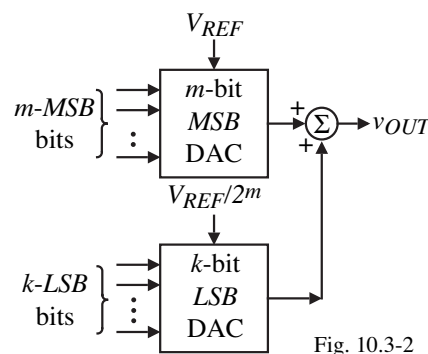
Reference Scaling - Subranging ApproachExample of combining a m -bit and k -bit subDAC to form a $m+k$ -bit DAC.

Fig. 10.3-2

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{m-1}}{2^m} \right) V_{REF} + \left(\frac{b_m}{2} + \frac{b_{m+1}}{4} + \cdots + \frac{b_{m+k-1}}{2^k} \right) \left(\frac{V_{REF}}{2^m} \right)$$

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{m-1}}{2^m} + \frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \cdots + \frac{b_{m+k-1}}{2^{m+k}} \right) V_{REF}$$

Accuracy considerations of this method are similar to the analog scaling approach.

Advantage: There are no dynamic limitations associated with the scaling factor of $1/2^m$.

Current Scaling Dac Using Two SubDACs

Implementation:

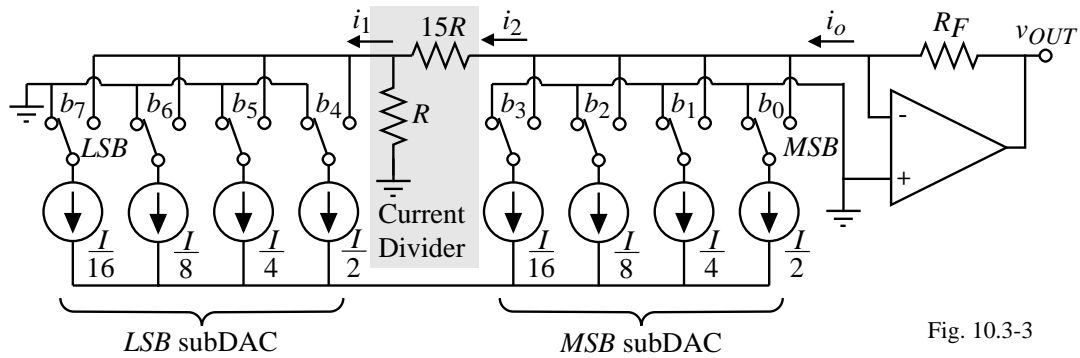


Fig. 10.3-3

$$v_{OUT} = R_F I \left[\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16} \right) + \frac{1}{16} \left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16} \right) \right]$$

Charge Scaling DAC Using Two SubDACs

Implementation:

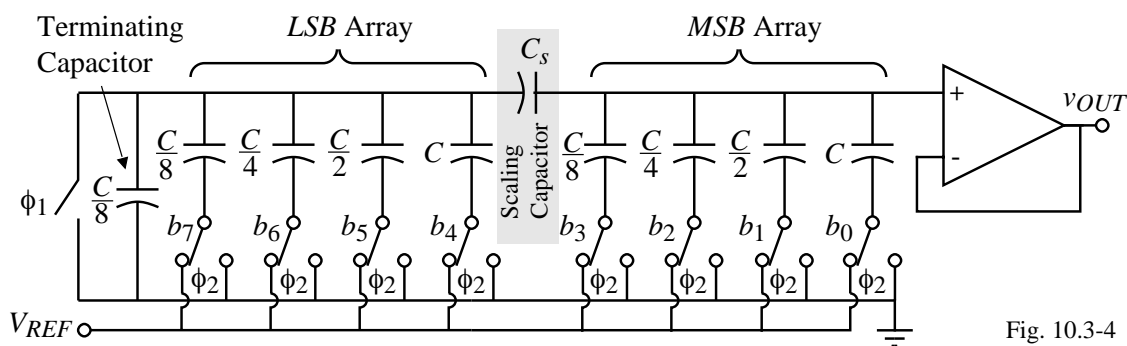


Fig. 10.3-4

Design of the scaling capacitor, C_s :

The series combination of C_s and the *LSB* array must terminate the *MSB* array or equal $C/8$. Therefore, we can write

$$\frac{C}{8} = \frac{1}{\frac{1}{C_s} + \frac{1}{2C}} \quad \text{or} \quad \frac{1}{C_s} = \frac{8}{C} - \frac{1}{2C} = \frac{16}{2C} - \frac{1}{2C} = \frac{15}{2C}$$

Equivalent Circuit of the Charge Scaling Dac Using Two SubDACs

Simplified equivalent circuit:

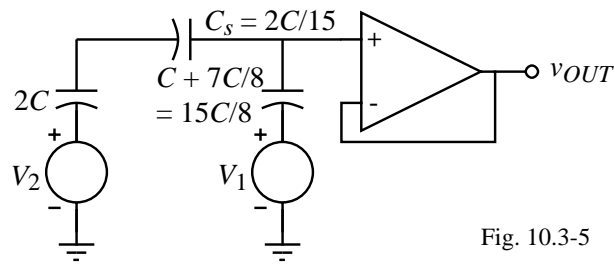


Fig. 10.3-5

where the Thevenin equivalent voltage of the *MSB* array is

$$V_1 = \left[\left(\frac{1}{15/8} \right) b_0 + \left(\frac{1/2}{15/8} \right) b_1 + \left(\frac{1/4}{15/8} \right) b_2 + \left(\frac{1/8}{15/8} \right) b_3 \right] V_{REF} = \frac{16}{15} \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16} \right) V_{REF}$$

and the Thevenin equivalent voltage of the *LSB* array is

$$V_2 = \left[\left(\frac{1/1}{2} \right) b_4 + \left(\frac{1/2}{2} \right) b_5 + \left(\frac{1/4}{2} \right) b_6 + \left(\frac{1/8}{2} \right) b_7 \right] V_{REF} = \left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16} \right) V_{REF}$$

Combining the elements of the simplified equivalent circuit above gives

$$v_{OUT} = \left(\frac{\frac{1}{2} + \frac{15}{2}}{\frac{1}{2} + \frac{15}{2} + \frac{8}{15}} \right) V_1 + \left(\frac{\frac{8}{15}}{\frac{1}{2} + \frac{15}{2} + \frac{8}{15}} \right) V_2 = \left(\frac{15 + 15 \cdot 15}{15 + 15 \cdot 15 + 16} \right) V_1 + \left(\frac{16}{15 + 15 \cdot 15 + 16} \right) V_2 = \frac{15}{16} V_1 + \frac{1}{16} V_2$$

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16} + \frac{b_4}{32} + \frac{b_5}{64} + \frac{b_6}{128} + \frac{b_7}{256} \right) V_{REF} = \sum_{i=0}^7 \frac{b_i V_{REF}}{2^{i+1}}$$

Charge Amplifier DAC Using Two Binary Weighted Charge Amplifier SubDACs

Implementation:

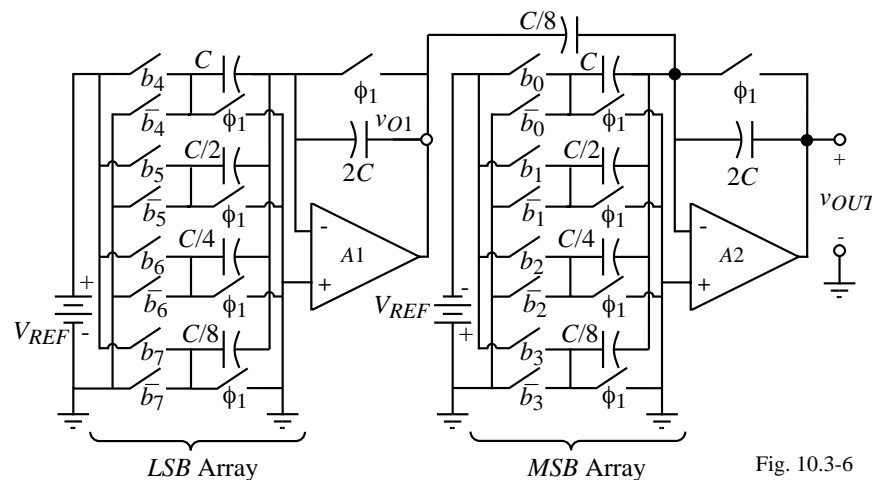


Fig. 10.3-6

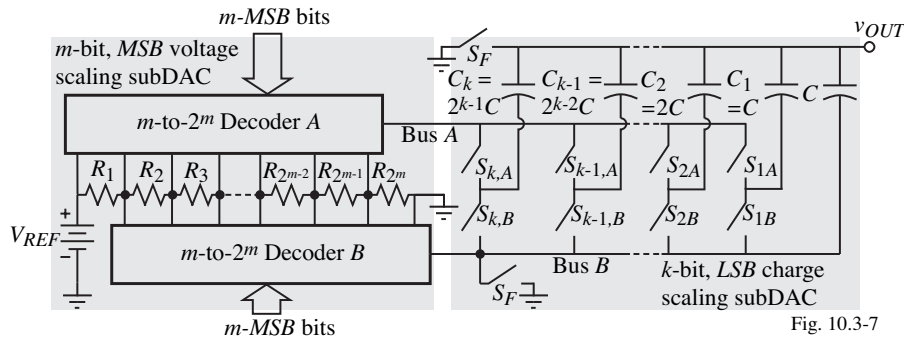
Attributes:

- *MSB* subDAC is not dependent upon the accuracy of the scaling factor for the *LSB* subDAC.
- Insensitive to parasitics, fast
- Limited to op amp dynamics (*GB*)
- No ICMR problems with the op amp

COMBINATION OF DIFFERENTLY SCALED SUBDACs

Voltage Scaling *MSB* SubDAC And Charge Scaling *LSB* SubDAC

Implementation:



Operation:

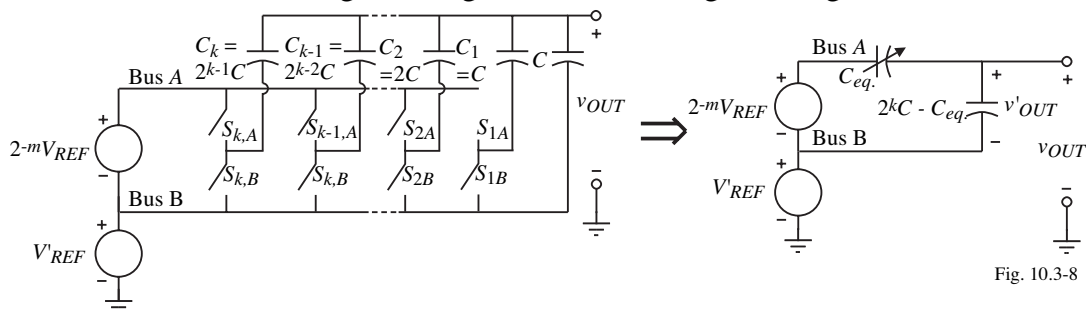
- 1.) Switches S_F and S_{1B} through $S_{k,B}$ discharge all capacitors.
- 2.) Decoders A and B connect Bus A and Bus B to the top and bottom, respectively, of the appropriate resistor as determined by the m -bits.
- 3.) The charge scaling subDAC divides the voltage across this resistor by capacitive division determined by the k -bits.

Attributes:

- *MSB*'s are monotonic but the accuracy is poor
- Accuracy of *LSBs* is good

Voltage Scaling *MSB* SubDAC And Charge Scaling *LSB* SubDAC - Continued

Equivalent circuit of the voltage scaling (*MSB*) and charge scaling (*LSB*) DAC:



where,

$$V'_{REF} = V_{REF} \left(\frac{b_0}{2^1} + \frac{b_1}{2^2} + \dots + \frac{b_{m-2}}{2^{m-1}} + \frac{b_{m-1}}{2^m} \right)$$

and

$$v'_{OUT} = \frac{V_{REF}}{2^m} \left(\frac{b_m}{2} + \frac{b_{m+1}}{2^2} + \dots + \frac{b_{m+k}}{2^{k-1}} + \frac{b_{m+k-1}}{2^k} \right) = V_{REF} \left(\frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \dots + \frac{b_{m+k}}{2^{m+k-1}} + \frac{b_{m+k-1}}{2^{m+k}} \right)$$

Adding V'_{REF} and v'_{OUT} gives the DAC output voltage as

$$v_{OUT} = V'_{REF} + v'_{OUT} = V_{REF} \left(\frac{b_0}{2^1} + \frac{b_1}{2^2} + \dots + \frac{b_{m-2}}{2^{m-1}} + \frac{b_{m-1}}{2^m} + \frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \dots + \frac{b_{m+k}}{2^{m+k-1}} + \frac{b_{m+k-1}}{2^{m+k}} \right)$$

which is equivalent to an $m+k$ bit DAC.

Charge Scaling *MSB* SubDAC and Voltage Scaling *LSB* SubDAC

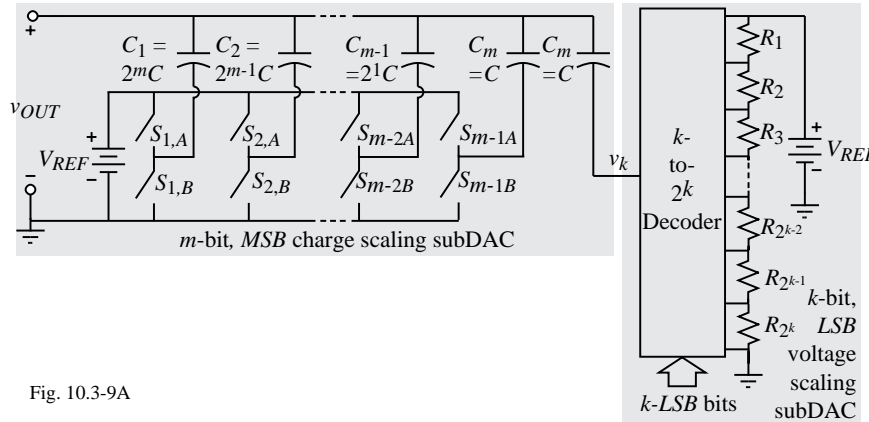


Fig. 10.3-9A

$$v_{OUT} = \left(\frac{b_0}{2^1} + \frac{b_1}{2^2} + \dots + \frac{b_{m-2}}{2^{m-1}} + \frac{b_{m-1}}{2^m} \right) V_{REF} + \frac{v_k}{2^m} \quad \text{where} \quad v_k = \left(\frac{b_m}{2^1} + \frac{b_{m+1}}{2^2} + \dots + \frac{b_{m+k}}{2^{k-1}} + \frac{b_{m+k-1}}{2^k} \right) V_{REF}$$

$$\therefore v_{OUT} = \left(\frac{b_0}{2^1} + \frac{b_1}{2^2} + \dots + \frac{b_{m-2}}{2^{m-1}} + \frac{b_{m-1}}{2^m} + \frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \dots + \frac{b_{m+k}}{2^{m+k-1}} + \frac{b_{m+k-1}}{2^{m+k}} \right) V_{REF}$$

Attributes:

- *MSBs* have good accuracy
- *LSBs* are monotonic, have poor accuracy - require trimming for good accuracy

Tradeoffs in SubDAC Selection to Enhance Linearity Performance

Assume a m -bit *MSB* subDAC and a k -bit *LSB* subDAC.

MSB Voltage Scaling SubDAC and *LSB* Charge Scaling SubDAC ($n = m+k$)

INL and *DNL* of the m -bit *MSB* voltage-scaling subDAC:

$$INL(R) = 2^{m-1} \left(\frac{2^n}{2^m} \right) \frac{\Delta R}{R} = 2^{n-1} \frac{\Delta R}{R} \text{ LSBs} \quad \text{and} \quad DNL(R) = \frac{\pm \Delta R}{R} \left(\frac{2^n}{2^m} \right) = 2^k \frac{\pm \Delta R}{R} \text{ LSBs}$$

INL and *DNL* of the k -bit *LSB* charge-scaling subDAC:

$$INL(C) = 2^{k-1} \frac{\Delta C}{C} \text{ LSBs} \quad \text{and} \quad DNL(C) = (2^{k-1}) \frac{\Delta C}{C} \text{ LSBs}$$

Combining these relationships:

$$INL = INL(R) + INL(C) = \left(2^{n-1} \frac{\Delta R}{R} + 2^{k-1} \frac{\Delta C}{C} \right) \text{ LSBs}$$

and

$$DNL = DNL(R) + DNL(C) = \left(2^k \frac{\Delta R}{R} + (2^{k-1}) \frac{\Delta C}{C} \right) \text{ LSBs}$$

MSB Charge Scaling SubDAC and *LSB* Voltage Scaling SubDAC

$$INL = INL(R) + INL(C) = \left(2^{k-1} \frac{\Delta R}{R} + 2^{n-1} \frac{\Delta C}{C} \right) \text{ LSBs}$$

and

$$DNL = DNL(R) + DNL(C) = \left(\frac{\Delta R}{R} + (2^{n-1}) \frac{\Delta C}{C} \right) \text{ LSBs}$$

Example 10.3-2 - Design of a DAC using Voltage Scaling for *MBSs* and Charge Scaling for *LSBs*

Consider a 12-bit DAC that uses voltage scaling for the *MSBs* charge scaling for the *LSBs*. To minimize the capacitor element spread and the number of resistors, choose $m = 5$ and $k = 7$. Find the tolerances necessary for the resistors and capacitors to give an *INL* and *DNL* equal to or less than 2 *LSB* and 1 *LSB*, respectively.

Solution

Substituting $n = 12$ and $k = 7$ into the previous equations gives

$$2 = 2^{11} \frac{\Delta R}{R} + 2^6 \frac{\Delta C}{C} \quad \text{and} \quad 1 = 2^7 \frac{\Delta R}{R} + (2^7 - 1) \frac{\Delta C}{C}$$

Solving these two equations simultaneously gives

$$\frac{\Delta C}{C} = \frac{2^4 - 2}{2^{11} - 2^6 - 2^4} = 0.0071 \rightarrow \frac{\Delta C}{C} = 0.71\%$$

$$\frac{\Delta R}{R} = \frac{2^8 - 2^6 - 2}{2^{18} - 2^{13} - 2^{11}} = 0.0008 \rightarrow \frac{\Delta R}{R} = 0.075\%$$

We see that the capacitor tolerance will be easy to meet but that the resistor tolerance will require resistor trimming to meet the 0.075% requirement. Because of the 2^{n-1} multiplying $\Delta R/R$ in the relationship, we are stuck with approximately 0.075%. Therefore, choose $m = 2$ (which makes the 0.075% easier to achieve) and let $k = 10$ which gives $\Delta R/R = 0.083\%$ and $\Delta C/C = 0.12\%$.

Example 10.3-3 - Design of a DAC using Charge Scaling for *MBSs* and Voltage Scaling for *LSBs*

Consider a 12-bit DAC that uses charge scaling for the *MSBs* voltage scaling for the *LSBs*. To minimize the capacitor element spread and the number of resistors, choose $m = 7$ and $k = 5$. Find the tolerances necessary for the resistors and capacitors to give an *INL* and *DNL* equal to or less than 2 *LSB* and 1 *LSB*, respectively.

Solution

Substituting the values of this example into the relationships developed on a previous slide, we get

$$2 = 2^4 \frac{\Delta R}{R} + 2^{11} \frac{\Delta C}{C} \quad \text{and} \quad 1 = \frac{\Delta R}{R} + (2^{12} - 1) \frac{\Delta C}{C}$$

Solving these two equations simultaneously gives

$$\frac{\Delta C}{C} = \frac{2^4 - 2}{2^{16} - 2^{11} - 2^4} = 0.000221 \rightarrow \frac{\Delta C}{C} = 0.0221\% \quad \text{and} \quad \frac{\Delta R}{R} \approx \frac{3}{2^5 - 1} = 0.0968 \rightarrow \frac{\Delta R}{R} = 9.68\%$$

For this example, the resistor tolerance is easy to meet but the capacitor tolerance will be difficult. To achieve accurate capacitor tolerances, we should decrease the value of m and increase the value of k to achieve a smaller capacitor value spread and thereby enhance the tolerance of the capacitors. If we choose $m = 4$ and $k = 8$, the capacitor tolerance is 0.049% and the resistor tolerance becomes 0.79% which is still reasonable. The largest to smallest capacitor ratio is 8 rather than 64 which will help to meet the capacitor tolerance requirements.

Summary of Extended Resolution DACs

- DAC resolution can be achieved by combining several subDACs with smaller resolution
- Methods of combining include scaling the output or the reference of the non-*MSB* subDACs
- SubDACs can use similar or different scaling methods
- Tradeoffs in the number of bits per subDAC and the type of subDAC allow minimization of the *INL* and *DNL*

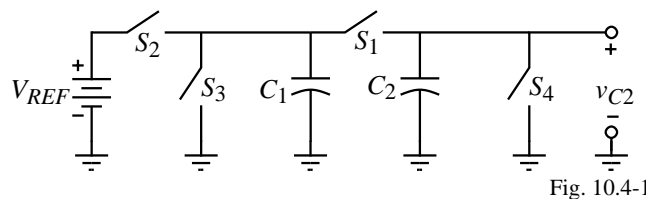
SECTION 10.4 - SERIAL DIGITAL-ANALOG CONVERTERS

Serial DACs

- Typically require one clock pulse to convert one bit
- Types considered here are:
Charge-redistribution
Algorithmic

Charge Redistribution DAC

Implementation:



Operation:

Switch S_1 is the redistribution switch that parallels C_1 and C_2 sharing their charge

Switch S_2 precharges C_1 to V_{REF} if the i th bit, b_i , is a 1

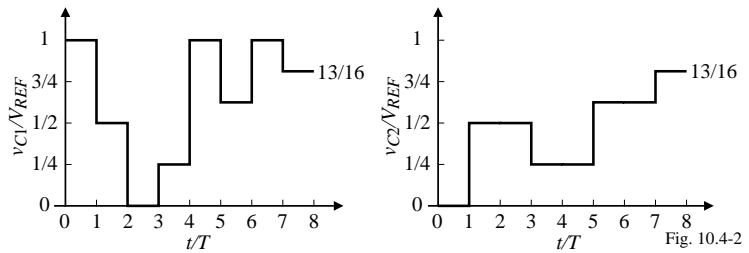
Switch S_3 discharges C_1 to zero if the i th bit, b_i , is a 0

Switch S_4 is used at the beginning of the conversion process to initially discharge C_2

Conversion always begins with the *LSB* bit and goes to the *MSB* bit.

Example 10.4-1 - Operation of the Serial, Charge Redistribution DAC

Assume that $C_1 = C_2$ and that the digital word to be converted is given as $b_0 = 1, b_1 = 1, b_2 = 0$, and $b_3 = 1$. Follow through the sequence of events that result in the conversion of this digital input word.



Solution

- 1.) S_4 closes setting $v_{C2} = 0$.
- 2.) $b_3 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.
- 3.) Switch S_1 is closed causing $v_{C1} = v_{C2} = 0.5V_{REF}$.
- 4.) $b_2 = 0$, closes switch S_3 , causing $v_{C1} = 0V$.
- 5.) S_1 closes, the voltage across both C_1 and C_2 is $0.25V_{REF}$.
- 6.) $b_1 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.
- 7.) S_1 closes, the voltage across both C_1 and C_2 is $(1+0.25)/2V_{REF} = 0.625V_{REF}$.
- 8.) $b_0 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.
- 9.) S_1 closes, the voltage across both C_1 and C_2 is $(0.625 + 1)/2V_{REF} = 0.8125V_{REF} = (13/16)V_{REF}$.

Pipeline DAC

The pipeline DAC is simply an extension of the sub-DACs concept to the limit where the bits converted by each sub-DAC is 1.

Implementation:

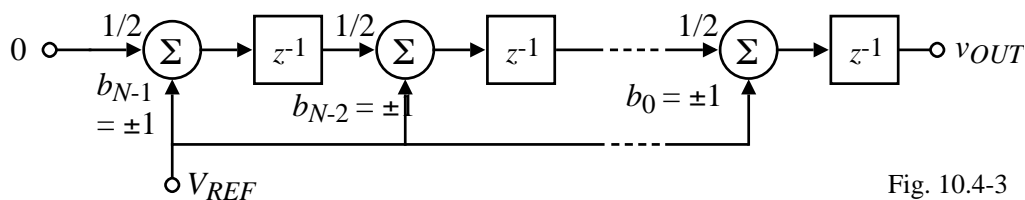


Fig. 10.4-3

$$V_{out}(z) = [b_0 z^{-1} + 2^{-1} b_1 z^{-2} + \dots + 2^{-(N-2)} b_{N-2} z^{-(N-1)} + b_{N-1} z^{-N}] V_{REF}$$

where b_i is either ± 1 if the i th bit is high or low. The z^{-1} blocks represent a delay of one clock period between the 1-bit sub-DACs.

Attributes:

- Takes $N+1$ clock cycles to convert the digital input to an analog output
- However, a new analog output is converted every clock after the initial $N+1$ clocks

Algorithmic (Iterative) DAC

Implementation:

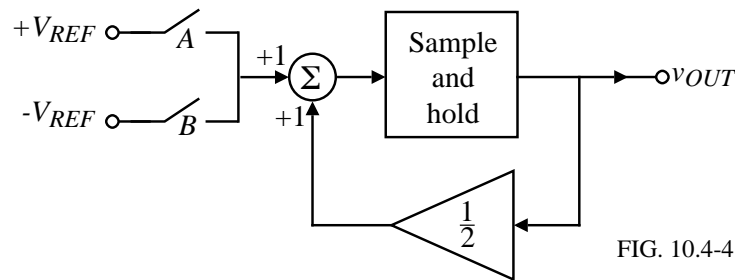


FIG. 10.4-4

Closed form of the previous series expression is,

$$V_{out}(z) = \frac{b_i z^{-1} V_{REF}}{1 - 0.5z^{-1}}$$

Operation:

Switch *A* is closed when the *i*th bit is 1 and switch *B* is closed when the *i*th bit is 0. Start with the *LSB* and work to the *MSB*.

Example 10.4-2 - Digital-Analog Conversion Using the Algorithmic Method

Assume that the digital word to be converted is 11001 in the order of *MSB* to *LSB*. Find the converted output voltage and sketch a plot of v_{OUT}/V_{REF} as a function of t/T , where T is the period for one conversion.

Solution

- 1.) The conversion starts by zeroing the output (not shown on Fig. 10.4-4).
- 2.) The *LSB* = 1, switch *A* is closed and V_{REF} is summed with zero to give an output of $+V_{REF}$.
- 3.) The next *LSB* = 0, switch *B* is closed and $v_{OUT} = -V_{REF} + 0.5V_{REF} = -0.5V_{REF}$.
- 4.) The next *LSB* = 0, switch *B* is closed and $v_{OUT} = -V_{REF} + 0.5(-0.5V_{REF}) = -1.25V_{REF}$.
- 5.) The next *LSB* = 1, switch *A* is closed and $v_{OUT} = V_{REF} + 0.5(-1.25V_{REF}) = 0.375V_{REF}$.
- 6.) The *MSB* = 1, switch *A* is closed and $v_{OUT} = V_{REF} + 0.5(0.375V_{REF}) = 1.1875V_{REF} = (19/16)V_{REF}$. (Note that because the actual V_{REF} of this example is $\pm V_{REF}$ or $2V_{REF}$, the analog value of the digital word 11001 is $19/32$ times $2V_{REF}$ or $(19/16)V_{REF}$.)

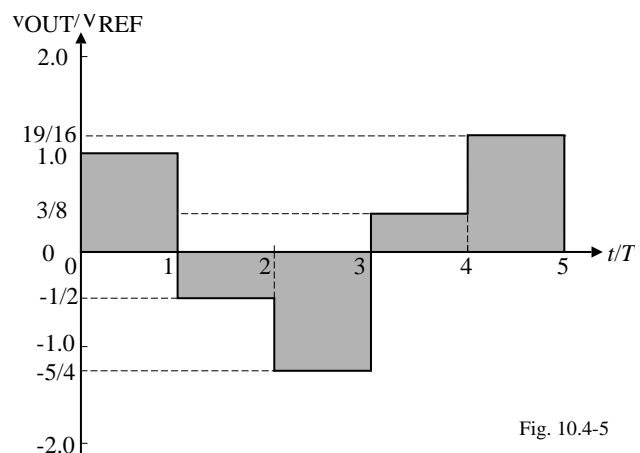


Fig. 10.4-5

Summary of Serial DACS

Table 10.4-1 - Summary of the Performance of Serial DACs

Serial DAC	Figure	Advantage	Disadvantage
Serial, Charge Redistribution	10.4-1	Simple, minimum area	Slow, requires complex external circuitry, precise capacitor ratios
Serial, algorithmic	10.4-3	Simple, minimum area	Slow, requires complex external circuitry, precise capacitor ratios

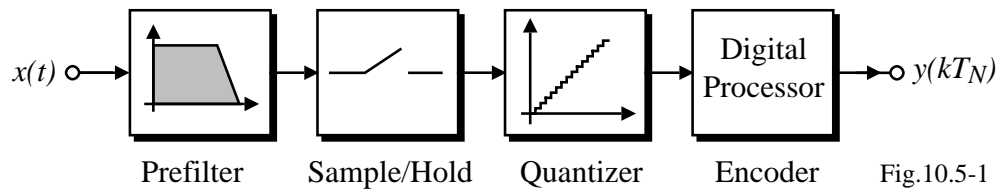
SUMMARY OF THE PERFORMANCE OF DIGITAL-ANALOG CONVERTERS

DAC	Figure	Primary Advantage	Primary Disadvantage
Current-scaling, binary weighted resistors	10.2-3	Fast, insensitive to parasitic capacitance	Large element spread, nonmonotonic
Current-scaling, R-2R ladder	10.2-4	Small element spread, increased accuracy	Nonmonotonic, limited to resistor accuracy
Current-scaling, active devices	10.2-5	Fast, insensitive to switch parasitics	Large element spread, large area
Voltage-scaling	10.2-7	Monotonic, equal resistors	Large area, sensitive to parasitic capacitance
Charge-scaling, binary weighted capacitors	10.2-10	Best accuracy	Large area, sensitive to parasitic capacitance
Binary weighted, charge amplifier	10.2-12	Best accuracy, fast	Large element spread, large area
Current-scaling subDACs using current division	10.3-3	Minimizes area, reduces element spread which enhances accuracy	Sensitive to parasitic capacitance, divider must have $\pm 0.5LSB$ accuracy
Charge-scaling subDACs using charge division	10.3-4	Minimizes area, reduces element spread which enhances accuracy	Sensitive to parasitic capacitance, slower, divider must have $\pm 0.5LSB$ accuracy
Binary weighted charge amplifier subDACs	10.3-6	Fast, minimizes area, reduces element spread which enhances accuracy	Requires more op amps, divider must have $\pm 0.5LSB$ accuracy
Voltage-scaling (<i>MSBs</i>), charge-scaling (<i>LSBs</i>)	10.3-7	Monotonic in <i>MSBs</i> , minimum area, reduced element spread	Must trim or calibrate resistors for absolute accuracy
Charge-scaling (<i>MSBs</i>), voltage-scaling (<i>LSBs</i>)	10.3-8	Monotonic in <i>LSBs</i> , minimum area, reduced element spread	Must trim or calibrate resistors for absolute accuracy
Serial, charge redistribution	10.4-1	Simple, minimum area	Slow, requires complex external circuits
Pipeline, algorithmic	10.4-3	Repeated blocks, output at each clock after <i>N</i> clocks	Large area for large number of bits
Serial, iterative algorithmic	10.4-4	Simple, one precise set of components	Slow, requires additional logic circuitry

10.5 - CHARACTERIZATION OF ANALOG-DIGITAL CONVERTERS

INTRODUCTION

General Block Diagram of an Analog-Digital Converter



- Prefilter - Avoids the aliasing of high frequency signals back into the baseband of the ADC
- Sample-and-hold - Maintains the input analog signal constant during conversion
- Quantizer - Finds the subrange that corresponds to the sampled analog input
- Encoder - Encoding of the digital bits corresponding to the subrange

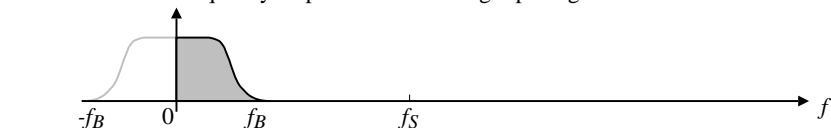
Nyquist Frequency Analog-Digital Converters

The sampled nature of the ADC places a practical limit on the bandwidth of the input signal. If the sampling frequency is f_S , and f_B is the bandwidth of the input signal, then

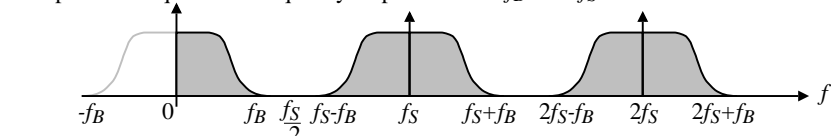
$$f_B < 0.5f_S$$

which is simply the *Nyquist* relationship which states that to avoid aliasing, the sampling frequency must be greater than twice the highest signal frequency.

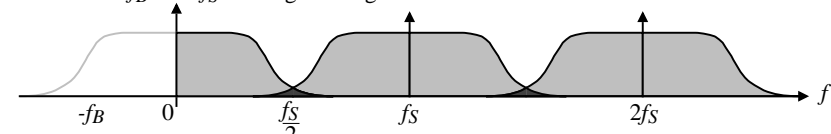
Continuous time frequency response of the analog input signal.



Sampled data equivalent frequency response where $f_B < 0.5f_S$.



Case where $f_B > 0.5f_S$ causing aliasing.



Use of an antialiasing filter to avoid aliasing.

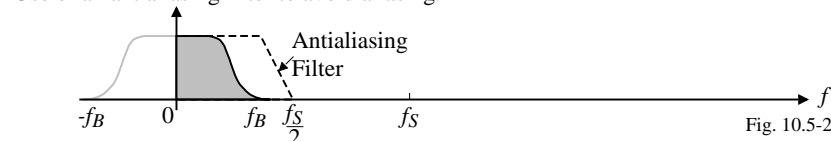


Fig. 10.5-2

Classification of Analog-Digital Converters

Analog-digital converters can be classified by the relationship of f_B and $0.5f_S$ and by their conversion rate.

- *Nyquist ADCs* - ADCs that have f_B as close to $0.5f_S$ as possible.
- *Oversampling ADCs* - ADCs that have f_B much less than $0.5f_S$.

Table 10.5-1 - Classification of Analog-to-Digital Converter Architectures

Conversion Rate	Nyquist ADCs	Oversampled ADCs
Slow	Integrating (Serial)	Very high resolution <14-16 bits
Medium	Successive Approximation 1-bit Pipeline Algorithmic	Moderate resolution <10-12 bits
Fast	Flash Multiple-bit Pipeline Folding and interpolating	Low resolution < 6-8 bits

STATIC CHARACTERIZATION OF ANALOG-TO-DIGITAL CONVERTERS

Digital Output Codes

Table 10.5-2 - Digital Output Codes used for ADCs

Decimal	Binary	Thermometer	Gray	Two's Complement
0	000	0000000	000	000
1	001	0000001	001	111
2	010	0000011	011	110
3	011	0000111	010	101
4	100	0001111	110	100
5	101	0011111	111	011
6	110	0111111	101	010
7	111	1111111	100	001

Input-Output Characteristics

Ideal input-output characteristics of a 3-bit ADC

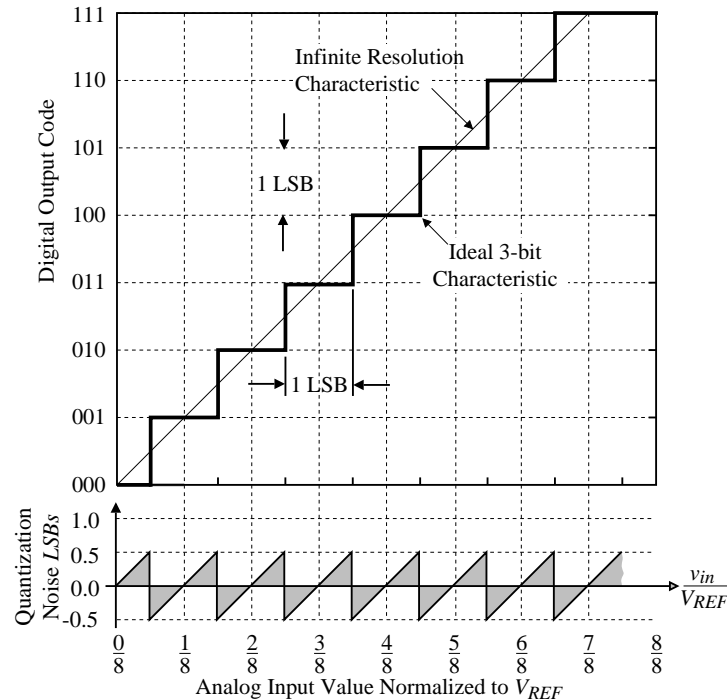


Figure 10.5-3 Ideal input-output characteristics of a 3-bit ADC.

Definitions

- The *dynamic range*, *signal-to-noise ratio (SNR)*, and the *effective number of bits (ENOB)* of the ADC are the same as for the DAC
- *Resolution* of the ADC is the smallest analog change that distinguishable by an ADC.
- *Quantization Noise* is the $\pm 0.5\text{LSB}$ uncertainty between the infinite resolution characteristic and the actual characteristic.
- *Offset Error* is the difference between the ideal finite resolution characteristic and actual finite resolution characteristic measured at full-scale input. This difference is *proportional* to the analog input voltage.
- *Gain Error* is the difference between the ideal finite resolution characteristic and actual finite resolution characteristic measured at full-scale input. This difference is *proportional* to the analog input voltage.

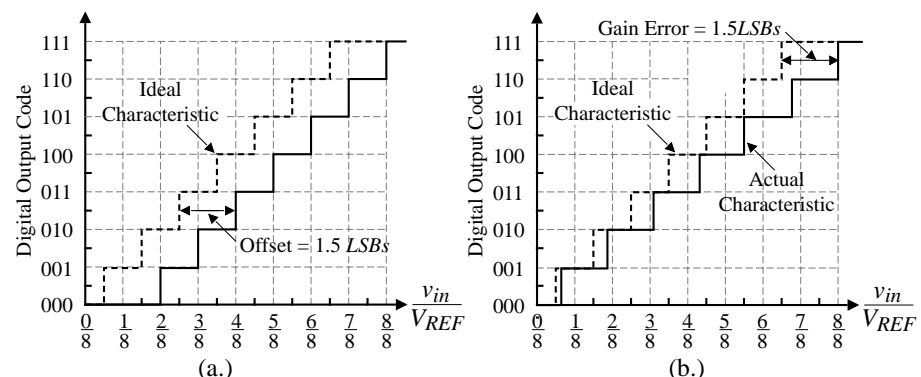


Figure 10.5-4 - (a.) Example of offset error for a 3-bit ADC. (b.) Example of gain error for a 3-bit ADC.

Integral and Differential Nonlinearity

The integral and differential nonlinearity of the ADC are referenced to the vertical (digital) axis of the transfer characteristic.

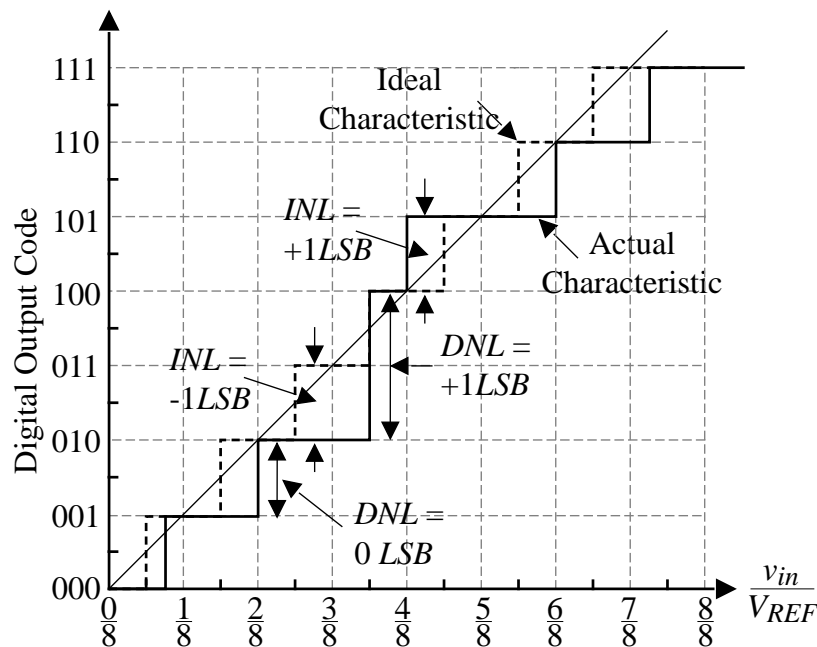
- *Integral Nonlinearity (INL)* is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*)
- *Differential Nonlinearity (DNL)* is a measure of the separation between adjacent levels measured at each vertical step (% or *LSB*).

$$DNL = (D_{cx} - 1) \text{ LSBs}$$

where D_{cx} is the size of the actual vertical step in *LSBs*.

Note that *INL* and *DNL* of an analog-digital converter will be in terms of integers in contrast to the *INL* and *DNL* of the digital-analog converter. As the resolution of the ADC increases, this restriction becomes insignificant.

Example of INL and DNL



Example of *INL* and *DNL* for a 3-bit ADC.) Fig.10.5-5

Note that the *DNL* and *INL* errors can be specified over some range of the analog input.

Monotonicity

A *monotonic* ADC has all vertical jumps positive. Note that monotonicity can only be detected by *DNL*.

Example of a nonmonotonic ADC:

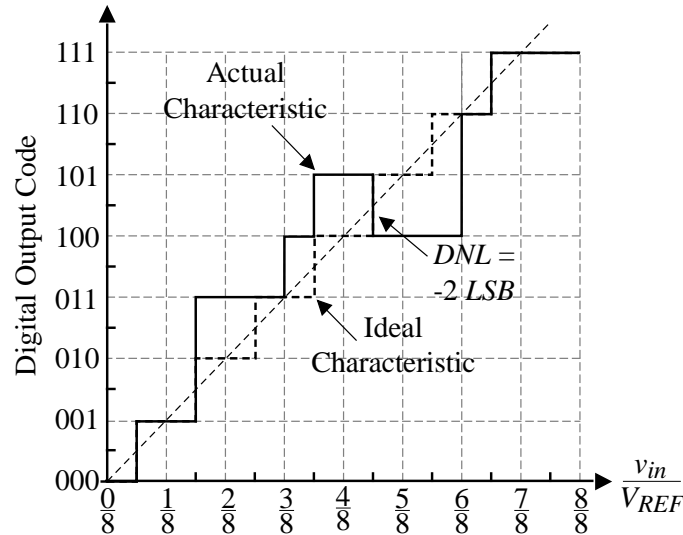


Fig. 10.5-6L

If a vertical jump is $2LSB$ or greater, missing output codes may result.
If a vertical jump is $-1LSB$ or less, the ADC is not monotonic.

Example 10.5-1 - *INL* and *DNL* of a 3-bit ADC

Find the *INL* and *DNL* for the 3-bit ADC shown on the previous slide.

Solution

With respect to the digital axis:

- 1.) The largest value of *INL* for this 3-bit ADC occurs between $3/16$ to $5/16$ or $7/16$ to $9/16$ and is $1LSB$.
- 2.) The smallest value of *INL* occurs between $11/16$ to $12/16$ and is $-2LSB$.
- 3.) The largest value of *DNL* occurs at $3/16$ or $6/8$ and is $+1LSB$.
- 4.) The smallest value of *DNL* occurs at $9/16$ and is $-2LSB$ which is where the converter becomes nonmonotonic.

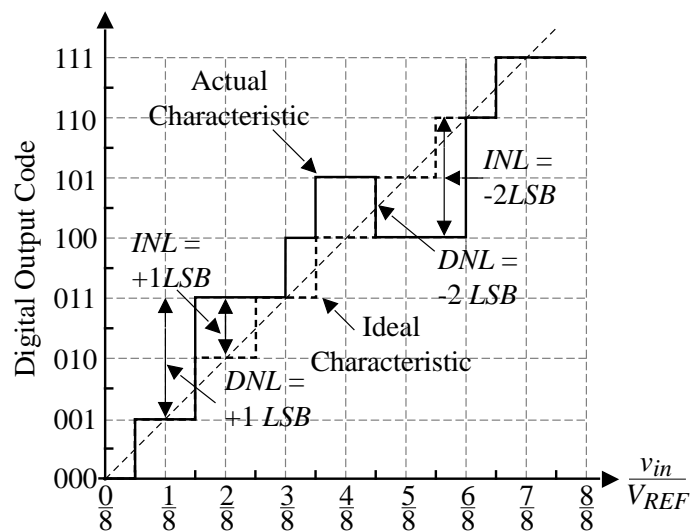


Fig. 10.5-6DL

DYNAMIC CHARACTERISTICS

What are the Important Dynamic Characteristics for ADCs?

The dynamic characteristics of ADCs are influenced by:

- Comparators
 - Linear response
 - Slew response
- Sample-hold circuits
- Circuit parasitics
- Logic propagation delay

Comparator

The comparator is the quantizing unit of ADCs.

Open-loop model:

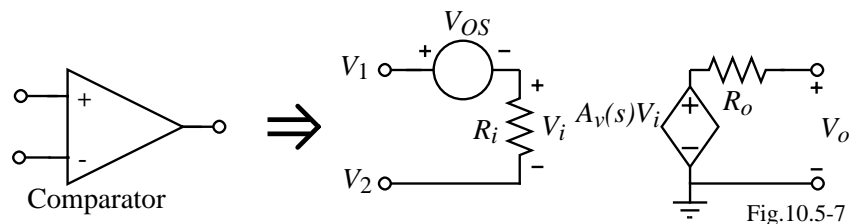


Fig.10.5-7

Nonideal aspects:

- Input offset voltage, V_{OS} (a static characteristic)
- Propagation time delay
 - Bandwidth (linear)

$$A_v(s) = \frac{A_v(0)}{\frac{s}{\omega_c} + 1} = \frac{A_v(0)}{s\tau_c + 1}$$

- Slew rate (nonlinear)

$$\Delta T = \frac{C \cdot \Delta V}{I} \quad (I \text{ constant}) = \frac{\Delta V}{\text{Slew Rate}}$$

Example 10.5-2 (Ex. 8.1-1) - Propagation Delay Time of a Comparator

Find the propagation delay time of an open loop comparator that has a dominant pole at 10^3 radians/sec, a dc gain of 10^4 , a slew rate of $1\text{V}/\mu\text{s}$, and a binary output voltage swing of 1V . Assume the applied input voltage is 10mV .

Solution

The input resolution for this comparator is $1\text{V}/10^4$ or 0.1mV . Therefore, the 10mV input is 100 times larger than $v_{in(\text{min})}$ giving a k of 100. Therefore, we get

$$t_p = \frac{1}{10^3} \ln\left(\frac{2 \cdot 100}{2 \cdot 100 - 1}\right) = 10^{-3} \ln\left(\frac{200}{199}\right) = 5.01\mu\text{s}$$

For slew rate considerations, we get

$$\text{Maximum slope} = \frac{10^4}{10^{-3}} \cdot 10\text{mV} = 10^5 \text{ V/sec.} = 0.1\text{V}/\mu\text{s}.$$

Therefore, the propagation delay time for this case is limited by the linear response and is $5.01\mu\text{s}$.

SAMPLE AND HOLD CIRCUITS**Requirements of a Sample and Hold Circuit**

The objective of the sample and hold circuit is to sample the unknown analog signal and hold that sample while the ADC decodes the digital equivalent output.

The sample and hold circuit must:

- 1.) Have the accuracy required for the ADC resolution, i.e. $\text{accuracy} = \frac{100\%}{2^N}$
- 2.) The sample and hold circuit must be fast enough to work in a two-phase clock. For an ADC with a 100 Megasample/second sample rate, this means that the sample and hold must perform its function within 5 nanoseconds.
- 3.) Precisely sample the analog signal at the same time for each clock. An advantage of the sample and hold circuit is that it removes the precise timing requirements from the ADC itself.
- 4.) The power dissipation of the sample and hold circuit must be small. The above requirements for accuracy and speed will mean that the power must be increased as the bits are increased and/or the clock period reduced.

Sample-and-Hold Circuit

Waveforms of a sample-and-hold circuit:

Definitions:

- *Acquisition time* (t_a) = time required to acquire the analog voltage
- *Settling time* (t_s) = time required to settle to the final held voltage to within an accuracy tolerance

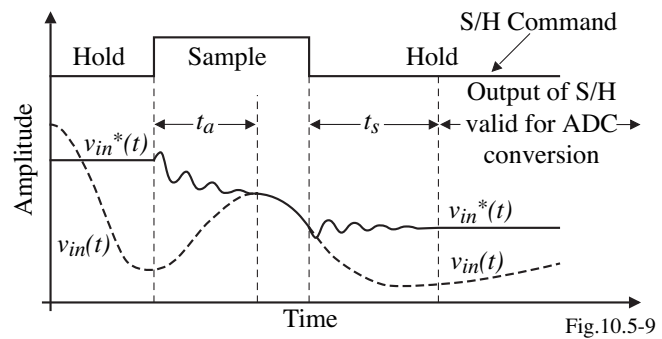


Fig.10.5-9

$$\therefore T_{sample} = t_a + t_s \quad \rightarrow \quad \text{Maximum sample rate} = f_{sample}(\max) = \frac{1}{T_{sample}}$$

Other considerations:

- *Aperture time* = the time required for the sampling switch to open after the S/H command is initiated
- *Aperture jitter* = variation in the aperture time due to clock variations and noise

Types of S/H circuits:

- No feedback - faster, less accurate
- Feedback - slower, more accurate

Open-Loop, Buffered S/H Circuit

Circuit:

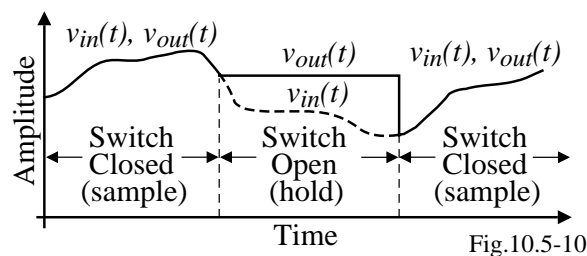
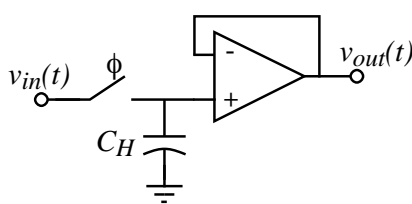


Fig.10.5-10

Attributes:

- Fast, open-loop
- Requires current from the input to charge C_H
- DC voltage offset of the op amp and the charge feedthrough of the switch will create dc errors

Settling Time

Assume the op amp has a dominant pole at $-\omega_a$ and a second pole at $-GB$.

The unity-gain response can be approximated as, $A(s) \approx \frac{GB^2}{s^2 + GB \cdot s + GB^2}$

The resulting step response is, $v_{out}(t) = 1 - \left(\sqrt{\frac{4}{3}} e^{-0.5GB \cdot t} \right) \sin\left(\sqrt{\frac{3}{4}} GB \cdot t + \phi \right)$

Defining the error as the difference between the final normalized value and $v_{out}(t)$, gives,

$$\text{Error}(t) = \varepsilon = 1 - v_{out}(t) = \sqrt{\frac{4}{3}} e^{-0.5GB \cdot t}$$

In most ADCs, the error is equal to $\pm 0.5LSB$. Since the voltage is normalized,

$$\frac{1}{2^{N+1}} = \sqrt{\frac{4}{3}} e^{-0.5GB \cdot t_s} \rightarrow e^{0.5GB \cdot t_s} = \frac{4}{\sqrt{3}} 2^N$$

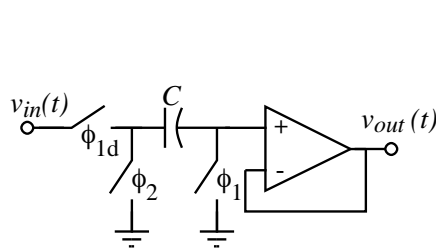
Solving for the time, t_s , required to settle with $\pm 0.5LSB$ from the above equation gives

$$t_s = \frac{2}{GB} \ln\left(\frac{4}{\sqrt{3}} 2^N \right) = \frac{1}{GB} [1.3863N + 1.6740]$$

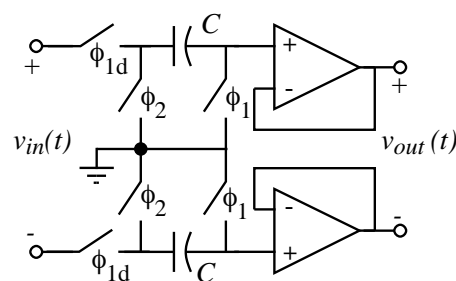
Thus as the resolution of the ADC increases, the settling time for any unity-gain buffer amplifiers will increase. For example, if we are using the open-loop, buffered S/H circuit in a 10 bit ADC, the amount of time required for the unity-gain buffer with a GB of 1MHz to settle to within 10 bit accuracy is $2.473\mu s$.

Open-Loop, Switched-Capacitor S/H Circuit

Circuit:



Switched capacitor S/H circuit.



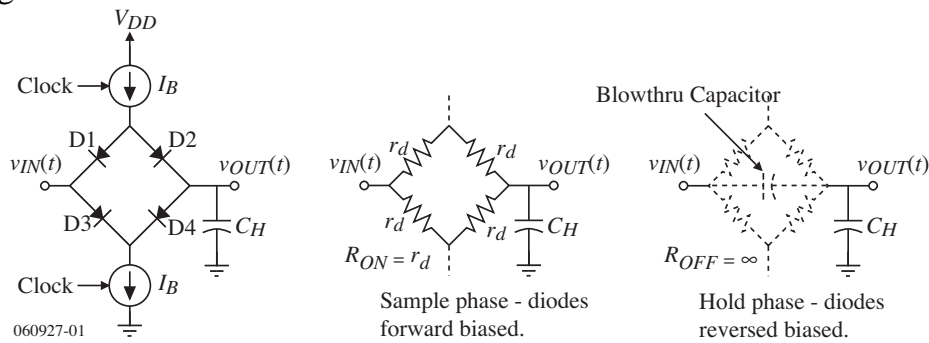
Differential switched-capacitor S/H

Fig.10.5-11

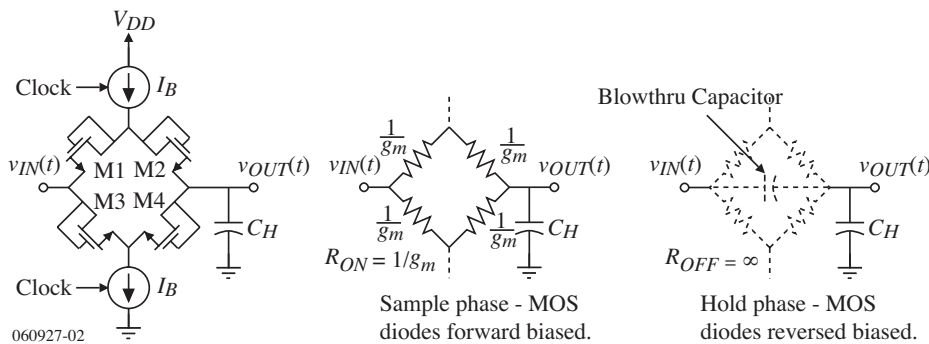
- Delayed clock used to remove input dependent feedthrough.
- Differential version has lower $PSRR$, cancellation of even harmonics, and reduction of charge injection and clock feedthrough

Open-Loop, Diode Bridge S/H Circuit

Diode bridge S/H circuit:



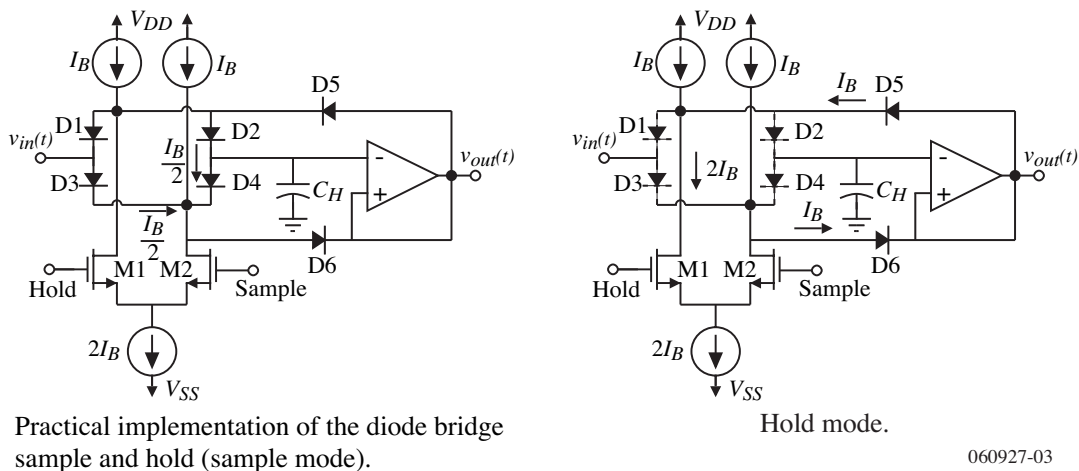
MOS diode bridge S/H circuit:



CMOS Analog Circuit Design

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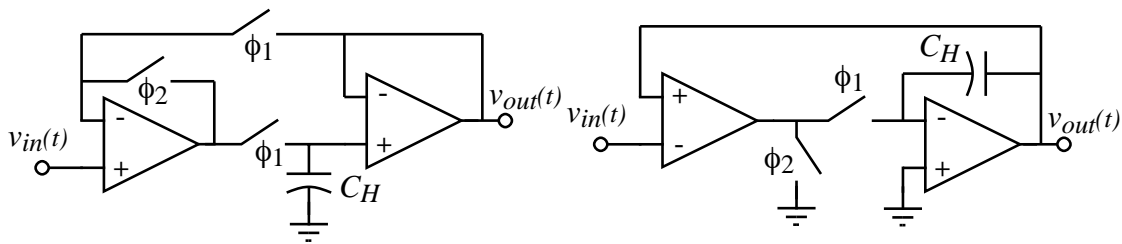
Practical Implementation of the Diode Bridge S/H Circuit



During the hold mode, the diodes D5 and D6 become forward biased and clamp the upper and lower nodes of the sampling bridge to the sampled voltage.

Closed-Loop S/H Circuit

Circuit:



Closed-loop S/H circuit. ϕ_1 is the sample phase and ϕ_2 is the hold phase.

An improved version.

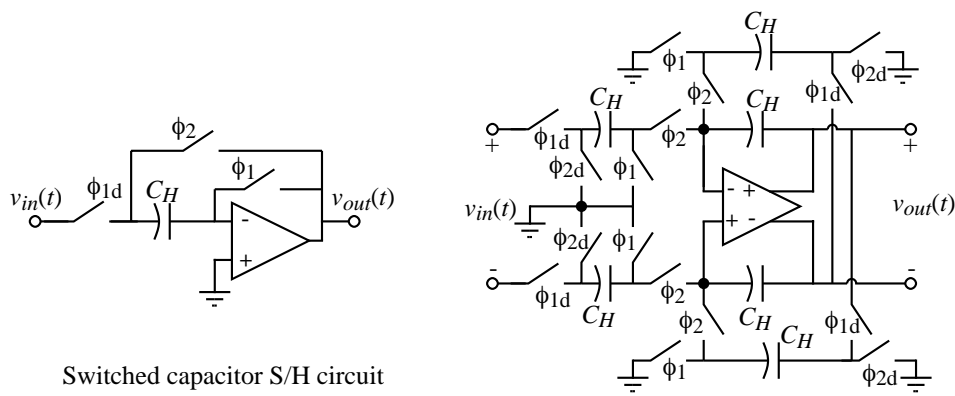
Fig.10.5-13

Attributes:

- Accurate
- First circuit has signal-dependent feedthrough
- Slower because of the op amp feedback loop

Closed-Loop, Switched Capacitor S/H Circuits

Circuit:



Switched capacitor S/H circuit which autozeroes the op amp input offset voltage.

A differential version that avoids large changes at the op amp output

Fig.10.5-14

Attributes:

- Accurate
- Signal-dependent feedthrough eliminated by a delayed clock
- Differential circuit keeps the output of the op amps constant during the ϕ_1 phase avoiding slew rate limits

Current-Mode S/H Circuit

Circuit:

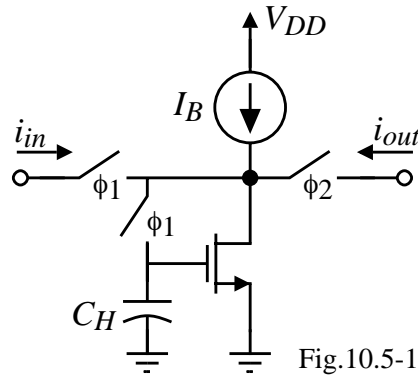


Fig.10.5-15

Attributes:

- Fast
- Requires current in and out
- Good for low voltage implementations

Aperature Jitter in S/H Circuits

Illustration:

If we assume that $v_{in}(t) = V_p \sin \omega t$, then the maximum slope is equal to ωV_p .

Therefore, the value of ΔV is given as

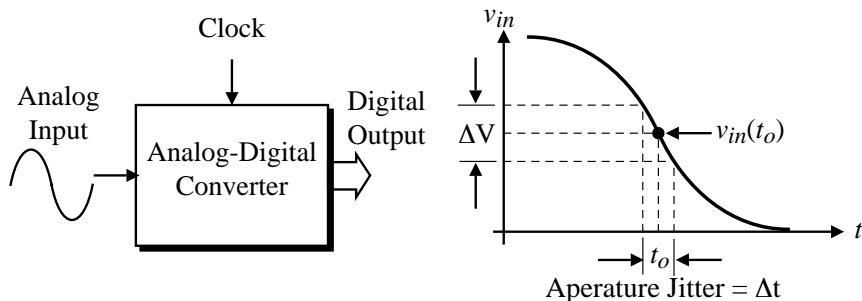


Figure10.5-14 - Illustration of aperature jitter in an ADC.

$$\Delta V = \left| \frac{dv_{in}}{dt} \right| \Delta t = \omega V_p \Delta t .$$

The rms value of this noise is given as

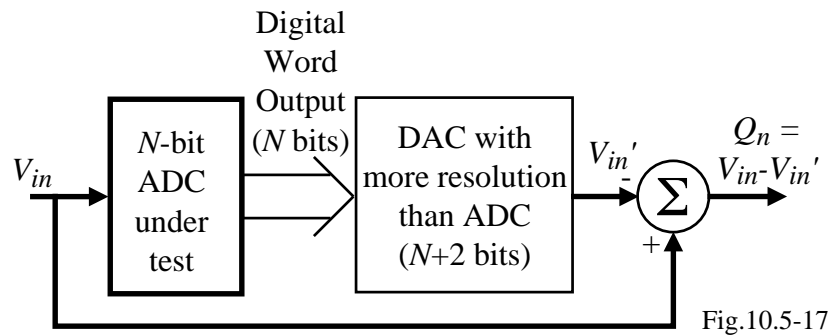
$$\Delta V(\text{rms}) = \left| \frac{dv_{in}}{dt} \right| \Delta t = \frac{\omega V_p \Delta t}{\sqrt{2}} .$$

The aperature jitter can lead to a limitation in the desired dynamic range of an ADC. For example, if the aperature jitter of the clock is 100ps, and the input signal is a full scale peak-to-peak sinusoid at 1MHz, the rms value of noise due to this aperature jitter is 111μV(rms) if the value of $V_{REF} = 1\text{V}$.

TESTING OF ADCs

Input-Output Test for an ADC

Test Setup:

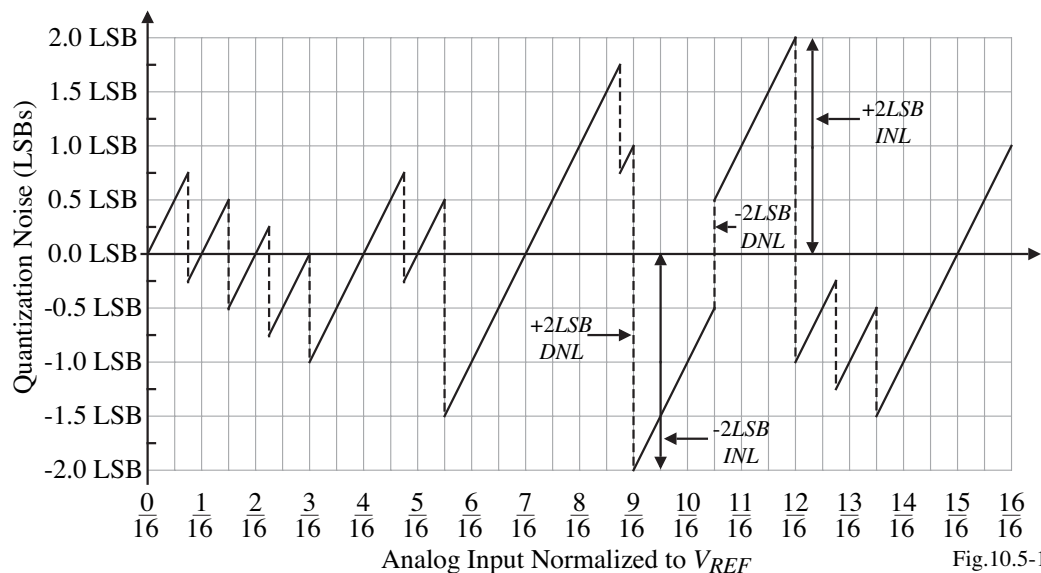


The ideal value of Q_n should be within $\pm 0.5LSB$

Can measure:

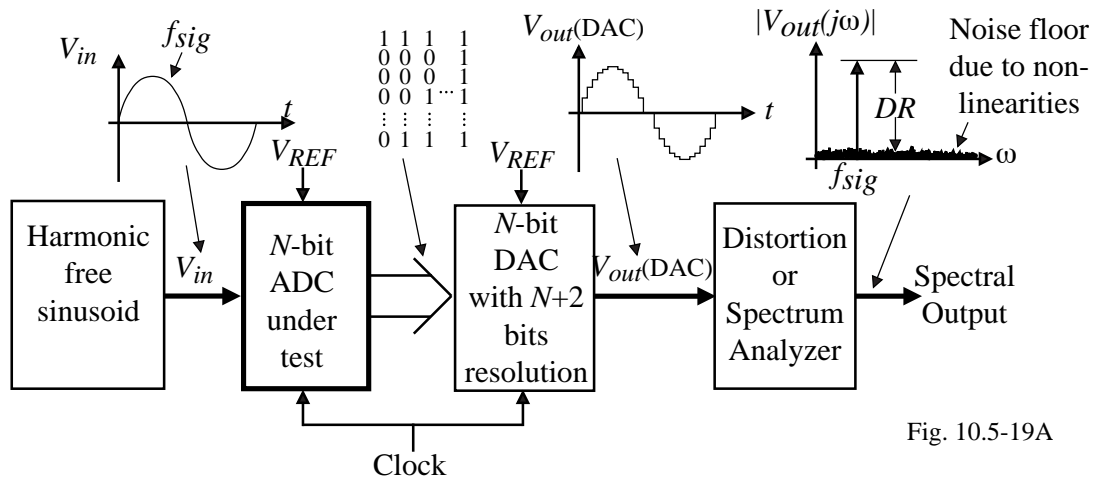
- Offset error = constant shift above or below the 0 LSB line
- Gain error = constant increase or decrease of the sawtooth plot as V_{in} is increased
- INL and DNL (see following page)

Illustration of the Input-Output Test for a 4-Bit ADC



Measurement of Nonlinearity Using a Pure Sinusoid

This test applies a pure sinusoid to the input of the ADC. Any nonlinearity will appear as harmonics of the sinusoid. Nonlinear errors will occur when the dynamic range (DR) is less than $6N$ dB where N = number of bits.

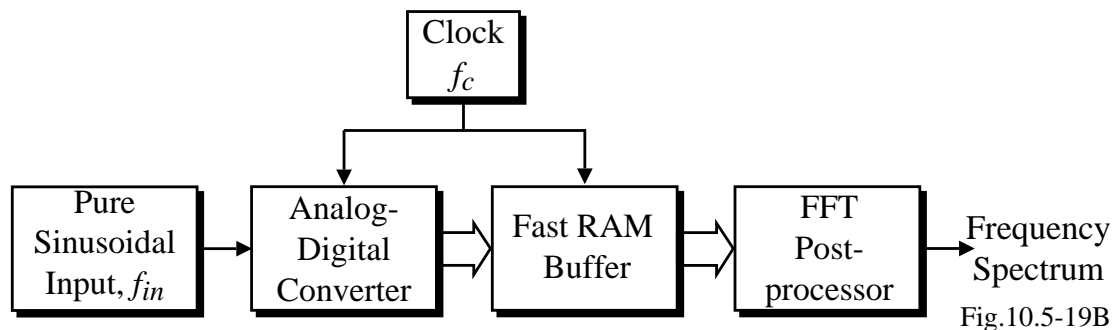


Comments:

- Input sinusoid must have less distortion than the required dynamic range
- DAC must have more accuracy than the ADC

FFT Test for an ADC

Test setup:



Comments:

- Stores the digital output codes of the ADC in a RAM buffer
- After the measurement, a postprocessor uses the FFT to analyze the quantization noise and distortion components
- Need to use a window to eliminate measurement errors (Raised Cosine or 4-term Blackmann-Harris are often used)
- Requires a spectrally pure sinusoid

Histogram Test for an ADC

The number of occurrences of each digital output code is plotted as a function of the digital output code.

Illustration:

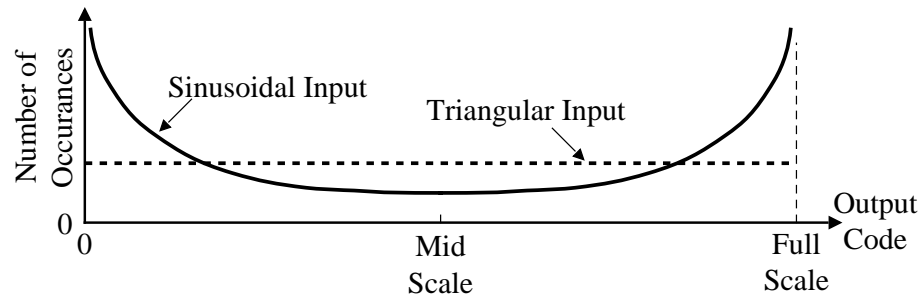


Fig.10.5-20

Comments:

- Emphasizes the time spent at a given level and can show *DNL* and missing codes
- *DNL*

$$DNL(i) = \frac{\text{Width of the bin as a fraction of full scale}}{\text{Ratio of the bin width to the ideal bin width}} - 1 = \frac{H(i)/N_t}{P(i)} - 1$$

where

$H(i)$ = number of counts in the i th bin

N_t = total number of samples

$P(i)$ = ratio of the bin width to the ideal bin width

- *INL* is found from the cumulative bin widths

Comparison of the Tests for Analog-Digital Converters

Other Tests

- Sinewave curve fitting (good for *ENOB*)
- Beat frequency test (good for a qualitative measure of dynamic performance)

Comparison

Test → Error ↓	Histogram or Code Test	FFT Test	Sinewave Curve Fit Test	Beat Frequency Test
<i>DNL</i>	Yes (spikes)	Yes (Elevated noise floor)	Yes	Yes
Missing Codes	Yes (Bin counts with zero counts)	Yes (Elevated noise floor)	Yes	Yes
<i>INL</i>	Yes (Triangle input gives <i>INL</i> directly)	Yes (Harmonics in the baseband)	Yes	Yes
Aperature Uncertainty	No	Yes (Elevated noise floor)	Yes	No
Noise	No	Yes (Elevated noise floor)	Yes	No
Bandwidth Errors	No	No	No	Yes (Measures analog bandwidth)
Gain Errors	Yes (Peaks in distribution)	No	No	No
Offset Errors	Yes (Offset of distribution average)	No	No	No

Bibliography on ADC Testing

- 1.) D. H. Sheingold, *Analog-Digital Conversion Handbook*, Analog Devices, Inc., Norwood, MA 02062, 1972.
- 2.) S.A. Tretter, *Introduction to Discrete-Time Signal Processing*, John Wiley & Sons, New York, 1976.
- 3.) J. Doernberg, H.S. Lee, and D.A. Hodges, “Full-Speed Testing of A/D Converters,” *IEEE J. of Solid-State Circuits*, Vol. SC-19, No. 6, December 1984, pp. 820-827.
- 4.) “Dynamic performance testing of A to D converters,” *Hewlett Packard Product Note* 5180A-2.

SECTION 10.6 – MODERATE SPEED ANALOG-DIGITAL CONVERTERS

INTRODUCTION

Moderate Speed ADC Topics

- Serial ADCs - require 2^NT for conversion where T = period of the clock
Types:
 - Single-slope
 - Dual-slope
- Successive approximation ADCs – require NT for conversion where T = the clock period
- 1-bit per stage, pipeline ADCs – require T for conversion after a delay of NT
- Iterative ADCs – require NT for conversion
- Self-calibration techniques

SERIAL ANALOG-DIGITAL CONVERTERS

Single-Slope ADC

Block diagram:

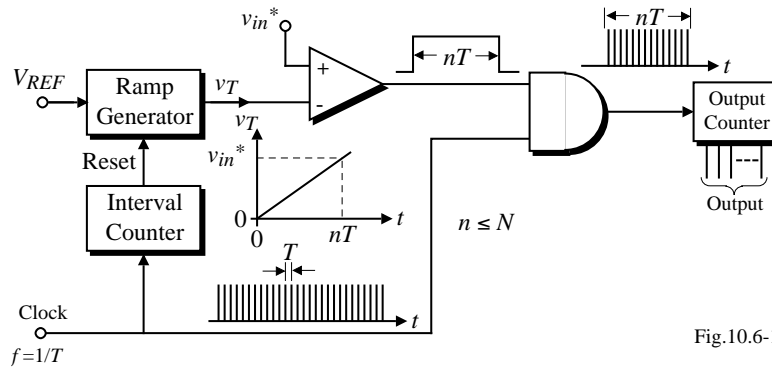


Fig.10.6-1

Attributes:

- Simplicity of operation
- Subject to error in the ramp generator
- Long conversion time $\leq 2^N T$

Dual-Slope ADC

Block diagram:

Waveforms:

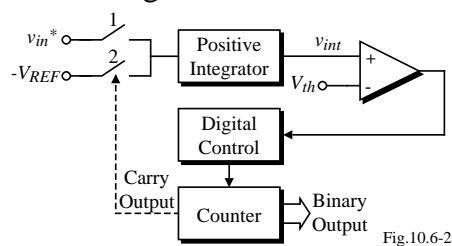


Fig.10.6-2

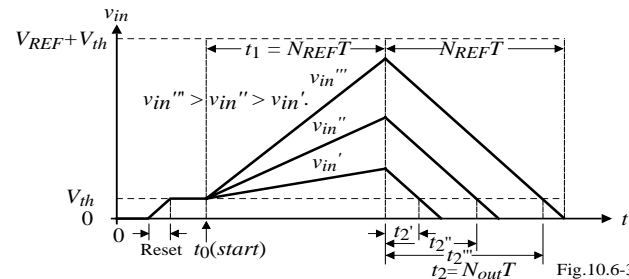


Fig.10.6-3

Operation:

- 1.) Initially $v_{int} = 0$ and v_{in} is sampled and held ($v_{IN}^* > 0$).
- 2.) Reset the positive integrator by integrating a positive voltage until $v_{int}(0) = V_{th}$.
- 3.) Integrate v_{in}^* for N_{REF} clock cycles to get,

$$v_{int}(t_1) = K \int_0^{N_{REF}T} v_{in}^* dt + v_{int}(0) = KN_{REF}T v_{in}^* + V_{th}$$

- 4.) After N_{REF} counts, the carry output of the counter closes switch 2 and $-V_{REF}$ is applied to the positive integrator. The output of the integrator at $t = t_1 + t_2$ is,

$$v_{int}(t_1 + t_2) = v_{int}(t_1) + K \int_{t_1}^{t_1 + t_2} (-V_{REF}) dt = V_{th} \rightarrow KN_{REF}T v_{in}^* + V_{th} - KN_{out}T V_{REF} = V_{th}$$

- 5.) Solving for N_{out} gives, $N_{out} = N_{REF} (v_{in}^* / V_{REF})$

Comments: Conversion time $\leq 2(2^N)T$ and the operation is independent of V_{th} and K .

SUCCESSIVE APPROXIMATION ANALOG-DIGITAL CONVERTERS

Introduction

Successive Approximation Algorithm:

- 1.) Start with the *MSB* bit and work toward the *LSB* bit.
- 2.) Guess the *MSB* bit as 1.
- 3.) Apply the digital word 10000.... to a DAC.
- 4.) Compare the DAC output with the sampled analog input voltage.
- 5.) If the DAC output is greater, keep the guess of 1. If the DAC output is less, change the guess to 0.
- 6.) Repeat for the next *MSB*.

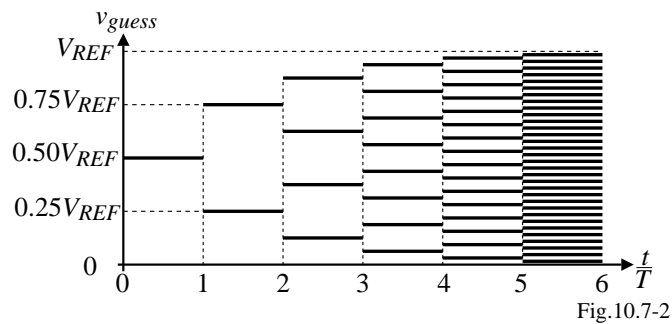


Fig.10.7-2

CMOS Analog Circuit Design

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Block Diagram of a Successive Approximation ADC[†]

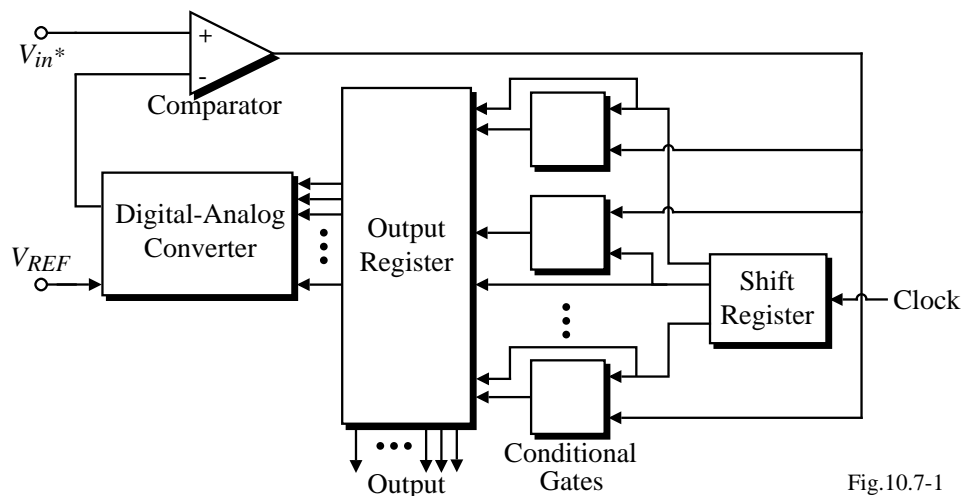


Fig.10.7-1

[†] R. Hnatek, *A User's Handbook of D/A and A/D Converters*, John Wiley and Sons, Inc., New York, NY, 1976.

5-Bit Successive Approximation ADC

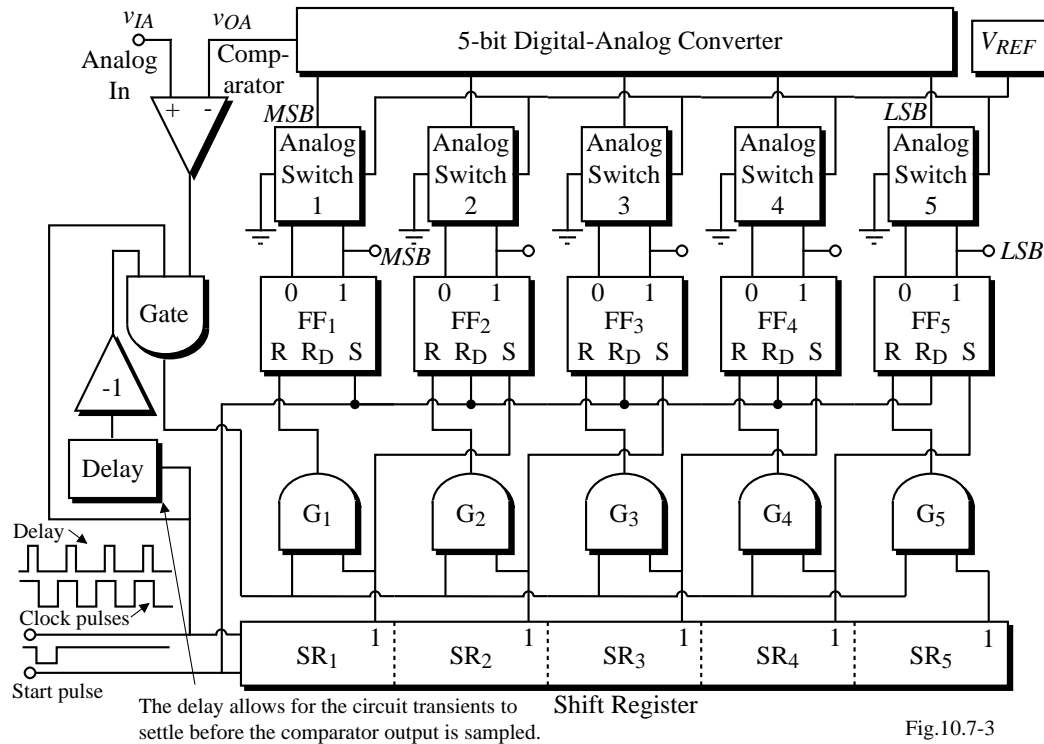


Fig.10.7-3

m -Bit Voltage-Scaling, k -Bit Charge-Scaling Successive Approximation ADC

Operation:

- 1.) With the two S_F switches closed, all capacitors are paralleled and connected to V_{in}^* which autozeros the comparator offset voltage.

- 2.) With all capacitors still in parallel, a successive approximation search is performed to find the resistor segment in which the analog signal lies.

- 3.) Finally, a successive approximation search is performed on charge scaling subDAC to establish the analog output voltage.

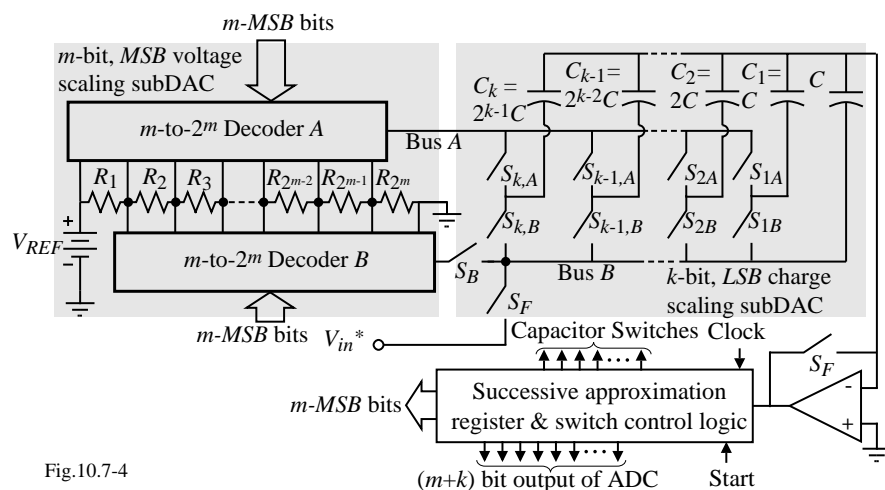


Fig.10.7-4

Voltage-Scaling, Charge-Scaling Successive Approximation ADC - Continued

Autozero Step

Removes the influence of the offset voltage of the comparator.

The voltage across the capacitor is given as,

$$v_C = V_{in}^* - V_{OS}$$

Successive Approximation Search on the Resistor String

The voltage at the comparator input is

$$v_{comp} = V_{Ri} - V_{in}^*$$

If $v_{comp} > 0$, then $V_{Ri} > V_{in}^*$, if $v_{comp} < 0$, then $V_{Ri} < V_{in}^*$

Successive Approx. Search on the Capacitor SubDAC

The input to the comparator is written as,

$$v_{comp} = (V_{Ri+1} - V_{in}^*) \frac{C_{eq}}{2^k C} + (V_{Ri} - V_{in}^*) \frac{2^k C - C_{eq}}{2^k C}$$

However, $V_{Ri+1} = V_{Ri} + 2^{-m} V_{REF}$

Combining gives,

$$\begin{aligned} v_{comp} &= (V_{Ri} + 2^{-m} V_{REF} - V_{in}^*) \frac{C_{eq}}{2^k C} + (V_{Ri} - V_{in}^*) \frac{2^k C - C_{eq}}{2^k C} \\ &= V_{Ri} - V_{in}^* + 2^{-m} V_{REF} \frac{C_{eq}}{2^k C} \end{aligned}$$

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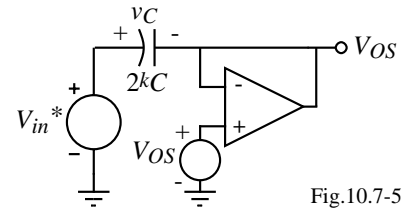


Fig. 10.7-5

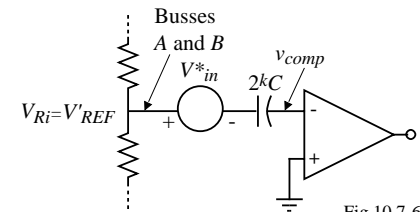


Fig. 10.7-6a

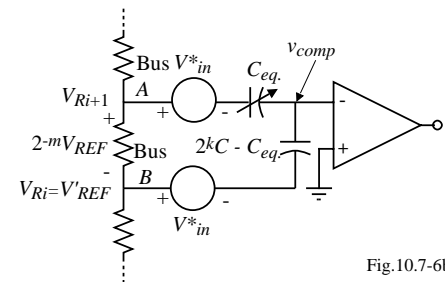


Fig. 10.7-6b

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SINGLE-BIT/STAGE, PIPELINE ANALOG-DIGITAL CONVERTERS

Single-Bit/Stage Pipeline ADC Architecture

Implementation:

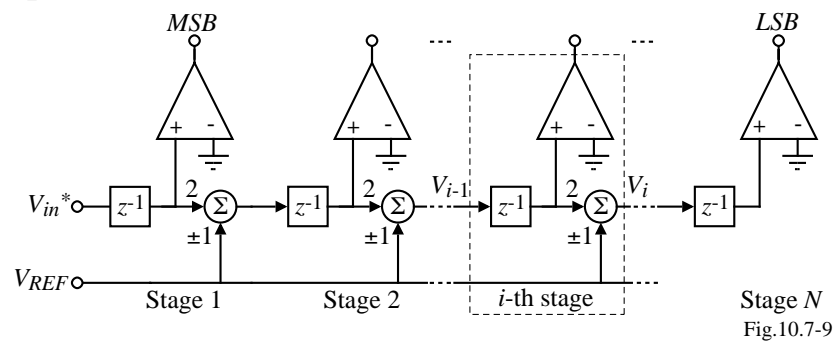


Fig. 10.7-9

Operation:

- Each stage multiplies its input by 2 and adds or subtracts V_{REF} depending upon the sign of the input.
- i -th stage,

$$V_i = 2V_{i-1} - b_i V_{REF}$$

where b_i is given as

$$b_i = \begin{cases} +1 & \text{if } V_{i-1} > 0 \\ -1 & \text{if } V_{i-1} < 0 \end{cases}$$

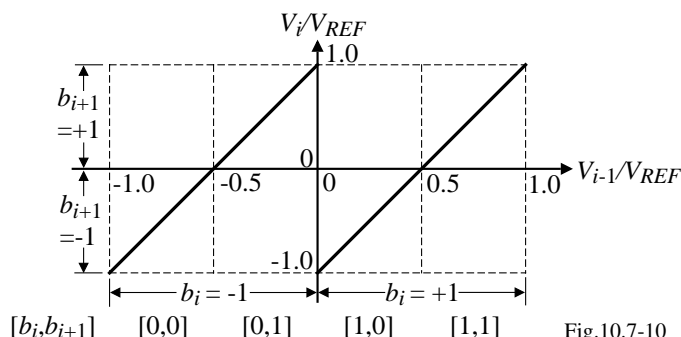


Fig. 10.7-10

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Example 10.6-1 - Illustration of the Operation of the Pipeline Algorithmic ADC

Assume that the sampled analog input to a 4-bit pipeline algorithmic analog-digital converter is 2.00 V. If V_{REF} is equal to 5 V, find the digital output word and the analog equivalent voltage.

Solution

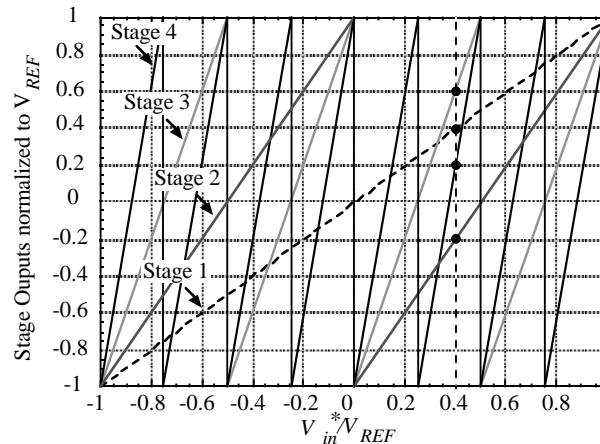
Stage No.	Input to the i th stage, V_{i-1}	$V_{i-1} > 0$?	Bit i
1	2V	Yes	1
2	$(2V \cdot 2) - 5 = -1V$	No	0
3	$(-1V \cdot 2) + 5 = 3V$	Yes	1
4	$(3V \cdot 2) - 5 = 1V$	Yes	1

Illustration:

$$V_{\text{analog}} = 5 \left(\frac{1}{2} - \frac{1}{4} + \frac{1}{8} + \frac{1}{16} \right)$$

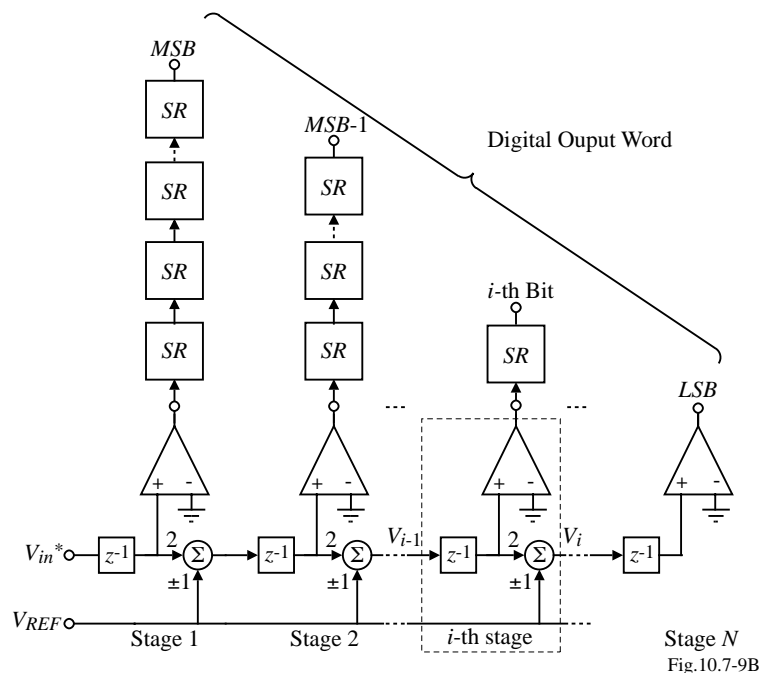
$$= 5(0.4375) = 2.1875$$

where $b_i = +1$ if the i th-bit is 1
and $b_i = -1$ if the i th bit is 0

**Achieving the High Speed Potential of the Pipeline Algorithmic ADC**

If shift registers are used to store the output bits and align them in time, the pipeline ADC can output a digital word at every clock cycle with a latency of NT .

Illustration:

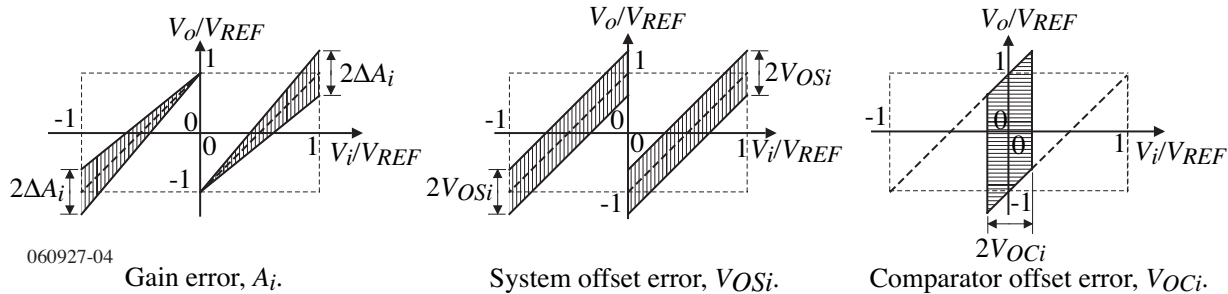


Errors in the Pipeline ADC

Types of errors:

- Gain errors – x2 amplifier or summing junctions
- Offset errors – comparators or summing junctions

Illustration of errors:

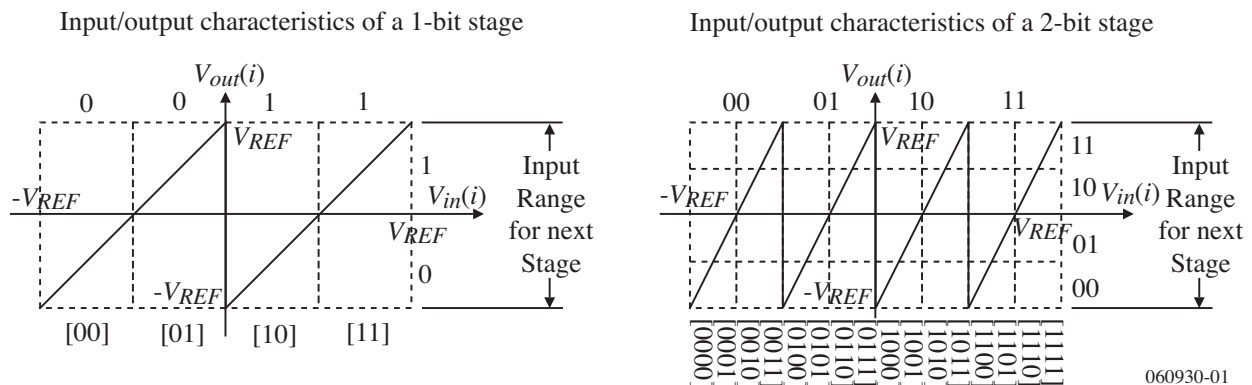


An error will occur if the output voltage of one stage exceeds $\pm V_{REF}$ (saturates).

Digital Error Correction

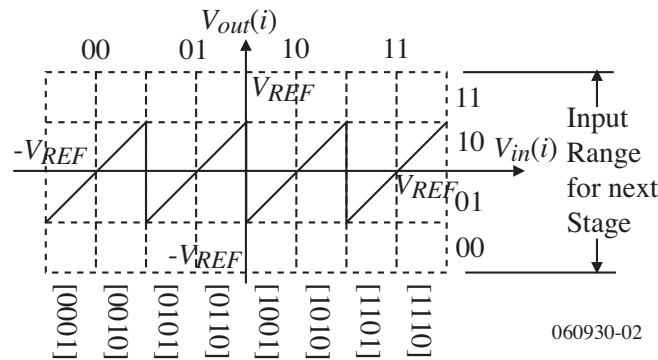
In the previous slide, we noted that if the analog output to the next stage exceeds $\pm V_{REF}$ that an error occurs. This error can be detected by adding one more bit to the following stage for the purposes of detecting the error.

Illustration (2nd bit not used for error correction):



Digital Error Correction – Continued

If the gain of 4 amplifier is reduced back to 2, the input/output characteristics of the 2-bit stage become:

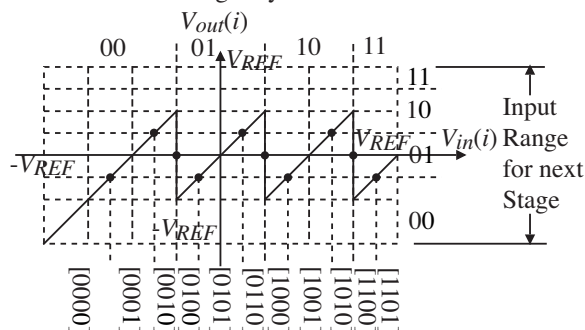


The output bits can be used to determine the error. If these bits are 00, then $0.5LSB$ must be added to get the correct digital output. If the bits are 11, then $0.5LSB$ must be subtracted to get the correct digital output.

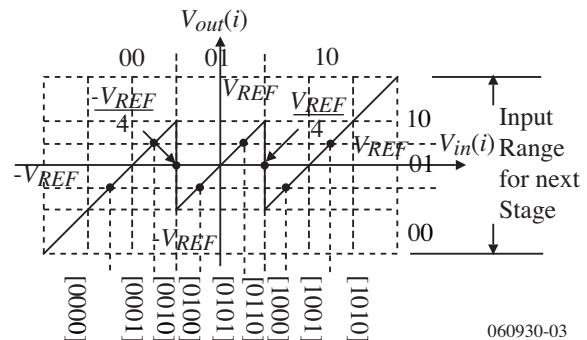
Modified Digital Error Correction (1.5 bits per stage)

In the previous slide, it was necessary sometimes to perform digital subtraction which is not easy to implement. To avoid this problem, a $0.5LSB$ shift has been added to the input/output characteristic resulting in the following.

Movement of all comparator thresholds to the right by $0.5LSB$.



Removal of the comparator at $0.75LSB$.

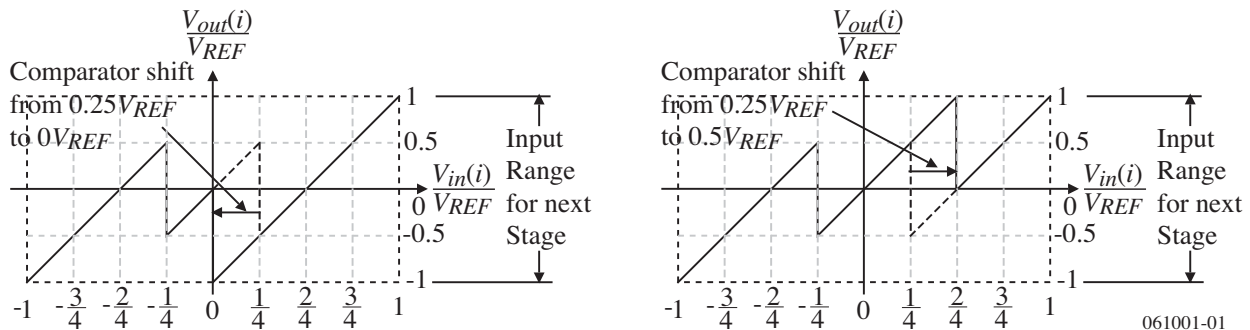


To obtain code 11 out of the stage after correction, the correction logic must increment the output of the stage.

To obtain code 00 from this stage after correction, the correction logic need do nothing. Therefore, only two comparators are needed which produce outputs of (00, 01, 10).

How Does the 1.5 Bit Stage Correct Offset Errors?

Consider a $\pm 0.25V_{REF}$ comparator offset shift in the input-output characteristics of the 1.5 bit stage.

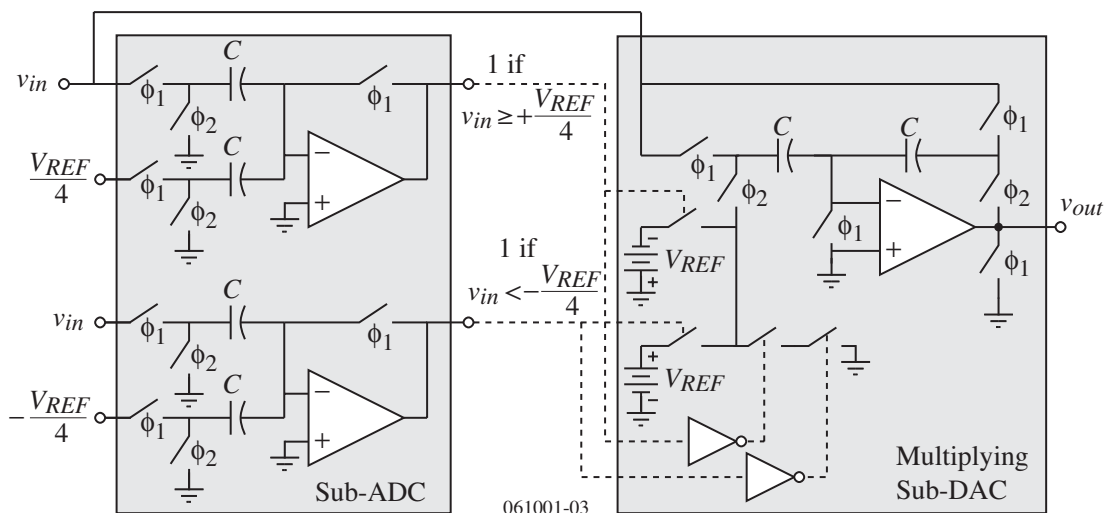


When the shift is to the left, the comparator will not be in error until the shift is greater than $0.25V_{REF}$. This is because the comparator thresholds were shifted to the right by $0.25V_{REF}$.

When the shift is to the right, the input to the next stage will be greater than $0.50V_{REF}$. This will cause the output code 10 which indicates that the digital word should be incremented by 1 bit.

The range of correction $\pm V_{REF}/2^{B+1}$ where B is the number of bits per stage.

Implementation of the 1.5 Bit Stage



The multiplying Sub-DAC must implement the following equation:

$$V_{out} = \begin{cases} 2 \cdot v_{in} - V_{REF} & \text{if } v_{in} > V_{REF}/4 \\ 2 \cdot v_{in} & \text{if } -V_{REF}/4 \leq v_{in} \leq V_{REF}/4 \\ 2 \cdot v_{in} + V_{REF} & \text{if } v_{in} < -V_{REF}/4 \end{cases}$$

Example 10.6-2 - Accuracy requirements for a 5-bit pipeline algorithmic ADC

Show that if $V_{in} = V_{REF}$, that the pipeline algorithmic ADC will have an error in the 5th bit if the gain of the first stage is $2-(1/8) = 1.875$ which corresponds to when an error will occur. Show the influence of V_{in} on this result for V_{in} of $0.65V_{REF}$ and $0.22V_{REF}$.

Solution

For $V_{in} = V_{REF}$, we get the results shown below. The input to the fifth stage is 0V which means that the bit is uncertain. If A_1 was slightly less than 1.875, the fifth bit would be 0 which is in error. This result assumes that all stages but the first are ideal.

i	$V_i(\text{ideal})$	Bit i (ideal)	$V_i(A_1=1.875)$	Bit i ($A_1=1.875$)
1	1	1	1.000	1
2	1	1	0.875	1
3	1	1	0.750	1
4	1	1	0.500	1
5	1	1	0.000	?

Now let us repeat the above results for $V_{in} = 0.65V_{REF}$. The results are shown below.

i	$V_i(\text{ideal})$	Bit i (ideal)	$V_i(A_1=1.875)$	Bit i ($A_1=1.875$)
1	+0.65	1	0.6500	1
2	+0.30	1	0.2188	1
3	-0.40	0	-0.5625	0
4	+0.20	1	-0.1250	0
5	-0.60	0	0.7500	1

Example 10.6-2 - Continued

Next, we repeat for the results for $V_{in} = 0.22V_{REF}$. The results are shown below. We see that no errors occur.

i	$V_i(\text{ideal})$	Bit i (ideal)	$V_i(A_1=1.875)$	Bit i ($A_1=1.875$)
1	+0.22	1	0.2200	1
2	-0.56	0	-0.5875	0
3	-0.12	0	-0.1750	0
4	+0.76	1	0.6500	1
5	+0.52	1	0.3000	1

Note the influence of V_{in} in the fact that an error occurs for $A_1 = 1.875$ for $V_{in} = 0.65V_{REF}$ but not for $V_{in} = 0.22V_{REF}$. Why? Note on the plot for the output of each stage, that for $V_{in} = 0.65V_{REF}$, the output of the fourth stage is close to 0V so any small error will cause problems. However, for $V_{in} = 0.22V_{REF}$, the output of the fourth stage is at $0.65V_{REF}$ which is further away from 0V and is less sensitive to errors.

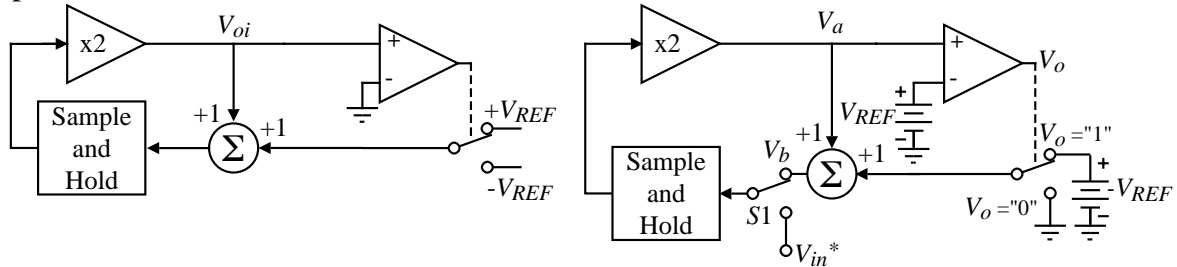
\therefore The most robust values of V_{in} will be near $-V_{REF}$, 0 and $+V_{REF}$. or when each stage output is furthest from the comparator threshold, 0V.

ITERATIVE ANALOG-DIGITAL CONVERTERS

Iterative (Cyclic) Algorithmic Analog-Digital Converter

The pipeline algorithmic ADC can be reduced to a single stage that cycles the output back to the input.

Implementation:



Iterative algorithm ADC

Different version of iterative algorithm ADC implementation

Fig. 10.7-13

Operation:

- 1.) Sample the input by connecting switch $S1$ to V_{in}^* .
- 2.) Multiply V_{in}^* by 2.
- 3.) If $V_a > V_{REF}$, set the corresponding bit = 1 and subtract V_{REF} from V_a .
If $V_a < V_{REF}$, set the corresponding bit = 0 and add zero to V_a .
- 4.) Repeat until all N bits have been converted.

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Example 10.6-3 - Conversion Process of an Iterative, Algorithmic Analog-Digital Converter

The iterative, algorithmic analog-digital converter is to be used to convert an analog signal of $0.8V_{REF}$. The figure below shows the waveforms for V_a and V_b during the process. T is the time for one iteration cycle.

- 1.) The analog input of $0.8V_{REF}$ gives $V_a = 1.6V_{REF}$ and $V_b = 0.6V_{REF}$ and the *MSB* as 1.
 - 2.) V_b is multiplied by two to give $V_a = 1.2V_{REF}$. The next bit is also 1 and $V_b = 0.2V_{REF}$.
 - 3.) The third iteration gives $V_a = 0.4V_{REF}$, making the next bit is 0 and $V_b = 0.4V_{REF}$.
 - 4.) The fourth iteration gives $V_a = 0.8V_{REF}$, giving $V_b = 0.8V_{REF}$ and the fourth bit as 0.
 - 5.) The fifth iteration gives $V_a = 1.6V_{REF}$, $V_b = 0.6V_{REF}$ and the fifth bit as 1.
- The digital word after the fifth iteration is 11001 and is equivalent to an analog voltage of $0.78125V_{REF}$.

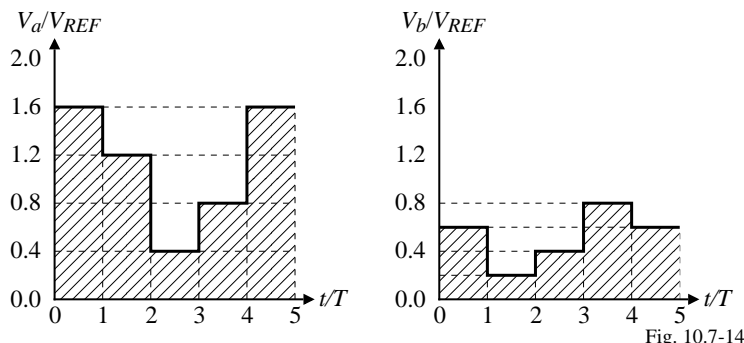
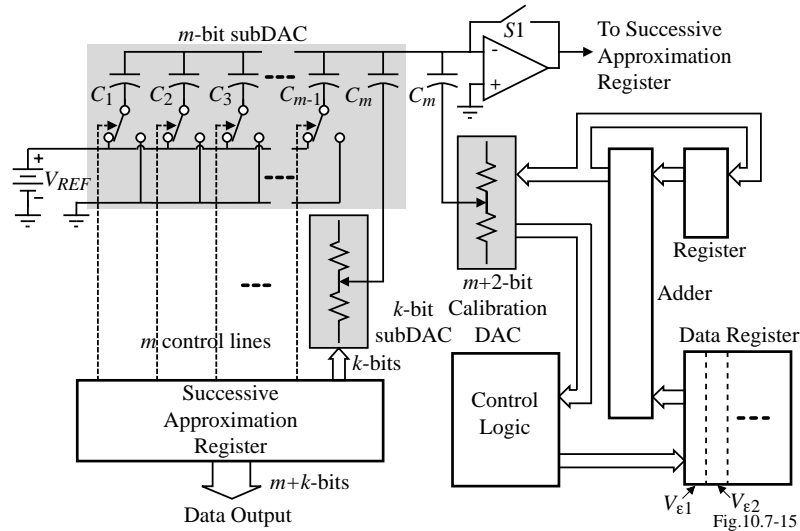


Fig. 10.7-14.

SELF-CALIBRATION TECHNIQUES

Self-Calibrating Analog-Digital Converters

Self-calibration architecture for a m -bit charge scaling, k -bit voltage scaling successive approximation ADC



Comments:

- Self-calibration can be accomplished during a calibration cycle or at start-up
- In the above scheme, the *LSB* bits are not calibrated
- Calibration can extend the resolution to 2-4 bits more than without calibration

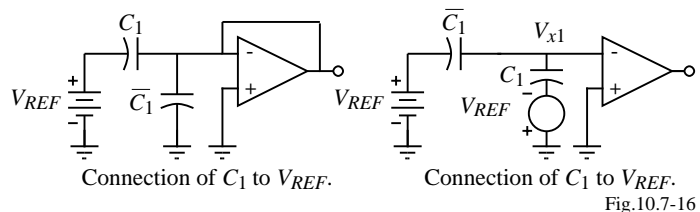
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Self-Calibrating Analog-Digital Converters - Continued

Self-calibration procedure starting with the *MSB* bit:

- 1.) Connect C_1 to V_{REF} and the remaining capacitors ($C_2+C_3+\dots+C_m+C_m=\overline{C_1}$) to ground and close S_F .
- 2.) Next, connect C_1 to ground and $\overline{C_1}$ to V_{REF} .



- 3.) The result will be $V_{x1} = \left(\frac{\overline{C_1} - C_1}{C_1 + \overline{C_1}} \right) V_{REF}$. If $C_1 = \overline{C_1}$, then $V_{x1} = 0$.
- 4.) If $V_{x1} \neq 0$, then the comparator output will be either high or low. Depending on the comparator output, the calibration circuitry makes a correction through the calibration DAC until the comparator output changes. At this point the *MSB* is calibrated and the *MSB* correction voltage, $V_{\epsilon 1}$ is stored.
- 5.) Proceed to the next *MSB* with C_1 out of the array and repeat for C_2 and $\overline{C_2}$. Store the correction voltage, $V_{\epsilon 2}$, in the data register.
- 6.) Repeat for C_3 with C_1 and C_2 out of the array. Continue until all of the capacitors of the *MSB* DAC have been corrected.

Note: For normal operation, the circuit adds the correct *combined* correction voltage.

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Summary of Moderate Speed Analog-Digital Converters

Type of ADC	Advantage	Disadvantage
Serial ADC	High resolution	Slow
Voltage-scaling, charge-scaling successive approximation ADC	High resolution	Requires considerable digital control circuitry
Successive approximation using a serial DAC	Simple	Slow
Pipeline algorithmic ADC	Fast after initial latency of NT	Accuracy depends on input
Iterative algorithmic ADC	Simple	Requires other digital circuitry

Successive approximation ADCs also can be calibrated extending their resolution 2-4 bits more than without calibration.

SECTION 10.7 - HIGH SPEED ANALOG-DIGITAL CONVERTERS

INTRODUCTION

Characteristics of High-Speed ADCs

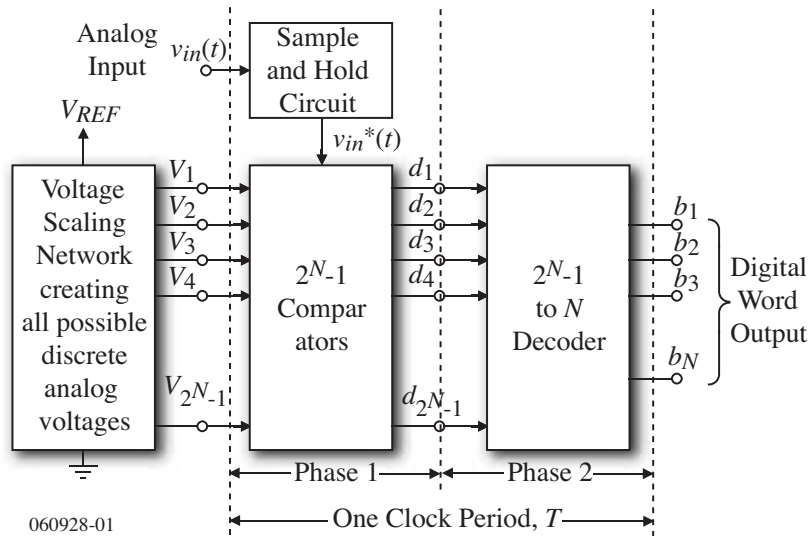
Conversion time is T where T is a clock period.

Types:

- Parallel or Flash ADCs
- Interpolating/averaging ADCs
- Folding ADCs
- Speed-Area Tradeoffs
 - Multiple-Bit, Pipeline ADCs
 - Digital Error Correction
- Time-Interleaved ADCs

PARALLEL/FLASH ADCs

Parallel/Flash ADC Architecture



- The notation, $v_{in}^*(t)$, means the signal is sampled and held.
- The sample and hold function can be incorporated into the comparators
- The digital words designated as d_i form a thermometer code

A 3-bit, parallel ADC

General Comments:

- Fast, in the first phase of the clock the analog input is sampled and applied to the comparators. In the second phase, the digital encoding network determines the correct output digital word.
- Number of comparators required is 2^N-1 which can become large if N is large
- The offset of the comparators must be less than $\pm V_{REF}/2^{N+1}$
- Errors occur as “bubbles” in the thermometer code and can be corrected with additional circuitry
- Typical sampling frequencies can be as high as 1000MHz for 6-bits in sub-micron CMOS technology.

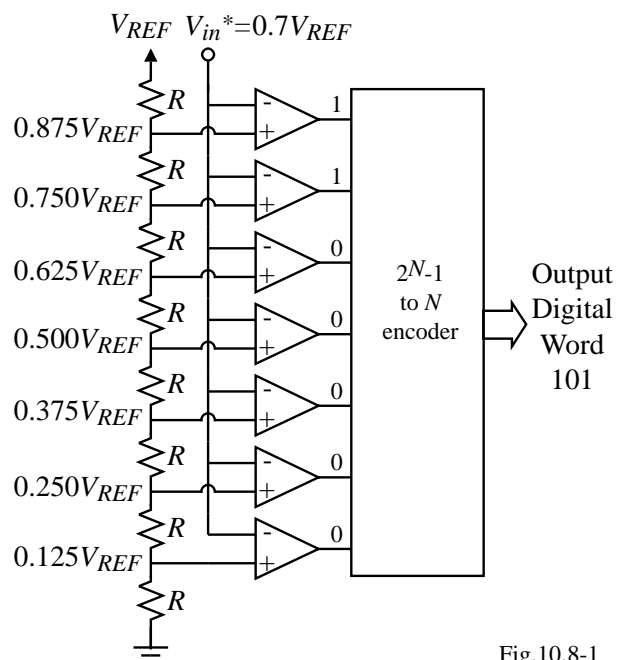


Fig.10.8-1

Example 10.7-1 - Comparator Bandwidth Limitations on the Flash ADC

The comparators of a 6-bit, flash ADC have a dominant pole at 10^4 radians/sec, a dc gain of 10^4 , a slew rate of $10\text{V}/\mu\text{s}$, and a binary output voltage of 1V and 0V. Assume that the conversion time is the time required for the comparator to go from its initial state to halfway to its final state. What is the maximum conversion rate of this ADC if $V_{REF} = 1\text{V}$? Assume the resistor ladder is ideal.

Solution:

The output of the i -th comparator can be found by taking the inverse Laplace transform of,

$$\mathcal{L}^{-1}\left[V_{out}(s) = \left(\frac{A_o}{(s/10^4) + 1}\right) \cdot \left(\frac{V_{in}^* - V_{Ri}}{s}\right)\right] \rightarrow v_{out}(t) = A_o(1 - e^{-10^4 t})(V_{in}^* - V_{Ri}).$$

The worst case occurs when

$$V_{in}^* - V_{Ri} = 0.5V_{LSB} = V_{REF}/2^7 = 1/128$$

$$\therefore 0.5\text{V} = 10^4(1 - e^{-10^4 T})(1/128) \rightarrow 64 \times 10^{-4} = 1 - e^{-10^4 T}$$

$$\text{or, } e^{10^4 T} = 1 - 64 \times 10^{-4} = 0.9936 \rightarrow T = 10^{-4} \ln(1.0064) = 0.6421 \mu\text{s}$$

$$\therefore \text{Maximum conversion rate} = \frac{1}{0.6421 \mu\text{s}} = 1.557 \times 10^6 \text{ samples/second}$$

Checking the slew rate shows that it does not influence the maximum conversion rate.

$$\text{SR} = 10\text{V}/\mu\text{s} \rightarrow \frac{\Delta V}{\Delta T} = 10\text{V}/\mu\text{s} \rightarrow \Delta V = 10\text{V}/\mu\text{s}(0.6421 \mu\text{s}) = 6.421\text{V} > 1\text{V}$$

Physical Consequences of High Speed Converters

Assume that clocked comparators are used in a 500MHz sampling frequency ADC of 8-bits. If the input frequency is 250MHz with a peak-to-peak value of V_{REF} , the clock accuracy must be

$$\Delta t \leq \frac{\Delta V}{\omega V_p} = \frac{V_{REF}/2^{N+1}}{2\pi f(0.5V_{REF})} = \frac{1}{2^9 \cdot \pi f} \approx 2.5\text{ps}$$

Since electrical signals travel at approximately $50\mu\text{m}/\text{ps}$ for metal on an IC, each metal path from the clock to each comparator must be equal to within $125\mu\text{m}$ to avoid LSB errors due to clock skew. Therefore, must use careful layout to avoid ADC inaccuracies at high frequencies.

An equal-delay, clock distribution system for a 4-bit parallel ADC:

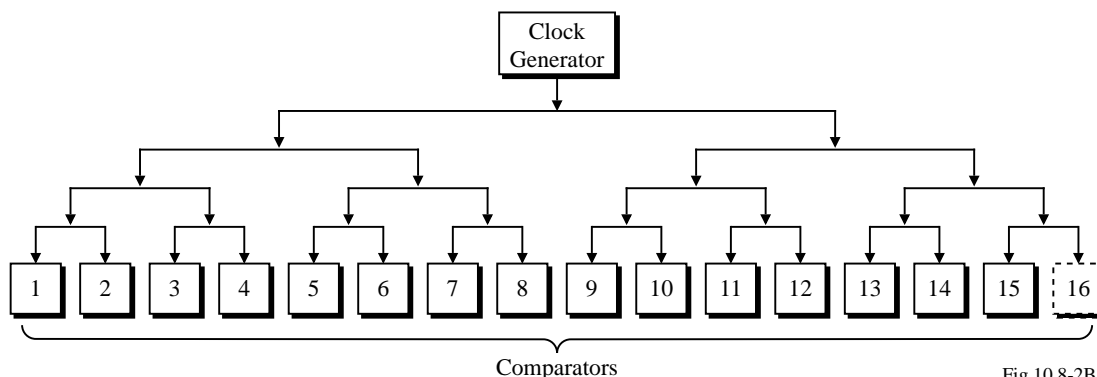


Fig.10.8-2B

Other Errors of the Parallel ADC

- Resistor string error - if current is drawn from the taps to the resistor string this will create a “bowing” effect on the voltage. This can be corrected by applying the correct voltage to various points of the resistor string.
- Input common mode range of the comparators - the comparators at the top of the string must operate with the same performance as the comparators at the bottom of the string.
- Kickback or flashback - influence of rapid transition changes occurring at the input of a comparator. Can be solved by using a preamplifier or buffer in front of the comparator.
- Metastability - uncertainty of the comparator output causing the transition of the thermometer code to be undetermined.

INTERPOLATING AND AVERAGING

Illustration of a 3-bit interpolating ADC using a factor of 4 interpolation

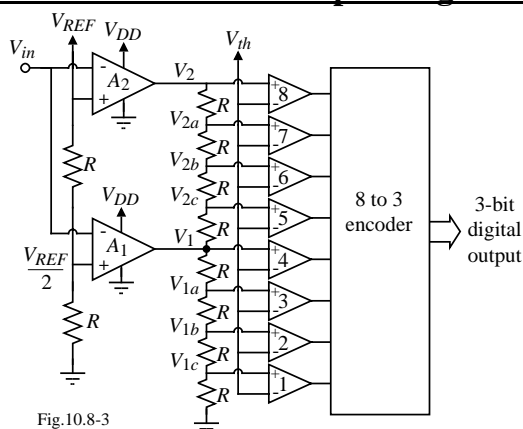


Fig.10.8-3

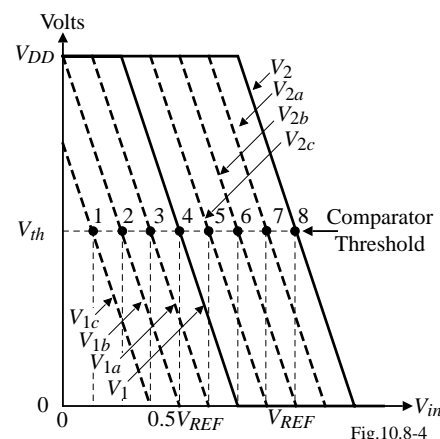


Fig.10.8-4

Comments:

- Capacitive loading at the input is reduced from 8 comparators to two amplifiers.
- The comparators no longer need a large *ICMR*
- V_1 and V_2 , are interpolated through the resistor string and applied to the comparators.
- Because of the amplification of the input amplifiers and a single threshold, the comparators can be simple and are often replaced by a latch.
- If the dots in Fig. 10.8-4 are not equally spaced, *INL* and *DNL* will result.

A 3-Bit Interpolating ADC with Equalized Comparator Delays

One of the problems in voltage (passive) interpolation is that the delay from the amplifier output to each comparator can be different due to different source resistance.

Solution:

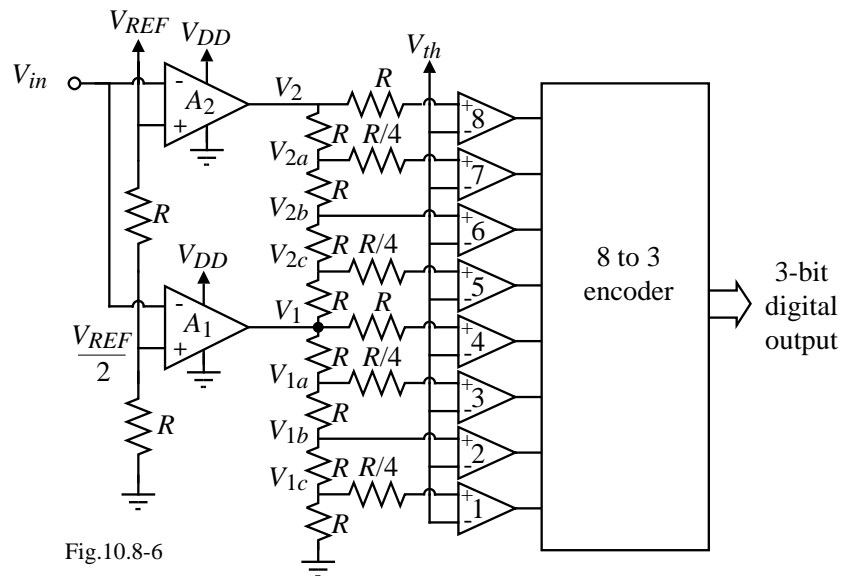
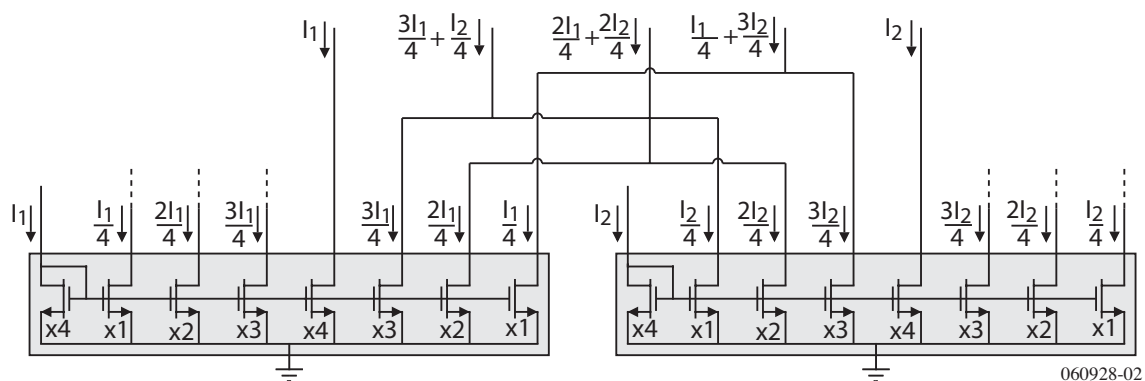


Fig.10.8-6

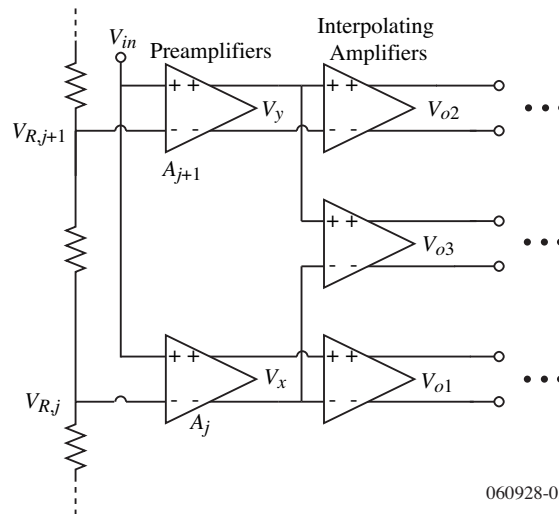
Active Interpolation

Example of a 3 level current interpolation:



This type of interpolation works well with current processing, i.e., current comparators.

Interpolation using Amplifiers

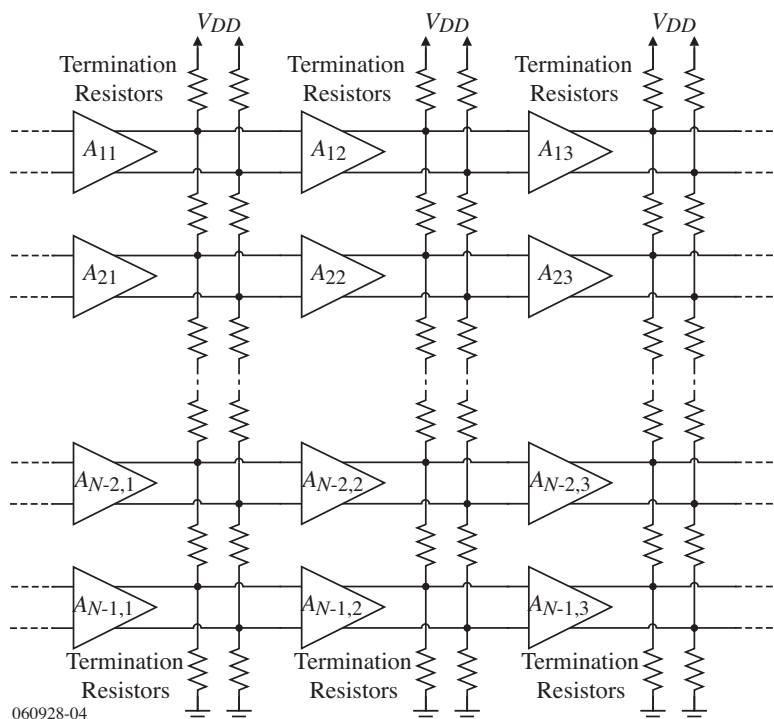


$V_{o3} = K(V_y - V_x)$ which is between V_y and V_x .

Averaging[†]

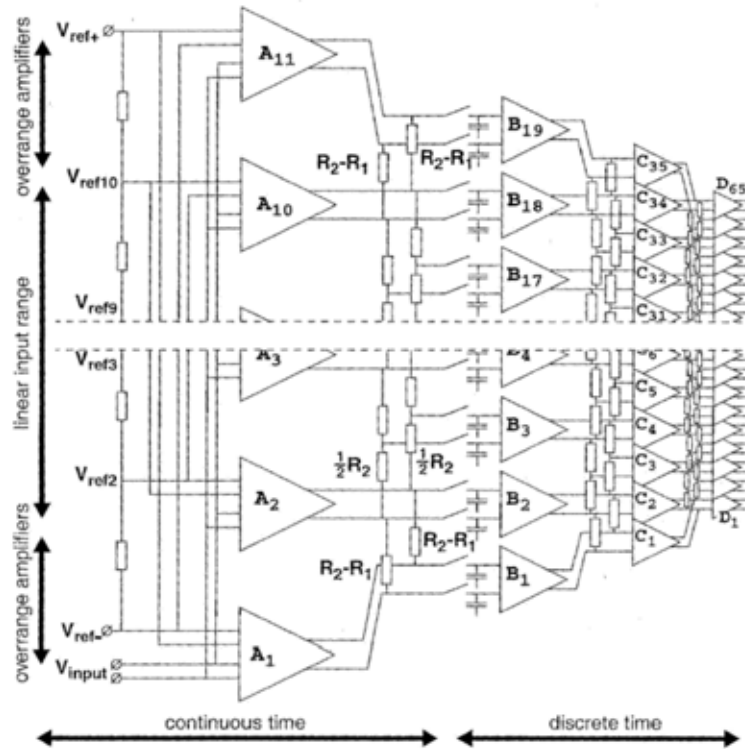
In many cases, the comparators consist of a number of pre-amplifiers followed by a latch. Averaging is the result of interconnecting the outputs of each stage of amplifiers so that the errors in one amplifier chain are balanced out by adjacent amplifier chains.

Result: The offsets are reduced allowing the transistors to be made smaller and therefore reducing the parasitics increasing the speed of the ADC.



[†] P.C.S. Scholtens and M. Vertregt, "A 6-b 1.6-Gsample/s Flash ADC in 0.18 μ m CMOS Using Averaging Termination, *IEEE J. of Solid-State Circuits*, vol. 37, no. 12, Dec. 2002, pp. 1599-1609.
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Analog Front End of an ADC using Averaging



FOLDING

Folding Analog-Digital Converters

Allows the number of comparators to be reduced below the value of 2^N-1 .

Architecture for a folded ADC:

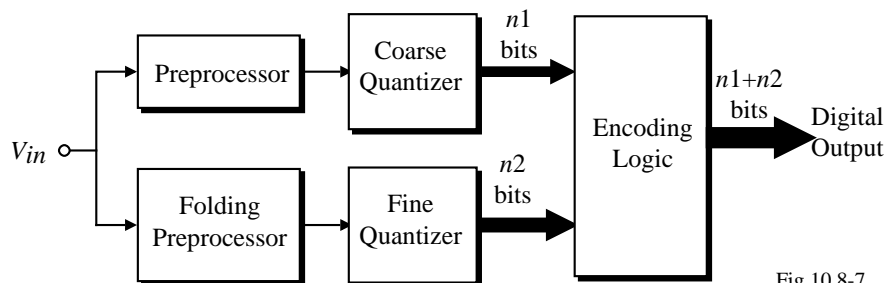


Fig.10.8-7

Operation:

The input is split into two or more parallel paths.

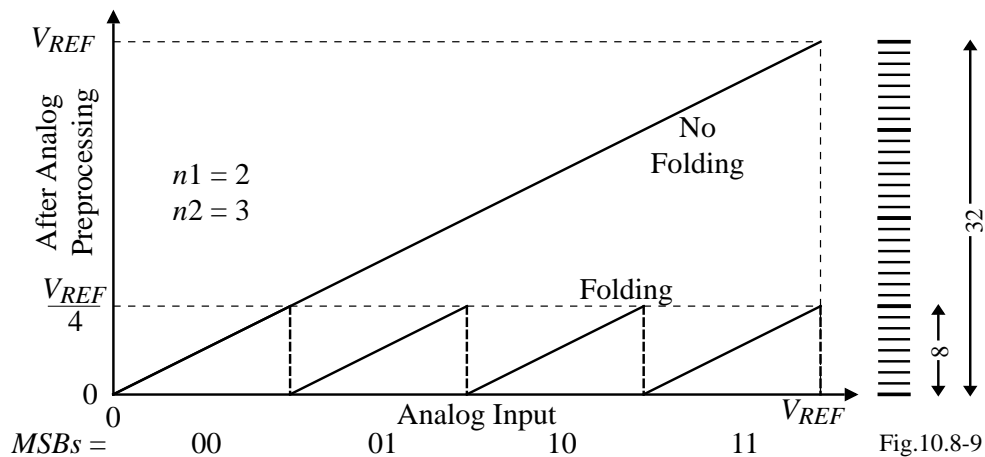
- First path uses a coarse quantizer to quantize the signal into 2^{n1} values
- The second path maps all of the 2^{n1} subranges onto a single subrange and applies this analog signal to a fine quantizer of 2^{n2} subranges.

Thus, the total number of comparators is $2^{n1}-1 + 2^{n2}-1$ compared with $2^{n1+n2}-1$ for a parallel ADC.

I.e., if $n1 = 2$ and $n2 = 4$, the folding ADC requires $3 + 15 = 18$ compared with 63 comparators.

Example of a Folding Preprocessor

Folding characteristic for $n1 = 2$ and $n2 = 3$.

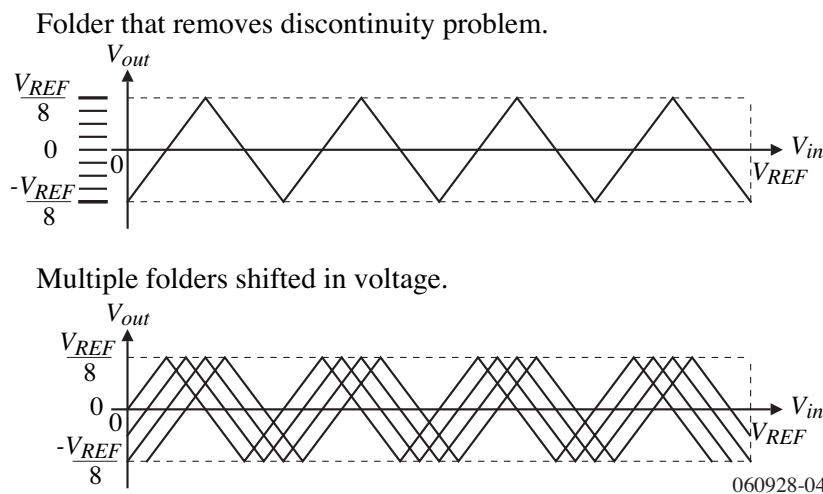


Problems:

- The sharp discontinuities of the folder are difficult to implement at high speeds.
- Fine quantizer must work at voltages ranging from 0 to $V_{REF}/4$ (subranging).
- The actual frequency of the folding signal is F times the input frequency where F is the number of folds

Modified Folding Preprocessors

The discontinuity problem can be removed by the following folding preprocessors:



In the second case, the reference voltage for all comparators is identical which removes any ICMR problems.

A 5-Bit Folding ADC Using 1-Bit Quantizers (Comparators)

Block diagram:

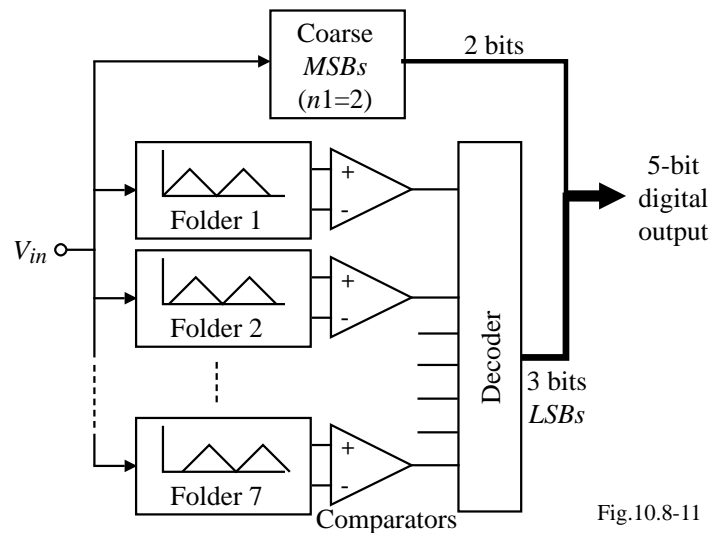


Fig.10.8-11

Comments:

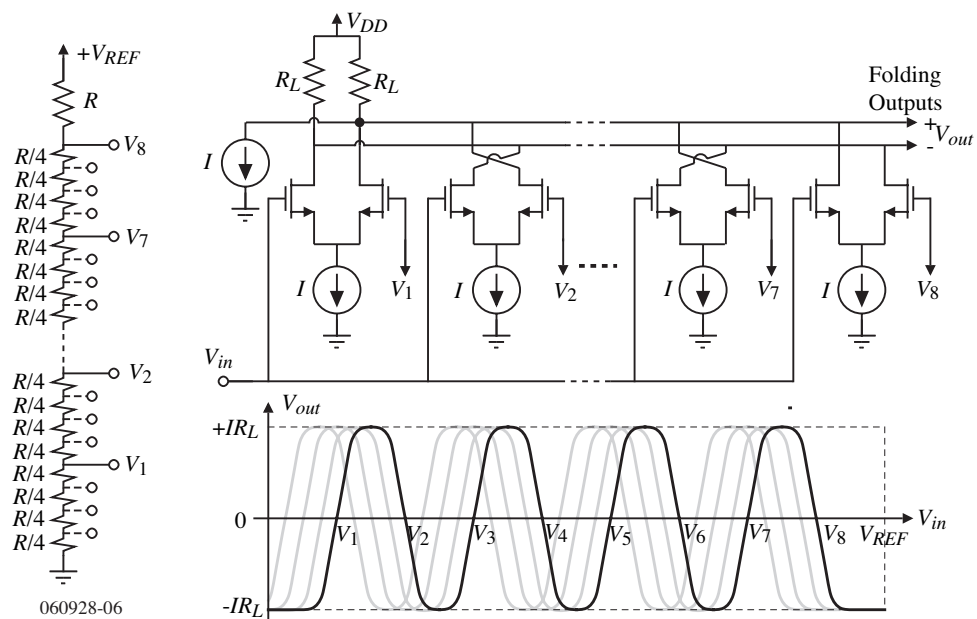
- Number of comparators is 7 for the fine quantizer and 3 for the course quantizer
- The zero crossings of the folders must be equally spaced to avoid linearity errors
- The number of folders can be reduced and the comparators simplified by use of interpolation

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Folding Circuits

Implementation of a times 4 folder:



Comments:

- Horizontal shifting is achieved by modifying the topmost and bottom resistors of the resistor string
- Folding and interpolation ADCs offer the most resolution at high speeds (≈ 8 bits at 500MHz)

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Use of a S/H in Front of the Folding ADC

Benefit of a S/H:

- With no S/H, the folding circuit acts as an amplitude-dependent frequency multiplier.

$BW \text{ of ADC} \geq BW \text{ of Folding Circuit}$

- With S/H, all inputs to the folding circuit arrive at the same time.
 - The folding circuit is no longer an amplitude-dependent frequency multiplier
 - BW of the ADC is now limited by the BW of the S/H circuit
 - Settling time of the folding and interpolating preprocessor is critical

Single S/H versus Distributed S/H:

- Single S/H requires high dynamic range for low THD
- Dynamic range requirement for distributed S/H reduced by the number of S/H stages
- If the coarse quantizer uses the same distributed S/H signals as the fine preprocessor, the coarse/fine synchronization is automatic
- The clock skew between the distributed S/H stages must be small. The clock jitter will have a greater effect on the distributed S/H approach.

Error Sources and Limitations of a Basic Folding ADC

Error Sources:

- Offsets in reference voltages due to resistor mismatch
- Preamp offset (reduced by large W/L for low $V_{GS}-V_T$, with common-centroid geometry)
- v_{in} feedthrough to reference ladder via C_{gs} of input pairs places a maximum value on ladder resistance which is dependent on the input frequency.
- Folder current-source mismatches (gives signal-dependent error \Rightarrow distortion)
- Comparator kickback (driving nodes should be low impedance)
- Comparator metastability condition (uncertainty of comparator output)
- Misalignment between coarse and fine quantization outputs (large code errors possible)

Sampling Speed Limitations:

- Folding output settling time
- Comparator settling time
- Clock distribution and layout
- Clock jitter

Input Bandwidth Limitations:

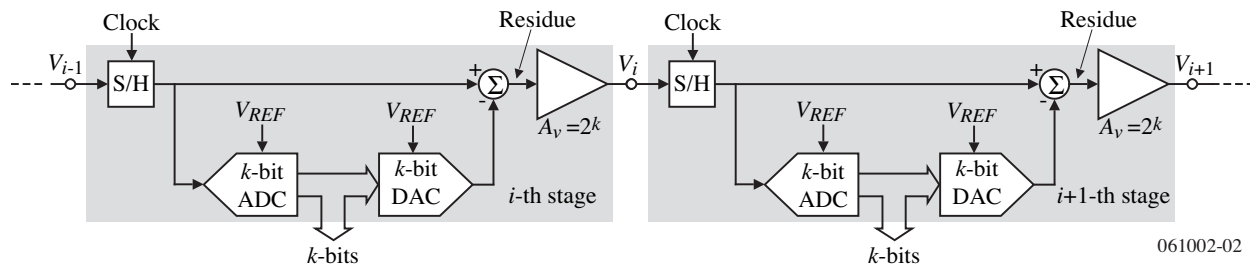
- Maximum folding signal frequency $\geq (F/2) \cdot f_{in}$, unless a S/H is used
- Distortion due to limited preamplifier linear range and frequency dependent delay
- Distortion due to the limited linear range and frequency dependent delay of the folder
- Parasitic capacitance of routing to comparators

HIGH-SPEED, HIGH-RESOLUTION ADCs

Multiple-Bit, Pipeline Analog-Digital Converters

A compromise between speed and resolution is to use a pipeline ADC with multiple bits/stage.

i -th stage of a k -bit per stage pipeline ADC with residue amplification:

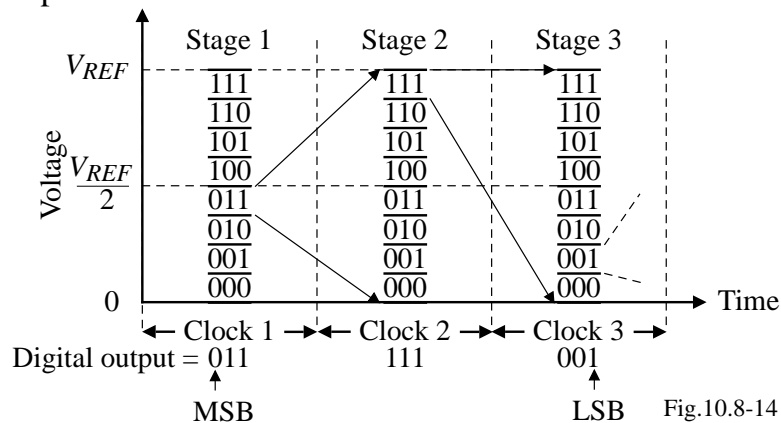


$$\text{Residue voltage} = V_{i-1} - \left(\frac{b_0}{2} + \frac{b_1}{2^2} + \dots + \frac{b_{k-2}}{2^{k-1}} + \frac{b_{k-1}}{2^k} \right) V_{REF}$$

Potential specifications range from 100-300 Mps and 10 to 14 bits.

A 3-Stage, 3-Bit Per Stage Pipeline ADC

Illustration of the operation:



Converted word is 011 111 001

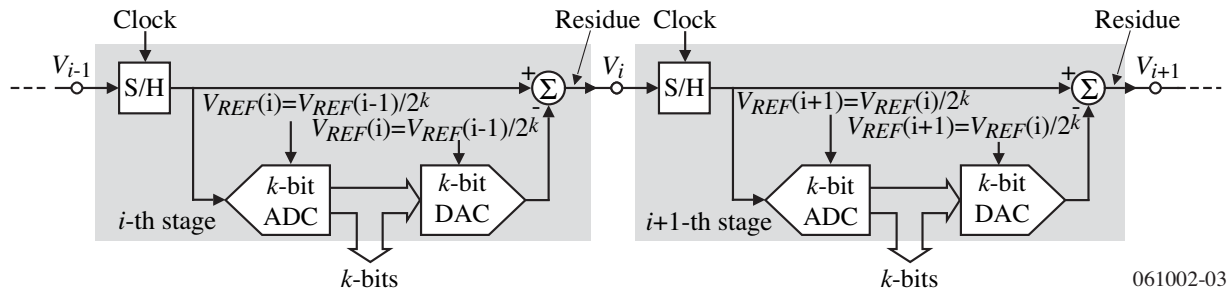
Comments:

- Only 21 comparators are required for this 9-bit ADC
- Conversion occurs in three clock cycles
- The residue amplifier will cause a bandwidth limitation,

$$GB = 50\text{MHz} \rightarrow f_{-3\text{dB}} = \frac{50\text{MHz}}{2^3} \approx 6\text{MHz}$$

Multiple-Bit, Pipeline Analog-Digital Converters - Subranging

The amplification of $A_v = 2^k$ for each stage places a bandwidth limitation on the converter. The subranging technique shown below eliminates this problem.



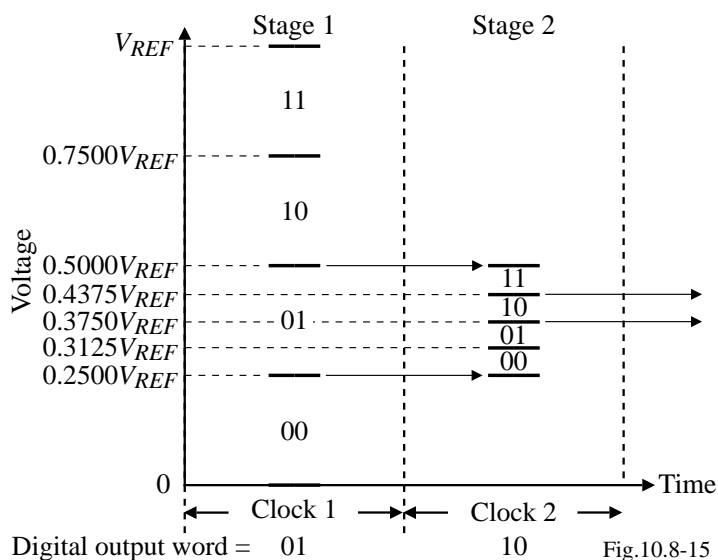
Note: the reference voltage of the previous stage ($i-1$) is divided by 2^k to get the reference voltage for the present stage (i), $V_{REF}(i)$, and so forth.

Subranging, Multiple-Bit, Pipeline ADCs

Illustration of a 2-stage, 2-bits/stage pipeline ADC:

Comments:

- Resolution of the comparators for the following stages increases but fortunately, the tolerance of each stage decreases by 2^k for every additional stage.
- Removes the frequency limitation of the amplifier



Implementation of the DAC in the Multiple-Bit, Pipeline ADC

Circuit:

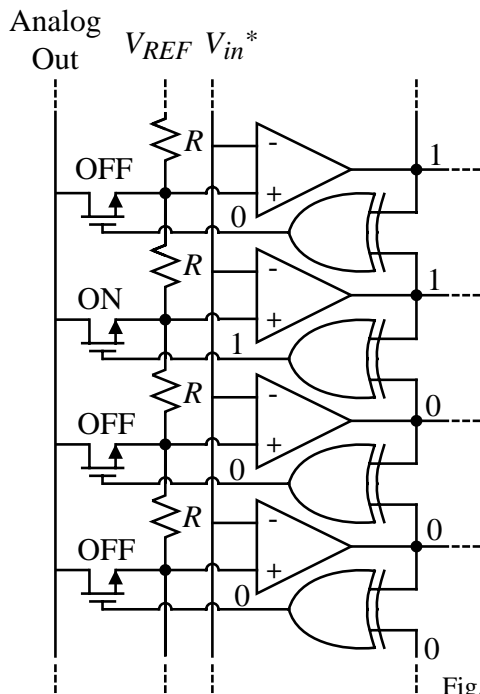


Fig.10.8-16

Comments:

- A good compromise between area and speed
- The ADC does not need to be a flash or parallel if speed is not crucial
- Typical performance is 10 bits at 50Msamples/sec

Example 10.7-3 - Examination of error in subranging for a 2-stage, 2-bits/stage pipeline ADC

The stages of the 2-stage, 2-bits/stage pipeline ADC shown below are ideal.

However, the second stage divides V_{REF} by 2 rather than 4. Find the $\pm INL$ and $\pm DNL$ for this ADC.

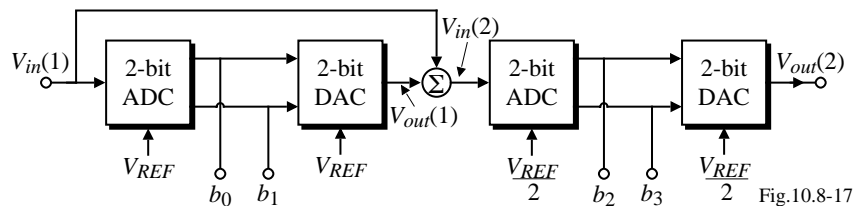


Fig.10.8-17

Solution

Examination of the first stage shows that its output, $V_{out}(1)$ changes at

$$\frac{V_{in}(1)}{V_{REF}} = \frac{1}{4}, \frac{2}{4}, \frac{3}{4}, \text{ and } \frac{4}{4}.$$

The output of the first stage will be

$$\frac{V_{out}(1)}{V_{REF}} = \frac{b_0}{2} + \frac{b_1}{4}.$$

The second stage changes at

$$\frac{V_{in}(2)}{V_{REF}} = \frac{1}{8}, \frac{2}{8}, \frac{3}{8}, \text{ and } \frac{4}{8}$$

where

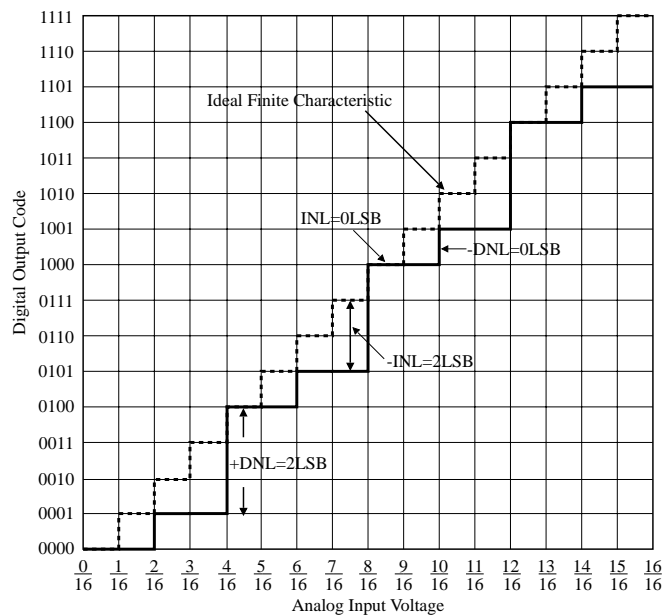
$$V_{in}(2) = V_{in}(1) - V_{out}(1).$$

The above relationships permit the information given in Table 10.7-1.

Example 10.7-3 - Continued

Table 10.7-1 Output digital word for Ex. 10.7-3

$V_{in(1)}$ V_{REF}	b_0	b_1	$V_{out(1)}$ V_{REF}	$V_{in(2)}$ V_{REF}	b_2	b_3	Ideal Output $b_0 b_1 b_2 b_3$			
0	0	0	0	0	0	0	0	0	0	0
1/16	0	0	0	1/16	0	0	0	0	0	1
2/16	0	0	0	2/16	0	1	0	0	1	0
3/16	0	0	0	3/16	0	1	0	0	1	1
4/16	0	1	4/16	0	0	0	0	1	0	0
5/16	0	1	4/16	1/16	0	0	0	1	0	1
6/16	0	1	4/16	2/16	0	1	0	1	1	0
7/16	0	1	4/16	3/16	0	1	0	1	1	1
8/16	1	0	8/16	0	0	0	1	0	0	0
9/16	1	0	8/16	1/16	0	0	1	0	0	1
10/16	1	0	8/16	2/16	0	1	1	0	1	0
11/16	1	0	8/16	3/16	0	1	1	0	1	1
12/16	1	1	12/16	0	0	0	1	1	0	0
13/16	1	1	12/16	1/16	0	0	1	1	0	1
14/16	1	1	12/16	2/16	0	1	1	1	1	0
15/16	1	1	12/16	3/16	0	1	1	1	1	1



Comparing the actual digital output word with the ideal output word gives the following:
 $+INL = 0LSB$, $-INL = 0111-0101 = -2LSB$, $+DNL = (1000-0101) - 1LSB = +2LSB$, and
 $-DNL = (0101-0100) - 1LSB = 0LSB$.

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Example of a Multiple-Bit, Pipeline ADC

Two-stages with 5-bits per stage resulting in a 10-bit ADC with a sampling rate of 5Msamples/second.

Architecture:

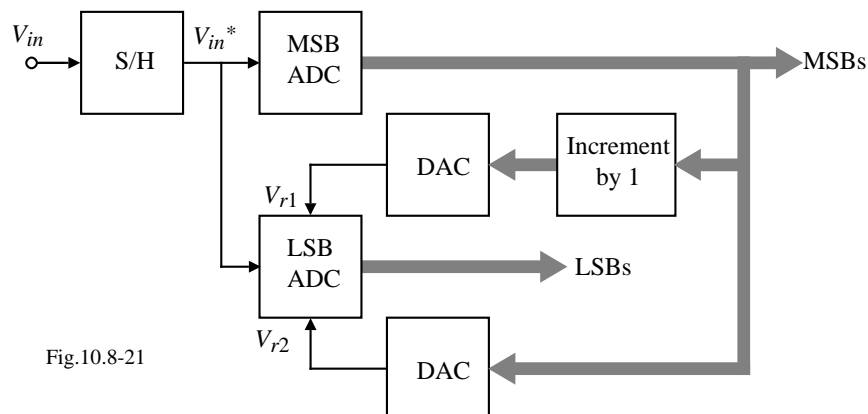


Fig.10.8-21

Features:

- Requires only $2^{n/2}-1$ comparators
- $LSBs$ decoded using 31 preset charge redistribution capacitor arrays
- Reference voltages used in the $LSBs$ are generated by the MSB ADC
- No op amps are used

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Example of a Multiple-Bit, Pipeline ADC - Continued

MSB Conversion:

Operation:

- 1.) Sample V_{in}^* on each $32C$ capacitance autozeroing the comparators
- 2.) Connect each comparator to a node of the resistor string generating a thermometer code.

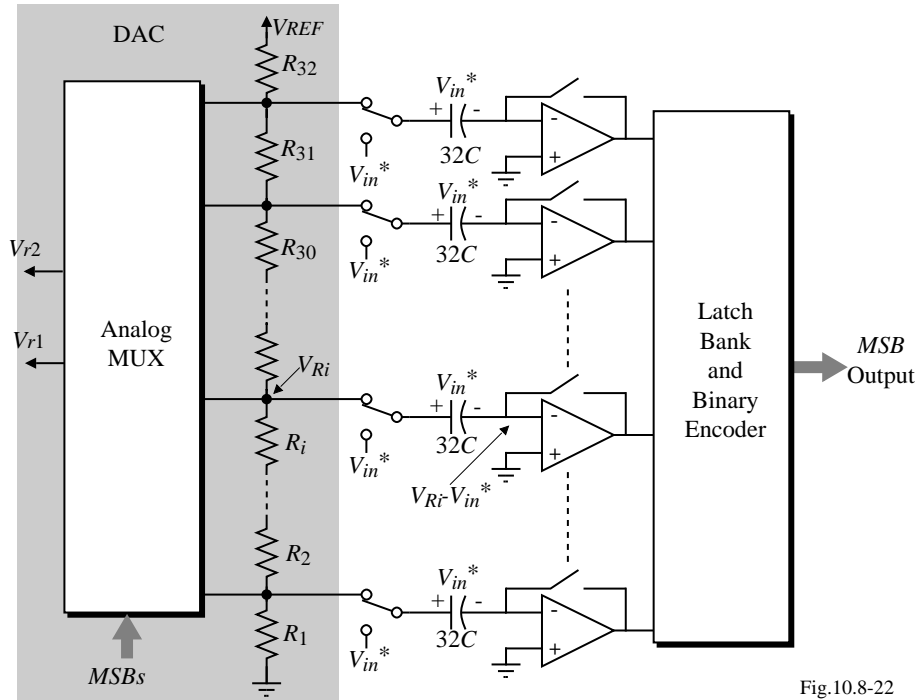


Fig.10.8-22

Example of a Multiple-Bit, Pipeline ADC - Continued

LSB Conversion:

Operation:

- 1.) MSB comparators are preset to each of the 31 possible digital codes.
- 2.) V_{r1} and V_{r2} are derived from the MSB conversion.
- 3.) Preset comparators will produce a thermometer code to the encoder.

Comments:

- Requires two full clock cycles
- Reuses the comparators
- Accuracy limited by resistor string and its dynamic loading
- Accuracy also limited by the capacitor array
- Comparator is a 3-stage, low-gain, wide-bandwidth, using internal autozeroing

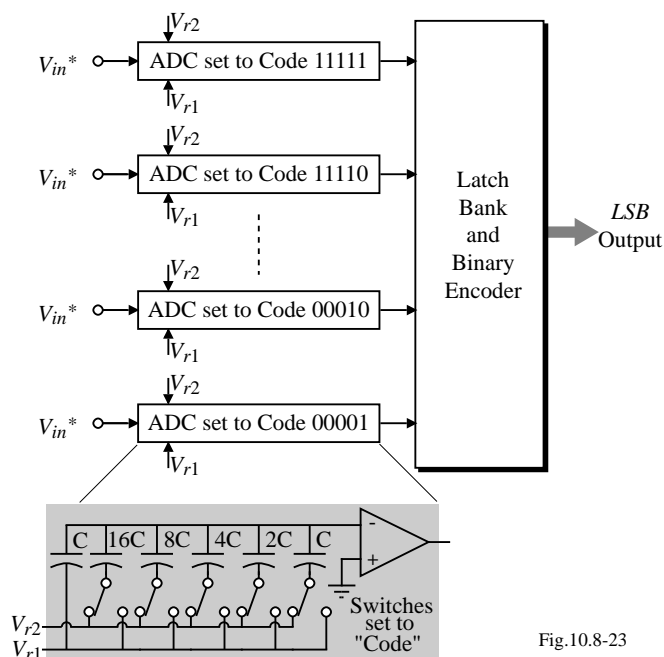
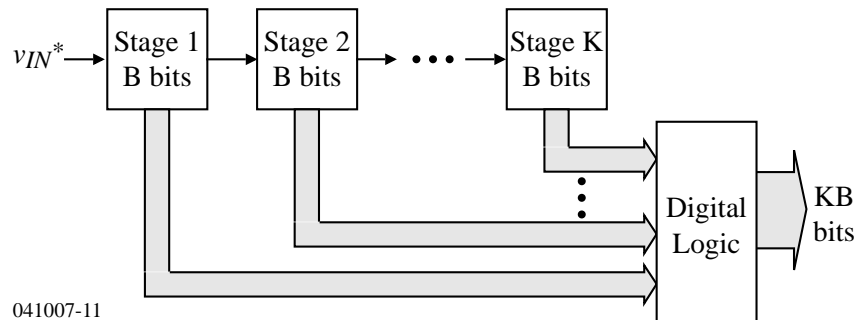


Fig.10.8-23

Digital Error Correction

Like many of the accuracy enhancing techniques, there are particular applications where certain correcting techniques are useful. In the pipeline, analog-digital converter, a technique called digital error correction is used to remove the imperfections of the components.

Pipeline ADC:

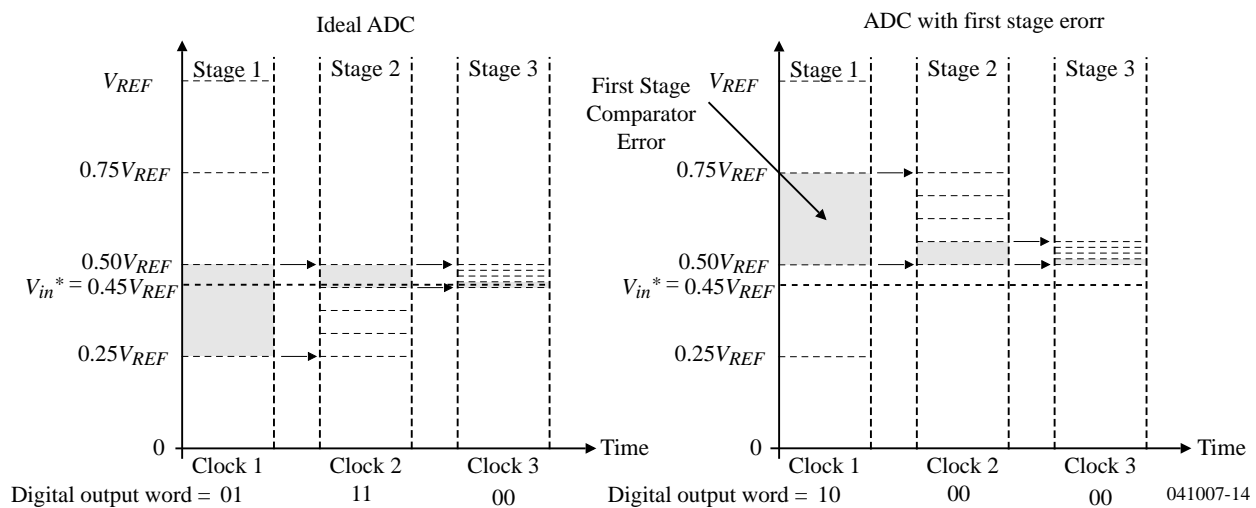


Operation:

- 1.) Stage 1 resolves the analog input signal to within one of B subranges which determines the first B bits.
- 2.) Stage 1 then creates the analog residue (analog input – quantized analog output) and passes on to Stage 2 by either amplifying or subranging.
- 3.) Stage 2 repeats this process which ends with Stage K .

Comparator Error in a Pipeline ADC

Subranging Pipeline ADC Example ($B=2$, $K=3$):

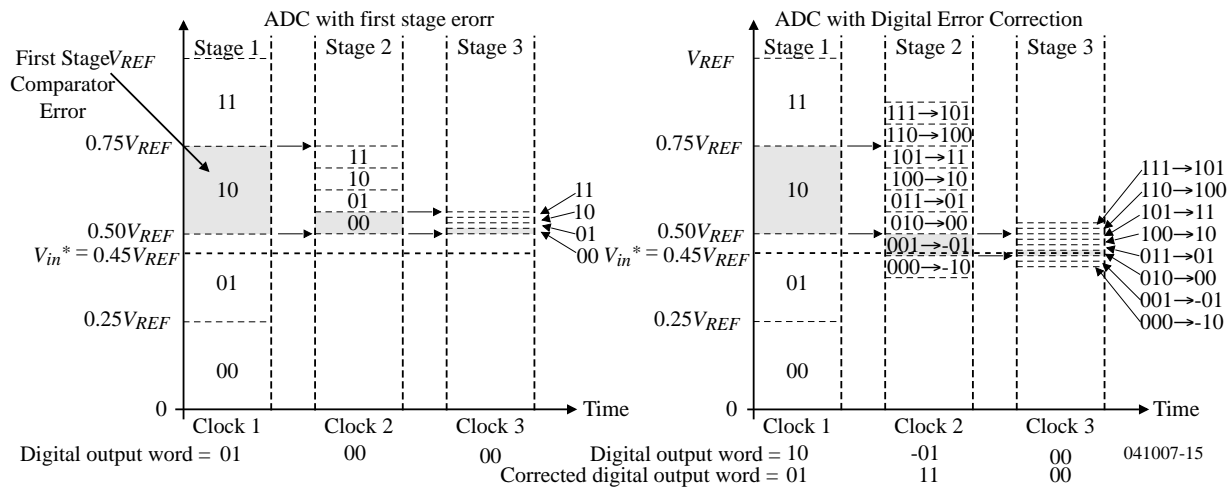


Note that if the comparator in the first stage makes the wrong choice, the converter cannot recover as shown in the example on the right.

Digital Error Correction – Continued

Digital error correction uses one of the bits of each stage (except the first) to correct for any errors caused by the previous stage.

Subranging Pipeline ADC Example ($B=2$, $K=3$) using Digital Error Correction:



Comments:

- Add a correcting bit to the following stage to correct for errors in the previous stage.
- The subranging or amplification of the next stage does not include the correcting bit.
- Correction can be done after all stages of the pipeline ADC have converted or after each individual stage.

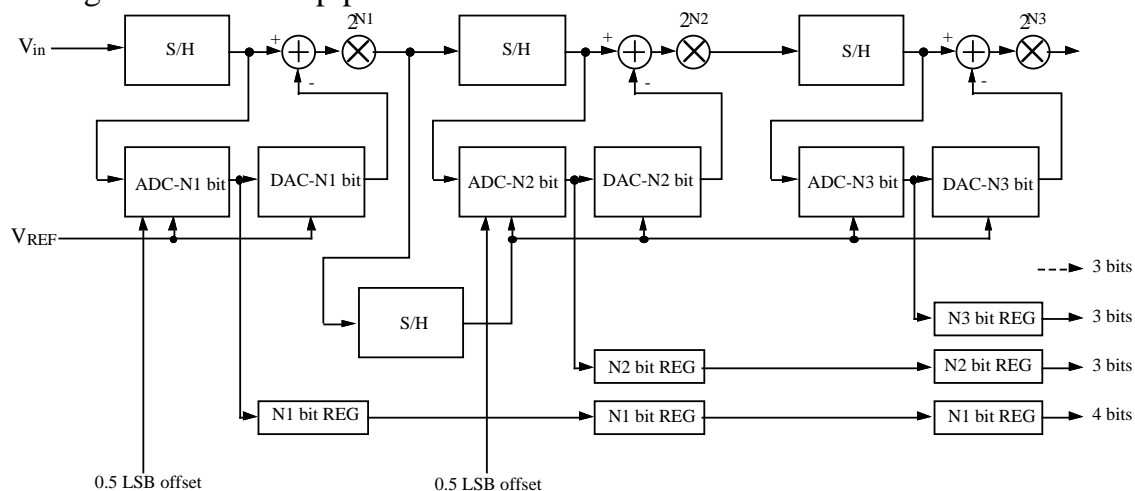
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Example of a Pipeline ADC with Digital Error Correction

ADC uses 4 stages of 4-bits each and employs a successive approximation ADC to get 13-bit resolution at 250 ksamples/sec.

Block diagram of a 13-bit pipeline ADC:



Comments:

- The ADC of the first stage uses 16 equal capacitors instead of 4 binary weighted for more accuracy
- One bit of the last three stages is used for error correction.

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12-Bit Pipeline ADC with Digital Error Correction & Self-Calibration[†]

Digital Error Correction:

- Avoids saturation of the next stage
- Reduces the number of missing codes
- Relaxed specifications for the comparators
- Compensates for wrong decisions in the coarse quantizers

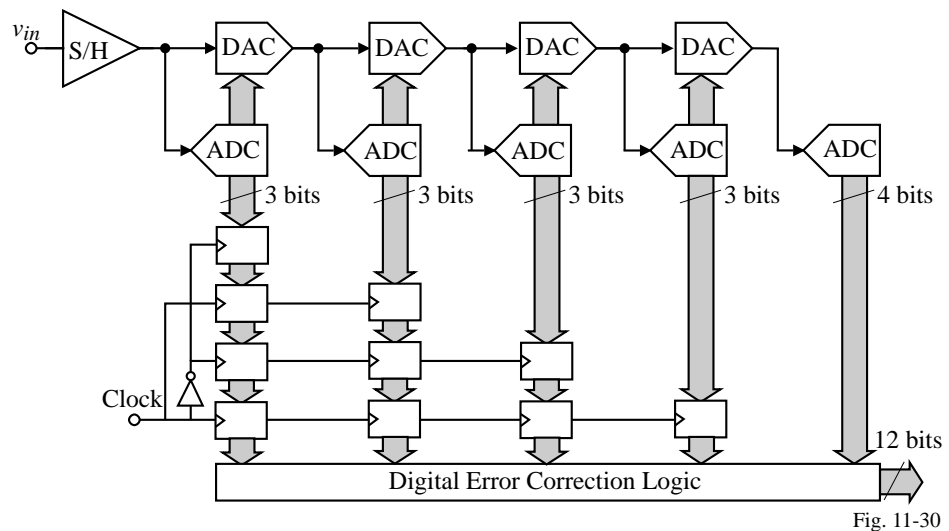


Fig. 11-30

Self-Calibration:

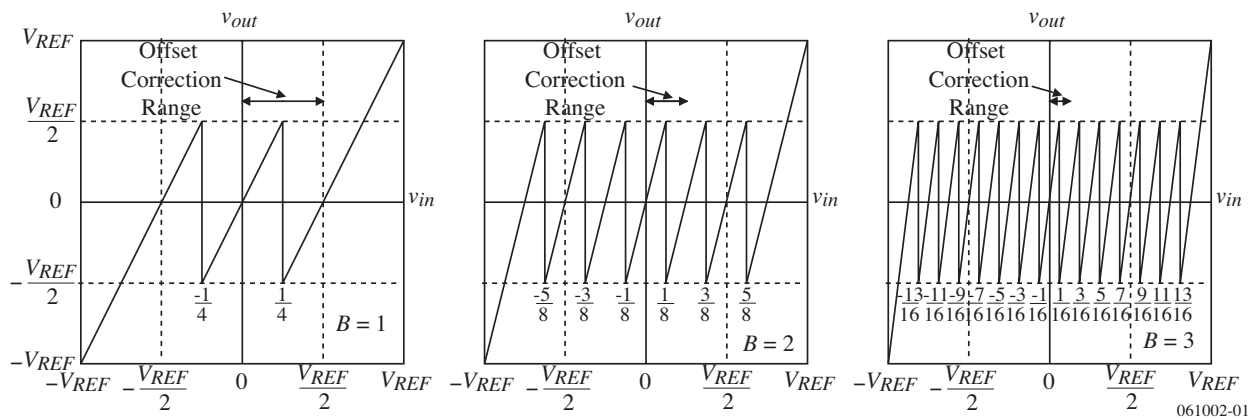
- Can calibrate the effects of the DAC nonlinearity and gain error
- Can be done by digital or analog methods or both

[†] J. Goes, et. al., *CICC'96*
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Digital Error Correction using B .5-Bit Pipeline Stages

The top and bottom comparators can be removed to achieve digital error correction more efficiently.

Input-output characteristics for different per-stage resolutions ($B = 1, 2$, and 3):



061002-01

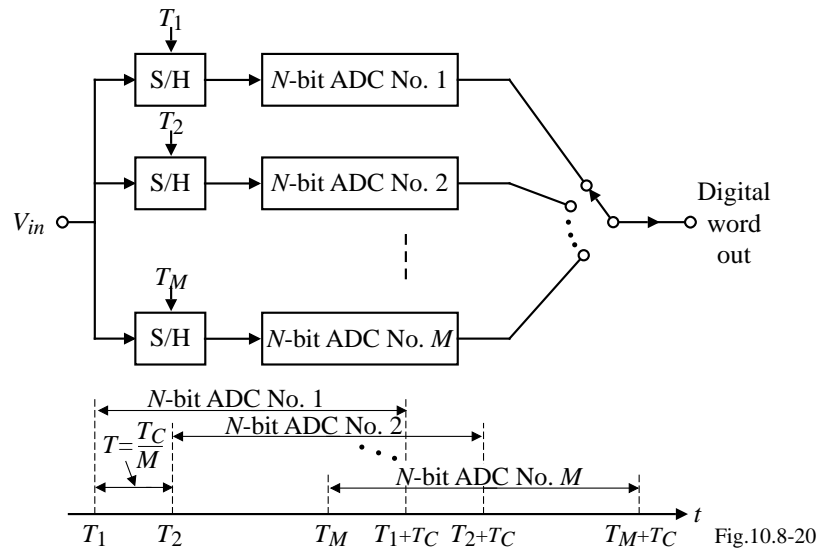
If all else is ideal, the offset voltage correction range is equal to $\pm \frac{V_{REF}}{2^{B+1}}$.

TIME-INTERLEAVED ADC CONVERTERS

Time-Interleaved Analog-Digital Converters

Slower ADCs are used
in parallel.

Illustration:



Comments:

- Can get the same throughput with less chip area
- If $M = N$, then a digital word is converted at every clock cycle
- Multiplexer and timing become challenges at high speeds

Summary of High-Speed Analog-Digital Converters

Type of ADC	Primary Advantage	Primary Disadvantage
Flash or parallel	Fast	Area is large if $N > 6$
Interpolating	Fast	Requires accurate interpolation
Folding	Fast	Bandwidth increases if no S/H used
Multiple-Bit, Pipeline	Increased number of bits	Slower than flash
Time-interleaved	Small area with large throughput	Precise timing and fast multiplexer

Typical Performance:

- 6-8 bits
- 500-2000 Msamples/sec.
- The $ENOB$ at the Nyquist frequency is typically 1-2 bits less than the $ENOB$ at low frequencies.
- Power is approximately 0.3 to 1W

SECTION 10.8 - OVERSAMPLING CONVERTERS

INTRODUCTION

What is an oversampling converter?

An oversampling converter uses a noise-shaping modulator to reduce the in-band quantization noise to achieve a high degree of resolution.

- What is the range of oversampling?

The oversampling ratio, called M , is a ratio of the clock frequency to the Nyquist frequency of the input signal. This oversampling ratio can vary from 8 to 256.

- The resolution of the oversampled converter is proportional to the oversampled ratio.
- The bandwidth of the input signal is inversely proportional to the oversampled ratio.

- What are the advantages of oversampling converters?

Very compatible with VLSI technology because most of the converter is digital
High resolution

Single-bit quantizers use a one-bit DAC which has no INL or DNL errors

Provide an excellent means of trading precision for speed (16-18 bits at 50ksps to 8-10 bits at sampling rates of 5-10Msps).

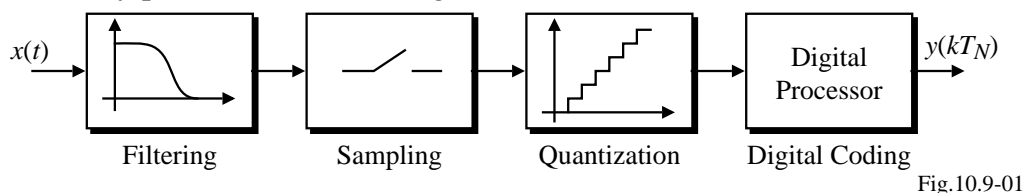
- What are the disadvantages of oversampling converters?

Difficult to model and simulate

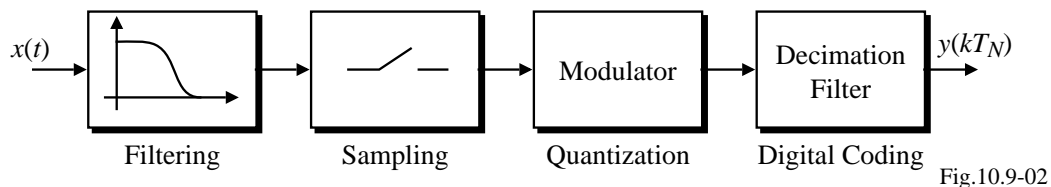
Limited in bandwidth to the clock frequency divided by the oversampling ratio

Nyquist Versus Oversampled ADCs

Conventional Nyquist ADC Block Diagram:



Oversampled ADC Block Diagram:



Components:

- Filter - Prevents possible aliasing of the following sampling step.
- Sampling - Necessary for any analog-to-digital conversion.
- Quantization - Decides the nearest analog voltage to the sampled voltage (determines the resolution).
- Digital Coding - Converts the quantizer information into a digital output signal.

Frequency Spectrum of Nyquist and Oversampled Converters

Definitions:

f_B = analog signal bandwidth

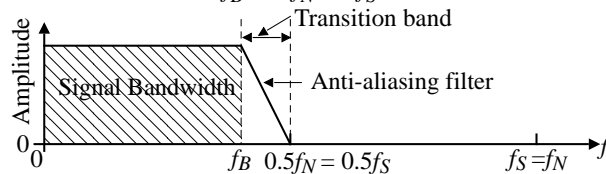
f_N = Nyquist frequency (two times f_B)

f_S = sampling or clock frequency

$$M = \frac{f_S}{f_N} = \frac{f_S}{2f_B} = \text{oversampling ratio}$$

Frequency perspective:

Conventional ADC with $f_B \approx 0.5f_N = 0.5f_S$.



Oversampled ADC with $f_B \approx 0.5f_N < f_S$.

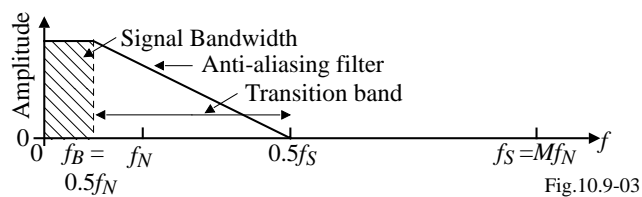
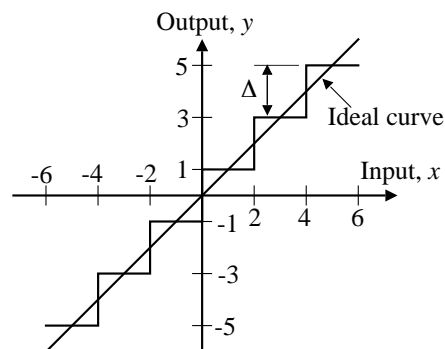


Fig.10.9-03

Quantization Noise of a Conventional (Nyquist) ADC

Multilevel Quantizer:



The quantized signal y can be represented as,

$$y = Gx + e$$

where

G = gain of the ADC, normally 1

e = quantization error

The mean square value of the quantization error is

$$e_{rms}^2 = S_Q = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e(x)^2 dx = \frac{\Delta^2}{12}$$

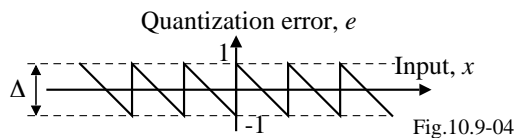


Fig.10.9-04

Quantization Noise of a Conventional (Nyquist) ADC - Continued

Spectral density of the sampled noise:

When a quantized signal is sampled at $f_S (= 1/\tau)$, then all of its noise power folds into the frequency band from 0 to $0.5f_S$. Assuming that the noise power is white, the spectral density of the sampled noise is,

$$E(f) = e_{rms} \sqrt{\frac{2}{f_S}} = e_{rms} \sqrt{2\tau}$$

where $\tau = 1/f_S$ and $f_S =$ sampling frequency

The inband noise energy n_o is

$$n_o^2 = \int_0^{f_B} E^2(f) df = e_{rms}^2 (2f_B \tau) = e_{rms}^2 \left(\frac{2f_B}{f_S} \right) = \frac{e_{rms}^2}{M} \Rightarrow n_o = \frac{e_{rms}}{\sqrt{M}}$$

What does all this mean?

- One way to increase the resolution of an ADC is to make the bandwidth of the signal, f_B , less than the clock frequency, f_S . In other words, give up bandwidth for precision.
- However, it is seen from the above that a doubling of the oversampling ratio M , only gives a decrease of the inband noise, n_o , of $1/\sqrt{2}$ which corresponds to -3dB decrease or an increase of resolution of 0.5 bits

As a result, increasing the oversampling ratio of a Nyquist analog-digital converter is not a very good method of increasing the resolution.

CMOS Analog Circuit Design

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Oversampled Analog-Digital Converters

Classification of oversampled ADCs:

- 1.) Straight-oversampling - The quantization noise is assumed to be equally distributed over the entire frequency range of dc to $0.5f_S$. This type of converter is represented by the Nyquist ADC.

- 2.) Predictive oversampling - Uses noise shaping plus oversampling to reduce the inband noise to a much greater extent than the straight-oversampling ADC. Both the signal and noise quantization spectrums are shaped.

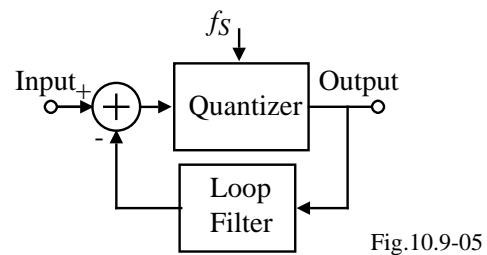


Fig.10.9-05

- 3.) Noise-shaping oversampling - Similar to the predictive oversampling except that only the noise quantization spectrum is shaped while the signal spectrum is preserved.

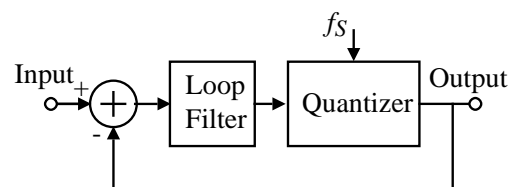
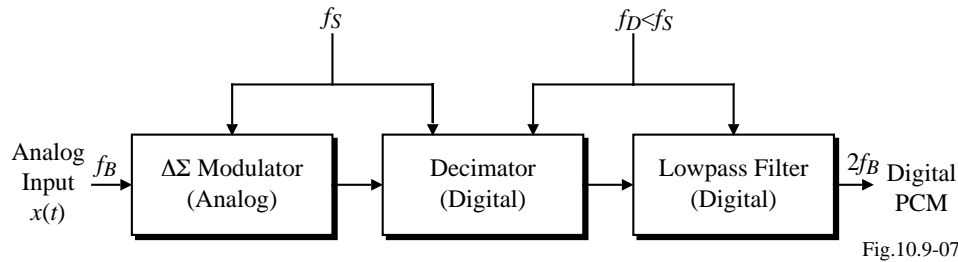


Fig.10.9-06

The noise-shaping oversampling ADCs are also known as *delta-sigma* ADCs. We will only consider the delta-sigma type oversampling ADCs.

DELTA-SIGMA MODULATORS

General block diagram of an oversampled ADC



Components of the Oversampled ADC:

- 1.) $\Delta\Sigma$ Modulator - Also called the noise shaper because it can shape the quantization noise and push the majority of the inband noise to higher frequencies. It modulates the analog input signal to a simple digital code, normally a one-bit serial stream using a sampling rate much higher than the Nyquist rate.
- 2.) Decimator - Also called the down-sampler because it down samples the high frequency modulator output into a low frequency output and does some pre-filtering on the quantization noise.
- 3.) Digital Lowpass Filter - Used to remove the high frequency quantization noise and to preserve the input signal.

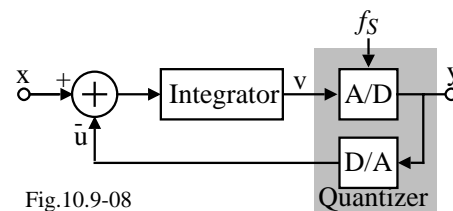
Note: Only the modulator is analog, the rest of the circuitry is digital.

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First-Order, Delta-Sigma Modulator

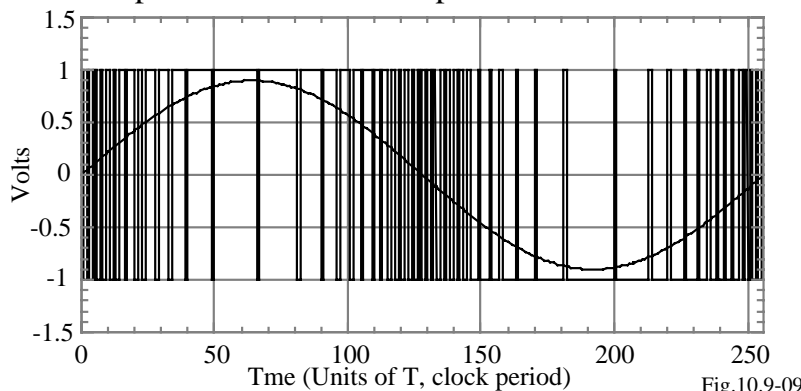
Block diagram of a first-order, delta-sigma modulator:



Components:

- Integrator (continuous or discrete time)
- Coarse quantizer (typically two levels)
 - A/D which is a comparator for two levels
 - D/A which is a switch for two levels

First-order modulator output for a sinusoidal input:



Sampled-Data Model of a First-Order $\Delta\Sigma$ Modulator

Writing the following relationships,

$$y[nT_s] = q[nT_s] + v[nT_s]$$

$$v[nT_s] = w[(n-1)T_s] + v[(n-1)T_s]$$

$$\therefore y[nT_s] = q[nT_s] + w[(n-1)T_s] + v[(n-1)T_s]$$

$$y[(n-1)T_s] = q[(n-1)T_s] + \{x[(n-1)T_s] - y[(n-1)T_s]\} + v[(n-1)T_s]$$

But the first equation can be written as

$$y[(n-1)T_s] = q[(n-1)T_s] + v[(n-1)T_s] \rightarrow q[(n-1)T_s] = y[(n-1)T_s] - v[(n-1)T_s]$$

Substituting this relationship into the above gives,

$$y[nT_s] = x[(n-1)T_s] + q[nT_s] - q[(n-1)T_s]$$

Converting this expression to the z -domain gives,

$$Y(z) = z^{-1}X(z) + (1-z^{-1})Q(z)$$

Definitions:

$$\text{Signal Transfer Function} = STF = \frac{Y(z)}{X(z)} = z^{-1}$$

$$\text{Noise Transfer Function} = NTF = \frac{Y(z)}{Q(z)} = 1 - z^{-1}$$

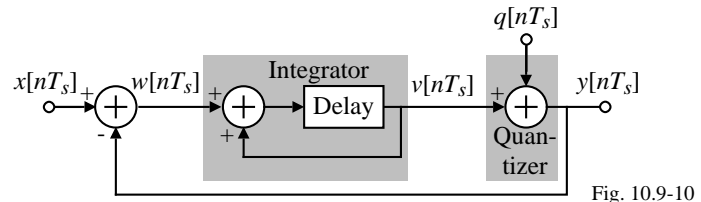


Fig. 10.9-10

Higher-Order $\Delta\Sigma$ Modulators

A second-order, $\Delta\Sigma$ modulator:

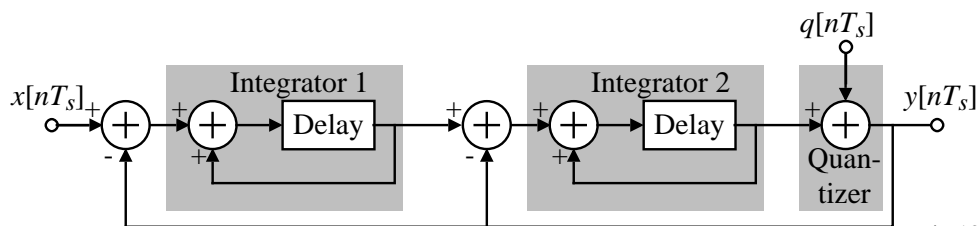


Fig. 10.9-11

It can be shown that the z -domain output is,

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2Q(z)$$

The general, L -th order $\Delta\Sigma$ modulator has the following form,

$$Y(z) = z^{-L}X(z) + (1-z^{-1})^LQ(z)$$

Note that noise transfer function, NTF , has L -zeros at the origin resulting in a high-pass transfer function.

This high-pass characteristic reduces the noise at low frequencies.

Noise Transfer Function

The noise transfer function can be written as,

$$NTF_Q(z) = (1-z^{-1})^L$$

Evaluate $(1-z^{-1})$ by replacing z by $e^{j\omega T_s}$ to get

$$(1-z^{-1}) = (1 - e^{-j\omega T_s}) \left(\frac{2j}{2j} \right) \frac{e^{j\pi f/f_s}}{e^{j\pi f/f_s}} = \left(\frac{e^{j\pi f/f_s} - e^{-j\pi f/f_s}}{2j} \right) 2j e^{-j\pi f/f_s} = \sin(\pi f/T_s) 2j e^{-j\pi f/f_s}$$

$$|1-z^{-1}| = (2\sin\pi f T_s) \rightarrow |NTF_Q(f)| = (2\sin\pi f T_s)^L$$

Magnitude of the noise transfer function,

Note: Single-loop modulators having noise shaping characteristics of the form $(1-z^{-1})^L$ are unstable for $L > 2$ unless an L -bit quantizer is used.

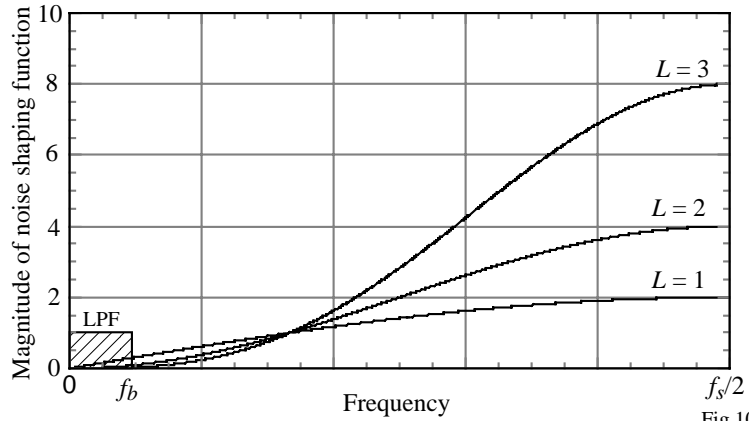


Fig.10.9-12

In-Band Rms Noise of Single-Loop $\Delta\Sigma$ Modulator

Assuming noise power is white, the power spectral density of the $\Delta\Sigma$ modulator, $S_E(f)$, is

$$S_E(f) = |NTF_Q(f)|^2 \frac{|S_Q(f)|}{f_s}$$

Next, integrate $S_E(f)$ over the signal band to get the inband noise power using $S_Q = \frac{\Delta^2}{12}$

$$\therefore S_B = \frac{1}{f_s} \int_{-f_b}^{f_b} (2\sin\pi f T_s)^{2L} \frac{\Delta^2}{12} df \approx \left(\frac{\pi^{2L}}{2^{L+1}} \right) \left(\frac{1}{M^{2L+1}} \right) \left(\frac{\Delta^2}{12} \right) \quad \text{where } \sin\pi f T_s \approx \pi f T_s \text{ for } M \gg 1.$$

Therefore, the in-band, rms noise is given as

$$n_0 = \sqrt{S_B} = \left(\frac{\pi^L}{\sqrt{2^{L+1}}} \right) \left(\frac{1}{M^{L+0.5}} \right) \left(\frac{\Delta}{\sqrt{12}} \right) = \left(\frac{\pi^L}{\sqrt{2^{L+1}}} \right) \left(\frac{1}{M^{L+0.5}} \right) e_{rms}$$

Note that as the $\Delta\Sigma$ is a much more efficient way of achieving resolution by increasing M .

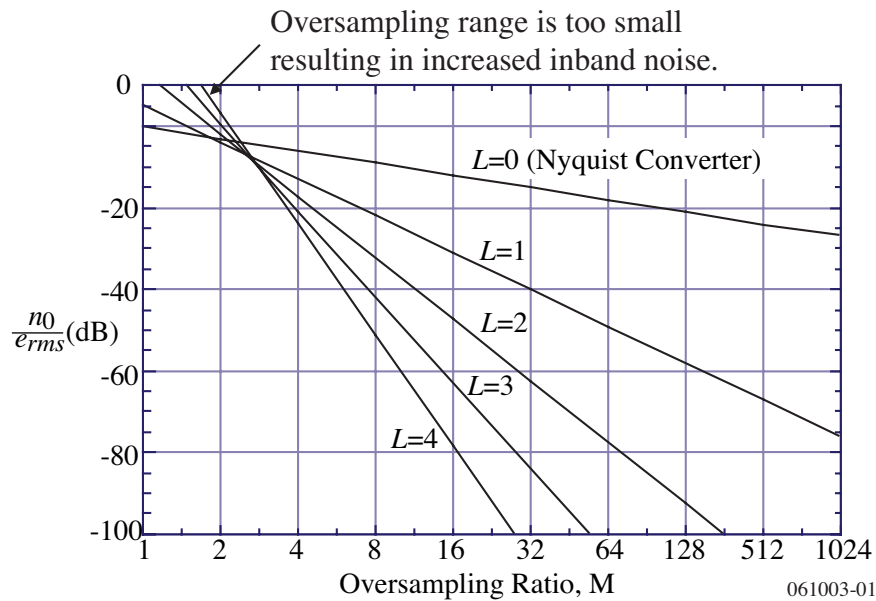
$n_0 \propto \frac{e_{rms}}{M^{L+0.5}} \Rightarrow$ Doubling of M leads to a $2^{L+0.5}$ decrease of in-band noise resulting in an extra $L+0.5$ bits of resolution!

\therefore The increase of the oversampling ratio is an excellent method of increasing the resolution of a $\Delta\Sigma$ oversampling analog-digital converter.

Illustration of RMS Noise Versus Oversampling Ratio for Single Loop $\Delta\Sigma$ Modulators

Plotting n_0/e_{rms} gives,

$$\frac{n_0}{e_{rms}} = \left(\frac{\pi^L}{\sqrt{2L+1}} \right) \left(\frac{1}{M^{L+0.5}} \right)$$



Dynamic Range of $\Delta\Sigma$ Analog-Digital Converters

Oversampled $\Delta\Sigma$ Converter:

The dynamic range, DR , for a 1 bit-quantizer with level spacing $\Delta = V_{REF}$, is

$$DR^2 = \frac{\text{Maximum signal power}}{S_B(f)} = \frac{\left(\frac{\Delta}{2\sqrt{2}} \right)^2}{\left(\frac{\pi^{2L}}{2L+1} \right) \left(\frac{1}{M^{2L+1}} \right) \left(\frac{\Delta^2}{12} \right)} = \frac{3}{2} \frac{2L+1}{\pi^{2L}} M^{2L+1}$$

Nyquist Converter:

The dynamic range of a N -bit Nyquist rate ADC is (now Δ becomes $\approx V_{REF}$ for large N),

$$DR^2 = \frac{\text{Maximum signal power}}{S_Q} = \frac{(V_{REF}/2\sqrt{2})^2}{\Delta^2/12} = \frac{3}{2} 2^{2N} \rightarrow DR = \sqrt{1.5} 2^N$$

Expressing DR in terms of dB (DR_{dB}) and solving for N , gives

$$N = \frac{DR_{dB} - 1.7609}{6.0206} \quad \text{or} \quad DR_{dB} = (6.0206N + 1.7609) \text{ dB}$$

Example: A 16-bit $\Delta\Sigma$ ADC requires about 98dB of dynamic range. For a second-order modulator, M must be 153 or 256 since we must use powers of 2.

Therefore, if the bandwidth is 20kHz, then the clock frequency must be 10.24MHz.

Multibit Quantizers

A single-bit quantizer:

$$\Delta = V_{REF}$$

Advantage is that the DAC is linear.

Multi-bit quantizer:

Consists of an ADC and DAC of B-bits.

$$\Delta = \frac{V_{REF}}{2^B - 1}$$

Disadvantage is that the DAC is no longer perfectly linear. To get large resolution delta-sigma ADCs requires highly precise DACs.

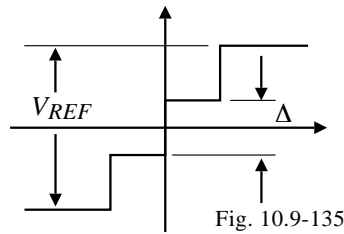


Fig. 10.9-13

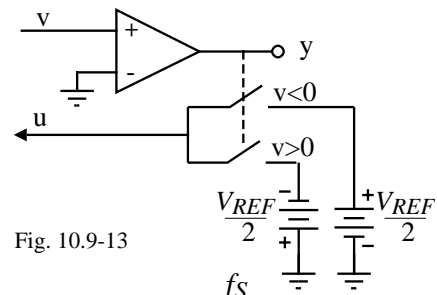


Fig. 10.9-13

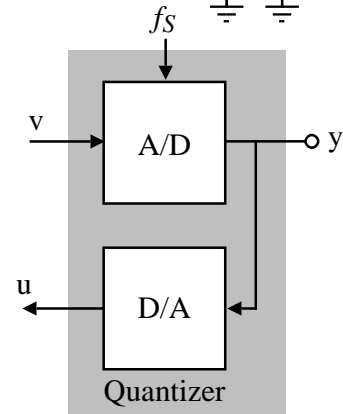


Fig. 10.9-14

Dynamic range of a multibit $\Delta\Sigma$ ADC:

$$DR^2 = \frac{3}{2} \frac{2L+1}{\pi^{2L}} M^{2L+1} (2^B - 1)^2$$

Example 10.8-1 - Tradeoff Between Signal Bandwidth and Accuracy of $\Delta\Sigma$ ADCs

Find the minimum oversampling ratio, M , for a 16-bit oversampled ADC which uses (a.) a 1-bit quantizer and third-order loop, (b.) a 2-bit quantizer and third-order loop, and (c.) a 3-bit quantizer and second-order loop. For each case, find the bandwidth of the ADC if the clock frequency is 10MHz.

Solution

We see that 16-bit ADC corresponds to a dynamic range of approximately 98dB.

(a.) Solving for M gives

$$M = \left(\frac{2}{3} \frac{DR^2}{2L+1} \frac{\pi^{2L}}{(2^B-1)^2} \right)^{1/(2L+1)}$$

Converting the dynamic range to 79,433 and substituting into the above equation gives a minimum oversampling ratio of $M = 48.03$ which would correspond to an oversampling rate of 64. Using the definition of M as $f_c/2f_B$ gives f_B as $10\text{MHz}/2 \cdot 64 = 78\text{kHz}$.

(b.) and (c.) For part (b.) and (c.) we obtain a minimum oversampling rates of $M = 32.53$ and 96.48, respectively. These values correspond to oversampling rates of 32 and 128, respectively. The bandwidth of the converters is 312kHz for (b.) and 78kHz for (c.).

Z-Domain Equivalent Circuits

The modulator structures are much easier to analyze and interpret in the z-domain.

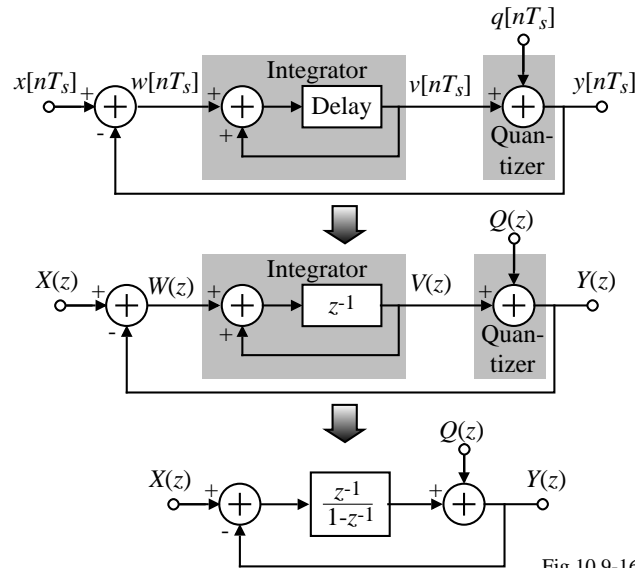


Fig.10.9-16

$$Y(z) = Q(z) + \left(\frac{z^{-1}}{1-z^{-1}} \right) [X(z) - Y(z)] \quad \rightarrow \quad Y(z) \left(\frac{1}{1-z^{-1}} \right) = Q(z) + \left(\frac{z^{-1}}{1-z^{-1}} \right) X(z)$$

$$\therefore Y(z) = (1-z^{-1})Q(z) + z^{-1}X(z) \quad \rightarrow \quad NTF_Q(z) = (1-z^{-1}) \text{ for } L = 1$$

Cascaded, Second-Order $\Delta\Sigma$ Modulator

Since the single-loop architecture with order higher than 2 are unstable, it is necessary to find alternative architectures that allow stable higher order modulators.

A cascaded, second-order structure:

$$Y_1(z) = (1-z^{-1})Q_1(z) + z^{-1}X(z)$$

$$X_2(z) = \left(\frac{z^{-1}}{1-z^{-1}} \right) (X(z) - Y_1(z))$$

$$= \left(\frac{z^{-1}}{1-z^{-1}} \right) X(z) - \left(\frac{z^{-1}}{1-z^{-1}} \right) [(1-z^{-1})Q_1(z) + z^{-1}X(z)]$$

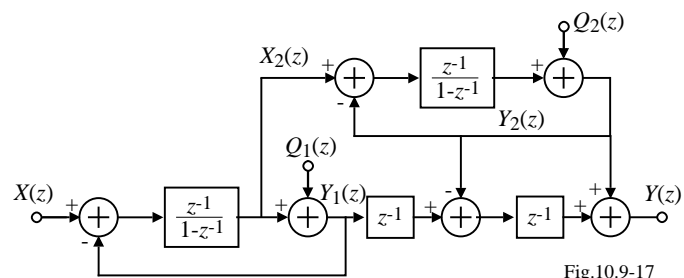


Fig.10.9-17

$$Y_2(z) = (1-z^{-1})Q_2(z) + z^{-1}X_2(z) = (1-z^{-1})Q_2(z) + \left(\frac{z^{-2}}{1-z^{-1}} \right) X(z) - z^{-2}Q_1(z) - \left(\frac{z^{-2}}{1-z^{-1}} \right) X(z)$$

$$= (1-z^{-1})Q_2(z) - z^{-2}Q_1(z)$$

$$Y(z) = Y_2(z) - z^{-1}Y_2(z) + z^{-2}Y_1(z) = (1-z^{-1})Y_2(z) + z^{-2}Y_1(z)$$

$$= (1-z^{-1})^2Q_2(z) - (1-z^{-1})z^{-2}Q_1(z) + (1-z^{-1})z^{-2}Q_1(z) + z^{-3}X(z) = (1-z^{-1})^2Q_2(z) + z^{-3}X(z)$$

$$\therefore Y(z) = (1-z^{-1})^2Q_2(z) + z^{-3}X(z)$$

Third-Order, MASH $\Delta\Sigma$ Modulator

It can be shown that

$$Y(z) = X(z) + (1-z^{-1})^3 Q_3(z)$$

This results in a 3rd-order noise shaping and no delay between the input and output.

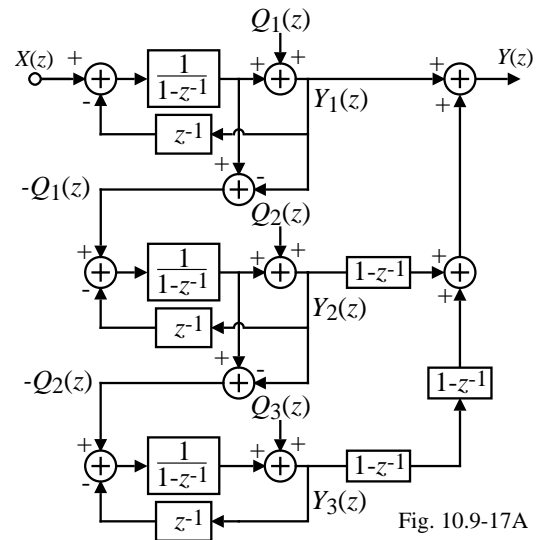
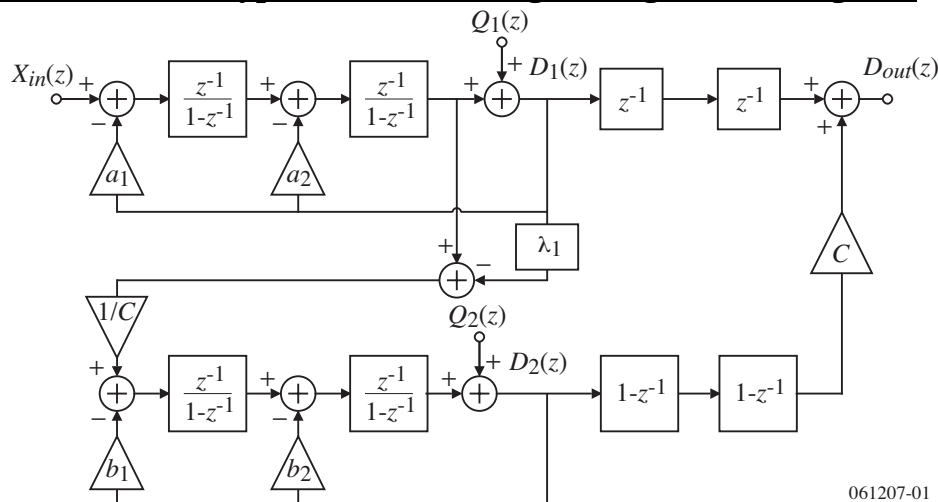


Fig. 10.9-17A

Comments:

- The above structures that eliminate the noise of all quantizers except the last are called *MASH* or multistage architectures.
- Digital error cancellation logic is used to remove the quantization noise of all stages, except that of the last one.

A Fourth-Order, MASH-type Modulator using Scaling of Error Signals[†]



061207-01

The various transfer functions are ($a_1=1$, $a_2=2$, $b_1=1$, $b_2=2$, $\lambda_1=2$ and $C=4$) :

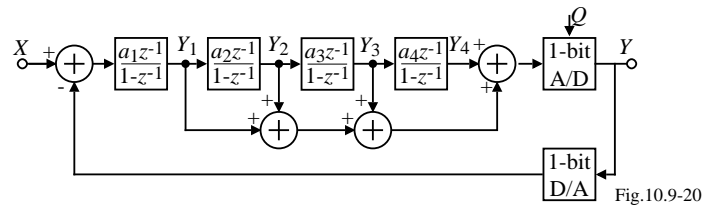
$$D_1(z) = X_{in}(z) + (1-z^{-1})^2 Q_1(z)$$

$$D_2(z) = (1/C)(-Q_1(z)) + (1-z^{-1})^2 Q_2(z)$$

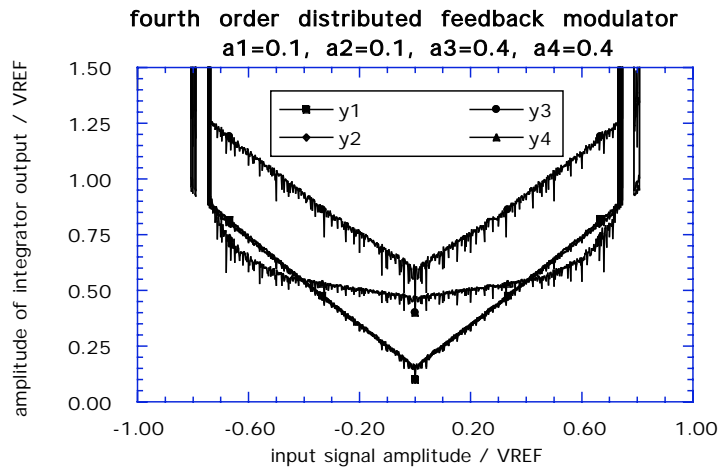
$$D_{out}(z) = X_{in}(z) + (1-z^{-1})^4 Q_2(z)$$

[†] U.S. Patent 5,061,928, Oct. 29, 1991.
CMOS Analog Circuit Design

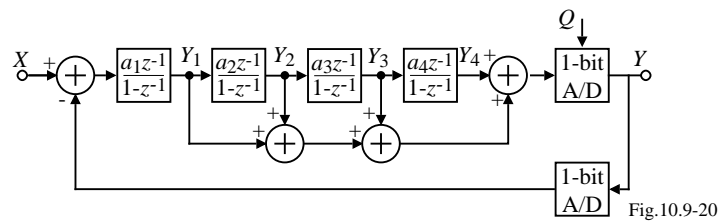
Distributed Feedback $\Delta\Sigma$ Modulator - Fourth-Order



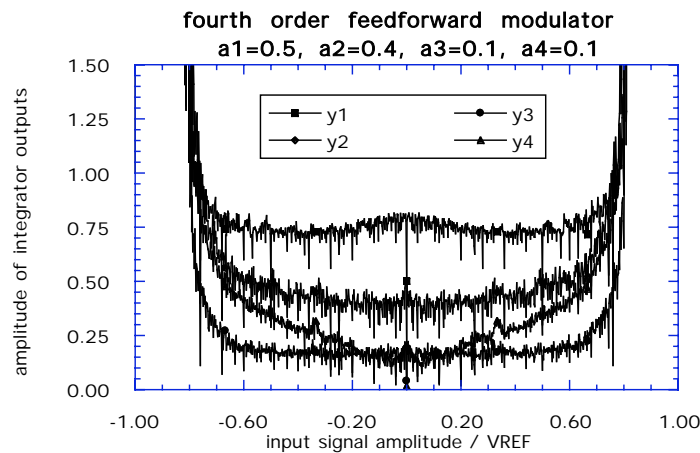
Amplitude of integrator outputs:



Distributed Feedback $\Delta\Sigma$ Modulator - Fourth-Order - Continued



Amplitude of integrator outputs:



Cascaded of a Second-Order Modulator with a First-Order Modulator

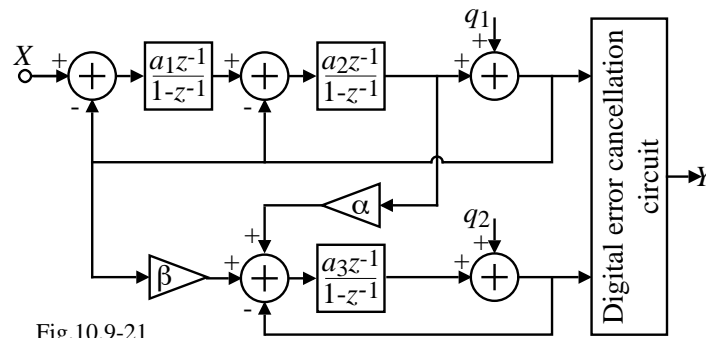


Fig.10.9-21

Comments:

- The stability is guaranteed for cascaded structures
- The maximum input range is almost equal to the reference voltage level for the cascaded structures
- All structures are sensitive to the circuit imperfection of the first stages
- The output of cascaded structures is multibit requiring a more complex digital decimator

Integrator Circuits for $\Delta\Sigma$ Modulators

Fundamental block of the $\Delta\Sigma$ modulator:

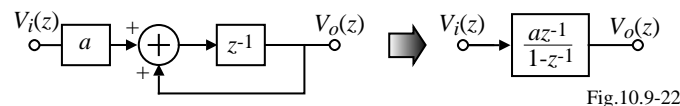


Fig.10.9-22

Fully-Differential, Switched Capacitor Implementation:

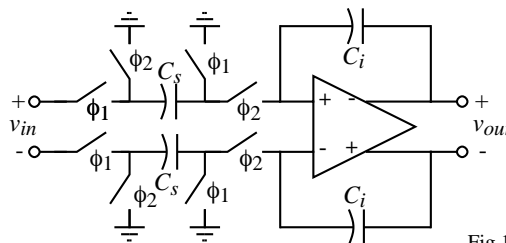


Fig.10.9-23

It can be shown (Chapter 9) that,

$$\frac{V_{out}(z)}{V_{in}(z)} = \left(\frac{C_s}{C_i}\right) \left(\frac{z^{-1}}{1-z^{-1}}\right) \Rightarrow \frac{V_{out}^o(e^{j\omega T})}{V_{in}^o(e^{j\omega T})} = \left(\frac{C_1}{C_2}\right) \frac{e^{j\omega T/2}}{j2 \sin(\omega T/2)} \left(\frac{\omega T}{\omega T}\right) = \left(\frac{C_1}{j\omega T C_2}\right) \left(\frac{\omega T/2}{\sin(\omega T/2)}\right) (e^{j\omega T/2})$$

$$\frac{V_{out}^o(e^{j\omega T})}{V_{in}^o(e^{j\omega T})} = (\text{Ideal}) \times (\text{Magnitude error}) \times (\text{Phase error}) \text{ where } \omega_l = \frac{C_1}{TC_2} \Rightarrow \text{Ideal} = \frac{\omega_l}{j\omega}$$

Power Dissipation Vs. Supply Voltage And Oversampling Ratio

The following is based on the above switched-capacitor integrator:

1.) Dynamic range:

The noise in the band $[-f_s, f_s]$ is kT/C while the noise in the band $[-f_s/2M, f_s/2M]$ is kT/MC . We must multiply this noise by 4; x2 for the sampling and integrating phases and x2 for differential operation.

$$\therefore DR = \frac{V_{DD}^2/2}{4kT/MC_s} = \frac{V_{DD}^2 MC_s}{8kT}$$

2.) Lower bound on the sampling capacitor, C_s : $C_s = \frac{8kT \cdot DR}{V_{DD}^2}$

3.) Static power dissipation of the integrator: $P_{int} = I_b V_{DD}$

4.) Settling time for a step input of $V_{o,max}$:

$$I_b = C_i \frac{V_{o,max}}{T_{settle}} = \left(\frac{C_i}{T_{settle}} \right) \left(\frac{C_s}{C_i} V_{DD} \right) = \frac{C_s V_{DD}}{T_{settle}} = C_s V_{DD} (2f_s) = 2M f_N C_s V_{DD}$$

$$\therefore P_{int} = 2M f_N C_s V_{DD}^2 = 16kT \cdot DR \cdot f_N$$

Because of additional feedback to the first integrator, the maximum voltage can be $2V_{DD}$.

$$P_{1st-int} = 32kT \cdot DR \cdot f_N$$

Implementation of $\Delta\Sigma$ Modulators

Most of today's delta-sigma modulators use fully differential switched capacitor implementations.

Advantages are:

- Doubles the signal swing and increases the dynamic range by 6dB
- Common-mode signals that may couple to the signal through the supply lines and substrate are canceled
- Charge injected by the switches are canceled to a first-order

Example:

First integrator dissipates the most power and requires the most accuracy.

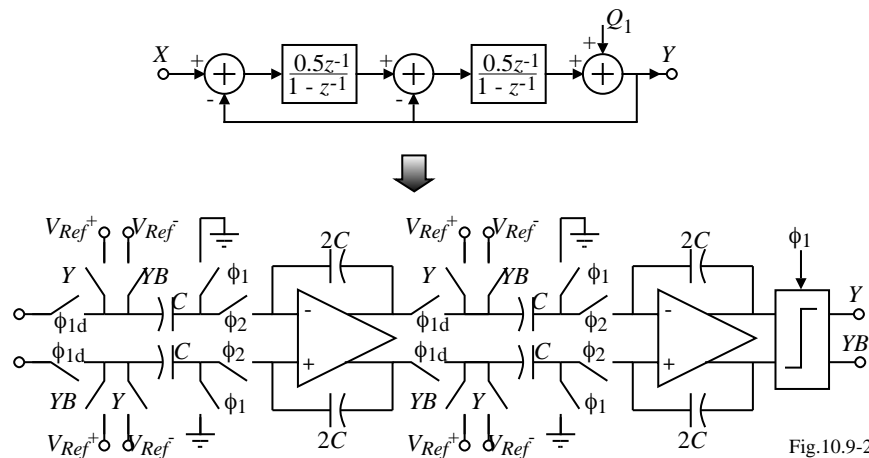


Fig. 10.9-24

Example - 1.5V, 1mW, 98db $\Delta\Sigma$ Analog-Digital Converter[†]

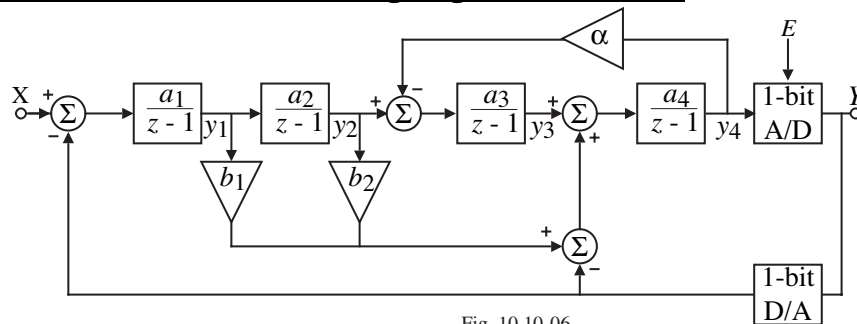


Fig. 10.10-06

where $a_1 = 1/3$, $a_2 = 3/25$, $a_3 = 1/10$, $a_4 = 1/10$, $b_1 = 6/5$, $b_2 = 1$ and $\alpha = 1/6$

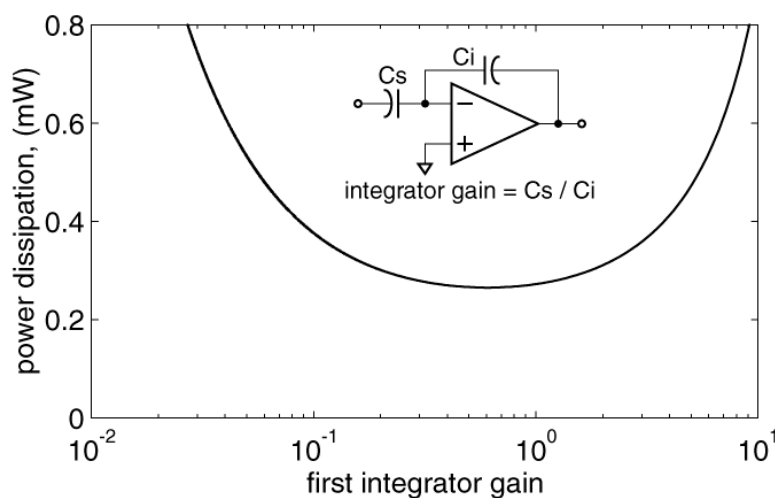
Advantages:

- The modulator combines the advantages of both DFB and DFF type modulators: Only four op amps are required. The 1st integrator's output swing is between $\pm V_{REF}$ for large input signal amplitudes ($0.6V_{REF}$), even if the integrator gain is large (0.5).
- A local resonator is formed by the feedback around the last two integrators to further suppress the quantization noise.
- The modulator is fully pipelined for fast settling.

[†] A.L. Coban and P.E. Allen, "A 1.5V, 1mW Audio $\Delta\Sigma$ Modulator with 98dB Dynamic Range," *Proc. of 1999 Int. Solid-State Circuits Conf.*, Feb. 1999, pp. 50-51.

1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

Integrator power dissipation vs. integrator gain



$DR = 98 \text{ dB}$

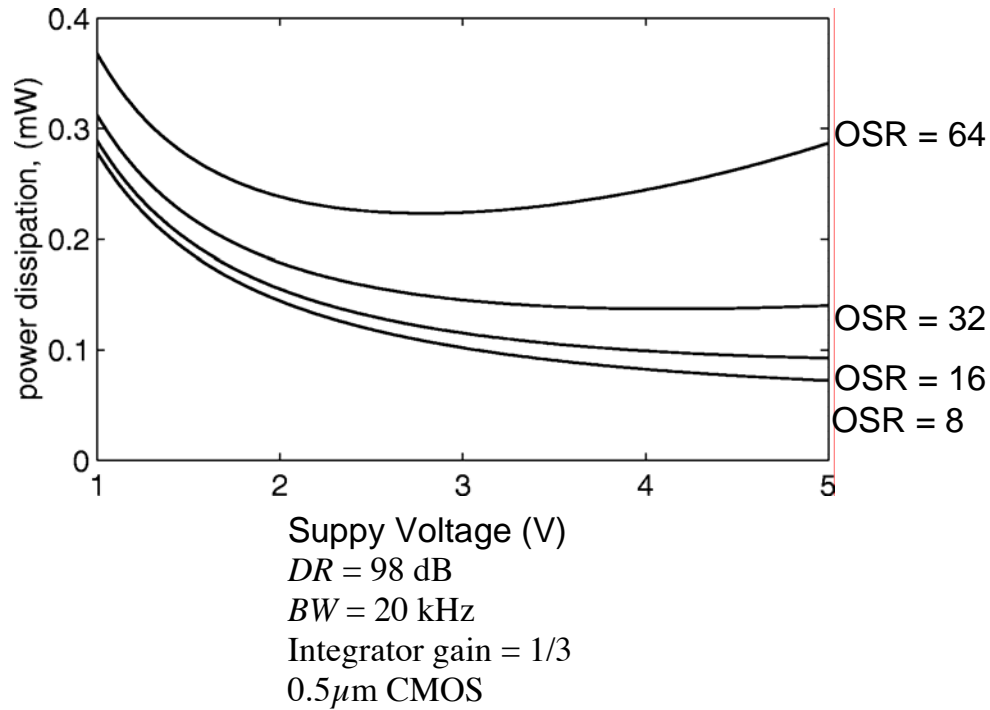
$BW = 20 \text{ kHz}$

$C_S = 5 \text{ pF}$

$0.5 \mu\text{m CMOS}$

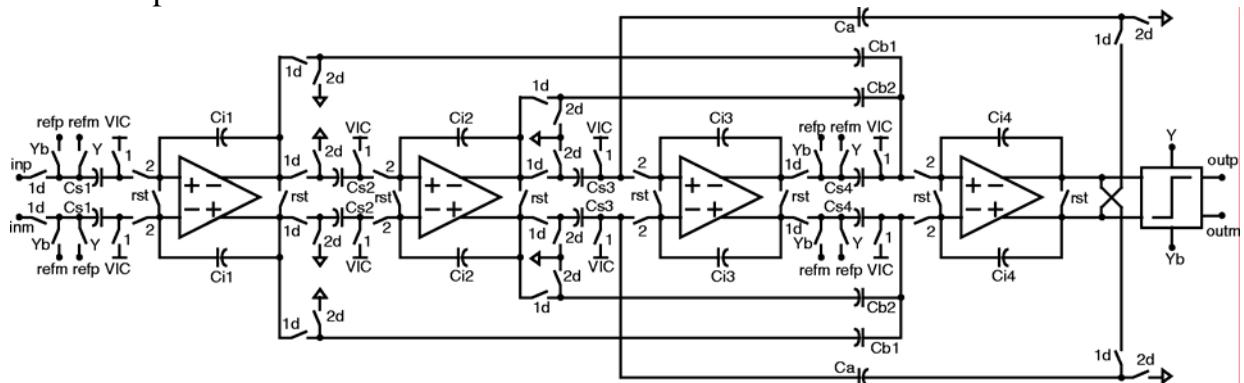
1.5V, 1mW, 98db $\Delta\Sigma$ Analog-Digital Converter - Continued

Modulator power dissipation vs. oversampling ratio



1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

Circuit Implementation:



Capacitor Values				
Capacitor	Integrator 1	Integrator 2	Integrator 3	Integrator 4
C_s	5.00pF	0.15pF	0.30pF	0.10pF
C_i	15.00pF	1.25pF	3.00pF	1.00pF
C_a	-	-	0.05pF	-
C_{b1}	-	-	-	0.12pF
C_{b2}	-	-	-	0.10pF

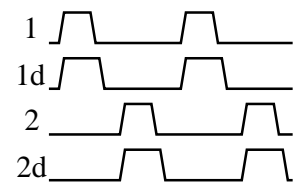
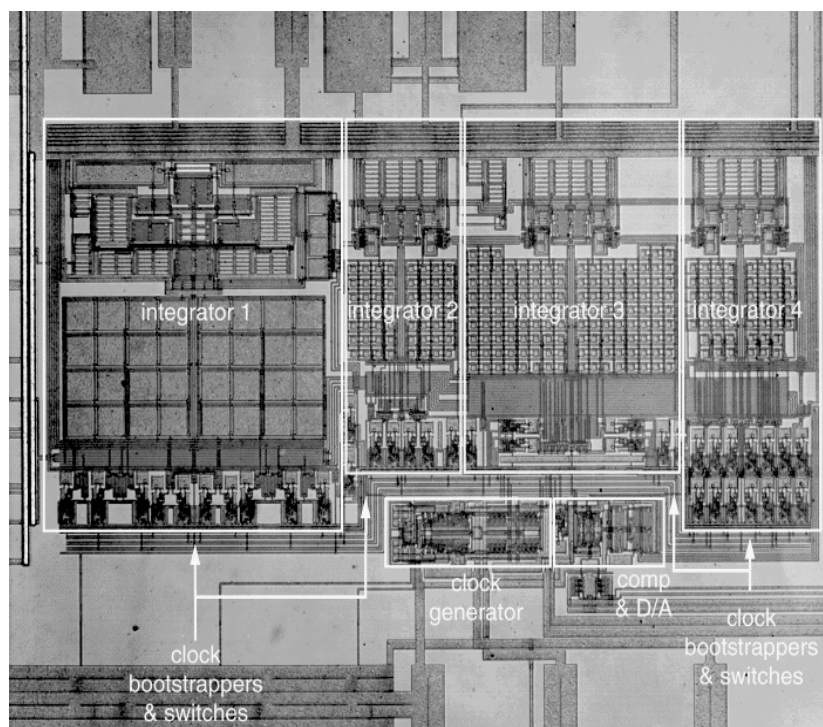


Fig.10.9-25

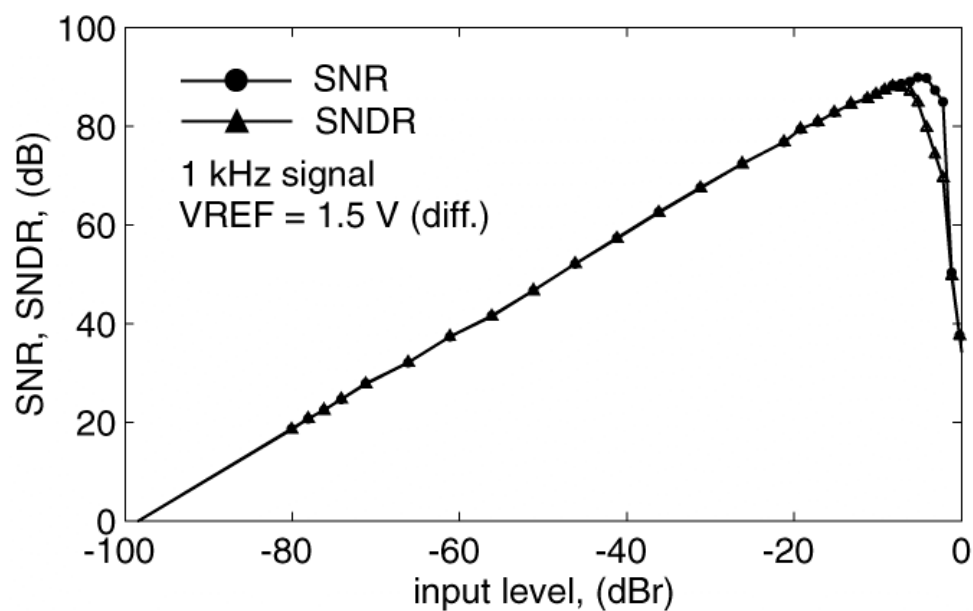
1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

Microphotograph of the $\Delta\Sigma$ modulator.



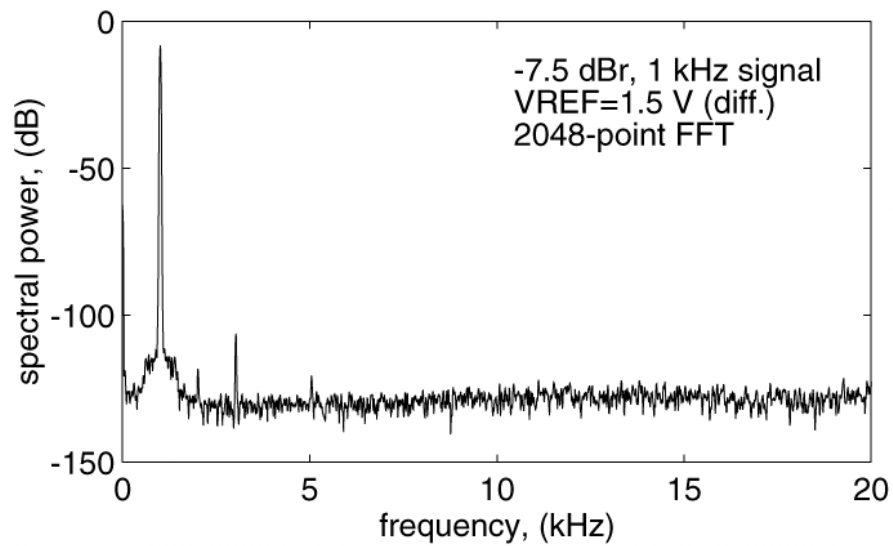
1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

Measured SNR and SNDR versus input level of the modulator.

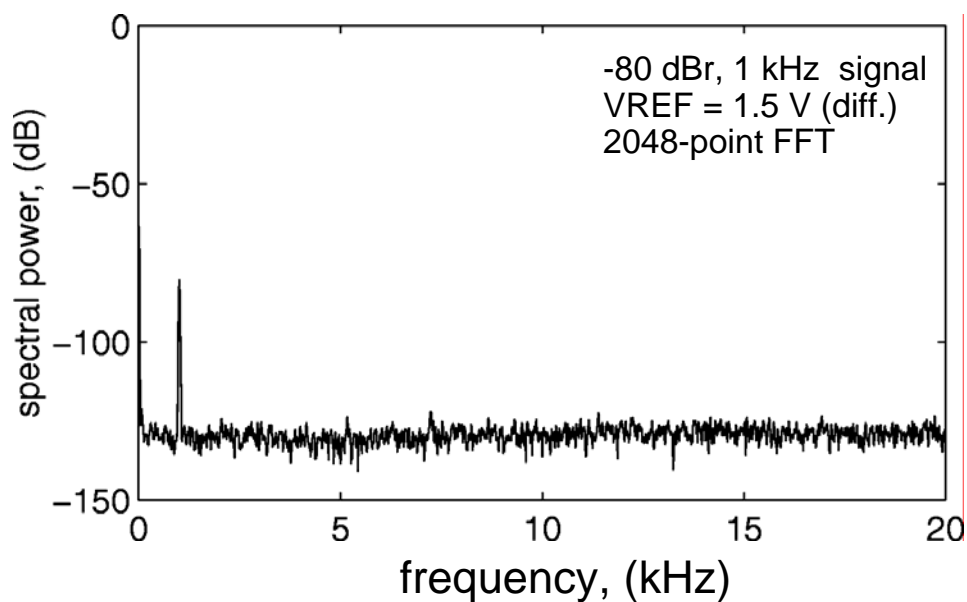


1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

Measured baseband spectrum for a -7.5dBr 1kHz input.

**1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued**

Measured baseband spectrum for a -80dBr 1kHz input.



1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

Measured 4th-Order $\Delta\Sigma$ Modulator Characteristics:

Table 5.4

Measured fourth-order delta-sigma modulator characteristics	
Technology : 0.5 μm triple-metal single-poly n-well CMOS process	
Supply voltage	1.5 V
Die area	1.02 mm x 0.52 mm
Supply current	660 μA
analog part	630 μA
digital part	30 μA
Reference voltage	0.75V
Clock frequency	2.8224MHz
Oversampling ratio	64
Signal bandwidth	20kHz
Peak SNR	89 dB
Peak SNDR	87 dB
Peak S/D	101dB
HD ₃ @ -5dBv 2kHz input	-105dBv
DR	98 dB

DECIMATION AND FILTERING

Delta-Sigma ADC Block Diagram

The decimator and filter are implemented digitally and consume most of the area and the power.

Function of the decimator and filter are;

- 1.) To attenuate the quantization noise above the baseband
- 2.) Bandlimit the input signal
- 3.) Suppress out-of-band spurious signals and circuit noise

Most of the $\Delta\Sigma$ ADC applications demand decimation filters with linear phase characteristics leading to the use of finite impulse response (FIR) filters.

FIR filters:

For a specified ripple and attenuation,

$$\text{Number of filter coefficients} \propto \frac{f_s}{f_t}$$

where f_s is the input rate to the filter (clock frequency of the quantizer) and f_t is the transition bandwidth.

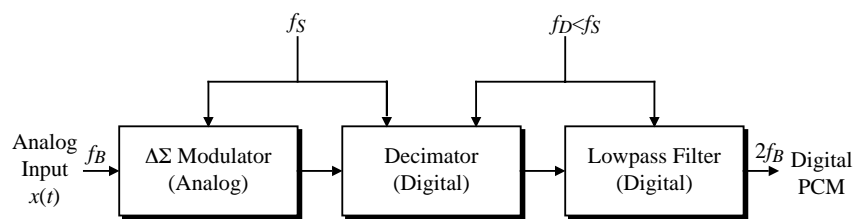


Fig.10.9-07

A Multi-Stage Decimation Filter

To reduce the number of stages, the decimation filters are implemented in several stages. Typical multi-stage decimation filter:

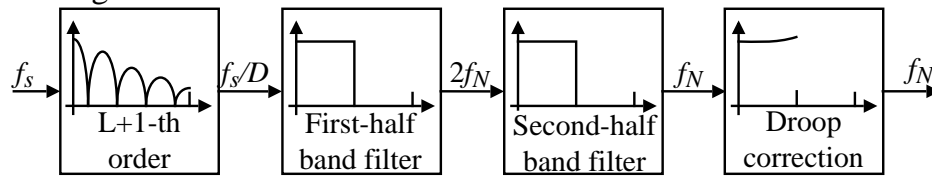


Fig.10.9-26

- 1.) For $\Delta\Sigma$ modulators with $(1-z^{-1})^L$ noise shaping comb filters are very efficient.
 - Comb filters are suitable for reducing the sampling rate to four times the Nyquist rate.
 - Designed to suppress the quantization noise that would otherwise alias into the signal band upon sampling at an intermediate rate of f_{s1} .
- 2.) The remaining filtering is performed by in stages by FIR or IIR filters.
 - Suppresses out-of-band components of the signal
- 3.) Droop correction - may be required depending upon the ADC specifications

Comb Filters

A comb filter that computes a running average of the last D input samples is given as

$$y[n] = \frac{1}{D} \sum_{i=0}^{D-1} x[n-i]$$

where D is the decimation factor given as

$$D = \frac{f_s}{f_{s1}}$$

The corresponding z -domain expression is,

$$H_D(z) = \sum_{i=1}^D z^{-i} = \frac{1}{D} \frac{1 - z^{-D}}{1 - z^{-1}}$$

The frequency response is obtained by evaluating $H_D(z)$ for $z = e^{j2\pi f T_s}$,

$$H_D(f) = \frac{1}{D} \frac{\sin \pi f D T_s}{\sin \pi f T_s} e^{-j2\pi f T_s / D}$$

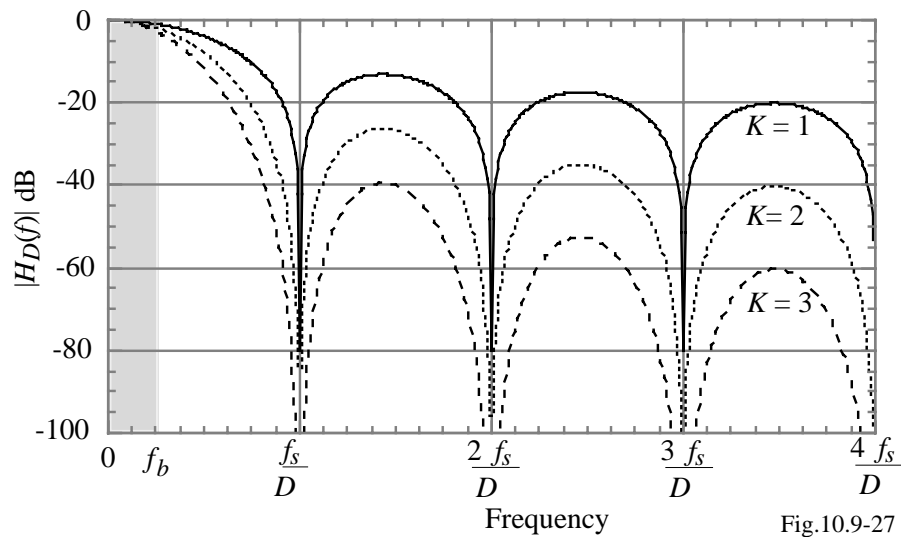
where T_s is the input sampling period ($=1/f_s$). Note that the phase response is linear.

For an L -th order modulator with a noise shaping function of $(1-z^{-1})^L$, the required number of comb filter stages is $L+1$. The magnitude of such a filter is,

$$|H_D(f)| = \left(\frac{1}{D} \frac{\sin \pi f D T_s}{\sin \pi f T_s} \right)^K$$

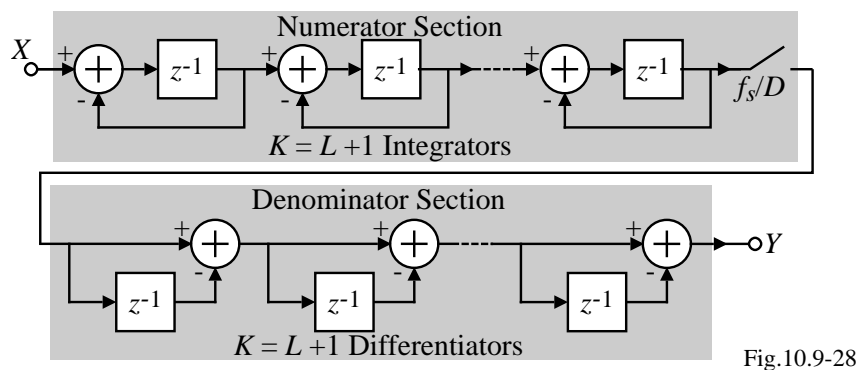
Magnitude Response of a Cascaded Comb Filter

$K = 1, 2$ and 3



Implementation of a Cascaded Comb Filter

Implementation:

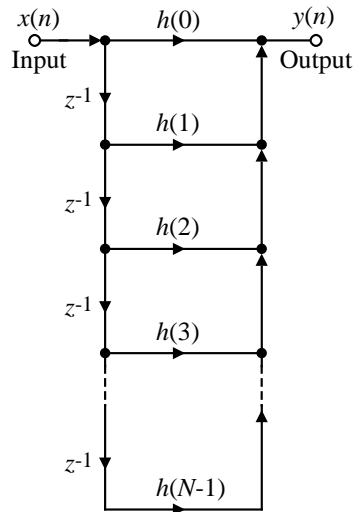


Comments:

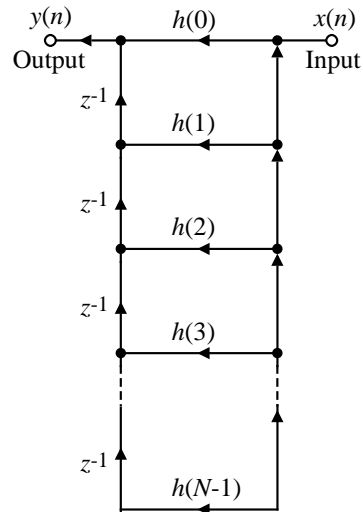
- 1.) The $L+1$ integrators operating at the sampling frequency, f_s , realize the denominator of $H_D(z)$.
- 2.) The $L+1$ differentiators operating at the output rate of $f_{s1} (= f_s/D)$ realize the numerator of $H_D(z)$.
- 3.) Placing the integrator delays in the feedforward path reduces the critical path from $L+1$ adder delays to a single adder delay.

Implementation of Digital Filters[†]

Digital filter structures:



Direct-form structure
for an FIR digital filter.



Transposed direct-form
FIR filter structure.

Fig.10.9-29

[†] S.R. Norsworthy, R. Schreier, and G.C. Temes, *Delta-Sigma Data Converters-Theory, Design, and Simulation*, IEEE Press, NY, Chapter 13, 1997.
CMOS Analog Circuit Design © P.E. Allen - 2006

Digital Lowpass Filter

Example of a typical digital filter used in removal of the quantization noise at higher frequencies

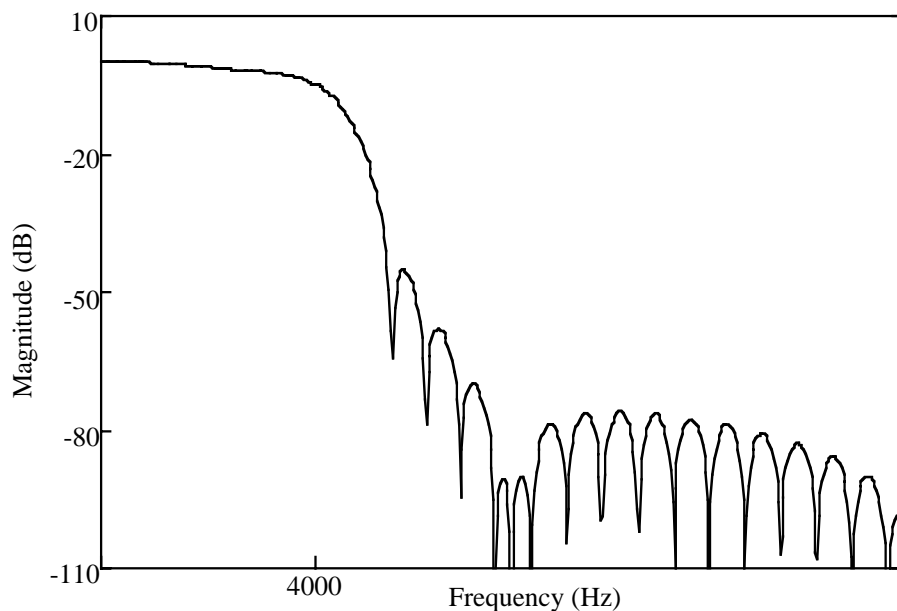
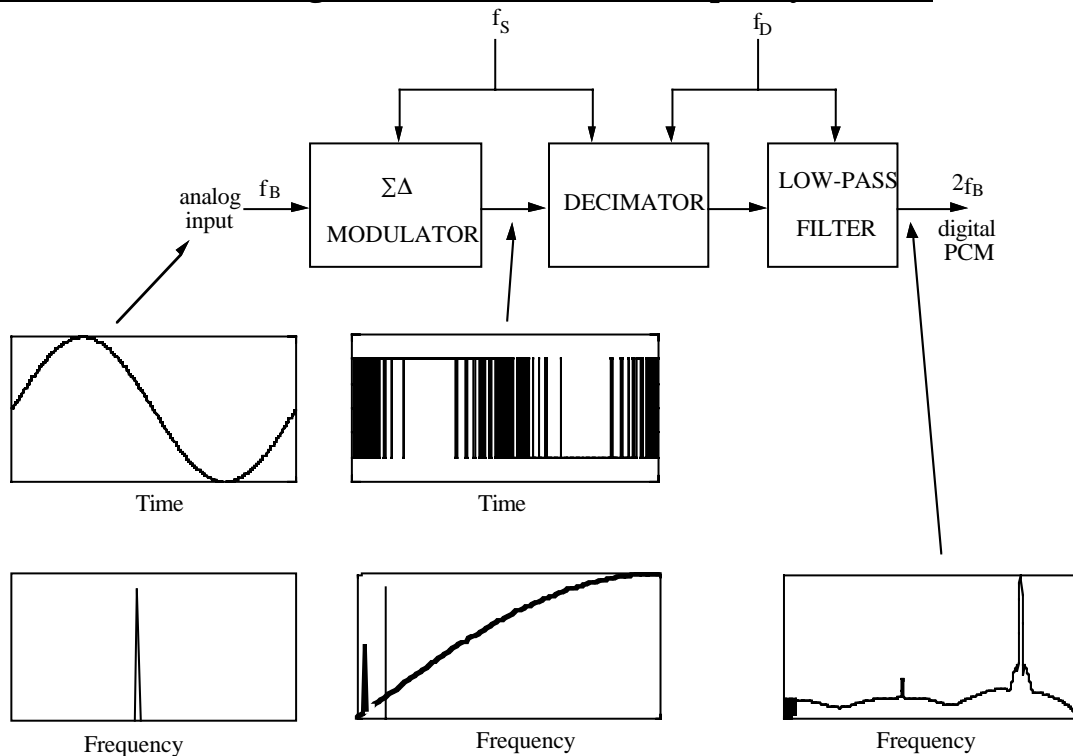


Illustration of the Delta-Sigma ADC in Time and Frequency Domain



BANDPASS DELTA-SIGMA MODULATORS

Bandpass $\Delta\Sigma$ Modulators

Block diagram of a bandpass modulator:

Components:

- Resonator - a bandpass filter of order $2N$, $N = 1, 2, \dots$
- Coarse quantizer (1 bit or multi-bit)

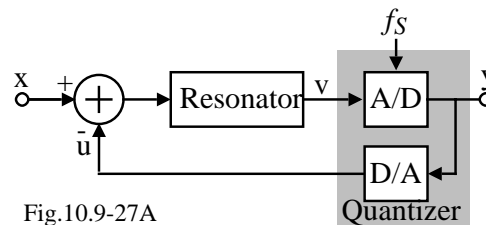


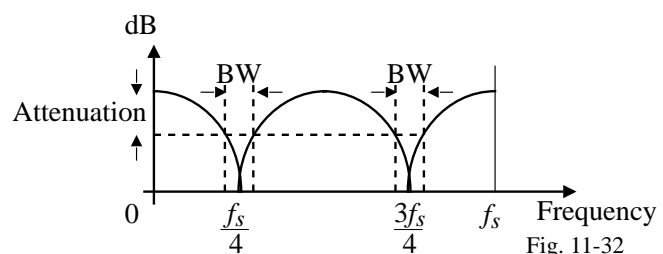
Fig.10.9-27A

The noise-shaping of the bandpass oversampled ADC has the following interesting characteristics:

$$\text{Center frequency} = f_s \cdot (2N-1)/4$$

$$\text{Bandwidth} = BW = f_s / M$$

Illustration of the Frequency Spectrum ($N=1$):



Application of the bandpass $\Delta\Sigma$ ADC is for systems with narrowband signals (IF frequencies)

A First-Order $\Delta\Sigma$ Bandpass Modulator

Bandpass Resonator:

$$V(z) = z^{-1} [X(z) - z^{-1}V(z)] = z^{-1}X(z) - z^{-2}V(z)$$

$$V(z) (1+z^{-2}) = z^{-1}X(z) \rightarrow \frac{V(z)}{X(z)} = \frac{z^{-1}}{1+z^{-2}}$$

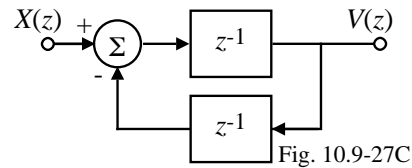


Fig. 10.9-27C

Modulator:

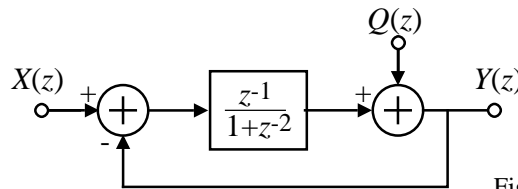


Fig.10.9-27B

$$Y(z) = Q(z) + [X(z) - Y(z)] \left(\frac{z^{-1}}{1+z^{-2}} \right) \rightarrow Y(z) = \left(\frac{1+z^{-2}}{1+z^{-1}-z^{-2}} \right) Q(z) + \left(\frac{z^{-1}}{1+z^{-1}-z^{-2}} \right) X(z)$$

$$NTF_Q(z) = \left(\frac{1+z^{-2}}{1+z^{-1}-z^{-2}} \right)$$

The $NTF_Q(z)$ has two zeros on the $j\omega$ axis.

Resonator Design

Resonators can be designed by applying a lowpass to bandpass transform as follows:

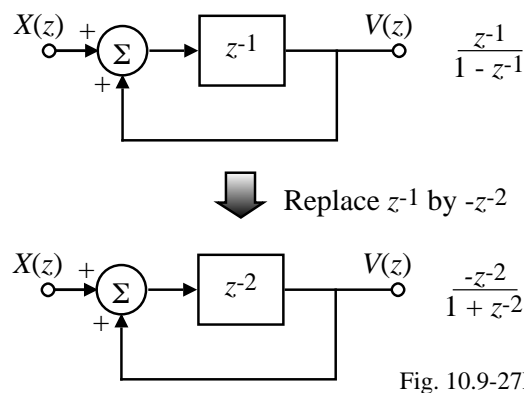


Fig. 10.9-27D

Result:

- Simple way to design the resonator
- Inherits the stability of a lowpass modulator
- Center frequency located at $f_s/4$

Fourth-Order Bandpass $\Delta\Sigma$ Modulator

Block diagram:

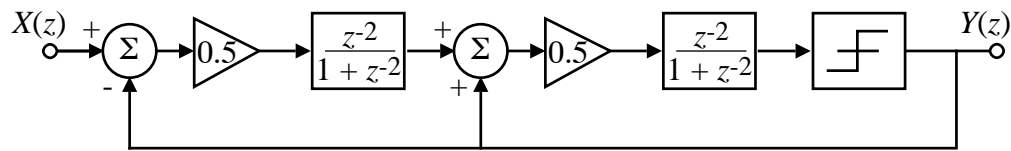


Fig. 10.9-27E

Comments:

- Designed by applying a lowpass to bandpass transform to a second-order lowpass $\Delta\Sigma$ modulator
- The stability and SNR characteristics are the same as those of a second-order lowpass modulator
- The z -domain output is given as,

$$Y(z) = z^{-4}X(z) + (1+z^{-2})^2Q(z)$$
- The zeros are located at $z = \pm j$ which corresponds to notches at $f_s/4$.

Resonator Circuit Implementation

Block diagram of $z^{-2}/(1+z^{-2})$:

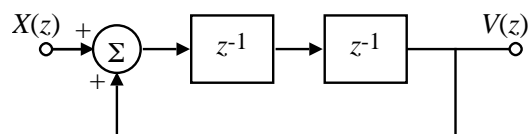


Fig. 10.9-27F

Fully differential switch-capacitor implementation:

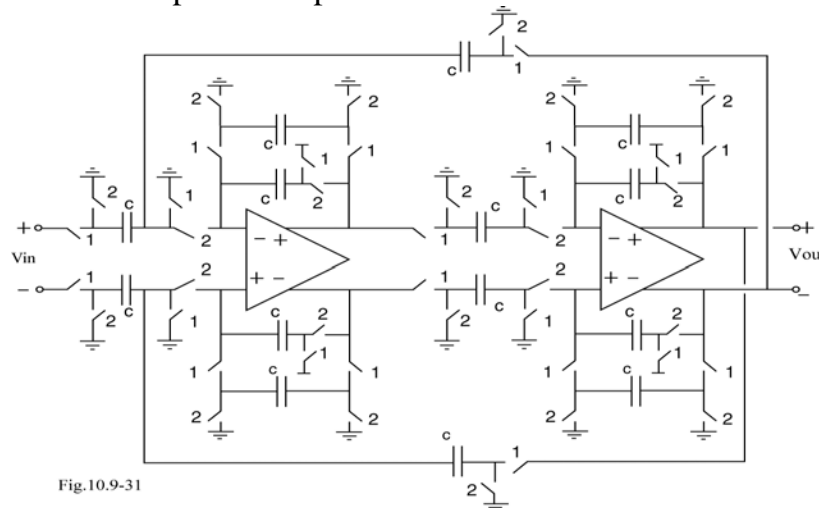
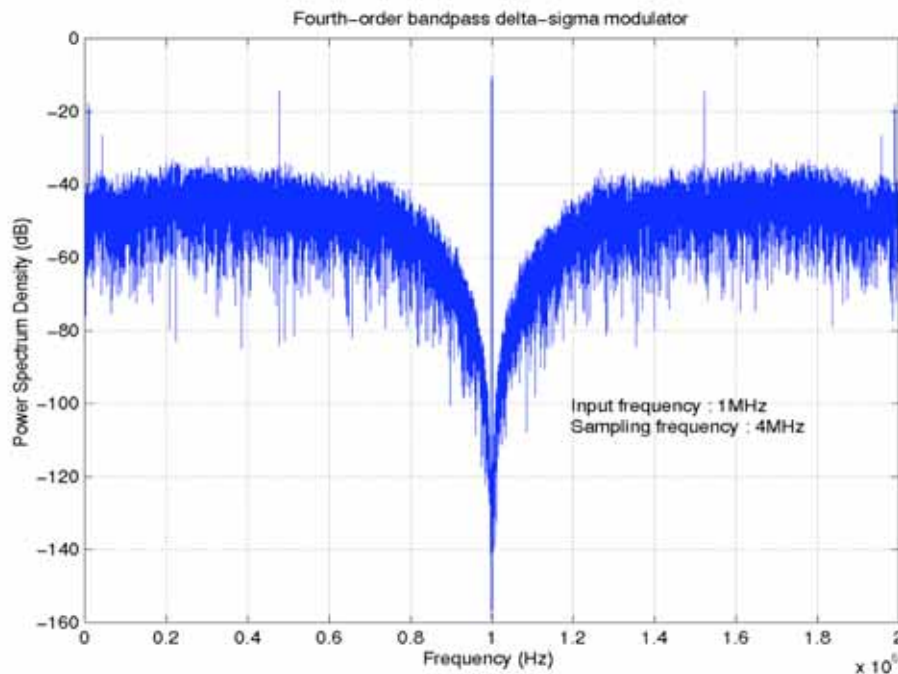


Fig. 10.9-31

Power Spectral Density of the Previous Fourth-Order Bandpass $\Delta\Sigma$ Modulator

Simulated result:



DELTA-SIGMA DIGITAL-TO-ANALOG CONVERTERS

Principles

The principles of oversampling and noise shaping are also widely used in the implementation of $\Delta\Sigma$ DACs.

Simplified block diagram of a delta-sigma DAC:

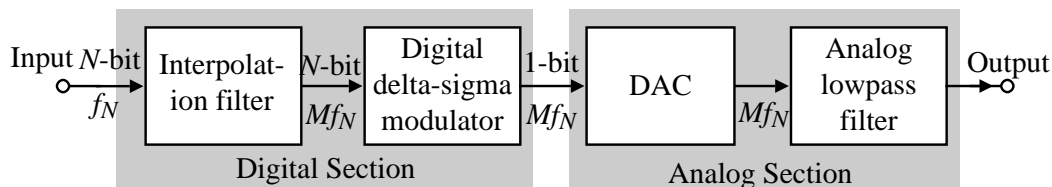


Fig10.9-29

Operation:

- 1.) A digital signal with N -bits with a data rate of f_N is sampled at a higher rate of Mf_N by means of an interpolator.
- 2.) Interpolation is achieved by inserting “0”s between each input word with a rate of Mf_N and then filtering with a lowpass filter.
- 3.) The MSB of the digital filter is applied to a DAC which is applied to an analog lowpass filter to achieve the analog output.

Block Diagram of a $\Delta\Sigma$ DAC

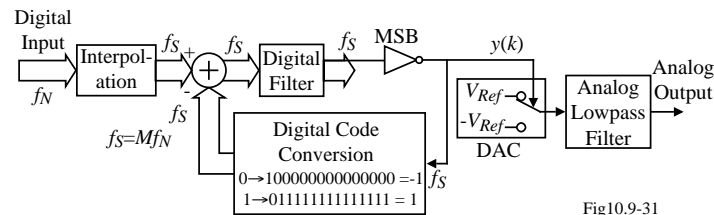


Fig10.9-31

Operation:

- 1.) Interpolate a digital word at the conversion rate of the converter (f_N) up to the sample frequency, f_s .
- 2.) The word length is then reduced to one bit with a digital sigma-delta modulator.
- 3.) The one bit PDM signal is converted to an analog signal by switching between two reference voltages.
- 4.) The high-frequency quantization noise is removed with an analog lowpass filter yielding the required analog output signal.

Sources of error:

- Device mismatch (causes harmonic distortion rather than DNL or INL)
- Component noise
- Device nonlinearities
- Clock jitter sensitivity
- Inband quantization error from the $\Delta\Sigma$ modulator

1-BitDAC for the $\Delta\Sigma$ Digital-to-Analog Converter - The Analog Part

The MSB output from the digital filter is used to drive a 1-bit DAC.

Possible architectures:

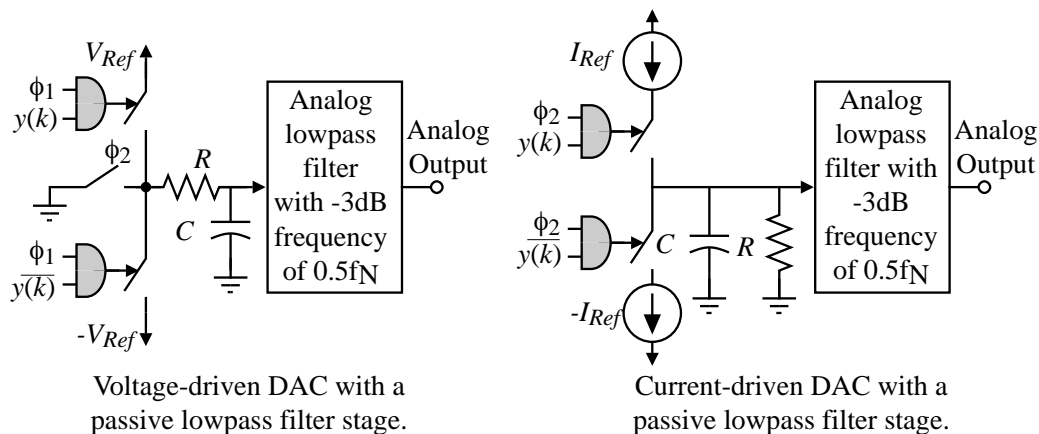


Fig10.9-32

Errors in the 1-Bit DAC

Offset Error:

$$V_{ref} \neq |-V_{ref}| \text{ or } I_{ref} \neq |-I_{ref}| \Rightarrow \text{Offset error}$$

Influence of offsets in the voltage reference:



The resulting transfer function is:

$$v(t) = V_{ref} + \Delta V_{ref1}, \quad y(k) = 1$$

or

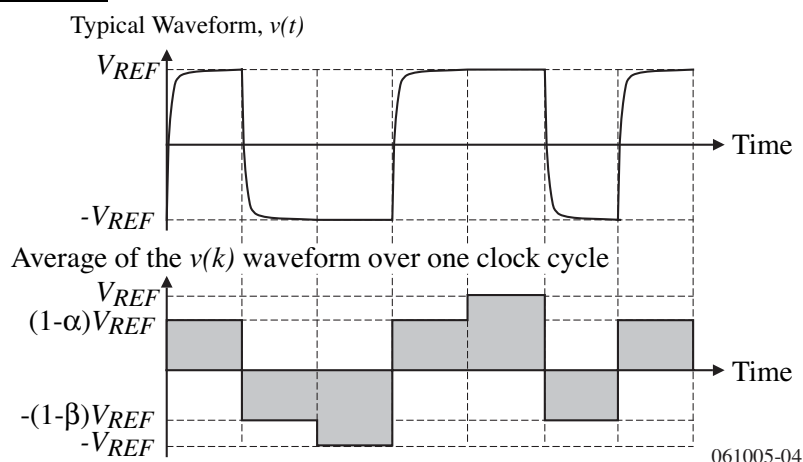
$$v(t) = -V_{ref} + \Delta V_{ref2}, \quad y(k) = -1$$

$$\therefore v(t) = \left(V_{ref} + \frac{\Delta V_{ref1} - \Delta V_{ref2}}{2} \right) y(k) + \frac{\Delta V_{ref1} + \Delta V_{ref2}}{2}$$

This results in a gain or an offset error, but the output is still linear.

Errors in the 1-Bit DAC - Continued

Switching Time Error:



Let, $v(k) = V_{REF}$, $y(k) = 1$
and $y(k-1) = 1$

$$v(k) = (1-\alpha)V_{REF}, \quad y(k) = 1 \text{ and } y(k-1) = -1$$

$$v(k) = -V_{REF}, \quad y(k) = -1 \text{ and } y(k-1) = -1$$

$$v(k) = -(1-\beta)V_{REF}, \quad y(k) = -1 \text{ and } y(k-1) = 1$$

Therefore, the transfer function becomes,

$$v(k) = [(\beta-\alpha) + (\alpha+\beta)y(k-1) + (4-\alpha-\beta)y(k) + (\alpha-\beta)y(k) \cdot y(k-1)] (V_{REF}/4)$$

(Note: The ϕ_2 switch in the voltage DAC removes this error by resetting the voltage at every clock.)

Switched-Capacitor DAC and Filter

Typically, the DAC and the first stage of the lowpass filter are implemented using switched-capacitor techniques.

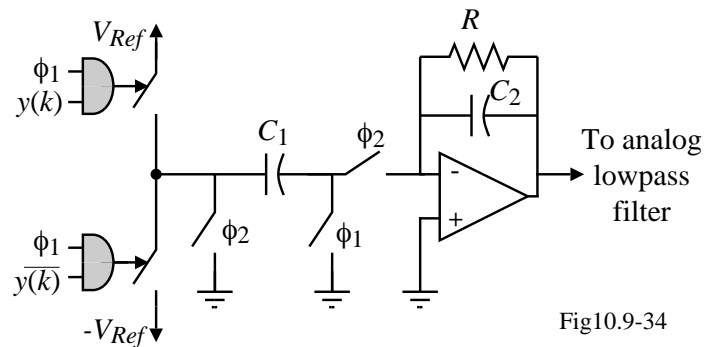


Fig10.9-34

It is necessary to follow the switched-capacitor filter by a continuous time lowpass filter to provide the necessary attenuation of the quantization noise.

Frequency Viewpoint of the $\Delta\Sigma$ DAC

Frequency spectra at different points of the delta-sigma ADC:

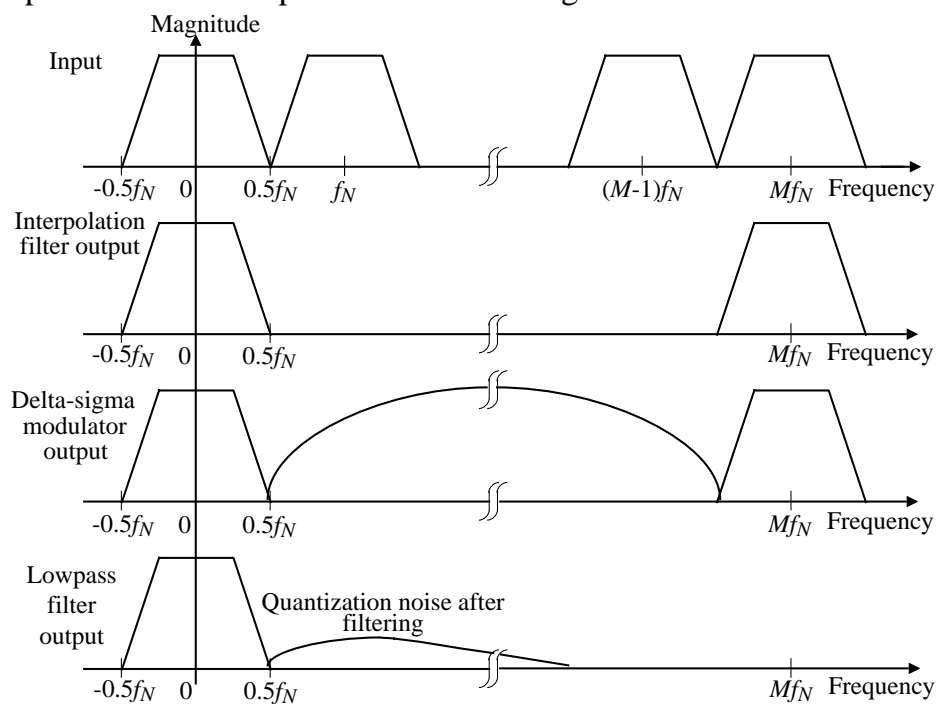


Fig10.9-33

Comparison of the $\Delta\Sigma$ ADC and $\Delta\Sigma$ DAC

Both the $\Delta\Sigma$ ADC and $\Delta\Sigma$ DAC have many of the same properties

- Loops with identical topologies have the same stability conditions
- Loops with identical topologies have the same amount of quantization noise for a given oversampling ratio
- Higher order loops give better noise shaping and more dynamic range
- Multiple bit DACs are also used in $\Delta\Sigma$ DACs as well as $\Delta\Sigma$ ADCs

SECTION 10.9 - SUMMARY

Comparison of the Various Types of ADCs

A/D Converter Type	Maximum Practical Number of Bits (± 1)	Speed (Expressed in terms of T a clock period)	Area Dependence on the number of bits, N , or other ADC parameters
Dual Slope	12-14 bits	$2(2NT)$	Independent
Successive Approximation with self-correction	12-15 bits	NT	$\propto N$
1-Bit Pipeline	10 bits	T (After NT delay)	$\propto N$
Algorithmic	12 bits	NT	Independent
Flash	6 bits	T	$\propto 2^N$
Two-step, flash	10-12 bits	$2T$	$\propto 2^{N/2}$
Multitple-bit, M-pipe	12-14 bits	MT	$\propto 2^{N/M}$
Δ - Σ Oversampled (1-bit, L loops and M = oversampling ratio = $f_{\text{clock}}/2f_b$)	15-17 bits	MT	$\propto L$

Comparison of Recent ADCs

Resolution versus conversion rate:

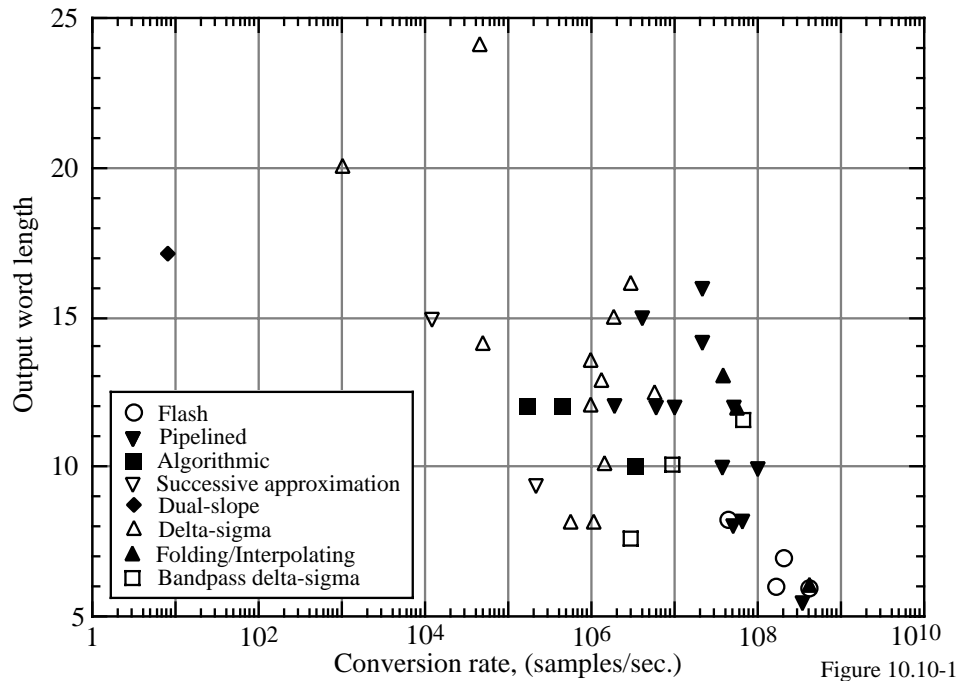


Figure 10.10-1

Comparison of Recent ADCs - Continued

Power dissipation versus conversion rate:

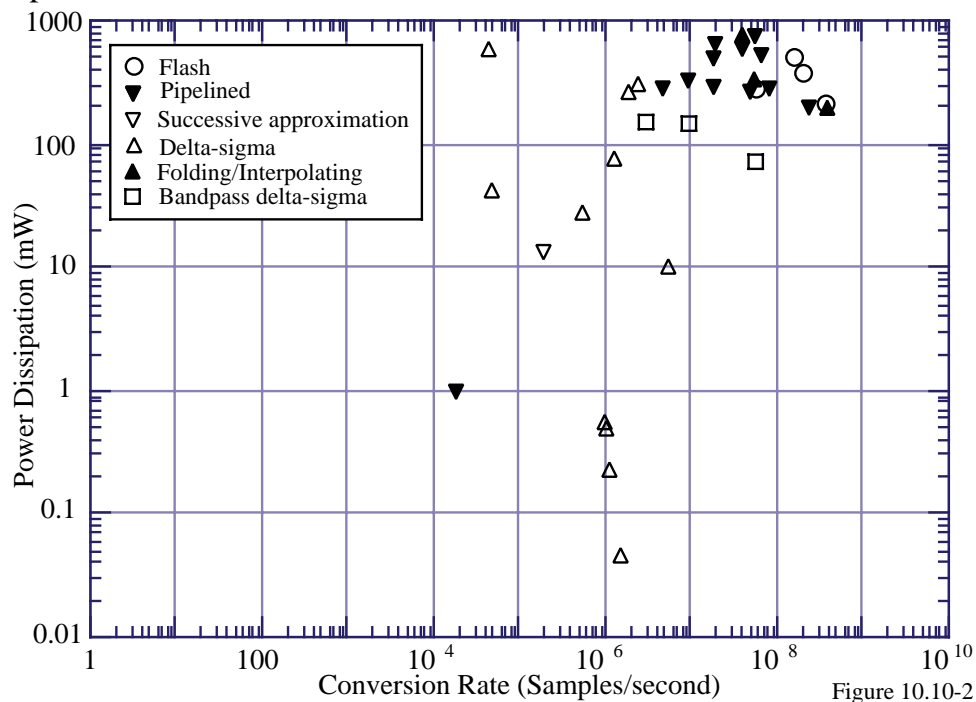


Figure 10.10-2

References for Previous Figures

- [1] A 12-b, 60-MSample/s Cascaded Folding and Interpolating ADC. *Vorenkamp, P.*, IEEE J-SC, vol. 32, no. 12, Dec 97 1876-1886
- [2] A 15-b, 5-Msample/s Low-Spurious CMOS ADC. *Kwak, S. -U.*, IEEE J-SC, vol. 32, no. 12, Dec 97 1866-1875
- [3] Error Suppressing Encode Logic of FCDL in a 6-b Flash A/D Converter. *Ono, K.*, IEEE J-SC, vol. 32, no.9, Sep 97 1460-1464
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CONCLUSION

- Key aspects:

- 1.) Square law relationship:

$$i_D = \frac{K'W}{2L} (v_{GS} - V_T)^2$$

- 2.) Small-signal transconductance formula:

$$g_m = \sqrt{\frac{2K'WI_D}{L}}$$

- 3.) Small-signal simplification:

$$g_m \approx 10g_{mbs} \approx 100g_{ds}$$

- 4.) Saturation relationship:

$$V_{DS}(\text{sat}) = \sqrt{\frac{2I_D}{K'(W/L)}}$$

- Remember to think and understand the problem before using the simulator.
- Any questions concerning the course can be e-mailed to palen@ece.gatech.edu
- Other analog resources can be found at www.aicdesign.org