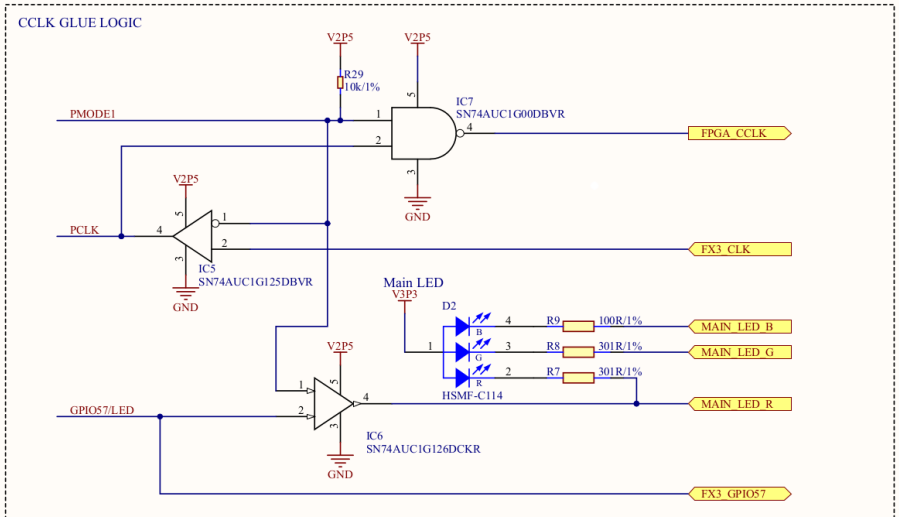


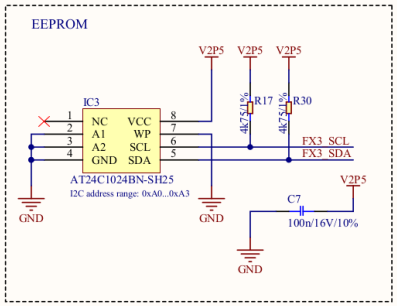


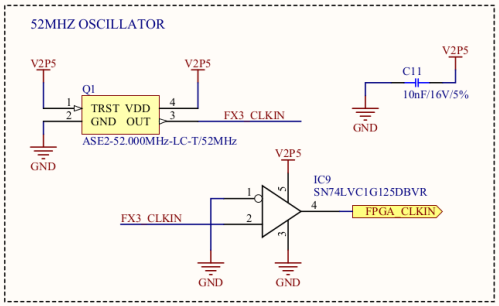


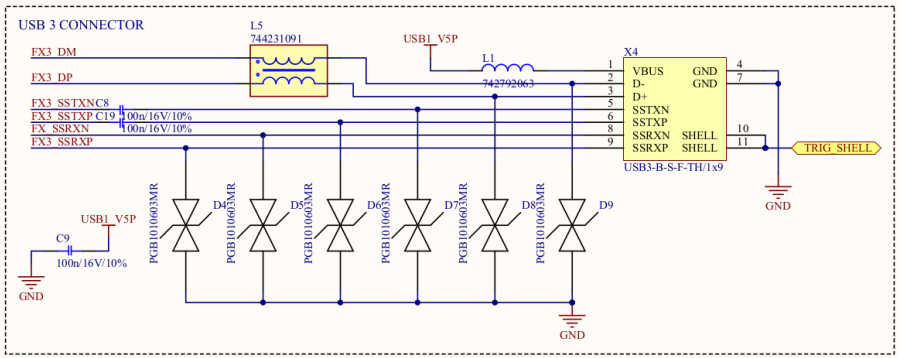


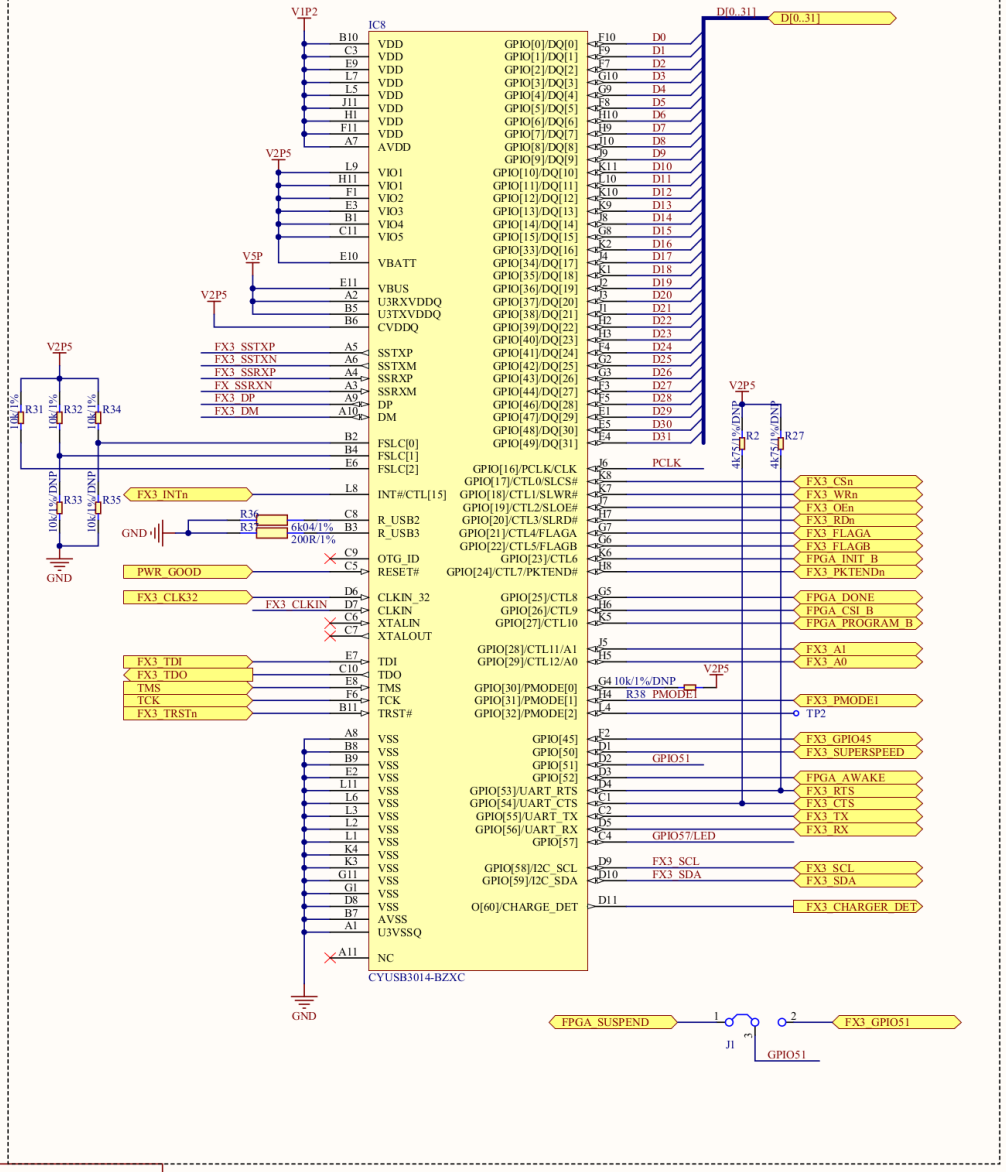


## Layout Rules

1. The following signals are I2C bus signals and must be routed carefully to avoid crosstalk: FX3_SCL, FX3_SDA
2. D0 to D31 have to be routed carefully and as short as possible (100 MHz)
3. See EZ-USB FX3 Hardware Design Guidelines (AN70707.pdf) for further layout recommendations
4. The following signals are asynchronous signals and must be routed carefully to avoid crosstalk: FX3_TRSTn, FX3_INTn
5. The following signals are clocks and must be routed carefully to avoid crosstalk: FPGA_CLKIN, FX3_CLKIN, FPGA_CCLK, TCK

Content: FX3 USB 3.0 Controller, EEPROM

Customer:

Project:

Date: 09.01.2013 | Rev.: 0.1 | Size A3

File: P09_USB3_Controller_EEPROM.SchDoc | Sheet 9 of 12