样例程序: ASC\_SSC\_IIC 例程

1.简介

本程序实现功能如下:

利用三个USIC模块,通过PC串口传送一个字节的数据给一个USIC模块,该USIC模块 通过SSC把数据传送给另一个USIC模块,再通过IIC把数据传输给另一个USIC,最后传送给 PC机。

使用到的模块: USIC

2. XE164F/XE164FM USIC模块介绍

USIC模块介绍:

USIC(通用串行接口通道)是一个灵活的接口模块,支持多种串行通信协议。XE164F/XE164FM中有3个USIC模块,每个USIC模块包含两个独立的通信通道

USIC模块支持以下协议:

- UART (ASCII, 异步串行通道)
  - 模块功能:接收器/发送器,最大波特率f<sub>sys</sub>/4 目标波特率范围: 1.2kBaud-3.5MBaud 每个数据帧包含的数据个数: 1-63 MSB或LSB在先
- 硬件支持的LIN协议(低成本网络,波特率最高20kBaud) 基于ASC协议的数据传送 可由内置波特率发生器的捕获事件实现波特率检测 软件控制校验和产生(实现更高的灵活性)
- SSC/SPI(带有/不带从控选择线的同步串行通道) 模块功能:从控模式,最大波特率f<sub>SYS</sub>/2 模块功能:主控模式,最大波特率f<sub>SYS</sub>/2 目标波特率范围: 2kBaud-10MBaud 每个数据帧包含1-63位数据,对于超过63位的数据帧,需明确定义数据帧的结

束

MSB或LSB在先

- IIC (Inter-IC总线) 波特率范围: 100kBaud-400kBaud 支持7位或10位寻址 完整的主控和从控器件功能
- IIS(信息娱乐音频总线)
   模块功能:接收器,最大波特率f<sub>sys</sub>
   模块功能:发送器,最大波特率f<sub>sys</sub>/2
   目标波特率范围:高达26MBaud

USIC结构不仅能灵活的选择通信协议,还能降低系统负载(CPU负载)、从而保证高效的数据处理。

3.操作流程



# 4.DAVE 配置

# 4.1 New Project:选择XE164F/XE164FM XE164F

XE164FM

B DAvE - New Project	Ave - New Project
16-Bit Microcontrollers 8-Bit Microcontrollers	16-Bit Microcontrollers 8-Bit Microcontrollers
XCT64CM XE164FM XCT64GM XE167F XCT64KM XE167FM XCT64LM XCT64LM XCT64LM XCT64TM XCT64TM XE164FM XE164F	XC164CM XE164FM XC164GM XE167FM XC164KM XE167FM XC164KM XE167FM XC164LM XC164LM XC164TM XC164TM XE162FM XE164FM XE164F
Create Cancel Help	Create Cancel Help

4. 2 The project settings

# XE164F

ROM Size 576 KRote ROM Ture Flath
Max CPU Clock 80 MHz
Main Header File

# XE164FM

e XE164F-96F	66 •	ROM Size 768 K	Byte ROM Type Flash	-
Source File		Main Header	File	
name MAIN.	С	File name	MAIN.H	
name MAIN.	c	File name	MAIN.H	

System clock

XE164F

eneral System Clock Global Settings CPUCON1 / VI	ECSEG   Notes
System Frequency ISYS C ISYS [MHz] = 80.00 F ISYS [MHz] = 66.00 C ISYS Through PLL Note: External Oscillator Frequency (OSC is 8 MHz.	Clock Dutput Control Enable Clock Output Clock Source (EXTCON.SEL) ISYS as ext ck Clock Source (EXTCON.SEL)
Configuration of PLL Configure PLL (SVS (MHz) n-a	Configure IOUT

# XE164FM

System Frequency fSYS       Clock Output Control            ••• fSYS [MHz] = 80.00           □•• Enable Clock Output             ••• fSYS [MHz] = 66.00           □•• Clock Source (EXTCON.SEL)	
(FSYS [MHz] = 80.00     [SYS [MHz] = 66.00     [SYS [MHz] = 66.00     [SYS [MHz] = 66.00	
C (SYS IMHz) = 66.00 Clock Source (EXTCON.SEL)	
	fSYS as ext clk 💌
C Use Pin P2.8 as CLKOUT	
C ISYS Through PLL C Use Pin P7.1 as CLKOUT	
Note: External Uscillator Frequency (USC is 8 MHz. C) Use both pins P2.8, P7.1	as CLKOUT
Configuration of PLL	

# 4.3 配置USIC0模块(XE164F和XE164FM的配置基本相同,以XE164F为例) 点击USIC0



一个通道选ASC另一个通道选SSC

😨 Universal Serial Interface Channel (USICO)	×
🔁 🚛 - 💡	
Protocol	
USIC0 Channel 0 Protocol Selection	
USIC Protocol for U0C0	
USIC0 Channel 1 Protocol Selection	
USIC Protocol for U0C1 SSC	

# 点击CH0



fodule Enable U0C0 — ▼ Enable module kerne	el clock and module functionality	Input Clock Input clock [MHz] [66
Peration Mode Full-Duplex Half-Duplex LoopBack Data IrDA	Half-Duplex Connection Type External C Internal Pin Selection Transmit (TxD) P7.3 Receive (RxD) P7.4	Baud Rate Required baud rate [kbaud] [9.600 Step value (STEP) 0x1DD Divider factor (PDIV) 0x063 Real Baud rate [kbaud] 9.600
CRL Settings Pulse Length 0 -		Parity Selection No parity C Even parity C Odd parity

使能该模块,全双工,发送端口P7.3,接收端口P7.4,波特率9600,无校验位,一位停止位

# 选择需要DAvE生成的函数

iitia 7	U0C0_ASC_vInit File name	0.C	Header File File name UOCO.H			
uno	ction Library (Part 1)	Fu	inction Libra	ry (Part 2)		
7	U0C0_ASC_vSendData	Г	UOCO_AS	C_VFIIITxFIFD		
7	U0C0_ASC_uwGetData	Г	UOCO_AS	C_uwGetRxFIF0Data		
7	U0C0_ASC_ubTxDataReady	Г	UOCO_ASC_ubisRxFIFObusy			
	U0C0_ASC_ubTxBufFree	Г	U0C0_ASC_ublsTxFIF0busy			
-	U0C0_ASC_ubRxDataReady	Г	UUCO_ASC_ubisRxFIFD/ull			
1	UOCO_ASC_VIOIC	Г	UOCO_AS	C_ublsTxFIF0full		
1	UCCO_ASC_vitIC	Г	UOCO_AS	C_ublsRxFIFDempty		
1	UOCO_ASC_VI2IC	Г	UOCO_AS	C_ublsTxFIFOempty		
	UOCO_ASC_VI3IC_CC2	Г	UOCO_AS	C_ubGetRxFIFDFillingLevel		
		Г	UOCO_AS	C_ubGetTxFIF0FillingLevel		
		Г	UOCO_AS	C_vFlushBxFIFD		
		Г	UOCO AS	© vFlushTxFIF0		

## 点击CH1



使能开模块, 主模式, 时钟输出P2.8, 发送P2.9, 接收P2.10, 波特率100k, LSB first ……

lodule Enable UOC1 -		- Input C	Clock	
Enable Module; the second s	e peripheral is supplied with the clo	ck signal Input	Clock [MHz] 66	
peration Mode	Pin Selection For Slave	Baud Ral	ie	
Master Mode)	Clock(CLK) Output	Required	Baud Rate [kbaud]	00.000
C Slave Mode	Tx Data Output P2.9	Step Val	ue (STEP)	308
oop Back Mode	Rx Data Input	0 J	actor (PDIV)	(OF9
– Enable Loop Back	SELOO None SELOI No	ne 🗾 Real Bar	ud Rate (kbaud)	00.000
eading Control (HB)-	Word Length/	Frame Length	Clock Polarity and P	hase
Transmit/Received	ELSB first Word Length	n [bits] 8 -	Clock Polarity	0 🔻
C Transmit/Receiv	e MSB first FrameLength	[bits] 8 -	Clock Phase	0 -

# 选择需要DAvE生成的函数



# 配置USIC1 点击USIC1



一个通道选择SSC,另一个通道选择IIC

😵 Universal Serial Interface Channel (USIC1)	×
Protocol	
USIC1 Channel 0 Protocol Selection	
USIC Protocol for U1C0 SSC	
USIC1 Channel 1 Protocol Selection	
USIC Protocol for U1C1	

配置CH0,

vlodule Enable U1C0 I⊄ Enable Module; ti	ne peripheral is su	oplied with the clock sign	Input C	lock Clock (MHz) 66
C Master Mode Master Mode Slave Mode Loop Back Mode Enable Loop Back	Pin Selection F Clock(CLK) In Tx Data Outp Rx Data Input Slave Select I	nput P10.11 • P10.13 • P10.12 • P10.12 • P10.12 •	Baud Rat Required Step Vak Divider F Real Bar	e I Baud Fible (baud) In a ve (STEP) In a actor (PDIV) In a id Role (baud) In a
Heading Control (HB) ( Transmit/Receiv Transmit/Receiv	e LSB first e MSB first	- Word Length/Frame I Word Length [bits] FrameLength [bits]	ength	Clock Polarity and Phase - Clock Polarity 0 Clock Phase 0

# 选择需要DAvE生成的函数

Initi.	zation Function J1C0_SSC_vinit File name		on Function Source File File name U1C0.C File name			
Fun	ction Library (Part 1)	10	Function Librar	(Part 2)		
7	U1C0_SSC_vSendData		T [1100_550	-VERTAFIED		
-	UTED_SSE_vSeiSELD		F GHCD_SSI	JunGHRINFIFED ata		
7	U1C0_SSC_uwGetData		U100_55	_ubhiPivPIPObusy		
Y.	U1C0_SSC_ubTxBufFree		IT MICE SS	UDI. THEFTED Sury		
5	U1C0_SSC_ubTxDataReady		UTC0_SSI	LubleFixFIFDInd		
V	U1C0_SSC_ubRxDataReady		UTC0-59	_odd #Tid71F01ull		
	U100_5\$C_90IC		L1C0_58	LUGH FINETED emply		
Γ.	U100_\$57_\vit10		T UTCO SS	Ubl TxFFDempty		
-	UTED_SSE_VER		U102_58	UBG #RIFTFOFRIngLevel		
F	LITEQUESSE_WHILL CE2		T UTCO_SS	UbGerTyFIF0FilingLevel		
			T U100_56	OFINIAR FIFO		
			T DICO SSI	WEIGHT JEIEU		

配置CH1

Enable U1C1	is supplied with the input clock	IIC General Input clock [MHz]: 66
Operation mode Master mode Slave mode Address mode	Pin selection SCL pin P0.5 SDA pin P0.6	Baud rate Baud rate [kbaud] [100.000 Step value (STEP) [0x317
7 bit Addr     7 bit [0x0]     10 bit [0x0]     Stave acknowledge to addr	ess ) Iress,00H (ACK,00)	Real Baud rate [100,000 [kbaud]

选择需要DAvE生成的函	数

ier	neral   Control   FIFO   Interrupts   Int. Extension	Bank	Select   PEI	C Functions Notes
nitia Z	alization Function Source File U1C1_IIC_vInit File name	U1C	1.C	Header File File name U1C1.H
un	ction Library (Part 1)	- Fu	inction Libra	ry (Part 2)
1	U1C1_IIC_vMasterTransmit			_vFillTxFIFO
1	U1C1_IIC_vMasterReceive			uwGetRxFIF0Data
7	U1C1_IIC_vWriteData		UTELLIC	_ublsRxFIF0busy
7	U1C1_IIC_uwReadData		UTCI_IIC	LubisTxFIFObusy
7	U1C1_IIC_uwGetStatus		UTE1_IIC	_ablsRxFIF0full
7	U1C1_IIC_vResetStatus		U1C1_IIC	_ublsTxFIFOruli
7	U1C1_IIC_vEnableACK			_ublsRxFIF0empty
7	U1C1_IIC_vDisableACK		U1C1_IIC	_ublsTxFIFOempty
	U1C1_IIC_vInitSlaveMode			_ubGe)RxFIF0FillingLevel
	U1C1_IIC_violC		U1C1_IIC	ubGetTxFIFOFillingLevel
	UTCI_IIC_vitIC			vFlushRxFIFO
-	UTET HE VER		UTCI IIC	vFlushTxFIF0

# 配置USIC2



#### 一个通道选IIC

🚭 Universal Serial Interface Channel (USIC2)	×
💌 🐠 - 🖇	
Protocol	
	1
USIC2 Channel 0 Protocol Selection	
USIC Protocol for U2C0	
- USIC2 Channel 1 Protocol Selection	
USIC Protocol for U2C1 None	

# 配置CH0

Enable U2C0 Enable module; the modu	le is supplied with the input clock	IIC General	66
Operation mode	Pin selection	Baud rate	-
C Master mode	SCL pin P1.7 💌	Baud rate [kbaud]	100.000
( Slave mode)	SDA pin P1.6	Step value (STEP)	0x317
Address mode			10 010
T bit Add	liess	Unvider factor (PDIV)	Inana
<ul> <li>C 10 bit</li> <li>☐ Slave acknowledge to ac</li> </ul>	01 diress 00H (ACK00)	Real Baud rate [kbaud]	100.000
Mata			

### 选择需要DAvE生成的函数

ier	neral Control FIFO Interrupts Int. Extension	n Bank	Select PEC	Functions Notes
nitia 7	alization Function Source File U2C0_IIC_vInit File name	020	0.C	Header File File name U2C0.H
un	ction Library (Part 1)	F	unction Library	(Part 2)
7)	U200_IIC_vMasterTransmit	Г	U208_IIC	VENTXEIFO
	U200_IIC_vMasterReceive	Г	U2DO_HC	uwGetR:/FIFDData
7	U2C0_IIC_vWriteData	Г	U200_HC	ubisRxFIFObusy
7	U2C0_IIC_uwReadData	Г	USCO_HC	ubisTxFIFBbusy
7	U2C0_IIC_uwGetStatus	Г	U208_IIC_	abisRxFIFD/al
7	U2C0_IIC_vResetStatus	Г	U2CO_IIC	ubisitxFIFOtul
7	U2C0_IIC_vEnableACK	Г	U200_110	ubicRxFIFO empty
7	U2C0_IIC_vDisableACK	T	U200_110	ubitItyFIFOemply
7	U2C0_IIC_vinitSlaveMode	Г	D2C8_HC	abGetAxFIFOFilingLevel
	U200_IIC_W0IC	Г	UZCO IIC	ubGerTxFIFOFillmaLevel
	U200_RC_willC	Г	U2DE IIC	vFilehBxFIFO
	U200 /UE w2IE	Г	U2C0 IIC	VENDATVEIED

## 5.利用DAVE 生成代码

点击 保存project, 点击 **A** DAVE 自动生成代码, 生成的代码即包括前面所选择 的函数。



6.修改用户代码

6.1 在project space中加入Project



Look in 的路径为DAvE所生成的文件所在路径 Files of type 中选 Infineon DAvE Project Files 选中Infineon DAvE Project文件

Select One or	More Projects to Add to P	roject Space	? ×
Look in:	ASC_SSC_ IIC	-) - 🗈 (	• 📰 *
ASC_SSC_	цс)		
File name:	ASC_SSC_IIC		Open
Files of type:	Infineon DAvE Project Files	<u> </u>	Cancel Help

# 点击已把DAvE生成的文件添加到project中

B ada (10 Eilea)	Project: H:\\XE164	FVASC_SSC_IICVASC_SSC_IIC.p
acc (10 Files)	Files:	
ASC_SSC_IIC (25 Files) asd (14 Files) can (2 Files) CC2 (4 Files) CC2 (4 Files) CCU6 (12 Files) CCU6 (12 Files) Gpt (11 Files) March (16 Files) March (18 Files)	H:\My Databases\XE164FV H:\My Databases\XE164FV	ASC_SSC_IIC/U1C0.C ASC_SSC_IIC/USIC1.H ASC_SSC_IIC/USIC1.C ASC_SSC_IIC/U1C1.H ASC_SSC_IIC/U1C1.C ASC_SSC_IIC/U2C0.H ASC_SSC_IIC/U2C0.C ASC_SSC_IIC/U2C0.C ASC_SSC_IIC/U2C0.C ASC_SSC_IIC/USIC2.H ASC_SSC_IIC/USIC2.C ASC_SSC_IIC/ASC_SSC_IIC.nf ASC_SSC_IIC/ASC_SSC_IIC.nf ASC_SSC_IIC/ASC_SSC_IIC.nf ASC_SSC_IIC/ASC_SSC_IIC.nf
iic3 (20 Files)	F Hide files already in proje	ect 0 of 25 selected
- io (o riles) - o pec (12 Files) - o pwm_m (8 Files) - o pwm_test (8 Files)	External Makefile: <none></none>	
Dimit (est for nes)	VCC Designation	

将该工程设定为当前工程

TASKING EDE	[ XE166 - H:\My Da	atabases\XE164F	\IIC3\iic3.pjt	1	
<u>Eile Edit Sea</u>	rch <u>Project</u> Build	Text Documer	t <u>G</u> ustomize	Tools 7	Window
***	1 6 1 5	i 🔏 🐂 📖  .	221		*
	0	×		-	
C:\	6 v8.7r3\bin\guo.psp				
guo (23 Proj	ects)	1			
🖻 🚱 adc (10 P	Files)				
E asc_ssc_	iic (20 Files)				
E C ASC SS					
🕀 🚳 asd (14 F	ile Set as Current	Project			
🖻 🐴 can (2 Fi	les Remove from F	Project Space			
🖽 🚱 CC2 (4 Fi	les Properties				
	_P Edit this menu.				
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	ilesj				
	Files)				
ic3 (20	Files				
io (8 Files	:				
1 . pec (12 F	Files)				
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C1. VE166 v8.7/3/bm/guo	pep				
guo (1 Project)	_				
Source Filet					
10 101					
探Drogonor					

#### 选择Processor

## XE164FM

E166 Project Options [ADC.PJT]			? ×
Application     Processor     Memory Model     Startup     C Compiler     Assembler     Macro Preprocessor     Linker/Locator     Output Format     IEEE-695 Output Format     IEEE-695 Output Format     Intel Hex Output Format     Hitex Output Format     Hitex Output Format     Hitex Output Format     Hitex Output Format     Gasses     Interrupt Vector Table	Processor Selection Manufacturer: Processor Processor derivative Use on-chip Rash Use on-chip RAM <u>CPU Problem Bypassy</u>	Jinfineon XE164F XE164F-96F	
Stack and Heap Locate Absolute Locate Order Section Size Adjust	<u>ок</u> 1	Cancel	Default

## XE164FM



## 选择Output Format

E166 Project Options [ADC.PTT]		<u>? ×</u>
E156 Project Options [ADC.PTT]  Application  Processor Memory Model  Startup C Compiler Assembler Macro Preprocessor Linker/Locator IEEE-695 Output Format Utal Hex Output Format	Output Format IEEE-695 I TASKING internal C166 formal Library Linker object Intel HEX records Motorola S records Hitex emulator Kontron emulator	<u><!--?</u--></u>
<ul> <li>Intel Hex Output Format (</li> <li>S-Record Output Format</li> <li>Hitex Output Format Optio</li> <li>Kontron Output Format O</li> <li>Map File</li> <li>Memory</li> <li>Classes</li> </ul>	IEEE-695 Output Format Options Intel Hex Output Format Options S-Record Output Format Options Hitex Output Format Options Kontron Output Format Options	
<ul> <li>Interrupt Vector Table</li> <li>Stack and Heap</li> <li>Locate Absolute</li> <li>Locate Order</li> <li>Section Size ∆rdiust</li> </ul>	Options string:  -WoPRINT("\$(OUTDIR)\adc.map") -Ms -x2 EXTEND2 -I  -cf "h:\my databases\xe164f\adc\_adc.ilo"	3hoeufmknladij 🔄
	OK Cancel	Default

#### 选择Intel Hex Output Format



```
6.2 添加用户代码(XE164F和XE164FM添加代码基本相同)
在main 函数中添加下列代码(在main 函数的末尾处)
/void main(void)
```

```
{
 // USER CODE BEGIN (Main,2)
  uword data1,data2,data3;
 // USER CODE END
 MAIN_vInit();
 while(1)
  {
  // USER CODE BEGIN (Main,4)
    data1=U0C0_ASC_uwGetData();
    U0C1_SSC_vSendData(data1);
    data2=U1C0_SSC_uwGetData();
    U1C1_IIC_vWriteData(U1C0TDF_MStart, 0x02);
    while(!(U2C0_PSR & 0x0001)); // PSR_SLSEL ó wait for slave select
    U1C0_IIC_vWriteData(U1C0TDF_MTxData,data2);
    data3=U2C0_IIC_uwReadData();
    U1C1_IIC_vWriteData(U1C0TDF_MStop, uwFFFFU1C0);
    U0C0_ASC_vSendData(data3);
  // USER CODE END
```

```
}
```

} // End of function main

7.编译

点击图标 进行编译连接。如有错误进行更改,直到出现-total errors: 0ø。

8.下载

利用memtool 软件将上面生成的hex 文件下载到单片机。

打开memtool 软件,点击菜单Targe-Change,选择Easy Kit with XE164-96F AB-Step(DAS)/ Kit with XE164FM-72F (DAS)界面如下

XE164F

Files in folder :	
nies in folder .	🔽 Show descriptions
Easy Kit with XE164-96F AB-Step (BSL/ASC) Easy Kit with XE164-96F AB-Step (BSL/ASC) Easy Kit with XE164-96F AB-Step (DAS) Easy Kit with XE164FM-72F (BSL/ASC) Easy Kit with XE164FM-72F (BSL)	

## XE164FM

C:\Program Files\	nfineon\Memtool4\Targets\	
iles in folder :		□ □ □ I Show description
Easy Kit with XC1 Easy Kit with XE1 Easy Kit with XE1 Easy Kit with XE1 Easy Kit with XE1 Easy Kit with XE1 MCB with XC866- MCB with XC886/ MCB with XC886/	64CS-32F (BSL/ASC) 64-96F AB-Step (BSL/ASC) 64-96F AB-Step (DAS) 64FM-72F (BSL/ASC) 54FM-72F (DAS) 54FM-72F (DAS) 4F (BB-Step and newer) 13F 888-6F 888-8F	

#### 点击OK 出现如下对话框。

the Brack of OP404PL date at the brack	201 KB to us this Design D ACII (astrongly)		TT Further
Viny Dakabases Vie 164F Vace Vour Vace nex	(re4 Keyre on chip Plogram FLASH (nor ready)	1	IA EUNDIG
Open File	1 0x00C00000 · 0x00C00FFF (4K) • #1 0x00C01000 · 0x00C01FFF (4K) •	RenoveAl	Epape
UnmeetAi	1 #2 0x00C02000 - 0x00C02FFF (4K) #3 0x00C03000 - 0x00C03FFF (4K)	Remove Set	Program
odd Sel	1 #5 0x000000 0x0000FFFF (15K)		Ven's
Sove Ar.	1 #7: 0x00C10000 - 0x00C1FFFF (64K) #8: 0x00C20000 - 0x00C2FFFF (64K) #9: 0x00C20000 - 0x00C2FFFF (64K)		Protect
Head	1 #10: 0x00C40000 · 0x00C40FFF (4K) #11: 0x00C41000 · 0x00C41FFF (4K)		State
Edi	I #12: 0x00042000 - 0x00042FFF 14K1 * Sector is protected	http://	Setup
E0/	I #12: 0x00C42000 - 0x00C42FFF 14K1	hRa	Setup

点击-connectø进行通讯连接。通讯成功之后,按照顺序open fileí -select all-add sel.>>将需 要下载的hex 文件添加到右边框中,然后选择øEraseí ø和øProgramø进行擦除、编程。如有必 要可点击øVerifyø进行校验。

9. 运行。

配置EASYKIT,连接如下管脚: P2.8接P10.11, P2.9接P10.12, P2.10接P10.13, P0.5接 P1.7加上拉, P0.6接P1.6加上拉

配置超级终端的 COM 口为 COM5 波特率为 9600,1 位结束位,无校验位。 在键盘上按下按键,在超级终端上就会有相应的显示