(12.1)

$\boxed{12.1}$ Ideally, $1\,LSB = 3.2/2^3 = 0.4$ V. The offset error is $v_O(000) = 0.2$ V $= +1/2$ LSB. To eliminate the offset error we decrease each output value by 0.2. This gives $v_O(111) = 2.9 - 0.2 = 2.7$ V. Ideally, we want $v_O(111) = V_{FSV} = 3.2 - 0.4 = 2.8$ V, indicating a gain error of -0.1 V $= -1/4$ LSB. To eliminate the gain error, multiply all new values of v_O by 2.8/2.7. The result is $v_O(000) = (0.2-0.2)28/27 = 0$, $v_O(001) = (0.5-0.2)28/27 = 0.3\overline{1}$, $v_O(010) = (1.1-0.2)28/27 = 0.9\overline{3}$, $1.2\overline{4}$, $1.\overline{5}$, $1.8\overline{6}$, $2.4\overline{8}$, and 2.8, all in volts. The ideal values are 0, 0.4, 0.8, 1.2, 1.6, 2.0, 2.4, and 2.8, all in volts. We have:

$INL_k = 0, -0.0\overline{8}, 0.1\overline{3}, 0.0\overline{4}, -0.0\overline{4}, -0.1\overline{3}, 0.0\overline{8}, 0$, in V

$DNL_k = -0.0\overline{8}, 0.\overline{2}, -0.0\overline{8}, -0.0\overline{8}, -0.0\overline{8}, 0.\overline{2}, -0.0\overline{8}$, in V.

Thus, $INL = 0.1\overline{3}$ V $= 1/3$ LSB; $DNL = 0.\overline{2}$ V $= 5/9$ LSB.

$\boxed{12.2}$ $SNR = 10 \log_{10}[(1\,W)/(0.6\,\mu W)] = 62.22$ dB. But, $SNR = 6.02n + 1.76 = 62.22$; so, $n = 10.04$ effective bits. Since $1/100 = -40$ dB, we have $SNR = 62.22 - 40 = 22.22$ dB.

(12.2)

12.3 1 LSB $= 1.600/2^6 = 25$ mV.

To find the offset error, set all bits to zero. Then, $v_O = V_{OS} = \pm 5$ mV $= \pm 1/5$ LSB.

To find the gain error, assume the offset error has been nulled, and set all bits to 1. Then,

$v_O = -(R_f/R_{eq})V_{ref}/(1+1/T)$, where

$R_{eq} = (2R)//(4R)//(8R)//\cdots//(64R) = (64/63)R$,

$\beta = R_{eq}/(R_{eq}+R_f) = (64/63)/[(64/63)+0.99] =$

0.506, $T = a\beta = 200 \times 0.506 = 101.3$. Substituting, $v_O = -\frac{0.99}{64/63} 1.6 \frac{1}{1+1/101.3} = -1.544$ V.

Ideally, $v_O = -1.600(1-2^{-6}) = -1.575$ V.

The gain error is thus $+30.3$ mV, or $+1.2$ LSB.

The worst-case value of v_O occurs when $V_{OS} = +5$ mV. Then,

$$v_O = \left[-\frac{R_f}{R_{eq}}V_{REF} + \frac{1}{\beta}V_{OS}\right]\frac{1}{1+1/T} = -1.535 \text{ V},$$

which differs from the ideal value of -1.575 V by $+40$ mV, or 1.6 LSB.

(12.3)

12.4 1 LSB = 3.200/2^4 = 0.2V. Ideally, we have $v_O(1111)$ = 3.2−0.2 = 3.00 V. In practice,

$$v_O(1111) = \left(\frac{9}{22} + \frac{9}{35} + \frac{9}{50} + \frac{9}{250}\right)V_{REF} = 2.823\ \text{V},$$

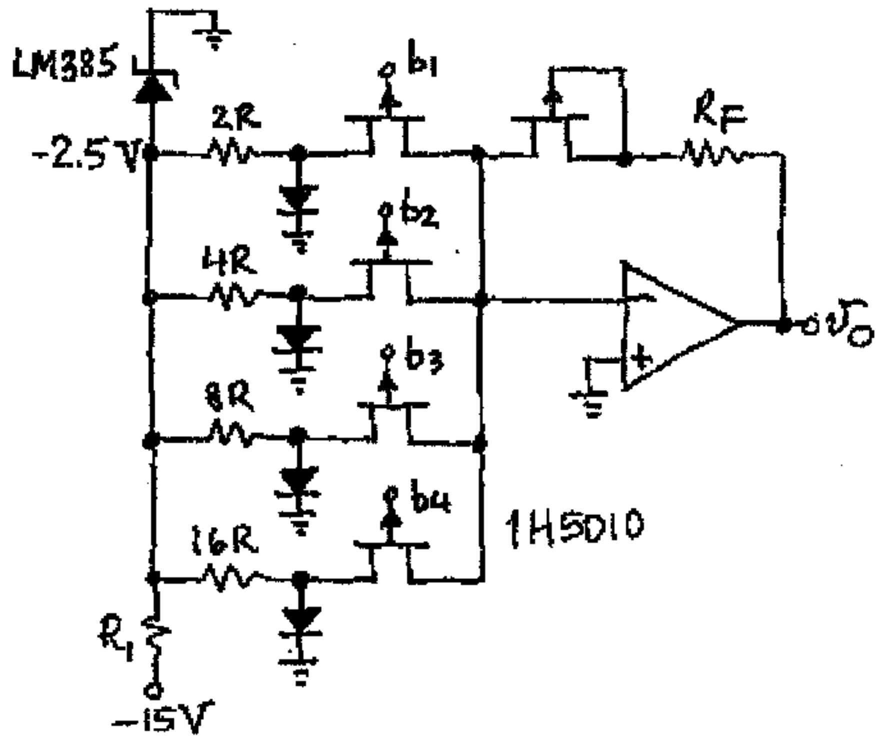
indicating a gain error of −0.88 LSB. To null this error, change R_f to 9×3/2.823 = 9.564 kΩ.

CODE	v_O(ideal)	v_O(actual)	INL_k	DNL_k
0000	0	0	0	0
0001	0.2	0.1224	−0.39	−0.39
0010	0.4	0.6121	1.06	1.45
0011	0.6	0.7345	0.67	−0.39
0100	0.8	0.8744	0.37	−0.30
0101	1.0	0.9968	−0.02	−0.39
0110	1.2	1.4865	1.43	1.45
0111	1.4	1.6089	1.04	−0.39
1000	1.6	1.3911	−1.04	−2.08
1001	1.8	1.5135	−1.43	0.39
1010	2.0	2.0032	0.02	1.45
1011	2.2	2.1256	−0.37	0.39
1100	2.4	2.2655	−0.67	−0.30
1101	2.6	2.3879	−1.06	−0.39
1110	2.8	2.8776	0.39	1.45
1111	3.0	3.0000	0	−0.39

INL = 1.43 LSB

DNL = −2.08 LSB ⇒ Nonmonotonic

12.5 (a) $V_{FSV} = V_{FSR}(1-2^{-4}) = 9.375$ V.



$v_O(1111) = (-R_F/R)(2^{-1}+2^{-2}+2^{-3}+2^{-4})(-2.5) = 9.375$ V. Let $2R = 10$ kΩ, $4R = 20$ kΩ, $8R = 40$ kΩ, $16R = 80$ kΩ. Then, $R_F = 20$ kΩ. The maximum current through the weighted-resistor network is $9.375/20 = 0.47$ mA. Imposing a minimum reference-diode current of 1 mA, we get $R_1 = (15-2.5)/(1+0.47) \cong 8.2$ kΩ.

(b) Taking $r_{ds(on)} \cong 0.1$ kΩ into consideration we have

$$v_O = 2.5 \times 20.1\left(\frac{b_1}{10.1} + \frac{b_2}{20.1} + \frac{b_3}{40.1} + \frac{b_4}{80.1}\right)$$

As $b_1b_2b_3b_4$ is varied from 0000 to 1111, v_O

(12.5) takes on the following values, in volts:
0, 0.627, 1.253, 1.880, 2.500, 3.127, 3.753, 4.380, 4.975, 5.603, 6.228, 6.856, 7.475, 8.103, 8.728, 9.356 V.

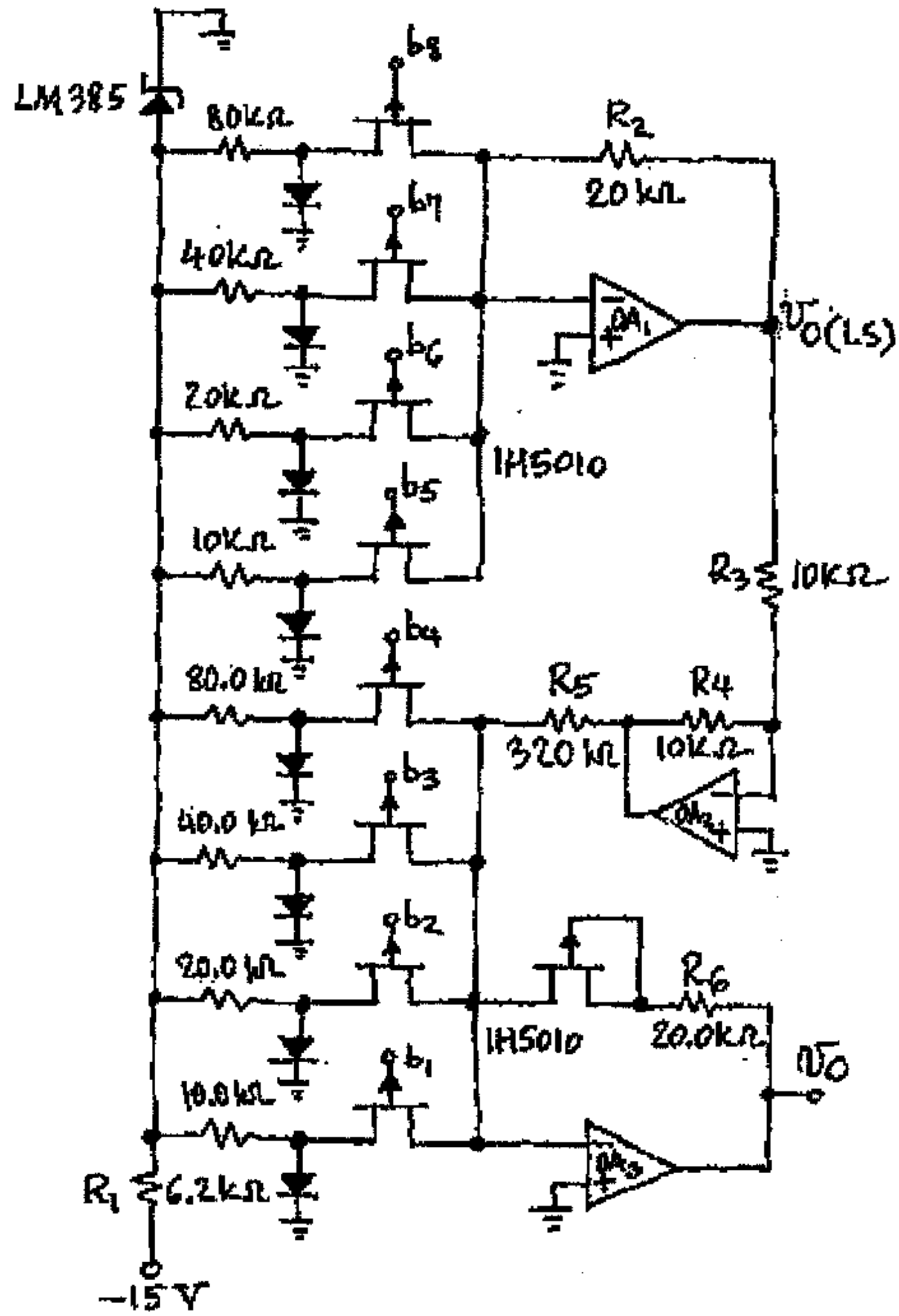
(c) We now have

$$v_O = 1\,\text{mV} + 2.501 \times 20.1\left(\frac{b_1}{10.1} + \frac{b_2}{20.1} + \frac{b_3}{40.1} + \frac{b_4}{80.1}\right).$$

v_O (Volts) = 0.001, 0.629, 1.254, 1.882, 2.502, … 8.733, 9.360. The offset error is 1 mV. After offset error nulling, $v_O(1111) = 9.359$ V, which differs from the ideal value of 9.375 V by −0.016 V. Thus, the gain error is −16 mV, or −1/40 LSB.

12.6 As shown in the accompanying figure, the 8-bit DAC consists of two 4-bit DACS with $V_{FSR} = 10.0$ V. The output of the LS 4-bit DAC is inverted and then scaled by R_5 to a current that is fed into OA_3's summing junction along with the four MS bits. R_1 is chosen on the basis of allowing a current of about 1 mA through the reference diode. Due to the presence of the dummy FET in the feedback path of OA_3, no dummy FET is used in the feedback

(12.6)



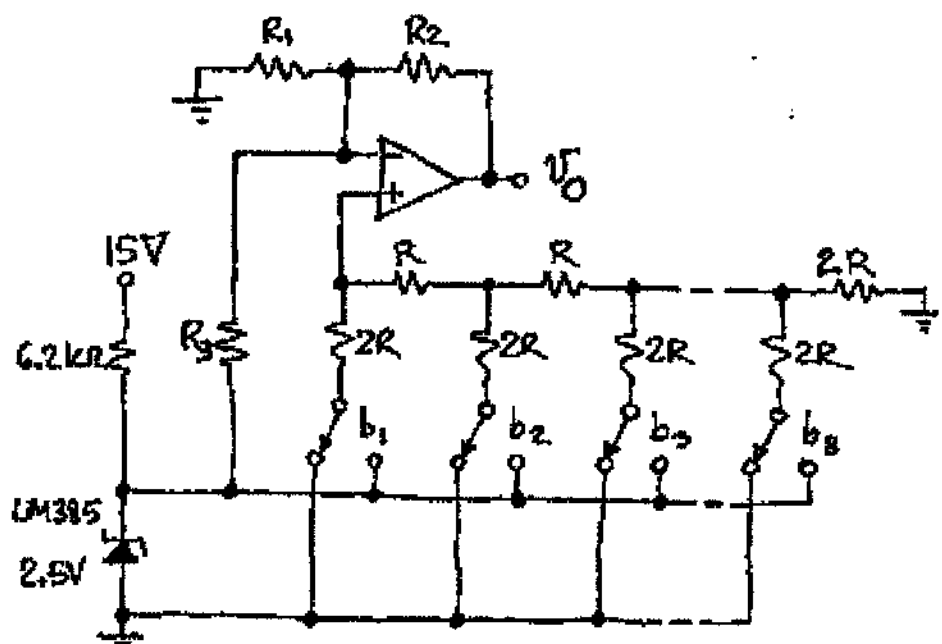
path of OA_1.

12.7 (a) With reference to the accompanying figure, we set the offsetting resistor R_3 to ∞ (R_3 is absent). Then, the condition

12.7

$10 = (1+R_2/R_1)2.5$ gives $R_2/R_1 = 3$. Use $R_1 = 10.0$ kΩ and $R_2 = 30.0$ kΩ. Clearly, $V_{FSV} = 10(1-2^{-8}) = 9.961$ V.

(b) With all switches flipped to the left we have $v_P = 0$ and we want $v_O = -5$ V. This requires $-5 = (-R_2/R_3)2.5$, or $R_2/R_3 = 2$. With all switches flipped to the right we have $v_P = 2.5(1-2^{-8})$, and we want $v_O = -5 + 10(1-2^{-8}) = 5(1-2^{-7})$. Using the superposition principle, we find that this requires $5(1-2^{-7}) = (-R_2/R_3)2.5 + [1 + R_2/(R_1 \| R_3)]2.5(1-2^{-8})$, or $5(1-2^{-7}) = -5 + [1 + R_2/R_1 + 2]2.5(1-2^{-8})$, or $R_2/R_1 = 1$. Use $R_3 = 10.0$ kΩ, $R_1 = R_2 = 20.0$ kΩ.



(12.8)

$\boxed{12.8}$ (a) All BJTs conduct the same current $I = V_{REF}/R_r$. By R-2R ladder properties, $R_o = R$. With SW_1 flipped to the left, $v_O = RI$; With SW_2 flipped to the left, $v_O = (RI)/2$; generalizing and using the superposition principle, we can write

$$i_o = \frac{v_O}{R} = b_1 I + b_2 \frac{I}{2} + b_3 \frac{I}{4} + b_4 \frac{I}{8}$$

$$= 2\frac{V_{REF}}{R_r}\left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + b_4 2^{-4}\right).$$

(b) $V_{FSR} = R_f I_{FSR} = (1\ \text{k}\Omega)(2\ \text{mA}) = 2\ \text{V}$;
$1/2\ \text{LSB} = V_{FSR}/2^{n+1} = 2/2^5 = 2^{-4}\ \text{V} = 62.5\ \text{mV}$.

$$v_O = \tfrac{1}{2}\text{LSB} + (V_{FSR} \times D_I)\,\frac{D_{I(max)} - \frac{1}{2}\text{LSB}}{D_{I(max)}}$$

$$= 62.5\ \text{mV} + 2D_I\left[(1-2^{-4}-2^{-5})/(1-2^{-4})\right]\text{V}$$

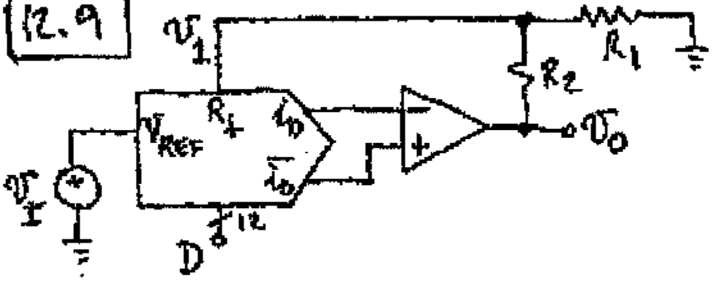
$$= [0.0625 + (29/15)D_I]\ \text{V}.$$

The requested actual (ideal) values of v_O are: $v_O(0000) = 0.0625\ \text{V}\ (0\ \text{V})$; $v_O(0100) = 0.5458\ \text{V}\ (0.5\ \text{V})$; $v_O(1000) = 1.0292\ \text{V}\ (1\ \text{V})$; $v_O(1100) = 1.5125\ \text{V}\ (1.5\ \text{V})$; $v_O(1111) = 1.8750\ \text{V}\ (1.875\ \text{V})$.

(c) $\beta = R_o/(R_o + R_f) = 1/2$; $f_{-3dB} = 25\ \text{MHz}$.

(12.9)

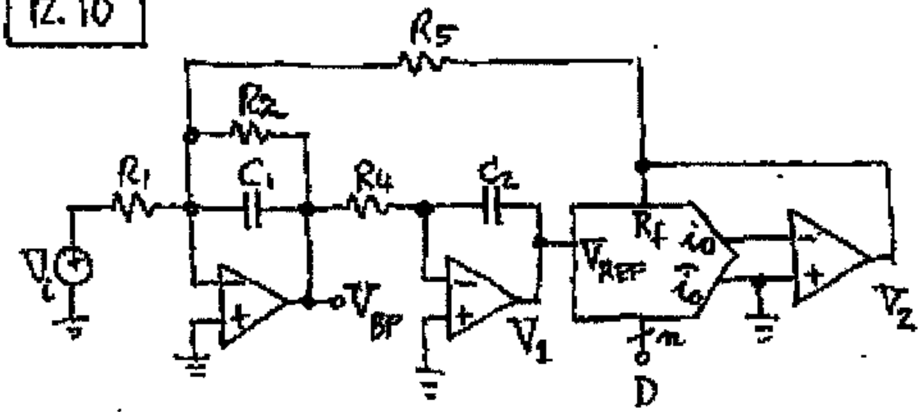
12.9



$v_1 = -Dv_I$; $\frac{0-v_1}{R_f} + \frac{0-v_1}{R_1} = \frac{v_1-v_0}{R_2}$

$v_0 = -(1+R_2/R_1+R_2/R_f)Dv_I$. To desensitize the circuit to process variations in the value of R_f, impose $R_1 \ll R_f$, e.g. let $R_1 = R_f/100 = 100\ \Omega$. Then, imposing $(1+R_2/0.1+R_2/10)(1-2^{-12})=64$ gives $R_2 = 6.24\ k\Omega$ (Use $6.19\ k\Omega$, 1%).

12.10



$V_2 = -DV_1 = -\frac{-D}{sR_4C_2}V_{BP} = \frac{1}{s(R_4/D)C_2} \Rightarrow R_4 \to \frac{R_4}{D}$;

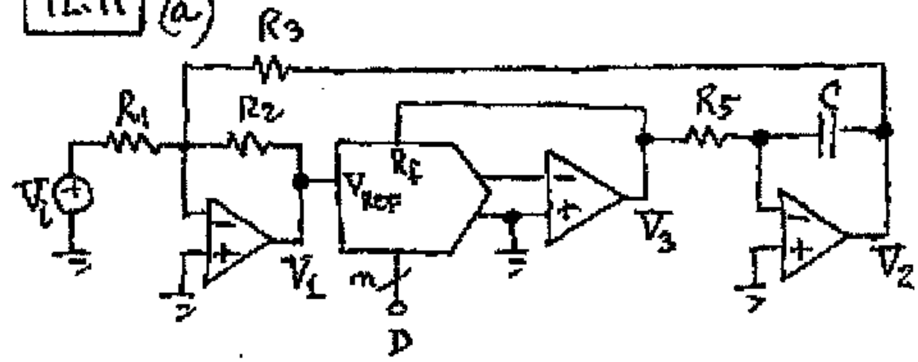
$H_{0BP} = -\frac{R_2}{R_1}$; $f_0 = \frac{1}{2\pi[(R_4/D)R_5C_1C_2]^{1/2}} = \frac{\sqrt{D}}{2\pi\sqrt{R_4R_5C_1C_2}}$;

$Q = [R_2^2C_1/(R_4/D)R_5C_2]^{1/2} = \sqrt{D}\sqrt{\frac{R_2^2C_1}{R_4R_5C_2}}$. Thus,

$f_0 \propto \sqrt{D}$, $Q \propto \sqrt{D}$, and $BW = f_0/Q = 1/2\pi R_2C_1$.

(12.10)

12.11 (a)



$V_1 = -\frac{R_2}{R_1}V_i - \frac{R_2}{R_3}V_2$; $V_2 = -\frac{1}{sR_5C}V_3 = \frac{D}{sR_5C}V_1$

$V_1\left(1+\frac{DR_2/R_3}{sR_5C}\right) = -\frac{R_2}{R_1}V_i$. Manipulating,

$\frac{V_1}{V_i} = -\frac{R_2}{R_1}\frac{j\omega/\omega_0}{1+j\omega/\omega_0}$, $\frac{V_2}{V_i} = -\frac{R_3}{R_1}\frac{1}{1+j\omega/\omega_0}$,

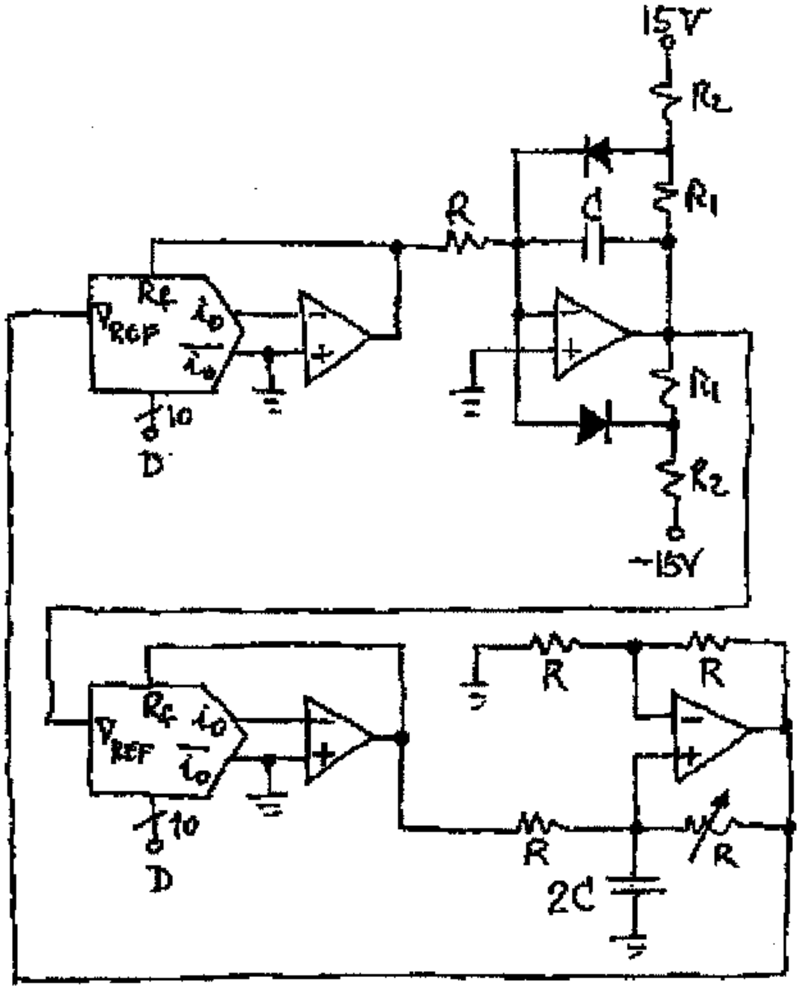
$\omega_0 = D\frac{R_2/R_3}{R_5C}$.

(b) $R_1 = 10.0\ k\Omega$, $R_2 = 10.0\ k\Omega$, $R_3 = 100\ k\Omega$

The full-scale frequency is $2\pi\times(2^{10}-1)5 = 2\pi\times$ 5,115 rad/s. Imposing $2\pi 5{,}115 = (1-2^{-10})\times (10/100)/R_5C$ gives $R_5C = 3.1085\ \mu s$. Use $C =$ 1 nF. Then, $R_5 = 3.11\ k\Omega$ (use $3.09\ k\Omega$, 1%).

12.12 $f_{0(max)} = 10(2^{10}-1) = 10.230$ kHz $= D_{max}/(2\pi RC) = (1-2^{-10})/RC \Rightarrow RC = 1/10240$ s. Let $C = 10$ nF, $2C = 20$ nF, $R = 9.76\ k\Omega$; variable R: 8.66 kΩ in series with a 2-kΩ potentiometer connected as a variable resistance. Imposing $5 = 0.7 + (R_1/R_2)(15+0.7)$ gives $R_2 = 3.65 R_1$; use $R_1 = 10\,k\Omega$, $R_2 = 36\ k\Omega$.

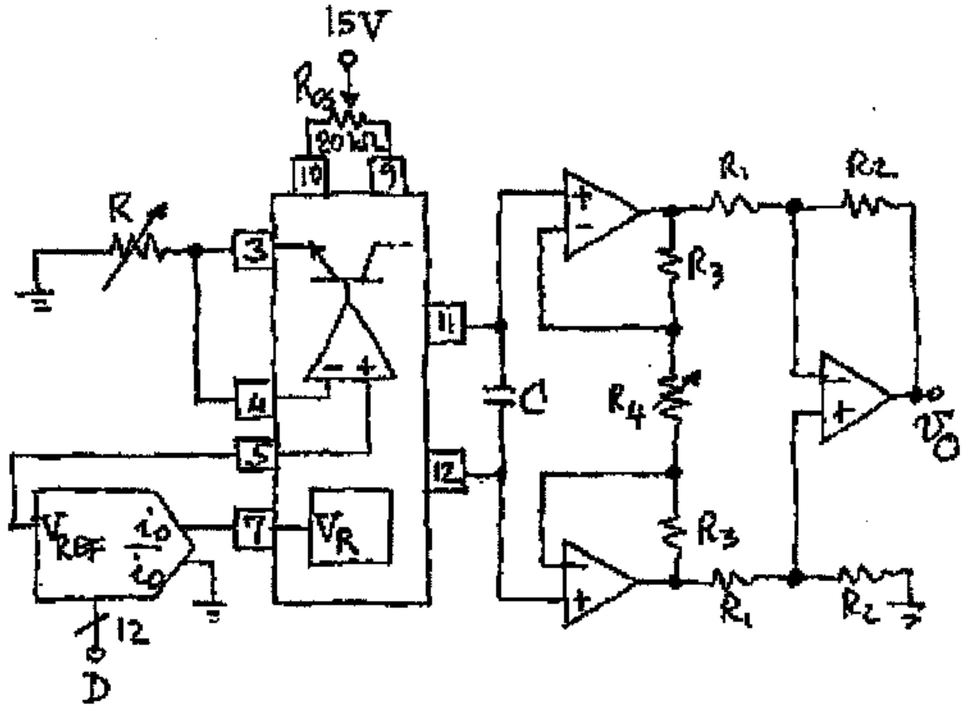
12.11



Use of amps with adequately fast dynamic characteristics.

$\boxed{12.13}$ As shown in the accompanying figure, the DAC is operated in the voltage mode to interpolate between 0 V and $V_R(1-2^{-12})$. By Eq. (10.28), $f_0 = DV_R/10RC$; $f_{0(max)} = (2^{12}-1)10 = 40{,}950\ \text{Hz} = (1-2^{-12})\times 1/RC \Rightarrow RC = 24.414$ μs. Use $C = 20$ nF, and $R = 1.00$ kΩ in series with a 500-Ω potentiometer connected as a variable resistance. Buffer and am-

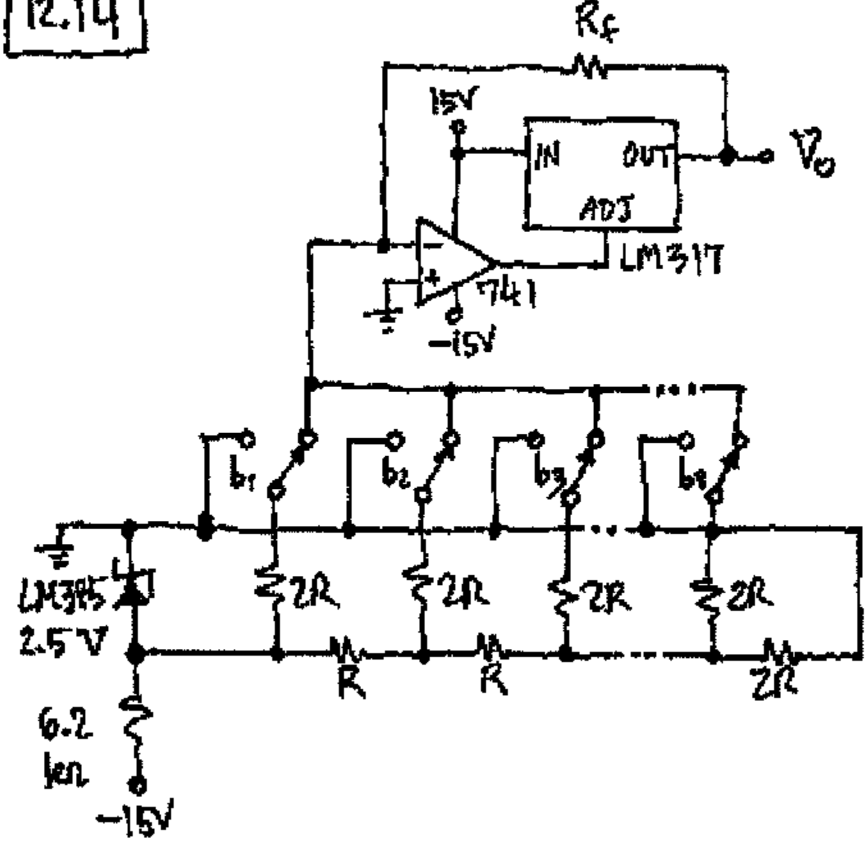
12.12



plify the triangular wave across C with an IA having gain $A = 10/(5/3) = 6$ V/V. Use $R_1 = 10.0$ kΩ, $R_2 = 20.0$ kΩ, $R_3 = 20.0$ kΩ, $R_4 = 15.0$ kΩ in series with a 10-kΩ pot connected as a variable resistance. To calibrate, set $D = 0\ldots0$ and adjust R_{os} so that the circuit is barely oscillating. Set $D = 1\ldots1$ and adjust R for $f_0 = 40{,}950$ Hz. With $D = 10\ldots0$, adjust R_4 for a peak-to-peak amplitude of 10 V at the output. Implement the IA with JFET-input op amps.

(12.13)

12.14



Use the LM 317 to boost the output current capability of the op amp. Assume $R = 10\,k\Omega$, and use a 6.2 kΩ resistor to bias the reference diode and ladder. To find R_f, impose

$$12 = -\frac{R_f}{R}\left(1-2^{-8}\right)\left(-2.5\right)$$

This gives $R_f = 48.19\ k\Omega$ (use $48.7\ k\Omega$).

12.15 (a) Let $v_I(t) = (V_{FSR}/2) \sin 2\pi f t$. Then, $|dv_I/dt|_{max} = 2\pi f V_{FSR}/2 = \pi f V_{FSR}$. Imposing $|dv_I/dt|_{max} \leq (1\ LSB)/t_{SAC}$ gives $\pi f V_{FSR} \leq V_{FSR}/2^n t_{SAC}$, or $f_{max} = 1/2^n \pi t_{SAC}$.

(b) $t_{SAC} = 1/10^6 = 1\ \mu s$; $f_{max} = 1/(2^8 \times \pi \times 10^{-6}) = 1.243$ kHz. With an ideal SHA preceding the ADC, we have, by the sampling theorem, $f_{max} = (1/2) 10^6 = 500$ kHz.

12.16 Require an accuracy of $\pm 1/2$ LSB, or $\pm V_{FSR}/2^{8+1} = \pm 10/2^9 = \pm 19.5$ mV. Thus, the reference must be 10.00 V $\pm$ 19.5 mV, and its temperature coefficient must be less than $(19.5\ mV)/(50°) = 390\ \mu V/°C = 39$ ppm/°C.

The comparator's hysteresis must be less than 19.5 mV, and its gain must be greater than $(V_{OH} - V_{OL})/(1/2\ LSB) = 5/(19.5 \times 10^{-3}) = 256$ V/V.

Allowing 1 clock cycle/bit plus an additional clock cycle for overhead operations (initialization and I/O commands), we have $T_{cycle} = (1\ \mu s)/9 \simeq 111$ ns. The combined settling time of the DAC and comparator, plus the delays of the digital control circuitry must thus be less than 111 ns.

$\boxed{12.17}$ $C_t = C + C/2 + C/4 + C/8 + C/8 = 2C = 16$ pF; $C_p = 4$ pF.

(1) Sample cycle: $v_P = 0$; C_p is discharged, while all remaining capacitances are pre-charged to $v_I = 1.00$ V.

(2) Hold cycle: SW_1 through SW_4 are connected to ground; C_t and C_p form a voltage divider to give

$$v_P = \frac{C_t}{C_t + C_p}(-v_I) = -\frac{16}{16+4}1 = -0.800 \text{ V.}$$

(3) 1st bit cycle: SW_1 is connected to V_{REF} to give

$$v_P = -0.800 + \frac{8}{20}3 = +0.4 \text{ V}$$

Since $v_P > 0$, SW_1 is flipped back to ground, returning v_P back to -0.800; $b_1 = 0$.

(4) 2d bit cycle: SW_2 is connected to V_{REF},

$$v_P = -0.800 + \frac{4}{20}3 = -0.200 \text{ V}$$

Since $v_P < 0$, leave SW_1 as is; $b_2 = 1$.

(5) 3d bit cycle: SW_3 is connected to V_{REF}

$$v_P = -0.200 + \frac{2}{20}3 = +0.1$$

Flip SW_3 back to ground: $b_3 = 0$.

(6) 4th bit cycle: SW_4 is connected to V_{REF},

(12.16)

$$v_p = -0.200 + \frac{1}{20}3 = -0.05\text{ V} \Rightarrow b_4 = 1.$$

Final result is $b_1b_2b_3b_4 = 0101$, which ideally corresponds to $DV_{FSR} = (0/2 + 1/4 + 0/8 + 1/16)3 = 0.9375$ V; the quantization error is $0.9375 - 1.00 = -0.0625$. Since $1\text{ LSB} = 3/2^4 = 0.1875$ V, this represents an error of $-1/3$ LSB, i.e. within $\pm 1/2$ LSB, as expected.

12.18 (a) We have $1\text{ LSB} = 2.560/2^8 = 10$ mV. The coarse flash ADC consists of 16 equal-valued resistors to establish 15 reference levels for the corresponding 15 comparators at $kV_{FSR}/2^4 = k0.16$ V, $k = 1, 2, \ldots, 15$. These levels are thus 0.16 V, 0.32 V, 0.48 V, ... 2.24 V, 2.40 V. Each level must be accurate within $\pm 1/2$ LSB $= \pm 5$ mV.

The fine flash ADC consists of 15 comparators with levels at 0.08 V, 0.24 V, 0.40 V, 0.56 V, ... 2.00 V, 2.16 V, and 2.32 V; each level must be accurate within $\pm 1/2(2.56/2^4) = \pm 80$ mV. Total # of comparators: 30.

(b) $v_I = 0.5$ V falls within the 3d and 4th level (0.48 V and 0.64 V) of the coarse DAC, so $b_1b_2b_3b_4 = 0011$; $v_{RES} = 0.5 - 0.48 = 0.02$ V; $2^4 v_{RES} = 0.32$ V, which

12.17

falls between the 2^d and 3^d level of the fine DAC; so, $b_5b_6b_7b_8 = 0010$. The code 00110010 corresponds, ideally, to $DV_{FSR} = (1/8+1/16+1/128)\times 2.560 = 0.500$ V, indicating zero quantization error.

$v_I = 1.054$ V falls between the 6th and 7th of the coarse DAC. So, $b_1b_2b_3b_4 = 0110$; $v_{RES} = 1.054 - 6\times 0.16 = 0.094$ V; $2^4 v_{RES} = 1.504$, which falls between the 9th and 10th level of the fine DAC. So, $b_5b_6b_7b_8 = 1001$. $D\times V_{FSR} = (1/4+1/8+1/32+1/256)\times 2.560 = 1.050$ V; the quantization error is -4 mV, or -0.4 LSB.

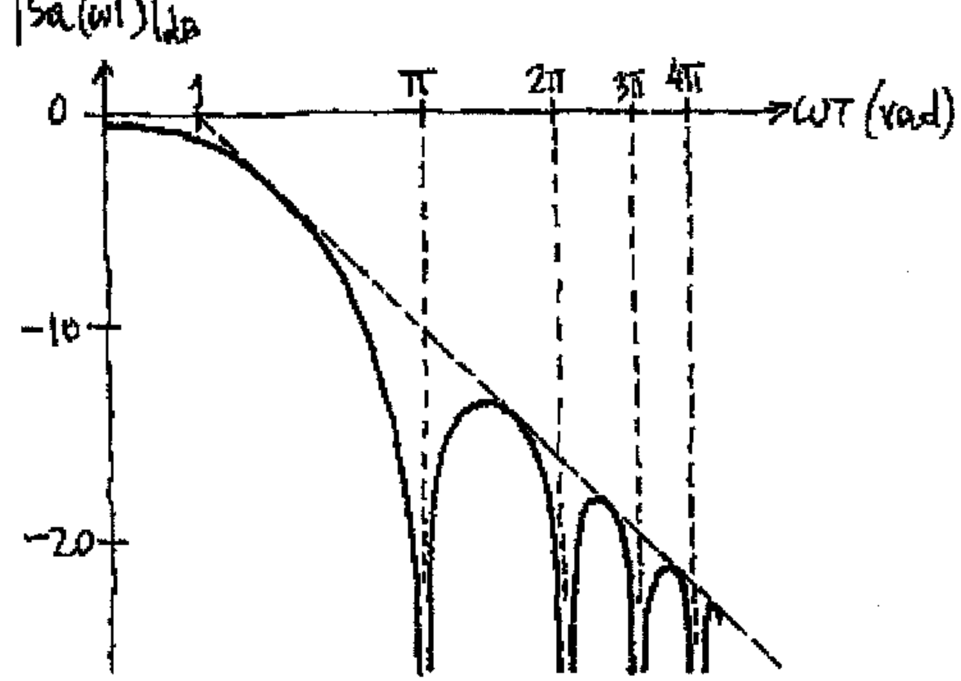
$v_I = 2.543\text{ V} \Rightarrow b_1b_2b_3b_4 = 1111$, $v_{RES} = 0.143$ V, $2^4 v_{RES} = 2.288\text{ V} \Rightarrow b_5b_6b_7b_8 = 1110$; quantization error $= 3$ mV, or $\frac{1}{3}$ LSB

12.19 Let $v_i = V_m\cos(\omega t+\theta)$ and $T = 2^n T_{CK}$. Define $V_i(\omega) \triangleq \frac{1}{RC}\int_0^T v_i(t)\,dt$. Then

$V_i(\omega) = \frac{1}{RC}\int_0^T V_m\cos(\omega t+\theta)\,dt = \frac{V_m}{\omega RC}\left[\sin(\omega T+\theta) - \sin\theta\right]$. For $\theta = 0$, this reduces to $V_i(\omega) =$

(12.18)

$\frac{V_m T}{RC} \frac{\sin \omega T}{\omega T} = \frac{V_m T}{RC} Sa(\omega T)$. The plot of $|Sa(\omega T)|_{dB}$ versus ωT rolls off at a rate of -20 dB/dec and has zeros at $\pi, 2\pi, 3\pi, 4\pi \ldots$



On the other hand, if we let $\theta = -90°$, so that $v_i(t) = V_m \sin \omega t$, then we obtain $V_i(\omega) = \frac{V_m T}{RC} \frac{1 - \cos \omega T}{\omega T}$, which again rolls off at a rate of -20 dB/dec, but with zeros at $0, 2\pi, 4\pi, 6\pi \ldots$ The zeros of $Sa(\omega T)$ at the odd multiples of π are due to the even-symmetry of the cos function. In the most general case of arbitrary symmetry of v_i, we consider only the zeros at even multiples of π, or $\omega T = 2\pi, 4\pi, 6\pi \ldots$, i.e. $f = 1/T, 2/T, 3/T \ldots$

(12.19)

$\boxed{12.20}$ (a) $v_O(0)=0$; $v_O(\infty)=-av_I=-10^3$ V;
$\tau = R_{eq}C = (1+a)RC \cong 10^3 RC$;
$v_O(t) = v_O(\infty) + [v_O(0) - v_O(\infty)]\, e^{-t/\tau}$, or
$v_O(t) \cong 10^3 \left[e^{-t/(10^3RC)} - 1\right]$ V.

(b) Ideally, $v_O(t) = v_O(0) - \frac{1}{RC}\int_0^t v_I\, dt$,
or $v_{O(ideal)}(t) = -\frac{1\text{V}}{RC}t$. Impose
$v_O(100\text{ ms}) - v_{O(ideal)}(100\text{ ms}) \le 1$ mV, or
$10^3\left[e^{-0.1/(10^3RC)} - 1\right] + \frac{0.1}{RC} \le 10^{-3}$. Expanding,
$10^3\left[1 - \frac{1}{10^4RC} + \frac{1}{2}\left(\frac{1}{10^4RC}\right)^2 + \cdots - 1\right] + \frac{1}{10RC} \le 10^{-3}$,
or $\frac{10^3}{2}\left(\frac{1}{10^4RC}\right)^2 \le 10^{-3}$, or $RC \ge \frac{1}{14.14\text{ s}}$.
We also have $v_{O(ideal)}(100\text{ ms}) = \frac{-1}{1/14.14} \times 0.1 =$
-1.141 V.

$\boxed{12.21}$ (a) $f_{ck} = 60 \times 2^{14} = 983.040$ kHz; $T =$
2×2^{14} cycles, or $T = 2^{15}/f_{ck} = 33.\bar{3}$ ms.

(b) $5/(2^{14}T_{ck}) = 2.5/RC \Rightarrow RC = 8.\bar{3}$ ms.

(c) $\tau_{new} = R(1+0.05)C(1-0.02) = 1.029RC$
$= 1.029\tau_{old}$. The new value of Δv_2 is thus
$\Delta v_2 = 5/1.029 = 4.859$ V, and accuracy is unaffected.

(12.20)

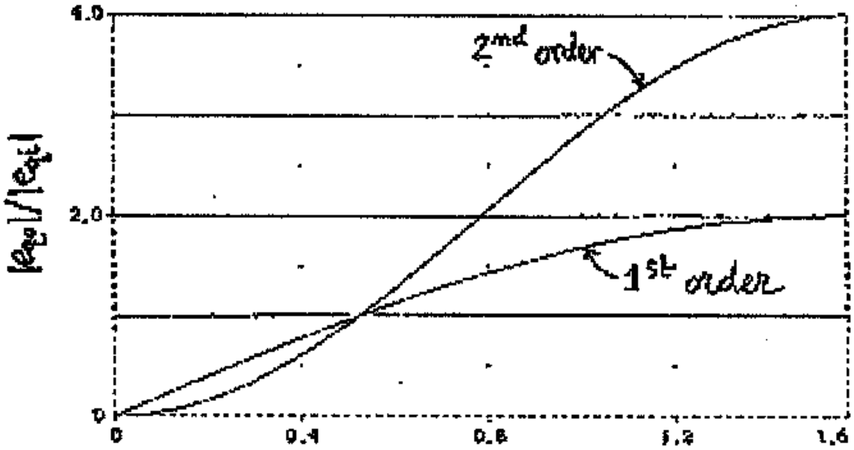
$\boxed{12.22}$ (a) 1st order Σ-Δ:

$$|e_{qo}| = 2\left(\sin\frac{\pi f}{kfs}\right)|e_{qi}| \cong 2\frac{\pi f}{kfs}\frac{q}{(kfs/2)^{1/2}} = \frac{2\sqrt{2}\pi q}{(kfs)^{3/2}}f$$

2nd order Σ-Δ:

$$|e_{qo}| = \left(2\sin\frac{\pi f}{kfs}\right)^2|e_{qi}| \cong 4\left(\frac{\pi f}{kfs}\right)^2\frac{q}{(kfs/2)^{1/2}} = \frac{4\sqrt{2}\pi^2 q}{(kfs)^{5/2}}f^2$$

These curves can be plotted using PSpice.



(b) 1st order Σ-Δ before filtering:

$$E_q^2 = \int_0^{kfs/2}|e_{qo}|^2 df = \int_0^{kfs/2} 2^2\sin^2\left(\frac{\pi f}{kfs}\right)\times\frac{q^2}{kfs/2}df$$

$$= \frac{(2q)^2}{kfs/2}\int_0^{kfs/2}\sin^2(af)\,df,\ a = \pi/kfs.$$ Using the integral tables,

$$E_q = \frac{2q}{(kfs/2)^{1/2}}\left[\frac{kfs/2}{2} - 0\right]^{1/2} = \sqrt{2}q,$$ indicating that noise shaping increases the total noise at the quantizer's output by $\sqrt{2}$, or 3dB.

(12.21)

2nd order Σ-Δ before filtering:

$$E_q^2 = \int_0^{kf_s/2} 4^2 \sin^4\left(\frac{\pi f}{kf_s}\right) \times \frac{q^2}{kf_s/2}\, df = 8q^2, \text{ or}$$

$E_q = \sqrt{8}\, q^2$, indicating that noise shaping now increases the total output noise by $\sqrt{8}$, or 9dB.

(c) 1st order Σ-Δ after filter/decimator:

$$E_t^2 \cong \frac{8\pi^2 q^2}{(kf_s)^3} \int_0^{f_s/2} f^2 df = \frac{8\pi^2 q^2}{(kf_s)^3} \frac{1}{3} \left(\frac{f_s}{2}\right)^3, \text{ or}$$

$E_t = (\pi q/\sqrt{3})/k^{3/2}$.

2nd order Σ-Δ after filter/decimator:

$$E_t^2 \cong \frac{32\pi^4 q^2}{(kf_s)^5} \int_0^{f_s/2} f^4 df, \text{ or } E_t = \frac{\pi^2 q}{\sqrt{5}} \frac{1}{k^{5/2}}.$$

(d) 1st order:

$$100 \frac{\sqrt{2}\, q - \pi q/(3k^3)^{1/2}}{\sqrt{2}\, q} = 100\left(1 - \frac{\pi}{(6k^3)^{1/2}}\right)$$

For k=16, this is 97.996%, indicating that only 2% of noise is left.

2nd order:

$$100 \frac{\sqrt{8}\, q - \pi^2 q/(5k^5)^{1/2}}{\sqrt{8}\, q} = 100\left(1 - \frac{\pi^2}{(40k^5)^{1/2}}\right)$$

For k=16 this is 99.8476%, indicating that only 0.152 of noise is left.

(12.22)

12.23 (a) By Eq. (12.21), the required SNR for a 16-bit ADC is SNR $= 6.02\times16+1.76 = 98.08$ dB. With a 1-bit quantizer ($n=1$), Eq. (12.25) indicates that we need $98.08 = 6.02(1+0.5m)+1.76$, or $m = 30$. Thus, $f_s = 2^{30}\times 44.1$ kHz $= 47{,}352$ GHz!

(b) By Eq. (12.31), $98.08 = 6.02\times(1+1.5m)-3.41$, or $m = 10.57$, so now $f_s = 2^{10.57}\times 44.1$ kHz $= 67.16$ MHz.

(c) Eq. (12.33) gives $m = 6.857$, so $f_s = 2^{6.857}\times 44.1$ kHz $= 5.113$ MHz.

12.24 (a) Since doubling the oversampling rate improves accuracy by 0.5 bits, for a 4-bit improvement we need $k = 2^{4/0.5} = 256$. So, $f_s = 2\times10^5\times256 = 51.2$ MHz.

(b) For a 4-bit improvement using a 1st order Σ-Δ we need, by Eq.s (12.21) and (12.31), $6.02\times12+1.76 = 6.02\times8+6.02\times1.5m-3.41$, or $m = 3.239$, or $k = 2^m = 9.44$. $f_s = 2\times10^5\times9.44 = 1.888$ MHz.

(c) By Eq. (12.33), $74 = 6.02\times8+6.02\times2.5m-11.4$, or $m = 2.547$, or $k = 2^m = 5.49$. $f_s = 2\times10^5\times5.49 = 1.09825$ MHz.

(12.23)

$\boxed{12.25}$ (a) Imposing

$$20\log_{10}\frac{1}{\sqrt{1+[20\times10^3\times2\pi RC]^2}} = -0.1\,dB$$

gives $RC = 1.21\times10^{-6}$. To allow for component tolerances, impose $RC = 1\,\mu s$; use $R = 1\,k\Omega$, $C = 1\,nF$.

(b) $1/2\ LSB = (2\,V)/2^{17} = 15.26\,\mu V$.

The first image band is $kf_S \pm 20\,kHz$, or $3.052\,MHz \le f \le 3.092\,MHz$. The attenuation of the RC filter over this band is approximately $1/\sqrt{1+(3.072\times10^6\times2\pi10^{-6})^2} = 0.0517$, or 25.7 dB. The rms noise of the first band is $E_1 = e_{nW}\sqrt{(3.092-3.052)\times10^6} = 200\,e_{nW}$. Imposing $0.0517\times200\,e_{nW} \le 15.26\,\mu V$ gives $e_{nW} \le 1.48\,\mu V/\sqrt{Hz}$.