Features

- Cost-effective single-chip solution for stereo headset and wireless speaker applications
- A2DP1.2 and AVRCP1.0 profiles enabled with SBC encoder for streaming audio over Bluetooth and for remote control functionality
- MP3 decoder for improved audio quality and reduced power consumption (MP3 decode functionality requires an appropriate licence from Thomson, see Section 17.1)
- Configurable A2DP 5-band EQ
- High-quality audio 95dB SNR on DAC playback
- 64MIPS Kalimba DSP coprocessor
- FastStream, CSR's low-latency codec for video and gaming applications
- HFP 1.5 (includes 3-way calling) and HSP 1.0 support
- cVc support for echo and noise reduction
- Low-power consumption: over 10 hours of audio playback from a 180mAh battery
- Fully qualified Bluetooth v2.1 + EDR specification system with support for secure simple pairing
- Best-in-class Bluetooth radio with 8dBm transmit power and -92dBm receive sensitivity
- 2 integrated linear regulators with 1.5V output from 1.7V to 1.95V input
- Integrated switch-mode regulator
- Integrated lithium battery charger
- 68-lead 8 x 8 x 0.9mm, 0.4mm pitch QFN package
- Green (RoHS compliant and no antimony or halogenated flame retardants)
- BlueTunes ROM stereo headset solution development kit available, includes example design. Order code BTN-003-1A

BlueTunes® ROM QFN

BlueTunes ROM Stereo Headset Solution

Single-chip Bluetooth® v2.1 + EDR System

Production Information

BC57F687A05

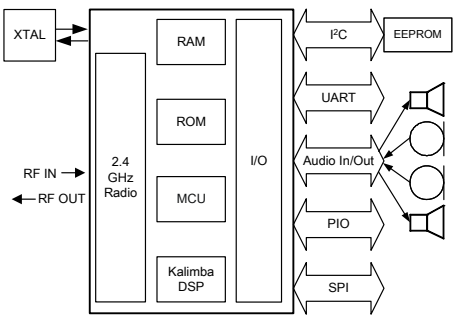
Issue 3

Prepared for Jerry Zeng, hotmail.com - Saturday, November 12, 2011

General Description

Based on **BlueCore®5-Multimedia ROM QFN**, the **BlueTunes ROM QFN** integrates a Bluetooth radio, baseband, DSP, high-quality audio codec, SMPS, LDO and a battery charger for minimal BOM, component count and PCB area.

BlueTunes ROM QFN uses advanced DSP features for the latest stereo enhancements and to improve audio quality, including SBC and MP3 decoder, support for FastStream (low-latency codec) and 5-band EQ.



Applications

- Stereo headset solution with support for echo and noise reduction
- Wireless stereo speakers

BlueTunes ROM QFN includes as standard cVc dual and single microphone algorithms for echo and noise suppression.

cVc dual-microphone algorithm can provide >30dB of noise suppression in both stationary and dynamic noise conditions such as; babble, road, music and competing voices. In addition an acoustic echo canceller is now integrated into the cVc dual-microphone solution, further enhancing the far-end user experience.

A cVc single-microphone provides full-duplex echo cancellation and a 10dB stationary noise suppressor.

BlueTunes ROM QFN includes secure simple pairing, which greatly simplifies the pairing process, making it even easier to use a Bluetooth headset.

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Document History

Revision	Date	Change Reason
1	23 OCT 08	Original publication of this document.
2	25 FEB 09	Production information.
3	22 MAR 10	Status Information, Ordering Information and ADC Digital Gain updates. Modification to Electrical Characteristics structure and various editorial changes. If you have any comments about this document, email comments@csr.com giving the number, title and section with your feedback.

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Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

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Production Information

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BlueTunes ROM QFN devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

BlueTunes ROM QFN devices are also free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products*.

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Prepared for Jun Zeng - hoperail.com - Saturday, November 12, 2011

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1 Device Details

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time
- Bluetooth v2.1 + EDR specification compliant

Transmitter

- 8dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch

Receiver

- Receiver sensitivity of -92dBm
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 16MHz to 26MHz or an external clock 12MHz to 52MHz

Physical Interfaces

- Synchronous serial interface for system debugging
- I²C compatible interface to external EEPROM containing device configuration data (PS Key)
- UART interface
- 2 LED drivers with faders

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shutdown and wake-up commands with an integrated low-power oscillator for ultra-low power Park/Sniff/Hold mode
- Clock request output to control external clock
- 2 integrated linear regulators: 1.5V output from 1.7V to 1.95V input
- Integrated high-efficiency switch-mode regulator: 1.8V output from 2.5V to 4.4V input
- Power-on-reset cell detects low-supply voltage
- 10-bit ADC available to applications
- Integrated charger for lithium ion/polymer batteries

Kalimba DSP

- Very low-power Kalimba DSP coprocessor, 64MIPS, 24-bit fixed point core
- Support for SBC and MP3 codec for improved audio quality (MP3 decode functionality requires an appropriate licence from Thomson, see Section 17.1)
- Single-cycle MAC; 24 x 24-bit multiply and 56-bit accumulator
- 32-bit instruction word, dual 24-bit data memory
- 6K x 32-bit program RAM, 8K x 24-bit + 8K x 24-bit data RAM
- 64 x 32-bit program memory cache when executing from ROM

Audio Codec

- 16-bit internal codec
- DAC for stereo audio
- ADC dual channel mono voice band audio
- Integrated amplifiers for driving 16Ω speakers; no need for external components
- Support for single-ended speaker termination and line output
- Integrated low-noise microphone bias

Baseband and Software

- Internal ROM
- 48KB of internal RAM, allows full-speed data transfer, mixed voice/data and full piconet support
- Logic for FEC, HEC, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air
- FastStream, CSR low latency codec significantly reduces the latency of the audio link, from source to sink, avoiding lip-sync issues when simultaneously listening to audio and watching video images
- Configurable stereo headset ROM software to set-up headset features and user interface
- HFP 1.5 (including 3-way calling) and HSP 1.0 support
- Bluetooth v2.1 + EDR specification Secure Simple Pairing support
- BlueTunes ROM QFN supports as standard a new high-performance DSP based dual-microphone noise reduction
- BlueTunes ROM QFN also supports a DSP based single-microphone cVc echo and noise reduction

Package Option

- QFN 68-lead, 8 x 8 x 0.9mm, 0.4mm pitch

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2 Functional Block Diagram

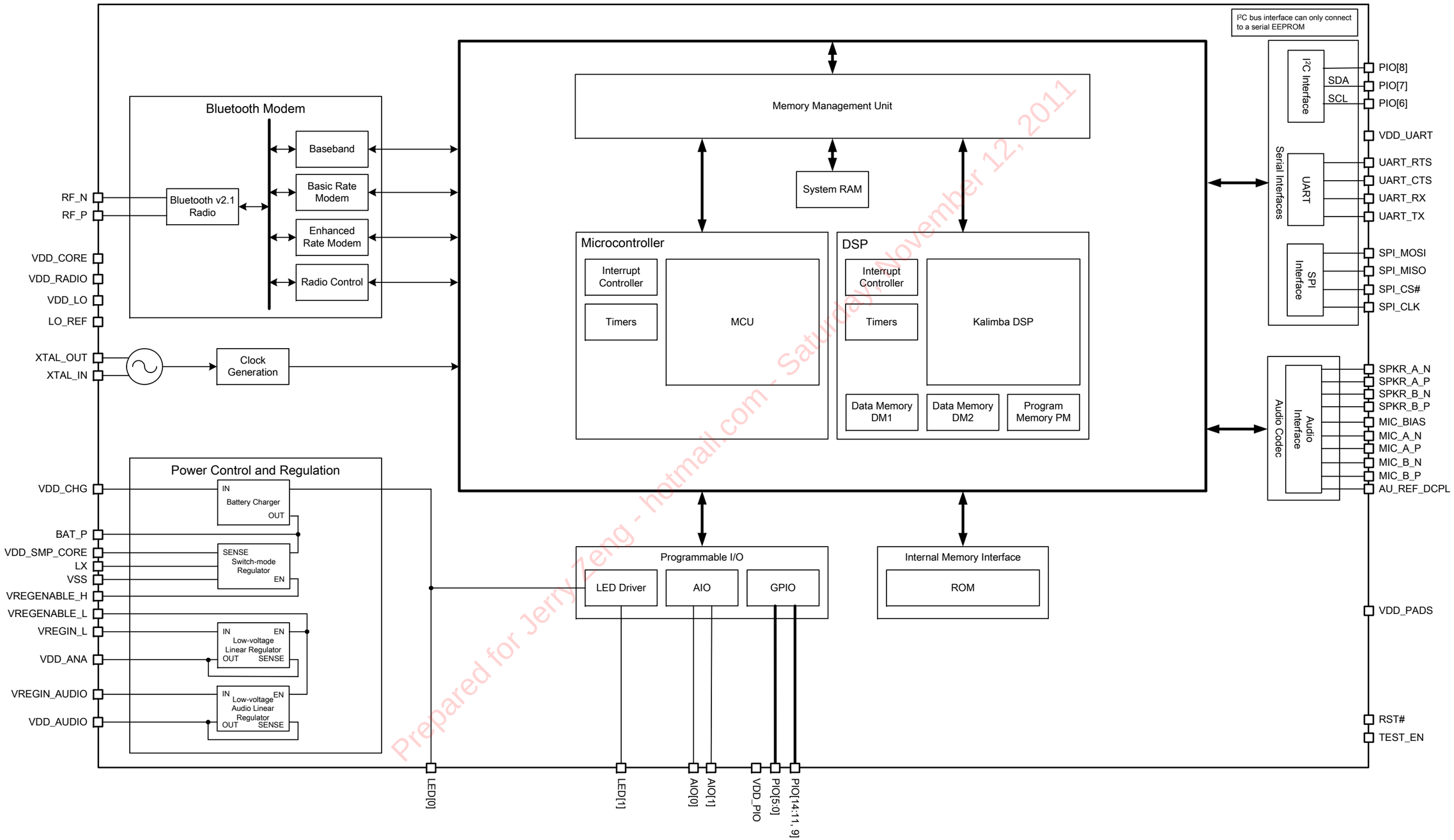

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Figure 2.1: BlueTunes ROM QFN Functional Block Diagram

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3 Package Information

3.1 Pinout Diagram

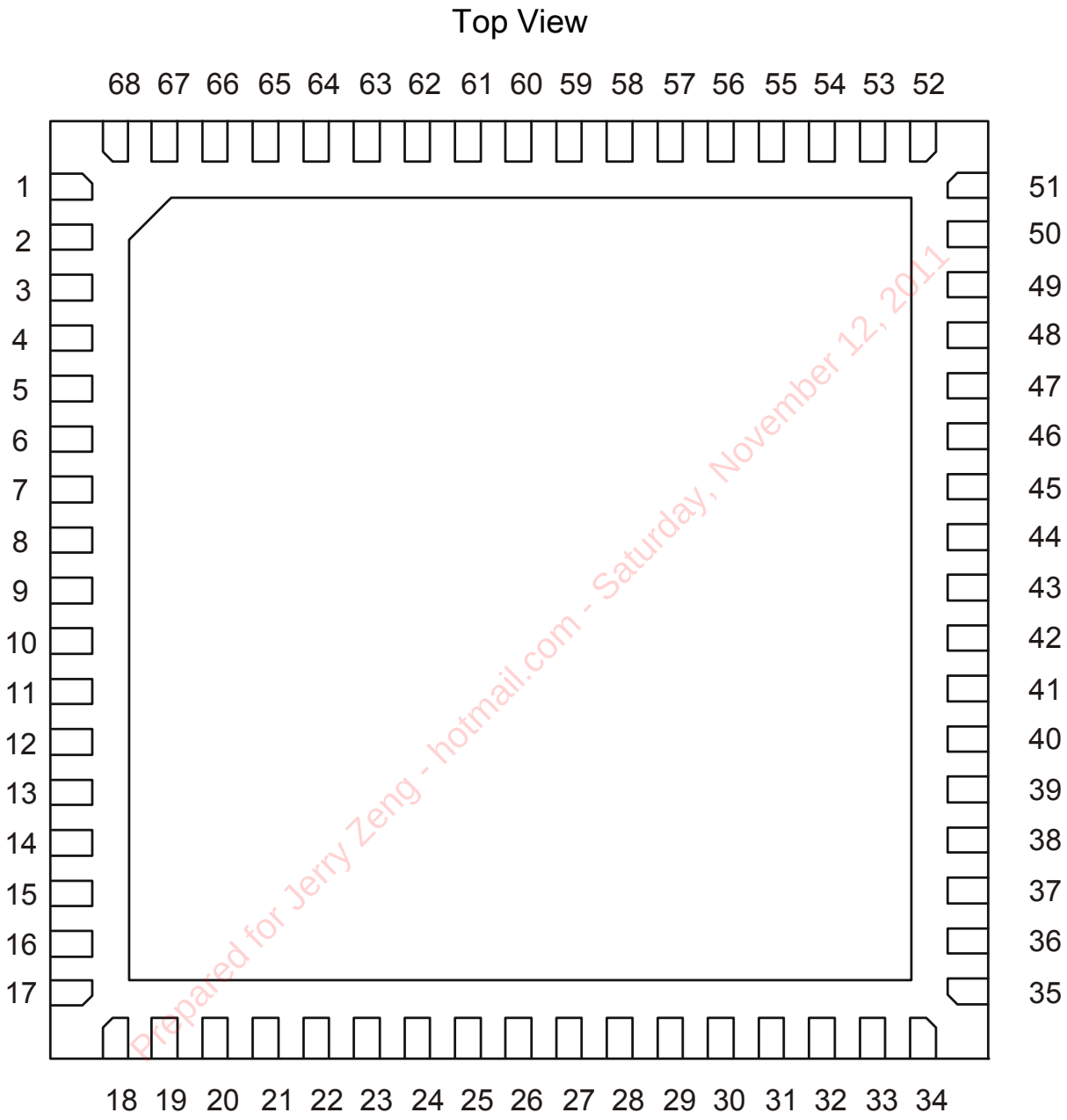

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Figure 3.1: BlueTunes ROM QFN Device Pinout

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3.2 Device Terminal Functions

Bluetooth Radio	Lead	Pad Type	Supply Domain	Description
RF_N	65	RF	VDD_RADIO	Transmitter output/switched receiver
RF_P	64	RF		Complement of RF_N

Synthesiser and Oscillator	Lead	Pad Type	Supply Domain	Description
XTAL_IN	3	Analogue	VDD_ANA	For crystal or external clock input
XTAL_OUT	4			Drive for crystal
LO_REF	5			Reference voltage to decouple the synthesiser

SPI Interface	Lead	Pad Type	Supply Domain	Description
SPI_MOSI	28	Input, with weak internal pull-down	VDD_PADS	SPI data input
SPI_CS#	30	Bidirectional with weak internal pull-down		Chip select for SPI, active low
SPI_CLK	29	Bidirectional with weak internal pull-down		SPI clock
SPI_MISO	31	Bidirectional with weak internal pull-down		SPI data output

UART Interface	Lead	Pad Type	Supply Domain	Description
UART_TX	9	Output, tristate, with weak internal pull-down	VDD_UART	UART data output, active high
UART_RX	10	Bidirectional with weak internal pull-down		UART data input, active high
UART_RTS	12	Bidirectional CMOS output, tristate, with weak internal pull-up		UART request to send active low
UART_CTS	11	CMOS input with weak internal pull-down		UART clear to send active low

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PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[14]	20	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
PIO[13]	19			
PIO[12]	18			
PIO[11]	15			
PIO[9]	14			
PIO[8]	21			
PIO[7]	22			
PIO[6]	23			
PIO[5]	24			
PIO[4]	25			
PIO[3]	58	Bidirectional with programmable strength internal pull-up/down	VDD_PIO	Programmable input/output line
PIO[2]	59			
PIO[1]	60			
PIO[0]	61			
AIO[1]	6	Bidirectional	VDD_ANA	Programmable input/output line
AIO[0]	7			

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Audio	Lead	Pad Type	Supply Domain	Description
SPKR_A_N	56	Analogue	VDD_AUDIO	Speaker output, negative, channel A
SPKR_A_P	57	Analogue	VDD_AUDIO	Speaker output, positive, channel A
SPKR_B_N	53	Analogue	VDD_AUDIO	Speaker output, negative, channel B
SPKR_B_P	54	Analogue	VDD_AUDIO	Speaker output, positive, channel B
MIC_A_N	52	Analogue	VDD_AUDIO	Microphone input, negative, channel A
MIC_A_P	51	Analogue	VDD_AUDIO	Microphone input, positive, channel A
MIC_B_N	50	Analogue	VDD_AUDIO	Microphone input, negative, channel B
MIC_B_P	48	Analogue	VDD_AUDIO	Microphone input, positive, channel B
MIC_BIAS	45	Analogue	VDD_AUDIO, BAT_P	Microphone bias
AU_REF_DCPL	55	Analogue	VDD_AUDIO	Decoupling of audio reference, for high-quality audio

LED Drivers	Lead	Pad Type	Supply Domain	Description
LED[1]	33	Open drain output	Open drain	LED driver
LED[0]	32			LED driver

Test and Debug	Lead	Pad Type	Supply Domain	Description
RST#	26	Input with weak internal pull-up	VDD_PADS	Reset if low. Input debounced so must be low for >5ms to cause a reset.
TEST_EN	27	Input with strong internal pull-down		For test purposes only. Leave unconnected.

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Power Supplies Control	Lead	Description
VREGENABLE_L	68	Low-voltage linear regulator and low-voltage audio linear regulator enable, active high
VREGIN_L	1	Input to internal low-voltage linear regulator
VREGENABLE_H	35	Switch-mode regulator enable, active high
VREGIN_AUDIO	46	Input to internal low-voltage audio linear regulator
VDD_AUDIO	47	Positive supply for audio
LX	37	Switch-mode regulator output
VDD_ANA	2	Positive supply output for analogue circuitry and 1.5V regulated output, from internal low-voltage linear regulator
VDD_PIO	62	Positive supply for digital input/output ports PIO[3:0]
VDD_PADS	16	Positive supply for all other digital input/output ports including PIO[14:11,9:4]
VDD_CORE	17, 34	Positive supply for internal digital circuitry
VDD_RADIO	63, 66	Positive supply for RF circuitry
VDD_UART	13	Positive supply for UART ports
VDD_LO	67	Positive supply for local oscillator circuitry
BAT_P	38	Lithium ion/polymer battery positive terminal. Battery charger output and input to switch-mode regulator.
VDD_CHG	39	Lithium ion/polymer battery charger input
VDD_SMP_CORE	36	Positive supply for switch-mode control circuitry
VSS	Exposed Pad	Ground connections

Unconnected Leads (NCs)	Description
8, 40, 41, 42, 43, 44, 49	Leave unconnected

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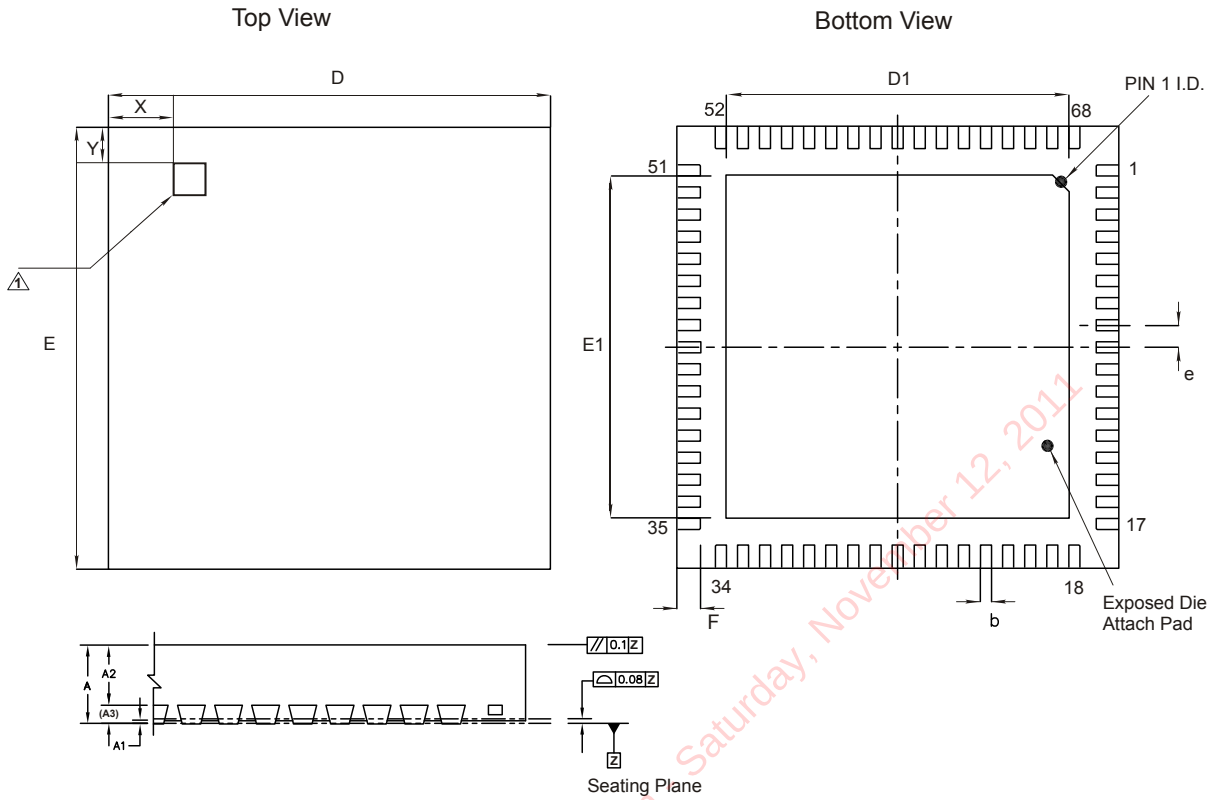
3.3 Package Dimensions



Description	68-lead Quad Flat No-lead Package			
Size	8 x 8 x 0.9mm			
Pitch	0.4mm			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A	0.80	0.85	0.90	1 Top-side polarity mark. The dimensions of the square polarity mark are 0.75 x 0.75mm.
A1	0.00	0.035	0.05	
A2	-	0.65	0.67	
A3	-	0.203	-	Coplanarity applies to leads, corner leads and die attach pad.
b	0.15	0.20	0.25	
D	7.90	8.00	8.05	
E	7.90	8.00	8.05	
e	-	0.40	-	
D1	6.10	6.20	6.30	
E1	6.10	6.20	6.30	
F	0.35	0.40	0.45	
X	-	1.00	-	
Y	-	0.85	-	
JEDEC	MO-220			
Unit	mm			

Figure 3.2: BlueTunes ROM QFN 68 Lead QFN Package Dimensions

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3.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 8 x 8 x 0.9mm QFN 68-lead package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- PCB land width should be 0.2mm and PCB land length should be 0.55mm to achieve maximum reliability.
- Solder paste must be used during the assembly process.

3.5 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

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4 Bluetooth Modem

4.1 RF Ports

4.1.1 RF_N and RF_P

RF_N and RF_P form a complementary balanced pair and are available for both transmit and receive. On transmit their outputs are combined using an external balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally.

Both terminals present similar complex impedances that may require matching networks between them and the balun. Viewed from the chip, the outputs can each be modelled as an ideal current source in parallel with a lossy capacitor. An equivalent series inductance can represent the package parasitics.

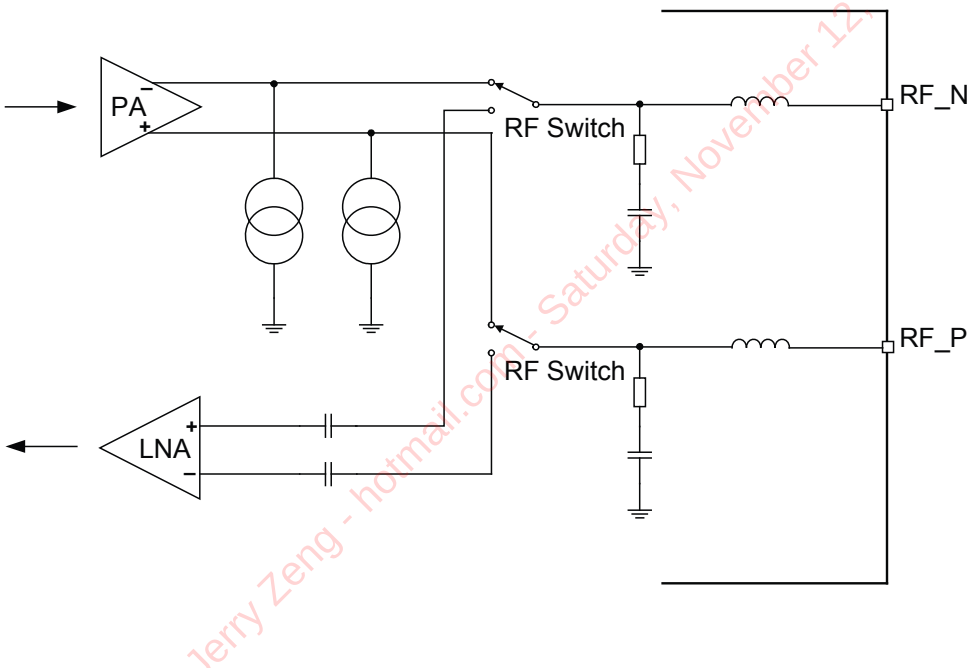

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Figure 4.1: Simplified Circuit RF_N and RF_P

RF_N and RF_P require an external DC bias. The DC level must be set at VDD_RADIO.

4.2 RF Receiver

The receiver features a near-zero IF architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input allows the receiver to be used in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. The use of a digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueTunes ROM QFN to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the demodulator contains an ADC which digitises the IF received signal. This information is then passed to the EDR modem.

4.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the shared RF port.

4.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

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4.3 RF Transmitter

4.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

4.3.2 Power Amplifier

The internal PA has a maximum output power that allows BlueTunes ROM QFN to be used in Class 2 and Class 3 radios without an external RF PA.

4.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.1 + EDR specification.

4.5 Baseband

4.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

4.5.2 Physical Layer Hardware Engine

4.6 Basic Rate Modem

The basic rate modem satisfies the basic data rate requirements of the Bluetooth v2.1 + EDR specification. The basic rate was the standard data rate available on the Bluetooth v1.2 specification and below, it is based on GFSK modulation scheme.

Including the basic rate modem allows BlueTunes ROM QFN compatibility with earlier Bluetooth products.

The basic rate modem uses the RF ports, receiver, transmitter and synthesiser, alongside the baseband components described in Section 4.5.

4.7 Enhanced Data Rate Modem

The EDR modem satisfies the requirements of the Bluetooth v2.1 + EDR specification. EDR has been introduced to provide 2x and 3x data rates with minimal disruption to higher layers of the Bluetooth stack. BlueTunes ROM QFN supports both the basic and enhanced data rates and is compliant with the Bluetooth v2.1 + EDR specification.

At the baseband level, EDR uses the same 1.6kHz slot rate and the 1MHz symbol rate defined for the basic data rate. EDR differs in that each symbol in the payload portion of a packet represents 2 or 3 bits. This is achieved using 2 new distinct modulation schemes. Table 4.1 and Figure 4.2 summarise these. Link Establishment and Management are unchanged and still use GFSK for both the header and payload portions of these packets.

The enhanced data rate modem uses the RF ports, receiver, transmitter and synthesiser, with the baseband components described in Section 4.5.

Data Rate Scheme	Bits Per Symbol	Modulation
Basic Rate	1	GFSK
EDR	2	π/4 DQPSK
EDR	3	8DPSK (optional)

Table 4.1: Data Rate Schemes

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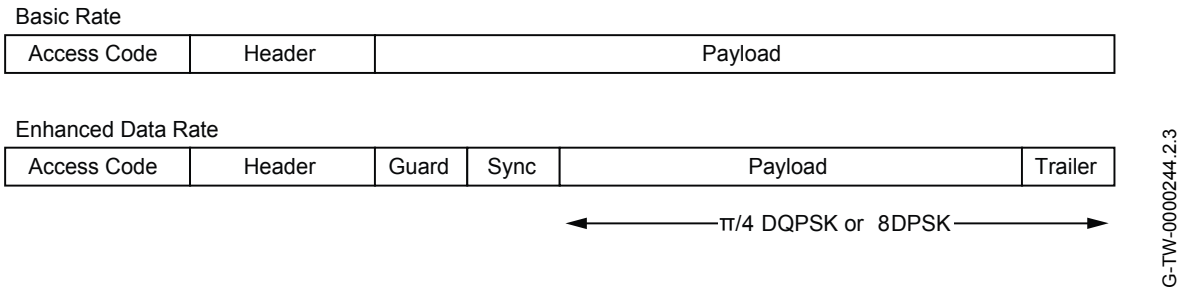

Figure 4.2: BDR and EDR Packet Structure

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5 Clock Generation

BlueTunes ROM QFN requires a Bluetooth reference clock frequency of 12MHz to 52MHz from either an externally connected crystal or from an external TCXO source.

All BlueTunes ROM QFN internal digital clocks are generated using a phase locked loop, which is locked to the frequency of either the external 12MHz to 52MHz reference clock source or an internally generated watchdog clock frequency of 1kHz.

The Bluetooth operation determines the use of the watchdog clock in low-power modes.

5.1 Clock Architecture

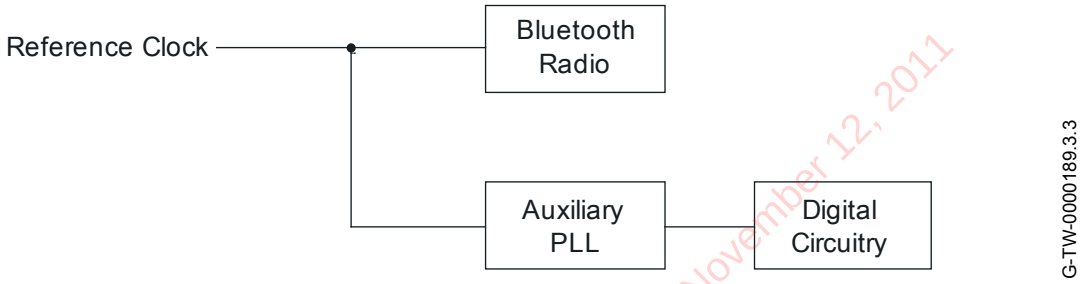

Figure 5.1: Clock Architecture

5.2 Input Frequencies and PS Key Settings

BlueTunes ROM QFN is configured to operate with a chosen reference frequency. This reference frequency is set by PSKEY_ANA_FREQ for all frequencies using an integer multiple of 250kHz. The input frequency default setting for BlueTunes ROM QFN is 26MHz depending on the software build. Full details are in the software release note for the specific build from www.csrsupport.com.

5.3 External Reference Clock

5.3.1 Input: XTAL_IN

The external reference clock is applied to the BlueTunes ROM QFN XTAL_IN input. BlueTunes ROM QFN is configured to accept the external reference clock at XTAL_IN by connecting XTAL_OUT to ground.

The external clock can be either a digital level square wave or sinusoidal, and this may be directly coupled to XTAL_IN without the need for additional components. A digital level reference clock gives superior noise immunity, as the high slew rate clock edges have lower voltage to phase conversion. If peaks of the reference clock are either below VSS or above VDD_ANA, it must be driven through a DC blocking capacitor (approximately 33pF) connected to XTAL_IN.

The external reference clock signal should meet the specifications in Table 5.1.

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			Min	Typ	Max	Unit
Frequency[a]			12	26	52	MHz
Duty cycle			20:80	50:50	80:20	-
Edge jitter (at zero crossing)			-	-	15	ps rms
Signal level	AC coupled sinusoid		0.4	-	VDD_ANA[b]	V pk-pk
	DC coupled digital	V_{IL}	-	VSS[c]	-	V
		V_{IH}	-	VDD_ANA[b] [c]	-	V

Table 5.1: External Clock Specifications

[a] The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

[b] VDD_ANA is 1.50V nominal

[c] If driven via a DC blocking capacitor max amplitude is reduced to 750mV pk-pk for non 50:50 duty cycle

5.3.2 XTAL_IN Impedance in External Mode

The impedance of XTAL_IN does not change significantly between operating modes, typically 10fF. When transitioning from deep sleep to an active state a spike of up to 1pC may be measured. For this reason CSR recommends that a buffered clock input is used.

5.3.3 Clock Start-up Delay

BlueTunes ROM QFN hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware, see Figure 5.2. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueTunes ROM QFN firmware provides a software function that extends the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 1ms to 31ms. Zero is the default entry for 5ms delay.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueTunes ROM QFN as low as possible. BlueTunes ROM QFN consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

5.3.4 Clock Timing Accuracy

As Figure 5.2 shows, the 250ppm timing accuracy on the external clock is required 2ms after the firmware begins to run. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v2.1 + EDR specification. Radio activity may occur after 6ms after the firmware starts. Therefore, at this point the timing accuracy of the external clock source must be within ±20ppm.

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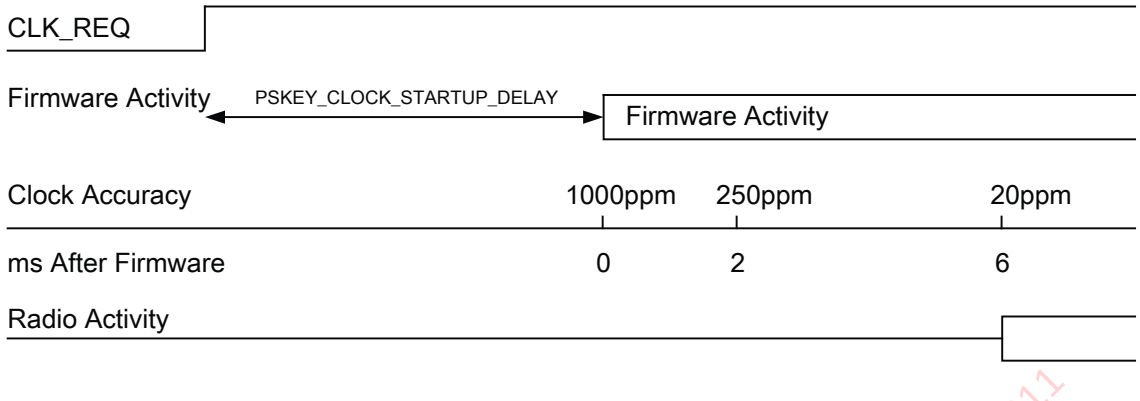

Figure 5.2: TCXO Clock Accuracy

5.4 Crystal Oscillator: XTAL_IN and XTAL_OUT

BlueTunes ROM QFN contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator. The external crystal is connected to pins XTAL_IN, XTAL_OUT.

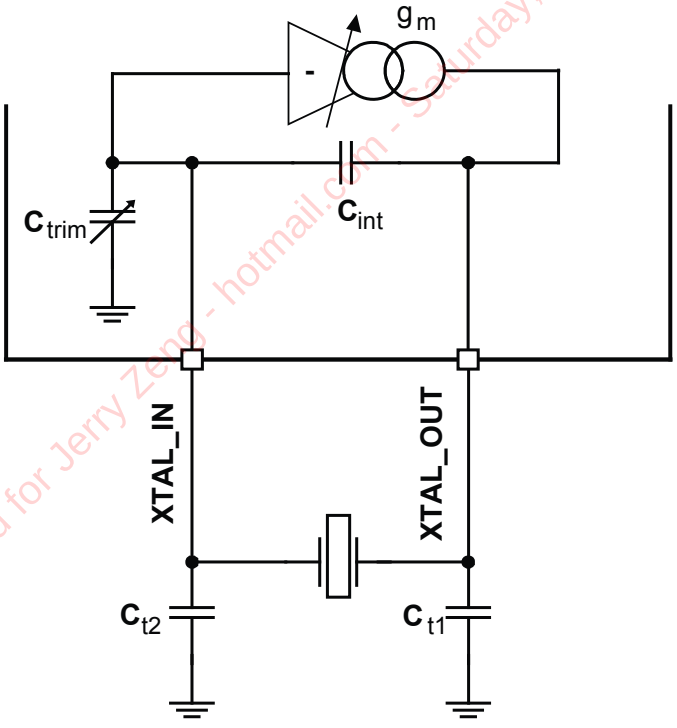

Figure 5.3: Crystal Driver Circuit

Figure 5.4 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

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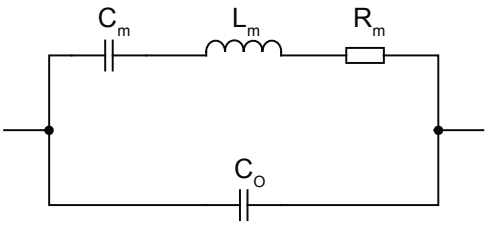

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Figure 5.4: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueTunes ROM QFN contains variable internal capacitors to provide a fine trim.

Parameter	Min	Typ	Max	Unit
Frequency	16	26	26	MHz
Initial Tolerance	-	±25	-	ppm
Pullability	-	±20	-	ppm/pF

Table 5.2: Crystal Specification

The BlueTunes ROM QFN driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

5.4.1 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueTunes ROM QFN provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing and slew rate at XTAL_IN (to which all on-chip clocks are referred).

Crystal load capacitance, C_l is calculated using Equation 5.1:

$$C_l = C_{int} + \frac{(C_{t2} + C_{trim})\ C_{t1}}{C_{t2} + C_{trim} + C_{t1}}$$

Equation 5.1: Load Capacitance

Note:

C_{trim} = 3.4pF nominal (mid-range setting)

C_{int} = 1.5pF

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

5.4.2 Frequency Trim

BlueTunes ROM QFN enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with an on-chip trim capacitor, C_{trim}. The value of C_{trim} is set by a 6-bit word in PSKEY_ANA_FTRIM. Its value is calculated as follows:

$$C_{trim} = 125fF \times PSKEY\_ANA\_FTRIM$$

Equation 5.2: Trim Capacitance

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The C_{trim} capacitor is connected between XTAL_IN and ground. When viewed from the crystal terminals, the combination of the tank capacitors and the trim capacitor presents a load across the terminals of the crystal which varies in steps of typically 125fF for each least significant bit increment of PSKEY_ANA_FTRIM.

Equation 5.3 describes the frequency trim.

$$\frac{\Delta(F_x)}{F_x} = \text{pullability} \times 0.110 \times \left(\frac{C_{t1}}{C_{t1} + C_{t2} + C_{trim}}\right)(\text{ppm/LSB})$$

Equation 5.3: Frequency Trim

Note:

F_x = crystal frequency

Pullability is a crystal parameter with units of ppm/pF

Total trim range is 0 to 63

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 5.4.

$$\frac{\partial(F_X)}{\partial(C_l)} = F_X \bullet \frac{C_m}{2(C_l + C_0)^2}$$

Equation 5.4: Pullability

Note:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model), see Figure 5.4

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

5.4.3 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueTunes ROM QFN uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit oscillates if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 5.5.

$$g_m > 3\,\frac{(2\pi F_x)^2\, R_m\, ((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + C_{t1}\,(C_{t2} + C_{trim}))}{C_{t1}\,(C_{t2} + C_{trim})}$$

Equation 5.5: Transconductance Required for Oscillation

BlueTunes ROM QFN guarantees a transconductance value of at least 2mA/V at maximum drive level.

Note:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance.

5.4.4 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueTunes ROM QFN crystal driver circuit is based on a transimpedance amplifier, it is possible to calculate an equivalent negative resistance for it using the formula in Equation 5.6.

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$$R_{neg} > \frac{C_{t1}(C_{t2} + C_{trim})}{g_m(2\pi F_x)^2(C_0 + C_{int})((C_{t1} + C_{t2} + C_{trim}) + C_{t1}(C_{t2} + C_{trim}))^2}$$

Equation 5.6: Equivalent Negative Resistance

Equation 5.6 shows the negative resistance of the BlueTunes ROM QFN driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

5.4.5 Crystal PS Key Settings

The BlueTunes ROM QFN firmware automatically controls the drive level on the crystal circuit to achieve optimum input swing. PSKEY_XTAL_TARGET_AMPLITUDE is used by the firmware to servo the required amplitude of crystal oscillation. Refer to the software build release note for a detailed description.

Configure the BlueTunes ROM QFN to operate with the chosen reference frequency.

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6 Bluetooth Stack Microcontroller

A 16-bit RISC MCU is used for low power consumption and efficient use of memory.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

6.1 Programmable I/O Ports, PIO and AIO

BlueTunes ROM QFN contains 14 lines of programmable bidirectional I/O.

BlueTunes ROM QFN has 2 general-purpose analogue interface pins, AIO[1:0], used to access internal circuitry and control signals. Auxiliary functions available on the analogue interface include a 10-bit ADC.

Note:

The PIO and AIO configuration is dependent on the BlueTunes ROM stereo headset solution.

PIO[14:11,9:4] are powered from VDD_PADS and PIO[3:0] are powered from VDD_PIO. AIO[1:0] are powered from VDD_ANA.

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7 Kalimba DSP

The Kalimba DSP is an open platformDSP allowing signal processing functions to be performed on over-air data or codec data in order to enhance audio applications. Noise cancellation and audio enhancement algorithms are hard-coded into the ROM. Figure 7.1 shows the Kalimba DSP interfaces to other functional blocks within BlueTunes ROM QFN.

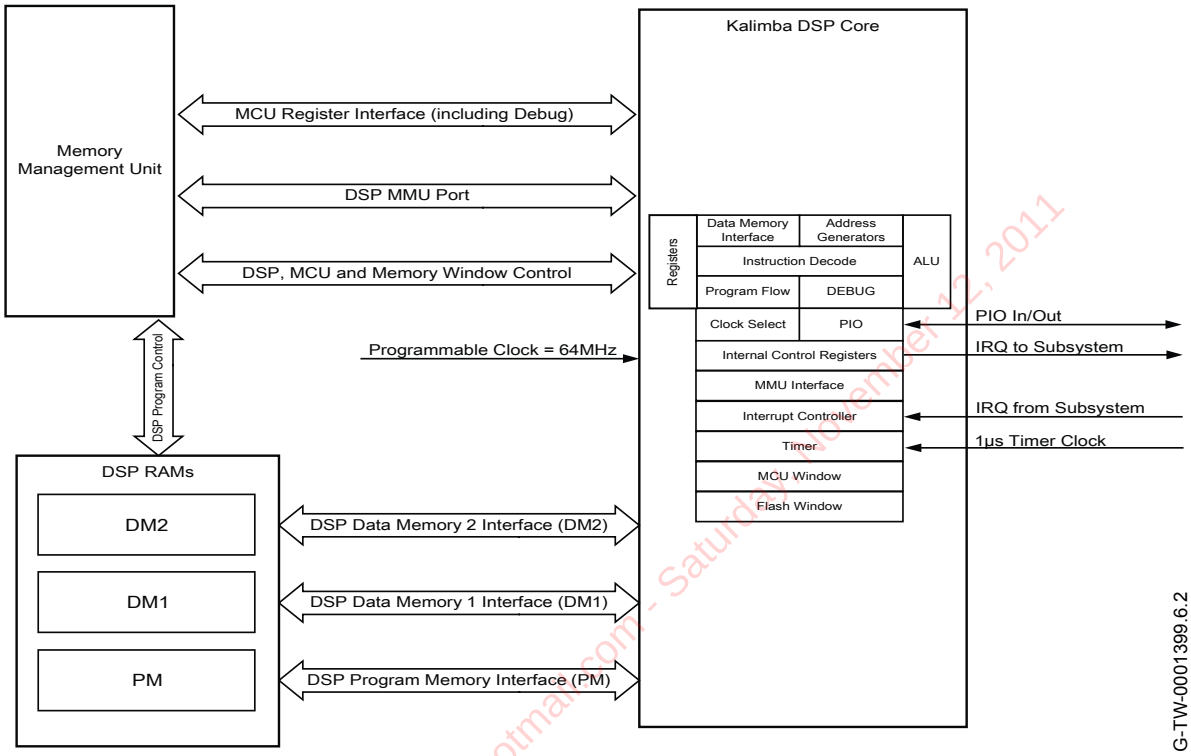

Figure 7.1: Kalimba DSP Interface to Internal Functions

The key features of the DSP include:

- 64MIPS performance, 24-bit fixed point DSP core
- Single cycle MAC of 24 x 24-bit multiply and 56-bit accumulate
- 32-bit instruction word
- Separate program memory and dual data memory, allowing an ALU operation and up to two memory accesses in a single cycle
- Zero overhead looping
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 24-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

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8 Memory Interface and Management

8.1 Memory Management Unit

The MMU provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host, the air or the Kalimba DSP. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

8.2 System RAM

48KB of on-chip RAM supports the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

8.3 Kalimba DSP RAM

Additional on-chip RAM is provided to support the Kalimba DSP:

- 8K x 24-bit for data memory 1 (DM1)
- 8K x 24-bit for data memory 2 (DM2)
- 6K x 32-bit for program memory (PM)

Note:

The Kalimba DSP can also execute directly from internal ROM, using a 64-instruction on-chip cache.

8.4 Internal ROM

Internal ROM is provided for system firmware implementation.

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9 Serial Interfaces

9.1 UART Interface

BlueTunes ROM QFN has a standard UART serial interface that provides a simple mechanism for communicating using RS232 protocol.

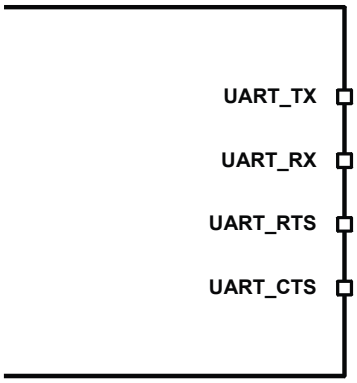

Figure 9.1: Universal Asynchronous Receiver

Figure 9.1 shows the 4 signals that implement the UART function. When BlueTunes ROM QFN is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, can implement RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using BlueTunes ROM QFN firmware.

Note:

To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 9.1: Possible UART Settings

The UART interface can reset BlueTunes ROM QFN on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 9.2. If t_{BRK} is longer than the value, defined by PSKEY_HOSTIO_UART_RESET_TIMEOUT a reset occurs. This feature allows a host to initialise the system to a known state. Also, BlueTunes ROM QFN can emit a break character that may be used to wake the host.

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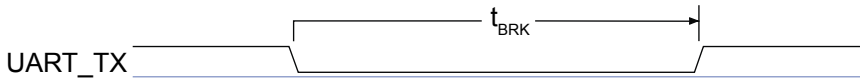

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Figure 9.2: Break Signal

Table 9.2 shows a list of commonly used baud rates and their associated values for PSKEY_UART_BAUDRATE. There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula in Equation 9.1.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

Equation 9.1: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%
3686400	0x3afb	15099	0.00%

Table 9.2: Standard Baud Rates

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9.1.1 UART Configuration While Reset is Active

The UART interface is tristate while BlueTunes ROM QFN is being held in reset. This allows the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tristate when BlueTunes ROM QFN reset is de-asserted and the firmware begins to run.

9.2 Programming and Debug Interface

BlueTunes ROM QFN uses a 16-bit data and 16-bit address programming and debug interface. Transactions can occur when the internal processor is running or is stopped.

Data may be written or read one word at a time, or the auto-increment feature is available for block access.

9.2.1 Instruction Cycle

The BlueTunes ROM QFN is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 9.3 shows the instruction cycle for a SPI transaction.

1	Reset the SPI interface	Hold SPI_CS# high for two SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CS# high

Table 9.3: Instruction Cycle for a SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueTunes ROM QFN on the rising edge of the clock line SPI_CLK. When reading, BlueTunes ROM QFN replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CS# high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueTunes ROM QFN offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

9.2.2 Multi-slave Operation

BlueTunes ROM QFN should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueTunes ROM QFN is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, BlueTunes ROM QFN outputs `0` if the processor is running or `1` if it is stopped.

9.3 I²C Interface

PIO[8:6] is available to form a master I²C interface. The interface is formed using software to drive these lines.

Note:

> The program memory for the BlueTunes ROM QFN is internal ROM so the I²C interface can only connect to a serial EEPROM, an example is shown in Figure 9.3. The EEPROM stores PS Keys and configuration information.
>
> EEPROM Supply in Figure 9.3 is 1.8V.

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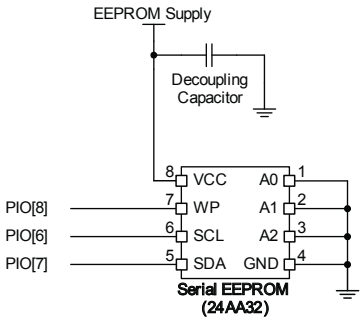

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Figure 9.3: Example EEPROM Connection

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10 Audio Interface

The BlueTunes ROM QFN audio interface circuit consists of:

- Stereo audio DAC and outputs
- Dual channel mono voice band ADC with dual microphone inputs

The audio interface supports all requirements of the BlueTunes ROM stereo headset solution and Figure 10.1 shows the functional blocks of the BlueTunes ROM QFN audio interface. The audio interface supports stereo playback of audio signals at multiple sample rates with 16-bit resolution.

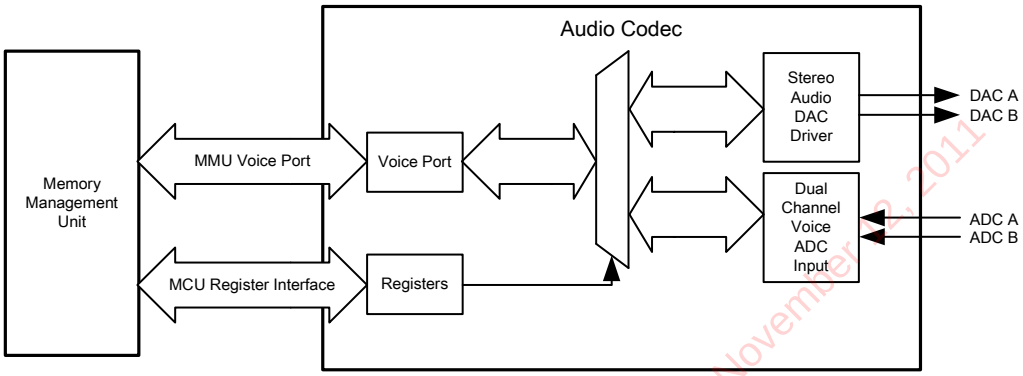

Figure 10.1: BlueTunes ROM QFN Audio Interface

10.1 Audio Input and Output

The audio input circuitry consists of a dual audio input that can be configured to be either single-ended or fully differential and programmed for either microphone or line input. It has an analogue and digital programmable gain stage for optimisation of different microphones.

The audio output circuitry consists of a dual differential class A-B output stage.

10.2 Audio Codec Interface

The main features of the interface are:

- Stereo and mono analogue output for voice band and audio band
- Dual mono analogue microphone input for voice band

Important Note:

To avoid any confusion regarding stereo operation this data sheet explicitly states which is the left and right channel for audio output. With respect to software and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel for output.

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10.2.1 Audio Codec Block Diagram

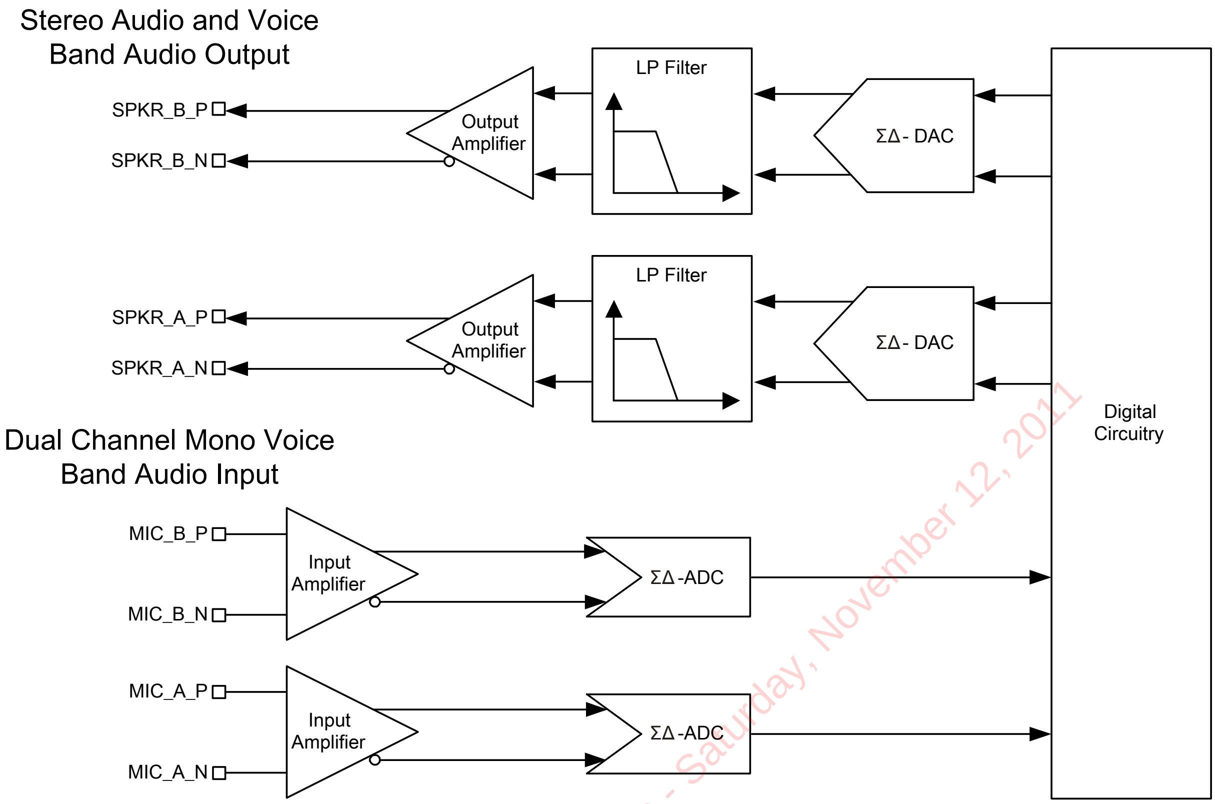

Figure 10.2: Codec Audio Input and Output Stages

The audio codec uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a single power-supply of 1.5V and uses a minimum of external components.

10.2.2 ADC

The ADC consists of:

- 2 second-order Sigma Delta converters allowing two separate channels that are identical in functionality, as shown in Figure 10.2.
- 2 gain stages for each channel, one of which is an analogue gain stage and the other is a digital gain stage.

10.2.3 ADC Sample Rate

Each ADC supports 8kHz sample rate only.

10.2.4 ADC Digital Gain

The digital gain stage has a programmable selection value in the range of 0 to 15 with the associated ADC gain settings summarised in Table 10.1. There is also a high resolution digital gain mode that allows the gain to be changed in 1/32 steps. Contact CSR for more information.

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Gain Selection Value	ADC Digital Gain Setting (dB)	Gain Selection Value	ADC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 10.1: ADC Digital Gain Rate Selection

10.2.5 ADC Analogue Gain

Figure 10.3 shows the equivalent block diagram for the ADC analogue amplifier. It is a two-stage amplifier:

- The first stage amplifier has a selectable gain of either bypass for line input mode or gain of 24dB gain for the microphone mode.
- The second stage has a programmable gain with 7 individual 3dB steps. By combining the 24dB gain selection of the microphone input with the 7 individual 3dB gain steps, the overall range of the analogue amplifier is approximately -3dB to 42dB in 3dB steps. The BlueTunes ROM stereo headset solution controls all the gain control of the ADC.

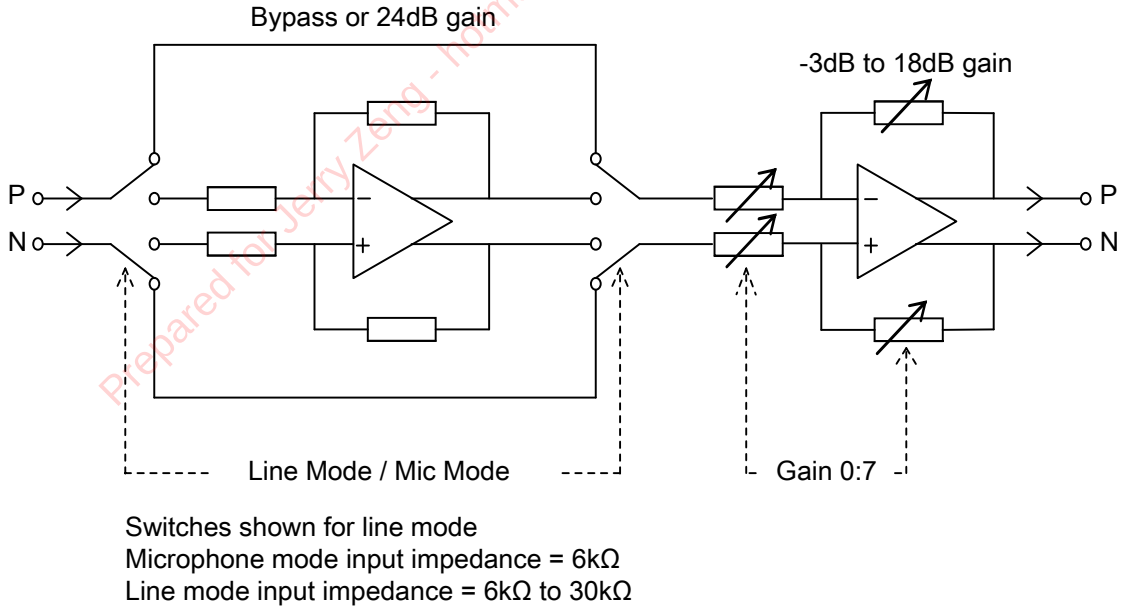

Figure 10.3: ADC Analogue Amplifier Block Diagram

10.2.6 DAC

The DAC consists of:

- 2 second-order Sigma Delta converters allowing 2 separate channels that are identical in functionality, as Figure 10.2 shows.
- 2 gain stages for each channel: one is an analogue gain stage and the other is a digital gain stage.

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10.2.7 DAC Sample Rate Selection

Each DAC supports the following samples rates:

- 8kHz
- 11.025kHz
- 12kHz
- 16kHz
- 22.050kHz
- 24kHz
- 32kHz
- 44.1kHz
- 48kHz

10.2.8 DAC Digital Gain

The digital gain stage has a programmable selection value in the range of 0 to 15 with associated DAC gain settings, summarised in Table 10.2. There is also a high resolution digital gain mode that allows the gain to be changed in 1/32dB steps. Contact CSR for more information.

The overall gain control of the DAC is controlled by the BlueTunes ROM stereo headset solution. Its setting is a combined function of the digital and analogue amplifier settings.

Digital Gain Selection Value	DAC Digital Gain Setting (dB)	Digital Gain Selection Value	DAC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 10.2: DAC Digital Gain Rate Selection

10.2.9 DAC Analogue Gain

Table 10.3 shows the DAC analogue gain stage consists of 8 gain selection values that represent seven 3dB steps.

The BlueTunes ROM stereo headset solution controls the overall gain control of the DAC. Its setting is a combined function of the digital and analogue amplifier settings.

Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)	Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)
7	3	3	-9
6	0	2	-12
5	-3	1	-15
4	-6	0	-18

Table 10.3: DAC Analogue Gain Rate Selection

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10.2.10 Microphone Input

Figure 10.4 shows recommended biasing for each microphone. The microphone bias, MIC_BIAS, derives its power from the BAT_P and requires a 1µF capacitor on its output.

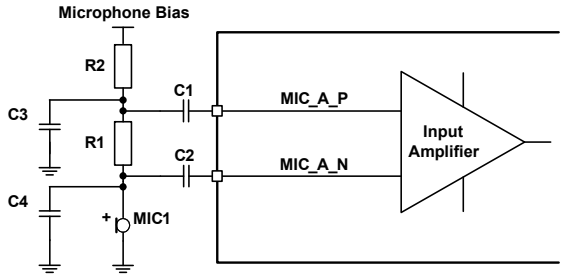

Figure 10.4: Microphone Biasing (Single Channel Shown)

The MIC_BIAS is like any voltage regulator and requires a minimum load to maintain regulation. The MIC_BIAS maintains regulation within the limits 0.200mA to 1.230mA. If the microphone sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.

The audio input is intended for use in the range from 1µA @ 94dB SPL to about 10µA @ 94dB SPL. With biasing resistors R1 and R2 equal to 1kΩ, this requires microphones with sensitivity between about –40dBV and –60dBV.

The input impedance at MIC_A_N, MIC_A_P, MIC_B_N and MIC_B_P is typically 6.0kΩ.

C1 and C2 should be 150nF if bass roll-off is required to limit wind noise on the microphone.

R1 sets the microphone load impedance and is normally in the range of 1kΩ to 2kΩ.

R2, C3 and C4 improve the supply rejection by decoupling supply noise from the microphone. Values should be selected as required. R2 may be connected to a convenient supply, in which case the bias network is permanently enabled, or to the MIC_BIAS output (which is ground referenced and provides good rejection of the supply), which may be configured to provide bias only when the microphone is required.

Table 10.4 shows the 4-bit programmable output voltage that the microphone bias provides, and Table 10.5 shows the 4-bit programmable output current.

The characteristics of the microphone bias include:

- Power supply:
  - BlueTunes ROM QFN microphone supply is BAT_P
  - Minimum input voltage = Output voltage + drop-out voltage
  - Maximum input voltage is 4.4V
  - Typically the microphone bias is at the same level as VDD_AUDIO (1.5V)
- Drop-out voltage:
  - 300mV minimum
  - Guaranteed for configuration of voltage or current output shown in Table 10.4 and Table 10.5
- Output voltage:
  - 4-bit programmable between 1.7V to 3.6V
  - Tolerance 90 to 110%
- Output current:
  - 4-bit programmable from 200µA to 1.230mA
  - Maximum current guaranteed to be >1mA
- Load capacitance:
  - Unconditionally stable for 1µF ± 20% and 2.2µF ± 20% pure C

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Output Step	VOL_SET[3:0]	Min	Typ	Max	Units
0	0000	-	1.71	-	V
1	0001	-	1.76	-	V
2	0010	-	1.82	-	V
3	0011	-	1.87	-	V
4	0100	-	1.95	-	V
5	0101	-	2.02	-	V
6	0110	-	2.10	-	V
7	0111	-	2.18	-	V
8	1000	-	2.32	-	V
9	1001	-	2.43	-	V
10	1010	-	2.56	-	V
11	1011	-	2.69	-	V
12	1100	-	2.90	-	V
13	1101	-	3.08	-	V
14	1110	-	3.33	-	V
15	1111	-	3.57	-	V

Table 10.4: Voltage Output Steps

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Output Step	CUR_SET[3:0]	Typ	Units
0	0000	0.200	mA
1	0001	0.280	mA
2	0010	0.340	mA
3	0011	0.420	mA
4	0100	0.480	mA
5	0101	0.530	mA
6	0110	0.610	mA
7	0111	0.670	mA
8	1000	0.750	mA
9	1001	0.810	mA
10	1010	0.860	mA
11	1011	0.950	mA
12	1100	1.000	mA
13	1101	1.090	mA
14	1110	1.140	mA
15	1111	1.230	mA

Table 10.5: Current Output Steps

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Note:

For BAT_P, the PSRR at 100Hz to 22kHz, with >300mV supply headroom, decoupling capacitor of 1.1µF, is typically 58.9dB and worst case 53.4dB.

For VDD_AUDIO, the PSRR at 100Hz to 22kHz, decoupling capacitor of 1.1µF, is typically 88dB and worst case 60dB.

10.2.11 Line Input

If the input analogue gain is set to less than 24dB, BlueTunes ROM QFN automatically selects line input mode. In line input mode the first stage of the amplifier is automatically disabled, providing additional power saving. In line input mode the input impedance varies from 6kΩ to 30kΩ, depending on the volume setting. Figure 10.5 and Figure 10.6 show 2 circuits for line input operation and show connections for either differential or single-ended inputs.

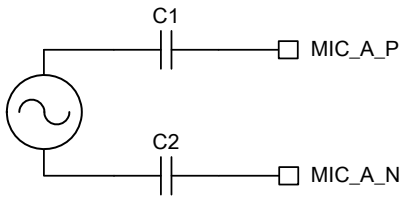

Figure 10.5: Differential Input (Single Channel Shown)

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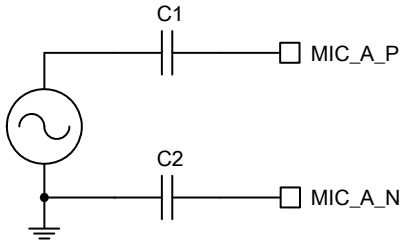

Figure 10.6: Single-ended Input (Single Channel Shown)

10.2.12 Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The output stage circuit comprises a DAC with gain setting and class AB output stage amplifier. The output is available as a differential signal between SPKR_A_N and SPKR_A_P for the left channel, as Figure 10.7 shows, and between SPKR_B_N and SPKR_B_P for the right channel.

The output stage is capable of driving a speaker directly when its impedance is at least 8Ω and an external regulator is used, but this will be at a reduced output swing.

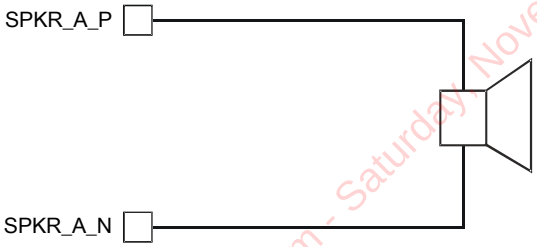

Figure 10.7: Speaker Output (Single Channel Shown)

A 3-bit programmable resistive divider controls the analogue gain of the output stage, which sets the gain in steps of approximately 3dB.

10.2.13 Mono Operation

Mono operation is a single-channel operation of the stereo codec. The left channel represents the single mono channel for audio in and audio out. In mono operation the right channel is the auxiliary mono channel that may be used in dual mono channel operation.

In single channel mono operation, disable the other channel to reduce power consumption.

Important Note:

For mono operation this data sheet uses the left channel for standard mono operation for audio input and output and with respect to software and any registers, channel 0 or channel A represents the standard mono channel for audio input and output. In mono operation the second channel which is the right channel, channel 1 or channel B can be used as a second mono channel if required and this channel is referred to as the auxiliary mono channel for audio input and output.

10.2.14 Side Tone

In some applications it is necessary to implement side tone. This involves feeding an attenuated version of the microphone signal to the earpiece. The BlueTunes ROM QFN codec contains side tone circuitry to do this. The side tone hardware is configured through the following PS Keys:

- PSKEY_SIDE_TONE_ENABLE
- PSKEY_SIDE_TONE_GAIN
- PSKEY_SIDE_TONE_AFTER_ADC
- PSKEY_SIDE_TONE_AFTER_DAC

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10.2.15 Integrated Digital Filter

BlueTunes ROM QFN has a programmable digital filter integrated into the ADC channel of the codec. The filter is a 2 stage, second order IIR and is used for functions such as custom wind noise rejection. The filter also has optional DC blocking.

The filter has 10 configuration words used as follows:

- 1 for gain value
- 8 for coefficient values
- 1 for enabling and disabling the DC blocking

The gain and coefficients are all 12-bit 2's complement signed integer with the format `XX.XXXXXXXXXX`

Note:

The position of the binary point is between bit[10] and bit[9], where bit[11] is the most significant bit.

For example:

`01.1111111111` = most positive number, close to 2

`01.0000000000` = 1

`00.0000000000` = 0

`11.0000000000` = -1

`10.0000000000` = -2, most negative number

Equation 10.1 shows the equation for the IIR filter. Equation 10.2 shows the equation for when the DC blocking is enabled.

The filter can be configured, enabled and disabled from the VM via the `CodecSetIIRFilterA` and `CodecSetIIRFilterB` traps. This requires firmware support. The configuration function takes 10 variables in the order shown below:

`0` : Gain

`1` : b_{01}

`2` : b_{02}

`3` : a_{01}

`4` : a_{02}

`5` : b_{11}

`6` : b_{12}

`7` : a_{11}

`8` : a_{12}

`9` : DC Block (1 = enable, 0 = disable)

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$$\text{Filter, } H(z) = \text{Gain} \times \frac{(1 + b_{01} z^{-1} + b_{02} z^{-2})}{(1 + a_{01} z^{-1} + a_{02} z^{-2})} \times \frac{(1 + b_{11} z^{-1} + b_{12} z^{-2})}{(1 + a_{11} z^{-1} + a_{12} z^{-2})}$$

Equation 10.1: IIR Filter Transfer Function, H(z)

$$\text{Filter with DC Blocking, } H_{DC}(z) = H(z) \times (1 - z^{-1})$$

Equation 10.2: IIR Filter plus DC Blocking Transfer Function, $H_{DC}(z)$

10.3 AuriStream Codec

The AuriStream codec is an ADPCM codec and works on the principle of transmitting the difference between the actual value of the signal and a prediction rather than the signal itself. Therefore, the information transmitted is reduced along with the power requirement. The quality of the output depends on the number of bits used to represent the sample.

Note:

The use of the AuriStream codec is as follows:

- The AuriStream codec is an alternative to standard CVSD
- It requires CSR devices supporting AuriStream at both ends of the link
- AuriStream is negotiated when the link is brought up. If either end does not support AuriStream the system will switch to standard CVSD ensuring full interoperability with any non-AuriStream Bluetooth devices.

The inclusion of the AuriStream codec can greatly enhance audio quality in the wideband mode and results in reduced power consumption compared to a CVSD implementation when used at both ends of the system.

The AuriStream codec on BlueTunes ROM QFN supports only one G726 mode of operation

- 4-bit, 8kHz sample rate, 32Kbps
  - Mode 1 gives 30% reduced power in both handset and headset Bluetooth ICs

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11 Power Control and Regulation

BlueTunes ROM QFN contains 3 regulators:

- 1 switch-mode regulator generates a 1.8V rail for the chip I/Os
- 2 low-voltage linear regulators which run in parallel to supply the 1.5V core supplies from the 1.8V rail

Various configurations for power control and regulation with BlueTunes ROM QFN are as follows:

- Powered from the switch-mode regulator and the low-voltage linear regulators in series, as Figure 11.1 shows
- Powered directly from an external 1.8V rail, omitting the switch-mode regulator
- Powered from an external 1.5V rail omitting all regulators

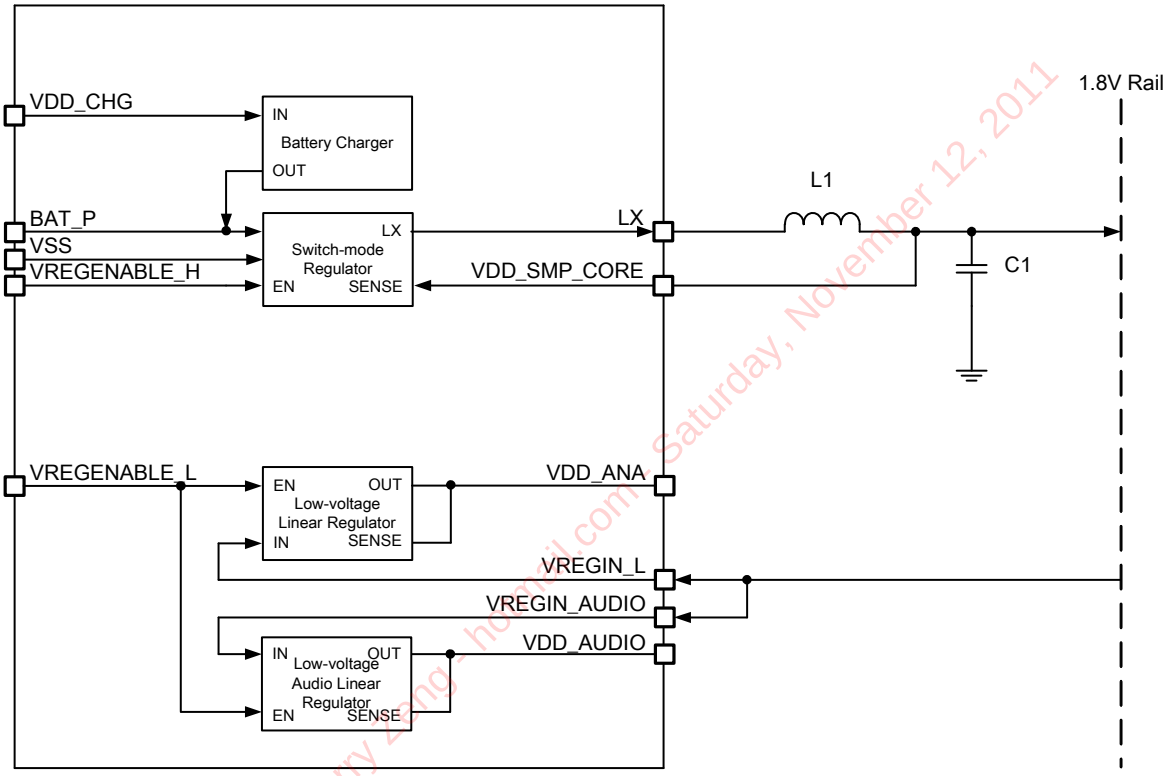

Figure 11.1: Voltage Regulator Configuration

11.1 Power Sequencing

The 1.50V supply rails are VDD_ANA, VDD_LO, VDD_RADIO, VDD_AUDIO and VDD_CORE. CSR recommends that these supply rails are all powered at the same time.

The digital I/O supply rails are VDD_PIO, VDD_PADS and VDD_UART.

The sequence of powering the 1.50V supply rails relative to the digital I/O supply rails is not important. If the digital I/O supply rails are powered before the 1.50V supply rails, all digital I/Os will have a weak pull-down irrespective of the reset state.

VDD_ANA, VDD_LO, VDD_RADIO and VDD_AUDIO can connect directly to a 1.50V supply.

A simple RC filter is recommended for VDD_CORE to reduce transients fed back onto the power supply rails.

The digital I/O supply rails are connected either together or independently to an appropriate voltage rail. Decoupling of the digital I/O supply rails is recommended.

11.2 External Voltage Source

If any of the supply rails for BlueTunes ROM QFN are supplied from an external voltage source, rather than one of the internal voltage regulators, CSR recommends that VDD_LO, VDD_RADIO and VDD_AUDIO should have less than 10mV rms noise levels between 0 and 10MHz. Also avoid single tone frequencies.

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The transient response of any external regulator used should match or be better than the internal regulator available on BlueTunes ROM QFN. For more information, refer to regulator characteristics in Section 13. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption jumps to high levels.

11.3 Low-voltage Linear Regulator

The low-voltage linear regulator is available to power a 1.5V supply rail. Its output is connected internally to VDD_ANA, and can be connected externally to the other 1.5V power inputs.

If the low-voltage linear regulator is used, connect a smoothing circuit using a low ESR 2.2µF capacitor and a 2.2Ω resistor to ground to the output of the low-voltage linear regulator, VDD_ANA. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The low-voltage linear regulator is enabled by either:

- VREGENABLE_L pin
- BlueTunes ROM QFN device firmware
- BlueTunes ROM QFN battery charger

The low-voltage linear regulator switches into a low power mode when the device is in deep sleep mode, or in reset.

When the low-voltage linear regulator is not used, either leave the terminal VREGIN_L unconnected, or tie it to VDD_ANA.

11.4 Low-voltage Audio Linear Regulator

The low-voltage audio linear regulator is available to power a 1.5V audio supply rail. Its output is connected internally to VDD_AUDIO, and can be connected externally to the other 1.5V audio power inputs.

If the low-voltage audio linear regulator is used, connect a smoothing circuit using a low ESR 2.2µF capacitor and a 2.2Ω resistor to ground to the output of the low-voltage audio linear regulator, VDD_AUDIO. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The low-voltage audio linear regulator is enabled by either:

- VREGENABLE_L pin
- BlueTunes ROM QFN device firmware

The low-voltage audio linear regulator switches into a low-power mode when no audio cells are enabled, or when the chip is in reset.

When this regulator is not used, either leave the terminal VREGIN_AUDIO unconnected or tie it to VDD_AUDIO.

11.5 Switch-mode Regulator

CSR recommends the on-chip switch-mode regulator to power the 1.8V supply rail.

An external LC filter circuit of a low-resistance series inductor, L1 (22µH), followed by a low ESR shunt capacitor, C1 (4.7µF), is required between the LX terminal and the 1.8V supply rail. A connection between the 1.8V supply rail and the VDD_SMP_CORE pin is required.

A 2.2µF decoupling capacitor is required between BAT_P and VSS.

To maintain high-efficiency power conversion and low supply ripple, it is essential that the series resistance of tracks between the BAT_P and VSS terminals, the filter and decoupling components, and the external voltage source are minimised.

The switch-mode regulator is enabled by either:

- VREGENABLE_H pin
- BlueTunes ROM QFN device firmware
- BlueTunes ROM QFN battery charger

The switch-mode regulator switches into a low-power pulse skipping mode when the device is sent into deep sleep mode, or in reset.

When the switch-mode regulator is not required the terminals BAT_P and LX must be grounded or left unconnected.

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11.6 Battery Charger

The battery charger is a constant current / constant voltage charger circuit, and is suitable for lithium ion/polymer batteries only. It shares a connection to the battery terminal, BAT_P, with the switch-mode regulator. However it may be used in conjunction with either of the high-voltage regulators on the device.

The constant current level can be varied to allow charging of different capacity batteries.

The charger enters various states of operation as it charges a battery, as listed below. A full operational description is in *BlueCore5 Charger Description and Calibration Procedure Application Note*:

- Off : entered when charger disconnected.
- Trickle charge: entered when battery is below 2.9V. The battery is charged at a nominal 4.5mA. This mode is for the safe charge of deeply discharged cells.
- Fast charge constant current: entered when battery is above 2.9V. The charger enters the main fast charge mode. This mode charges the battery at the selected constant current, I_{chgset}.
- Fast charge constant voltage: entered when battery has reached a selected voltage, V_{float}. The charger switches mode to maintain the cell voltage at the V_{float} voltage by adjusting the charge current.
- Standby: this is the state when the battery is fully charged and no charging takes place. The battery voltage is continuously monitored and if it drops by more than 150mV below the V_{float} voltage the charger will re-enter the fast charge constant current mode to keep the battery fully charged.

When a voltage is applied to the charger input terminal VDD_CHG, and the battery is not fully charged, the charger operates and an LED connected to the terminal LED[0] illuminates. By default, until the firmware is running, the LED pulses at a low-duty cycle to minimise current consumption.

The battery charger circuitry auto-detects the presence of a power source, allowing the firmware to detect, using an internal status bit, when the charger is powered. Therefore when the charger supply is not connected to VDD_CHG, the terminal must be left open-circuit. When not connected, the VDD_CHG pin must be allowed to float and not pulled to a power rail. When the battery charger is not enabled this pin may float to a low undefined voltage. Any DC connection increases current consumption of the device. Capacitive components may be connected such as diodes, FETs and ESD protection.

The battery charger is designed to operate with a permanently connected battery. If the application enables the charger input to be connected while the battery is disconnected, then the BAT_P pin voltage may become unstable. This in turn may cause damage to the internal switch-mode regulator. Connecting a 470µF capacitor to BAT_P limits these oscillations which prevents damage.

11.7 Voltage Regulator Enable Pins

The voltage regulator enable pins, VREGENABLE_H and VREGENABLE_L, are used to enable the BlueTunes ROM QFN device if the on-chip regulators are being used. Table 11.1 shows the enable pin responsible for each voltage regulator.

Enable Pin	Regulator
VREGENABLE_H	Switch-mode Regulator
VREGENABLE_L	Low-voltage Linear Regulator and Low-voltage Audio Linear Regulator

Table 11.1: BlueTunes ROM QFN Voltage Regulator Enable Pins

The voltage regulator enable pins are active high, with weak pull-downs.

BlueTunes ROM QFN boots-up when the voltage regulator enable pins are pulled high, enabling the appropriate regulators. The firmware then latches the regulators on and the voltage regulator enable pins may then be released.

The status of the VREGENABLE_H pin is available to firmware through an internal connection. VREGENABLE_H also works as an input line.

11.8 Reset, RST#

BlueTunes ROM QFN can be reset from several sources:

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- RST# pin
- Power-on reset
- UART break character
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset is performed between 1.5 and 4.0ms following RST# being active. CSR recommends that RST# be applied for a period greater than 5ms.

The power-on reset typically occurs when the VDD_CORE supply falls below 1.25V and is released when VDD_CORE rises above typically 1.30V. At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are tristate. Following a reset, BlueTunes ROM QFN assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueTunes ROM QFN is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueTunes ROM QFN free runs, again at a safe frequency.

11.8.1 Digital Pin States on Reset

Table 11.2 shows the pin states of BlueTunes ROM QFN on reset.

Pin Name / Group	I/O Type	No Core Voltage Reset	Full Chip Reset
UART_RX	Digital input with PD	PD	PD
UART_CTS	Digital input with PD	PD	PD
UART_TX	Digital bidirectional with PU	PU	PU
UART_RTS	Digital bidirectional with PU	PU	PU
SPI_MOSI	Digital input with PD	PD	PD
SPI_CLK	Digital input with PD	PD	PD
SPI_CS#	Digital input with PU	PU	PU
SPI_MISO	Digital tristate output with PD	PD	PD
RST#	Digital input with PU	PU	PU
TEST_EN	Digital input with PD	PD	PD
PIO[14:11,9:0]	Digital bidirectional with PU/ PD	PD	PD

Table 11.2: BlueTunes ROM QFN Digital Pin States on Reset

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Note:

PU = pull-up

PD = pull-down

Pull-up and pull-down default to weak values unless specified otherwise

11.8.2 Status after Reset

The chip status after a reset is as follows:

- Warm reset: data rate and RAM data remain available
- Cold reset: data rate and RAM data not available

11.9 LED Drivers

BlueTunes ROM QFN includes 2 pads dedicated to driving LED indicators. Both terminals can be controlled by firmware, while LED[0] can also be set by the battery charger.

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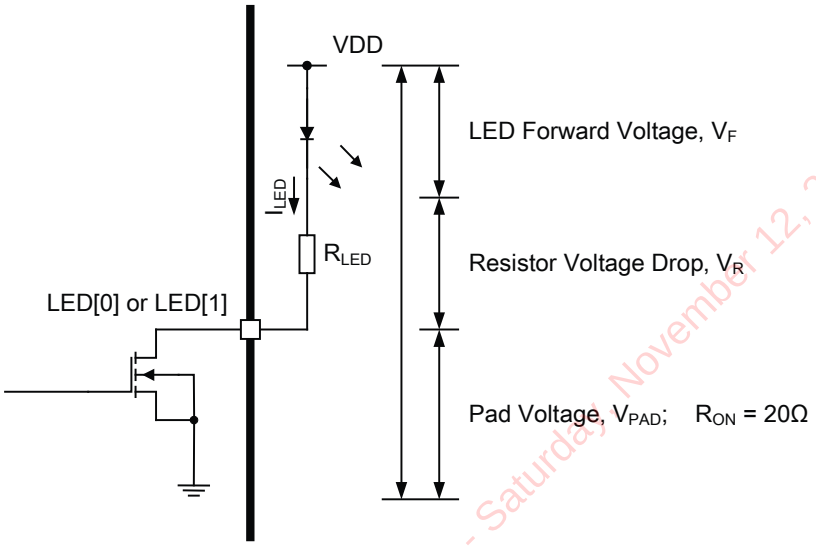
The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current limiting resistor.

CSR recommends that the LED pad, LED[0] or LED[1] pins, operate with a pad voltage below 0.5V. In this case, the pad is like a resistor, R_{ON}. The resistance together with the external series resistor sets the current, I_{LED}, in the LED. The current is also dependent on the external voltage, VDD, as Figure 11.2 shows.



G-TW-0000255.3.2

Figure 11.2: LED Equivalent Circuit

From Figure 11.2 it is possible to derive Equation 11.1 to calculate I_{LED}. If a known value of current is required through the LED to give a specific luminous intensity, then the value of R_{LED} can be calculated.

$$I_{LED} = \frac{VDD - V_F}{R_{LED} + R_{ON}}$$

Equation 11.1: LED Current

For the LED[0] or LED[1] pad to act as resistance, the external series resistor, R_{LED}, needs to be such that the voltage drop across it, V_R, keeps V_{PAD} below 0.5V. Equation 11.2 also applies.

$$VDD = V_F + V_R + V_{PAD}$$

Equation 11.2: LED PAD Voltage

Note:

The LED current adds to the overall current, so conservative selection of the LEDs will extend battery life.

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12 Example Application Schematic

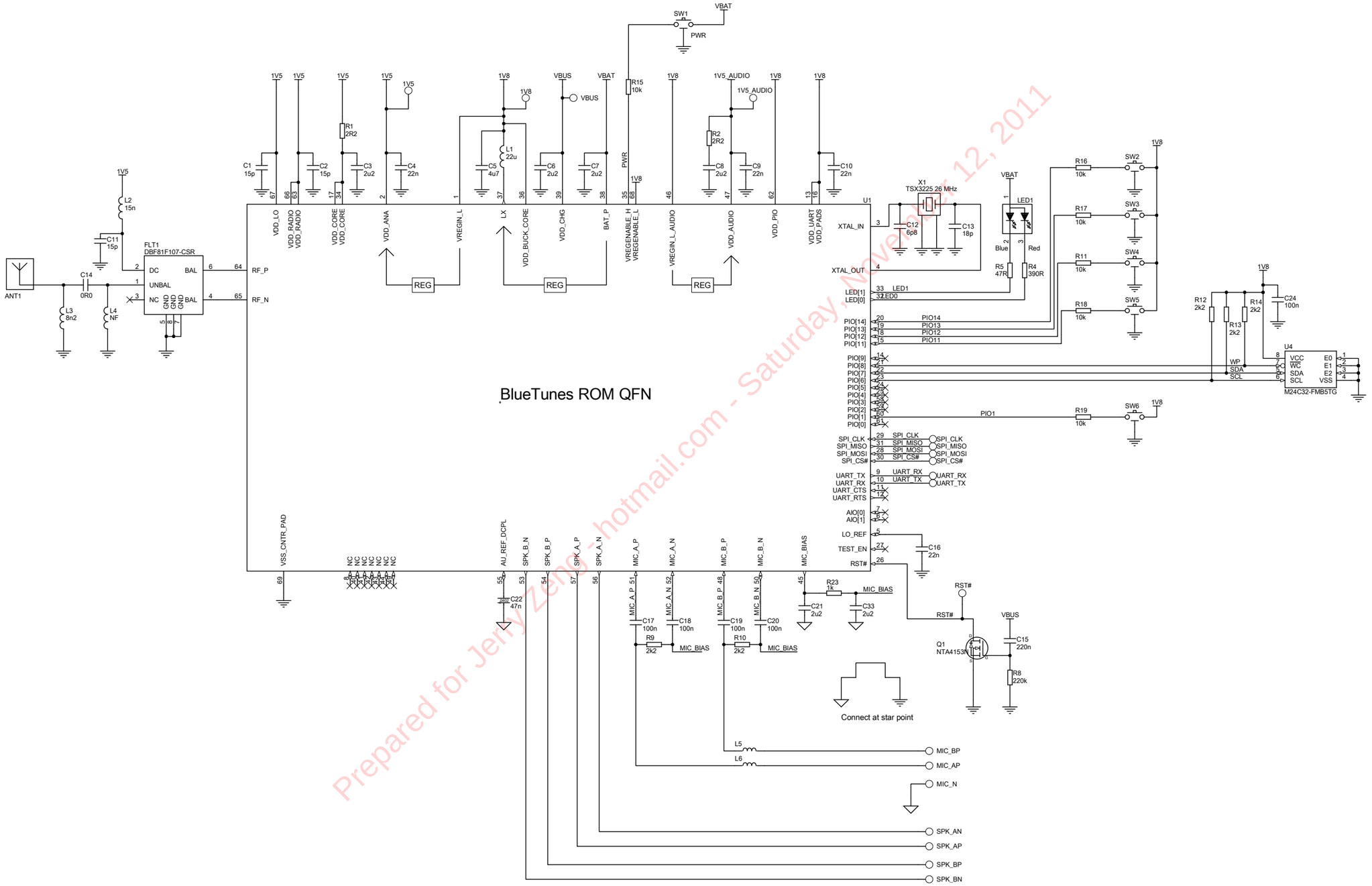

Figure 12.1: BlueTunes ROM QFN Example Application Schematic

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13 Electrical Characteristics

13.1 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage temperature		-40	105	°C
Core supply voltage	VDD_ANA, VDD_LO, VDD_RADIO, VDD_AUDIO and VDD_CORE	-0.4	1.65	V
I/O voltage	VDD_PIO, VDD_PADS and VDD_UART	-0.4	3.6	V
Supply voltage	VREGIN_L	-0.4	2.7	V
	VREGIN_AUDIO	-0.4	2.7	V
	VREGENABLE_H and VREGENABLE_L	-0.4	4.9	V
	BAT_P	-0.4	4.4	V
	LED[1:0]	-0.4	4.4	V
	VDD_CHG	-0.4	6.5	V
Other terminal voltages		VSS - 0.4	VDD + 0.4	V

13.2 Recommended Operating Conditions

Operating Condition		Min	Typ	Max	Unit
Operating temperature range		-20	20	70	°C
Core supply voltage	VDD_ANA, VDD_LO, VDD_RADIO, VDD_AUDIO and VDD_CORE	1.42	1.50	1.57	V
I/O supply voltage	VDD_PIO, VDD_PADS and VDD_UART	1.7	3.3	3.6	V

Note:

For radio performance over temperature refer to *BlueTunes ROM QFN Performance Specification*.

BlueTunes ROM QFN operates up to the maximum supply voltage given in the Absolute Maximum Ratings, but RF performance is not guaranteed above 4.2V.

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13.3 Input/Output Terminal Characteristics

Note:

For all I/O terminal characteristics:

- VDD_ANA, VDD_LO, VDD_RADIO, VDD_AUDIO and VDD_CORE at 1.50V unless shown otherwise.
- VDD_PIO, VDD_PADS and VDD_UART at 3.3V unless shown otherwise.
- Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

13.3.1 Low-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.70	1.80	1.95	V
Output voltage (I_{load} = 70mA / VREGIN_L = 1.7V)	1.42	1.50	1.57	V
Temperature coefficient	-300	0	300	ppm/°C
Output noise[a] [b]	-	-	1	mV rms
Load regulation (100µA < I_{load} < 90mA), ΔV_{out}	-	-	5	mV
Load regulation (100µA < I_{load} < 115mA), ΔV_{out}	-	-	25	mV
Settling time[a] [c]	-	-	50	µs
Output current	-	-	115	mA
Minimum load current	5	-	100	µA
Quiescent current (excluding load, I_{load} < 1mA)	50	90	150	µA
Low-power Mode [d]				
Quiescent current (excluding load, I_{load} < 100µA)	5	8	15	µA

[a] Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

[b] Frequency range 100Hz to 100kHz

[c] 1mA to 115mA pulsed load

[d] The regulator is in low power mode when the chip is in deep sleep mode, or in reset

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13.3.2 Low-voltage Linear Audio Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.70	1.80	1.95	V
Output voltage (I_{load} = 70mA / VREGIN_AUDIO = 1.7V)	1.42	1.50	1.57	V
Temperature coefficient	-300	0	300	ppm/°C
Output noise[a] [b]	-	-	1	mV rms
Load regulation (100µA < I_{load} < 70mA), ΔV_{out}	-	-	5	mV
Settling time[a] [c]	-	-	50	µs
Output current	-	-	70	mA
Minimum load current	5	-	100	µA
Quiescent current (excluding load, I_{load} < 1mA)	25	30	50	µA
Low-power Mode [d]				
Quiescent current (excluding load, I_{load} < 100µA)	5	8	15	µA

[a] Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

[b] Frequency range 100Hz to 100kHz

[c] 1mA to 70mA pulsed load

[d] The regulator is in low power mode when the chip is in deep sleep mode, or in reset

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13.3.3 Switch-mode Regulator

Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.5	-	4.4	V
Output voltage (I_{load} = 70mA)	1.70	1.80	1.90	V
Temperature coefficient	-250	-	250	ppm/°C
Normal Operation				
Output ripple	-	-	10	mV rms
Transient settling time[a]	-	-	50	µs
Maximum load current	200	-	-	mA
Conversion efficiency (I_{load} = 70mA)	-	90	-	%
Switching frequency[b]	-	1.333	-	MHz
Start-up current limit[c]	30	50	80	mA
Low-power Mode [d]				
Output ripple	-	-	1	mV rms
Transient settling time[e]	-	-	700	µs
Maximum load current	5	-	-	mA
Minimum load current	1	-	-	µA
Conversion efficiency (I_{load} = 1mA)	-	80	-	%
Switching frequency[f]	50	-	150	kHz

[a] For step changes in load of 30 to 80mA and 80 to 30mA

[b] Locked to crystal frequency

[c] Current is limited on start-up to prevent excessive stored energy in the filter inductor

[d] The regulator is in low power mode when the chip is in deep sleep mode, or in reset

[e] 100µA to 1mA pulsed load

[f] Defines minimum period between pulses. Pulses are skipped at low current loads

Note:

The external inductor used with the switch-mode regulator must have an ESR in the range 0.3Ω to 0.7Ω:

- Low ESR < 0.3Ω causes instability.
- High ESR > 0.7Ω derates the maximum current.

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13.3.4 Battery Charger

Battery Charger	Min	Typ	Max	Unit
Input voltage	4.5	-	6.5	V

Charging Mode (BAT_P rising to 4.2V)		Min	Typ	Max	Unit
Supply current[a]		-	4.5	6	mA
Battery trickle charge current[b]		-	4	-	mA
Maximum battery fast charge current (I-CTRL = 15)[c] [d]	Headroom[e] > 0.7V	-	140	-	mA
	Headroom = 0.3V	-	120	-	mA
Minimum battery fast charge current (I-CTRL = 0)[c] [d]	Headroom > 0.7V	-	40	-	mA
	Headroom = 0.3V	-	35	-	mA
Fast charge step size (I-CTRL = 0 to 15)	Spread ±17%	-	6.3	-	mA
Trickle charge voltage threshold		-	2.9	-	V
Float voltage (with correct trim value set), V_{FLOAT} [f]		4.17	4.2	4.23	V
Float voltage trim step size[f]		-	50	-	mV
Battery charge termination current, % of fast charge current		5	10	20	%

[a] Current into VDD_CHG does not include current delivered to battery (I_{VDD_CHG} - I_{BAT_P})

[b] BAT_P < trickle charge voltage threshold

[c] Charge current can be set in 16 equally spaced steps

[d] Trickle charge threshold < BAT_P < Float voltage

[e] Where headroom = VDD_CHG - BAT_P

[f] Float voltage can be adjusted in 15 steps. Trim setting is determined in production test and must be loaded into the battery charger by firmware during boot-up sequence

Standby Mode (BAT_P falling from 4.2V)	Min	Typ	Max	Unit
Supply current[a]	-	1.5	2	mA
Battery current	-	-5	-	µA
Battery recharge hysteresis[b]	100	-	200	mV

[a] Current into VDD_CHG; does not include current delivered to battery (I_{VDD_CHG} - I_{BAT_P})

[b] Hysteresis of (V_{FLOAT} - BAT_P) for charging to restart

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Shutdown Mode (VDD_CHG too low or disabled by firmware)		Min	Typ	Max	Unit
Supply current		-	1.5	2	mA
Battery current		-1	-	0	µA
VDD_CHG under-voltage threshold	VDD_CHG rising	-	3.90	-	V
	VDD_CHG falling	-	3.70	-	V
VDD_CHG - BAT_P lockout threshold	VDD_CHG rising	-	0.22	-	V
	VDD_CHG falling	-	0.17	-	V

13.3.5 Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.13	1.25	1.30	V
VDD_CORE rising threshold	1.20	1.30	1.35	V
Hysteresis	0.05	0.10	0.15	V

13.3.6 Regulator Enable

Switching Threshold	Min	Typ	Max	Unit
VREGENABLE_H				
Rising threshold	0.50	-	0.95	V
Falling threshold	0.35	-	0.80	V
Hysteresis	0.14	-	0.28	V
VREGENABLE_L				
Rising threshold	0.50	-	0.95	V
Falling threshold	0.35	-	0.80	V
Hysteresis	0.14	-	0.28	V

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13.3.7 Digital Terminals

Supply Voltage Levels		Min	Typ	Max	Unit
VDD_{PRE}	Pre-driver supply voltage	1.4	1.5	1.6	V
VDD I/O supply voltage (post-driver)	Full spec.	3.0	3.3	3.6	V
	Reduced spec.	1.7	-	3.0	V

Input Voltage Levels	Min	Typ	Max	Unit
V_{IL} input logic level low	-0.3	-	0.25 x VDD	V
V_{IH} input logic level high	0.625 x VDD	-	VDD + 0.3	V
$V_{SCHMITT}$ Schmitt voltage	0.25 x VDD	-	0.625 x VDD	V

Output Voltage Levels	Min	Typ	Max	Unit
V_{OL} output logic level low, I_{OL} = 4.0mA	0	-	0.125	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75 x VDD	-	VDD	V

Input and Tristate Currents	Min	Typ	Max	Unit
I_i input leakage current at V_{in} = VDD or 0V	-100	0	100	nA
I_{oz} tristate output leakage current at V_o = VDD or 0V	-100	0	100	nA
With strong pull-up	-100	-40	-10	µA
With strong pull-down	10	40	100	µA
With weak pull-up	-5	-1.0	-0.2	µA
With weak pull-down	-0.2	1.0	5.0	µA
C_I input capacitance	1.0	-	5.0	pF

Resistive Strength	Min	Typ	Max	Unit
R_{puw} weak pull-up strength at VDD - 0.2V	0.5	-	2	MΩ
R_{pdw} weak pull-down strength at 0.2V	0.5	-	2	MΩ
R_{pus} strong pull-up strength at VDD - 0.2V	10	-	50	kΩ
R_{pds} strong pull-down strength at 0.2V	10	-	50	kΩ

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13.3.8 Clocks

Clock Source	Min	Typ	Max	Unit
Crystal Oscillator				
Crystal frequency[a]	16	26	26	MHz
Digital trim range[b]	5.0	6.2	8.0	pF
Trim step size[b]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance[c]	870	1500	2400	Ω
External Clock				
Input frequency[d]	12	26	52	MHz
Clock input level[e]	0.4	-	VDD_ANA	V pk-pk
Edge jitter (allowable jitter), at zero crossing	-	-	15	ps rms
XTAL_IN input impedance	-	≥10	-	kΩ
XTAL_IN input capacitance	-	≤4	-	pF

[a] Integer multiple of 250kHz

[b] The difference between the internal capacitance at minimum and maximum settings of the internal digital trim

[c] XTAL frequency = 16MHz; XTAL C_0 = 0.75pF; XTAL load capacitance = 8.5pF

[d] Clock input can be any frequency between 12MHz to 52MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz

[e] Clock input can be either sinusoidal or square wave. If the peaks of the signal are below VSS or above VDD_ANA a DC blocking capacitor is required between the signal and XTAL_IN

13.3.9 LED Driver Pads

LED Driver Pads		Min	Typ	Max	Unit
Off current		-	1	2	µA
On resistance	V_{PAD} < 0.5V	-	20	33	Ω
On resistance, pad enabled by battery charger	V_{PAD} < 0.5V	-	20	50	Ω

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13.3.10 Mono Codec: Analogue to Digital Converter

Analogue to Digital Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	16	Bits
Input Sample Rate, F_{sample}	-		-	8	-	kHz
Signal to Noise Ratio, SNR	f_{in} = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 1% 150mV_{pk-pk} input	F_{sample}				
		8kHz	-	79	-	dB
Digital Gain	Digital Gain Resolution = 1/32		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		-	-	42	dB
Input full scale at maximum gain (differential)			-	4	-	mV rms
Input full scale at minimum gain (differential)			-	800	-	mV rms
3dB Bandwidth			-	20	-	kHz
Microphone mode input impedance			-	6.0	-	kΩ
THD+N (microphone input) @ 30mV rms input			-	0.04	-	%

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13.3.11 Stereo Codec: Digital to Analogue Converter

Digital to Analogue Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	16	Bits
Output Sample Rate, F_{sample}	-		8	-	48	kHz
Signal to Noise Ratio, SNR	f_{in} = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 0.01% 0dBFS signal Load = 100kΩ	F_{sample}				
		8kHz	-	95	-	dB
		11.025kHz	-	95	-	dB
		16kHz	-	95	-	dB
		22.050kHz	-	95	-	dB
		32kHz	-	95	-	dB
		44.1kHz	-	95	-	dB
		48kHz	-	95	-	dB
Digital Gain	Digital Gain Resolution = 1/32dB		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		0	-	-21	dB
Output voltage full-scale swing (differential)[(a)]			-	750	-	mV rms
Allowed Load		Resistive	-	16	O.C.	Ω
		Capacitive	-	-	500	pF
THD+N 100kΩ load			-	-	0.01	%
THD+N 16Ω load			-	-	0.1	%
SNR (Load = 16Ω, 0dBFS input relative to digital silence)			-	95	-	dB

[(a)] Any combination of gain (digital and / or analogue) and input signal which results in the output signal level exceeding the minimum or maximum signal level (analogue or digital) could result in distortion.

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13.3.12 Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Input voltage range[a]		0	-	VDD_ANA	V
Accuracy (Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%
Input bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate[b]		-	-	700	Samples/s

[a] LSB size = VDD_ANA/1023

[b] The auxiliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

13.4 ESD Precautions

BlueTunes ROM QFN is classified as a JESD22-A114 class 2 product. Apply ESD static handling precautions during manufacturing.

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14 HCI Power Consumption

DUT Role	Connection	Packet Type	Description	Average Current		Unit
				Low-voltage Linear Regulator	Switch-mode Regulator	
N/A	Deep Sleep	-	Host connection	0.07	0.07	mA
N/A	Page Scan	-	1280ms Interval	0.48	0.28	mA
N/A	Inquiry and Page Scan	-	Inquiry (1280ms interval) Page (1280ms interval)	0.85	0.49	mA
Master	ACL	DH1	No traffic	4.3	2.8	mA
Master	ACL	DH1	File transfer, TX	9.2	5.3	mA
Master	ACL	DH1	Sniff mode (40ms interval, 1 attempt)	2.2	1.4	mA
Master	ACL	DH1	Sniff mode (1280ms interval, 8 attempts)	0.20	0.14	mA
Master	SCO	HV1	-	39.8	22.3	mA
Master	SCO	HV3	-	22.2	12.4	mA
Master	SCO	HV3	Sniff mode (30ms interval, 1 attempt)	21.7	12.2	mA
Master	eSCO	EV3	-	22.3	12.4	mA
Master	eSCO	EV5	-	16.3	8.9	mA
Master	eSCO	EV3	Setting S1	23.7	13.3	mA
Master	eSCO	2EV3	Setting S2	22.8	12.6	mA
Master	eSCO	2EV3	Setting S3	16.7	9.3	mA
Master	eSCO	2EV3	Setting S3 with Sniff mode (100ms interval, 1 attempt)	15.7	8.7	mA
Slave	ACL	DH1	No Traffic	15.2	8.5	mA
Slave	ACL	DH1	File transfer, RX	17.2	9.3	mA
Slave	ACL	DH1	Sniff mode (40ms interval, 1 attempt)	1.9	1.2	mA
Slave	ACL	DH1	Sniff mode (1280ms interval, 8 attempts)	0.25	0.17	mA
Slave	SCO	HV1	-	39.9	22.3	mA
Slave	SCO	HV3	-	27.3	14.8	mA

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DUT Role	Connection	Packet Type	Description	Average Current		Unit
				Low-voltage Linear Regulator	Switch-mode Regulator	
Slave	SCO	HV3	Sniff mode (30ms interval, 1 attempt)	22.0	12.0	mA
Slave	eSCO	EV3	-	25.3	13.8	mA
Slave	eSCO	EV5	-	21.8	12.0	mA
Slave	eSCO	EV3	Setting S1	26.7	14.9	mA
Slave	eSCO	2EV3	Setting S2	26.8	15.0	mA
Slave	eSCO	2EV3	Setting S3	23.9	13.3	mA
Slave	eSCO	2EV3	Setting S3 with Sniff mode (100ms interval, 1 attempt)	16.5	9.2	mA

Note:

Current consumption values are taken with:

- VREGIN_L for low-voltage linear regulator = 1.8V
- BAT_P for switch-mode regulator = 3.7V
- Clock frequency = 16MHz
- UART baud rate is 115200
- QFN device

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15 CSR Green Semiconductor Products and RoHS Compliance

15.1 RoHS Statement

BlueTunes ROM QFN where explicitly stated in this Data Sheet meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the *Restriction of Hazardous Substance* (RoHS).

15.1.1 List of Restricted Materials

BlueTunes ROM QFN is compliant with RoHS in relation to the following substances:

- Cadmium
- Lead
- Mercury
- Hexavalent chromium
- Polybrominated Biphenyl
- Polybrominated Diphenyl Ether

In addition, the following substances are not intentionally added to BlueTunes ROM QFN devices:

- Halogenated flame retardant
- Antimony (Sb) and Compounds, including Antimony Trioxide flame retardant
- Polybrominated Diphenyl and Biphenyl Oxides
- Tetrabromobisphenol-A bis (2,3-dibromopropylether)
- Asbestos or Asbestos compounds
- Azo compounds
- Organic tin compounds
- Mirex
- Polychlorinated napthelenes
- Polychlorinated terphenyls
- Polychlorinated biphenyls
- Polychlorinated/Short chain chlorinated paraffins
- Polyvinyl Chloride (PVC) and PVC blends
- Formaldehyde
- Arsenic and compounds (except as a semiconductor dopant)
- Beryllium and its compounds
- Ethylene Glycol Monomethyl Ether or its acetate
- Ethylene Glycol Monoethyl Ether or its acetate
- Halogenated dioxins and furans
- Persistent Organic Pollutants (POP), including Perfluorooctane sulphonates
- Red phosphorous
- Ozone Depleting Chemicals (Class I and II): Chlorofluorocarbons (CFC) and Halons
- Radioactive substances

For further information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products.*

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16 BlueTunes ROM QFN Software Stack

BlueTunes ROM QFN is supplied with Bluetooth v2.1 + EDR specification compliant stack firmware, which runs on the internal RISC MCU.

The BlueTunes ROM QFN software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC MCU and an external host processor, if any. The upper layers of the Bluetooth stack, above the HCI, can be run either on-chip or on the host processor.

16.1 Stand-alone BlueTunes ROM QFN and Kalimba DSP Applications

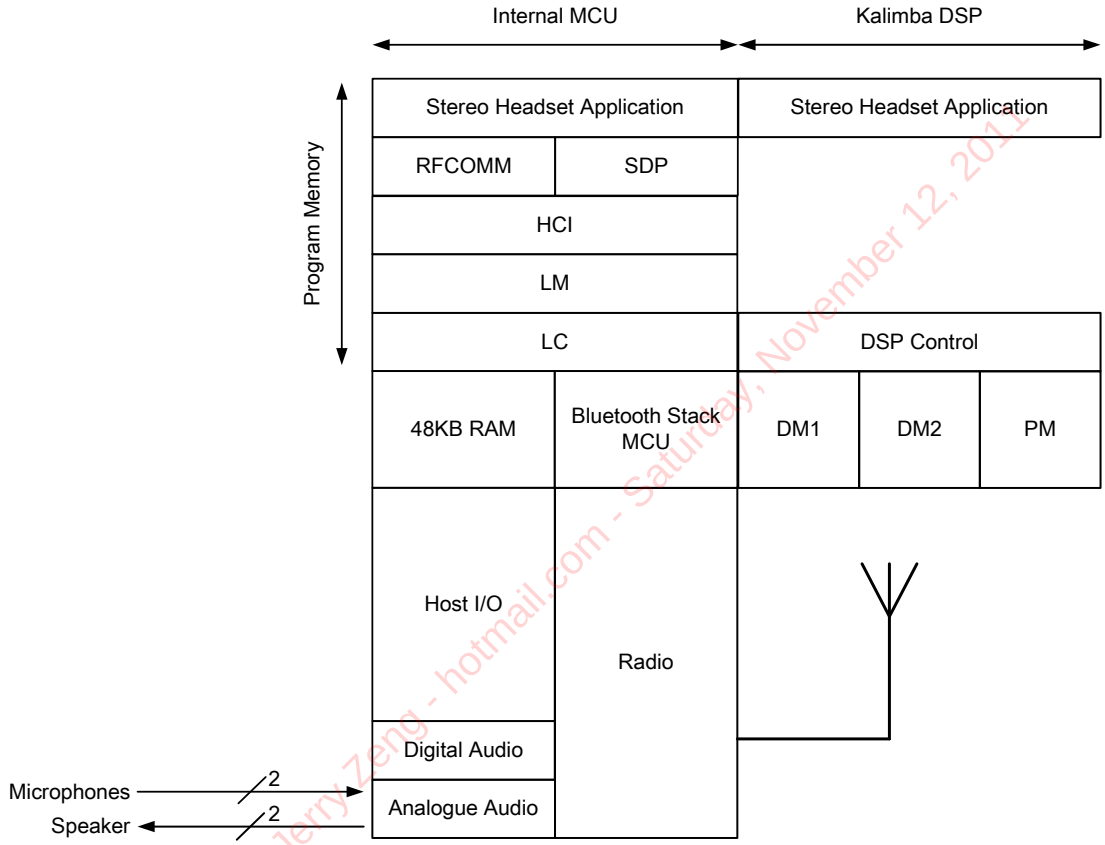

Figure 16.1: Stand-alone Application: BlueTunes ROM stereo headset solution

Note:

Program memory in Figure 16.1 is internal ROM.

Figure 16.1 shows how the BlueTunes ROM stereo headset solution is built on to the BlueTunes ROM QFN stack. The application requires no host processor, although it can use a host processor for debugging. All software layers, including the BlueTunes ROM stereo headset solution software, RFCOMM, HCI stack etc. run internally.

Section 16.2 describes the core functionality of the HCI stack available on the BlueTunes ROM QFN.

Section 16.3 describes the development tools for the BlueTunes ROM stereo headset solution.

Section 16.4 describes the features of the BlueTunes ROM stereo headset solution software. Some of these features are run as DSP application code in the DSP program memory RAM, e.g. cVc algorithm. This code executes alongside the main BlueTunes ROM QFN firmware.

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16.2 HCI Stack

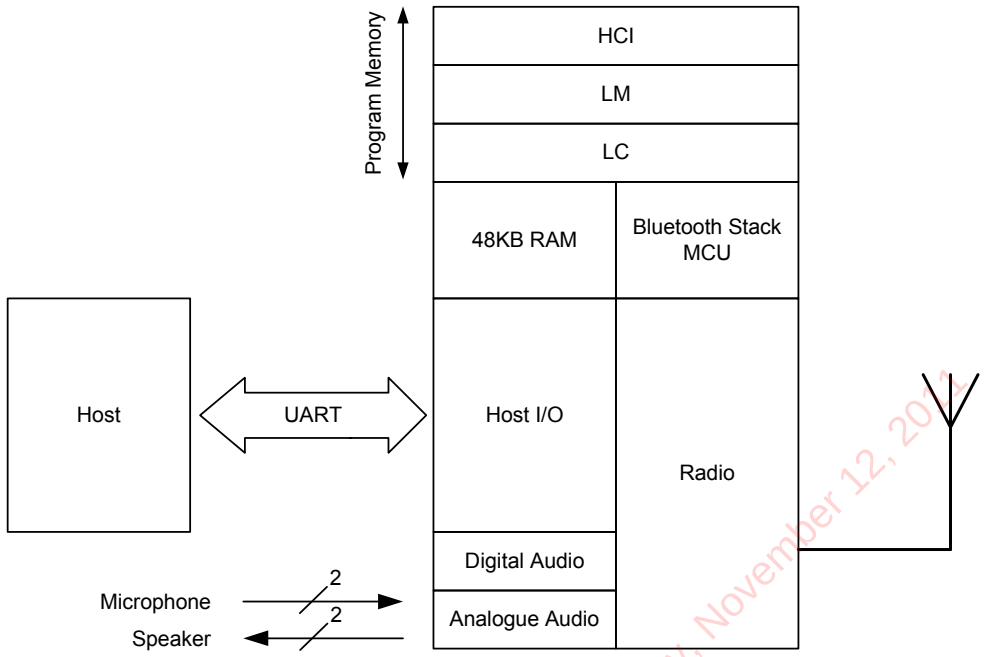

Figure 16.2: BlueCore HCI Stack

Note:

Program Memory in Figure 16.2 is internal ROM.

In the implementation shown in Figure 16.2 the internal processor runs the Bluetooth stack up to the HCI. The HCI stack is part of the overall application stack shown in Figure 16.1.

16.2.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

CSR supports the following Bluetooth v2.1 + EDR specification functionality:

- Secure simple pairing
- Sniff subrating
- Encryption pause resume
- Packet boundary flags
- Encryption
- Extended inquiry response

As well as the following mandatory functions of Bluetooth v2.0 + EDR specification:

- AFH, including classifier
- Faster connection: enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges

And optional Bluetooth v2.0 + EDR specification functionality:

- AFH as master and automatic channel classification
- Fast connect: interlaced inquiry and page scan plus RSSI during inquiry
- eSCO, eV3 + CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware was written against the Bluetooth v2.1 + EDR specification:

- Bluetooth components:

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  - Baseband including LC
  - LM
  - HCI
- Standard UART HCI Transport Layers
- All standard Bluetooth radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps
- Operation with up to 7 active slaves (this is the maximum Bluetooth v2.1 + EDR specification allows)
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7
- Maximum number of simultaneous active SCO connections: 3 (BlueTunes ROM QFN supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.1 + EDR specification)
- Operation with up to 3 SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers' transmit power via LMP
- Master/slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

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16.2.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BCSP, a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Supports H4DS, a proprietary alternative to the standard Bluetooth UART Host Transport, supporting deep sleep for low-power applications
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BCCMD, provides:
  - Access to BlueTunes ROM QFN general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware random number generator
  - Controls to set the default and maximum transmit powers; these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Bluetooth radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- A block of BCCMD commands provides access to the BlueTunes ROM QFN persistent store configuration database . The database sets the BlueTunes ROM QFN Bluetooth address, Class of Device, Bluetooth radio (transmit class) configuration, SCO routing, LM, etc.
- A UART break condition is used in 3 ways:
  - Presenting a UART break condition to the chip forcing the chip to perform a hardware reboot
  - Presenting a break condition at boot time holding the chip in a low power state, preventing normal initialisation while the condition exists
  - With BCSP, sends a break to the host before sending data, when the firmware can be configured. (This is normally used to wake the host from a deep sleep state.)
- A block of Bluetooth radio test or BIST commands allows direct control of the BlueTunes ROM QFN radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Hardware low power modes: shallow sleep and deep sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP).

Note:

Always refer to the Firmware Release Note for the specific functionality of a particular build.

16.3 BlueTunes ROM stereo headset solution Development Kit, BTN-003-1A

CSR's BlueTunes ROM stereo headset solution development kit for BlueTunes ROM QFN, order code BTN-003-1A, includes a headset demonstrator board, form-factor representative example design, audio adapter, music and voice dongle and necessary interface adapters and cables. In conjunction with the BlueTunes Configurator tool and other supporting utilities the development kit provides the best environment for designing a stereo headset solution with BlueTunes ROM QFN.

16.4 BlueTunes ROM QFN Stereo Headset ROM Software, BC57F687A05

- BlueTunes ROM QFN integrates a stereo audio codec and powerful DSP that enables SBC and MP3 decode, and a configurable 5-band EQ
- The headset supports A2DP1.2 and AVRCP1.0 profiles enabled with SBC encoder for streaming audio over Bluetooth and for remote control functionality
- The headset supports MP3 decoder for improved audio quality and 5-band EQ audio for better user experience
- The headset supports HFP1.5 and HSP1.0. Advanced features in these specifications are supported, including 3-way calling.
- Bluetooth v2.1 + EDR specification is supported in the ROM software including Secure Simple Pairing, greatly simplifying the pairing process.
- BlueTunes ROM QFN includes as standard cVc dual and single microphone algorithms for echo and noise suppression.
- cVc dual-microphone algorithm can provide >30dB of noise suppression in both stationary and dynamic noise conditions such as; babble, road, music and competing voices. In addition an acoustic echo canceller is now integrated into the cVc dual-microphone solution, further enhancing the far-end user experience.
- A licence key, provided as standard, is required to enable the dual-microphone algorithm.

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- A cVc single-microphone algorithmn provides full-duplex echo cancellation and a 10dB stationary noise suppressor.
- The cVc algorithm's are configured for different headset plastics using the Universal Parameter Manager tool.
- For more information see www.csrsupport.com/cvc
- Configure most headset features on the BlueTunes ROM QFN using the BlueTunes Configurator tool available from www.csrsupport.com/StereoHeadsetSolutions. The tool can be used to read and write headset configurations directly to the EEPROM or alternatively to a PSR file. Configurable headset features include:
  - Bluetooth v2.1 + EDR specification features
  - Reconnection policies, e.g. reconnect on power on
  - Audio features, including default volumes
  - 5-band EQ audio enhancements
  - Button events: configuring button presses and durations for certain events, e.g. double press on PIO[1] for Last Number redial
  - LED indications for states, e.g. headset connected, and events, such as power on
  - Indication tones for events and ringtones
  - Battery divider ratios and thresholds, e.g. thresholds for battery low indication, full battery etc.
  - The headset includes the FastStream, CSR's low latency codec which reduces the latency of the audio link (from source to sink) significantly to avoid lip-sync issues when listening to audio and watching video images at the same time.
- The ROM software has undergone extensive interoperability testing to ensure that it will work with the majority of phones on the market

Note:

Access to www.csrsupport.com/cvc and www.csrsupport.com/StereoHeadsetSolutions require appropriate access privileges. For more information contact a CSR representative, email sales@csr.com or go to www.csr.com/contacts.

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17 Ordering Information

Device	Package			Order Number
	Type	Size	Shipment Method	
BlueTunes ROM QFN CVC 1-mic	QFN 68-lead (Pb free)	8 x 8 x 0.9mm, 0.4mm pitch	Tape and Reel	BC57F687A05-IQF-E4
BlueTunes ROM QFN CVC 2-mic	QFN 68-lead (Pb free)	8 x 8 x 0.9mm, 0.4mm pitch	Tape and Reel	BS-BC5A05IQF-CVC-2MR3

Note:

MP3 decode functionality requires an appropriate licence from Thomson, see Section 17.1.

BlueTunes ROM QFN is a ROM-based device where the product code has the form BC57F687Axx. xx is the specific ROM-variant, 05 is the ROM-variant for BlueTunes ROM Stereo Headset Solution.

Minimum order quantity is 2kpcs taped and reeled.

To contact a CSR representative, email sales@csr.com or go to www.csr.com/contacts

17.1 MP3 Licence Statement

Supply of the BlueTunes ROM QFN does not convey a licence under the relevant intellectual property of Thomson and/or Fraunhofer Gesellschaft nor imply any right to use this product in any finished end user or ready-to-use final product. An independent licence for such use is required. For details, please visit http://www.mp3licensing.com.

17.2 Development Kit Ordering Information

Description	Order Number
BlueTunes ROM Stereo Headset Solution Development Kit, including headset example design	BTN-003-1A

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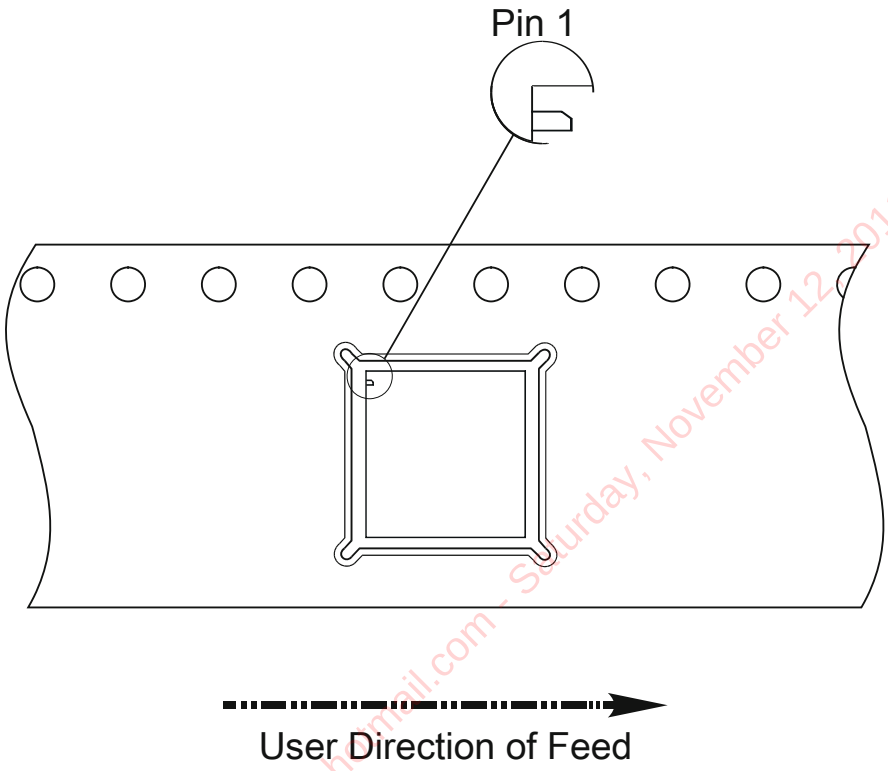
18 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

18.1 Tape Orientation

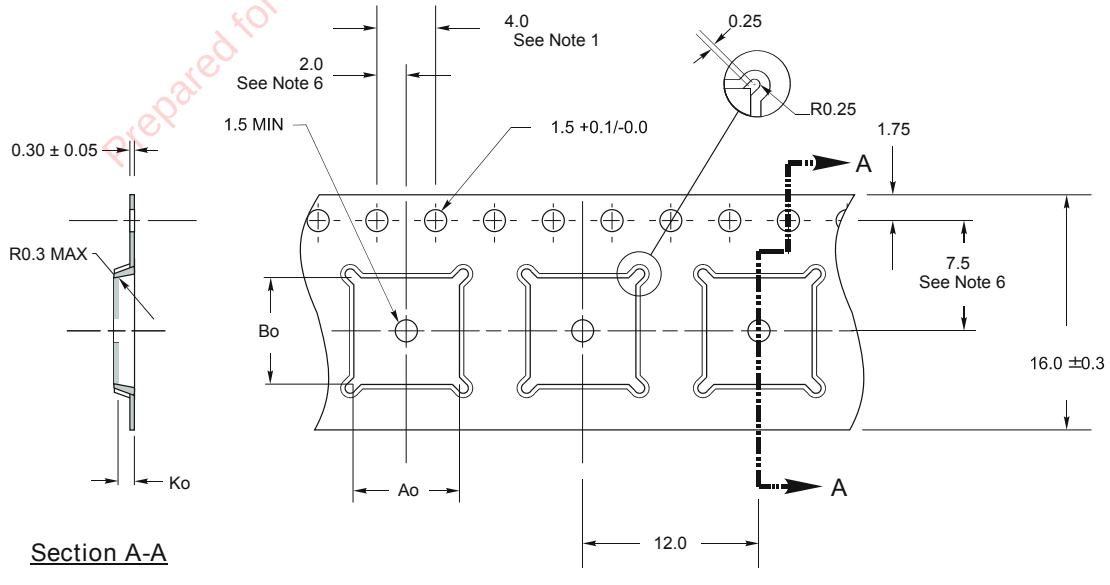
Figure 18.1 shows the BlueTunes ROM QFN packing tape orientation.



G-TW-0002812.2.2

Figure 18.1: BlueTunes ROM QFN Tape Orientation

18.2 Tape Dimensions



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A_0	B_0	K_0	Unit	Notes
8.30	8.30	1.10	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.2 2. Camber not to exceed 1mm in 100mm 3. Material: PS + C 4. A_0 and B_0 measured as indicated 5. K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier 6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

18.3 Reel Information

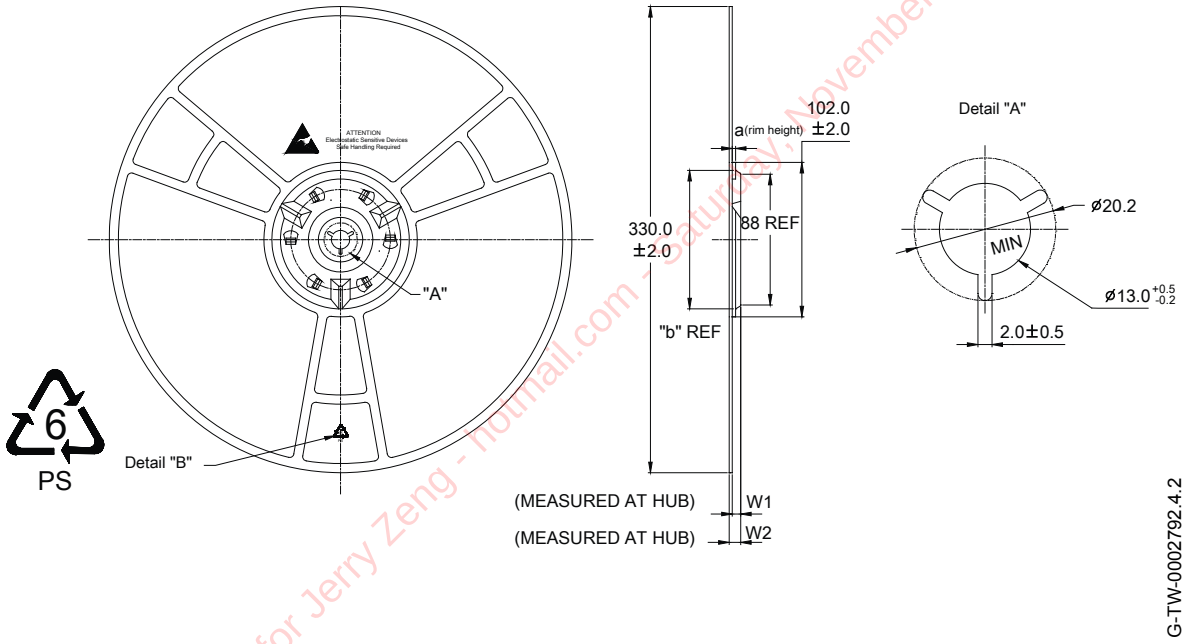

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Figure 18.2: Reel Dimensions

Package Type	Nominal Hub Width (Tape Width)	a	b	W1	W2 Max	Units
8 x 8 x 0.9mm QFN	16	4.5	98.0	16.4 (3.0/-0.2)	19.1	mm

18.4 Moisture Sensitivity Level

BlueTunes ROM QFN is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

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19 Document References

Document	Reference, Date
BlueCore5 Charger Description and Calibration Procedure Application Note	CS-113282-ANP, 2007
BlueCore5-Multimedia External Recommendations for ESD Protection	CS-114058-ANP, 2007
Bluetooth and IEEE 802.11 b/g Co-existence Solutions Overview	bcore-an-066P, 2005
BlueTunes ROM QFN Performance Specification	CS-122327-SPP, 2009
Core Specification of the Bluetooth System	v2.1 + EDR, 2007
IC Packing and Labelling Specification	CS-112584-SPP, 2007
Moisture / Reflow Sensitivity Classification for Nonhermitic Solid State Surface Mount Devices	IPC / JEDEC J-STD-020
Optimising BlueCore5-Multimedia ADC Performance Application Note	CS-120059-AN, 2008
Selection of I^2C EEPROMS for Use with BlueCore	bcore-an-008P, 2003
Test Suite Structure (TSS) and Test Purposes (TP) System Specification 1.2/2.0/2.0 + EDR/ 2.1/2.1 + EDR	RF.TS/2.1.E.0, 2006
Typical Solder Reflow Profile for Lead-free Devices	CS-116434-ANP, 2007

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Terms and Definitions

Term	Definition
8DPSK	8-phase Differential Phase Shift Keying
π/4 DQPSK	π/4 rotated Differential Quaternary Phase Shift Keying
μ-law	Audio companding standard (G.711)
A-law	Audio companding standard (G.711)
A2DP	Advanced Audio Distribution Profile
AC	Alternating Current
ACL	Asynchronous Connection-oriented
ADC	Analogue to Digital Converter
ADPCM	Adaptive Differential Pulse Code Modulation (e.g G.726)
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
AIO	Analogue Input/Output
ALU	Arithmetic logic unit
AuriStream	CSR proprietary ADPCM codec
AVRCP	Audio/Video Remote Control Profile
BCCMD	BlueCore Command
BCSP	BlueCore Serial Protocol
BIST	Built-In Self-Test
BlueCore®	Group term for CSR's range of Bluetooth wireless technology ICs
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
BOM	Bill of Materials
CFC	Chlorofluorocarbon
codec	Coder decoder
CRC	Cyclic Redundancy Check
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVC	Clear Voice Capture
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
DC	Direct Current
DNL	Differential Non Linearity (ADC accuracy parameter)
DSP	Digital Signal Processor
DUT	Device Under Test
e.g.	*exempli gratia*, for example
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
EQ	EQualiser
eSCO	Extended SCO
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance

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Term	Definition
etc	*et cetera*, and the rest, and so forth
FEC	Forward Error Correction
FET	Field Effect Transistor
FHS	Frequency Hop Synchronisation
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
GSM	Global System for Mobile communications
H4DS	H4 Deep Sleep
HCI	Host Controller Interface
HEC	Header Error Check Correction
HFP	Hands-Free Profile
HSP	HeadSet Profile
I²C	Inter-Integrated Circuit Interface
I/O	Input/Output
IC	Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Response (filter)
INL	Integral Non Linearity (ADC accuracy parameter)
IQ	In-Phase and Quadrature
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
Kalimba	An open platform DSP co-processor, enabling support of enhanced audio applications, such as echo and noise suppression, and file compression / decompression
KB	Kilobyte
LC	An inductor (L) and capacitor (C) network
LC	Link Controller
LDO	Low (voltage) Drop-Out
LED	Light-Emitting Diode
LM	Link Manager
LMP	Link Manager Protocol
LNA	Low Noise Amplifier
LSB	Least-Significant Bit (or Byte)
MAC	Medium Access Control
MAC	Multiplier and ACcumulator
Mbps	Megabits per second
MCU	MicroController Unit
MIPS	Million Instructions Per Second
MISO	Master In Slave Out
MMU	Memory Management Unit
MP3	MPEG-1 audio layer 3
N/A	Not Applicable
NC	Not Connect
NSMD	Non Solder Mask Defined
O.C.	Open Circuit

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Term	Definition
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PIO	Programmable Input/Output
plc	Public Limited Company
POP	Persistent Organic Pollutants
ppm	parts per million
PS Key	Persistent Store Key
PSRR	Power Supply Rejection Ratio
PVC	Poly Vinyl Chloride
QFN	Quad-Flat No-lead
RAM	Random Access Memory
RC	Resistor Capacitor
RF	Radio Frequency
RFCOMM	Radio Frequency COMMunication. Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RTS	Request To Send
RX	Receive or Receiver
SBC	Sub-band Coding
SCO	Synchronous Connection-Oriented
SIG	(Bluetooth) Special Interest Group
SMPS	Switch Mode Power Supply
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
TCXO	Temperature Controlled crystal Oscillator
THD+N	Total Harmonic Distortion and Noise
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
VCO	Voltage Controlled Oscillator
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access

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