U A H

CPE/EE 421
Microcomputers

WEEK #10

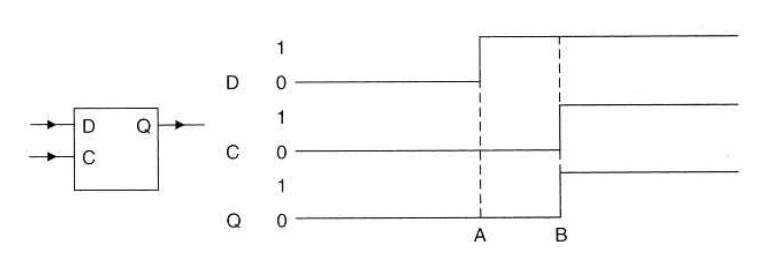
U A H

Interpreting the Timing Diagram

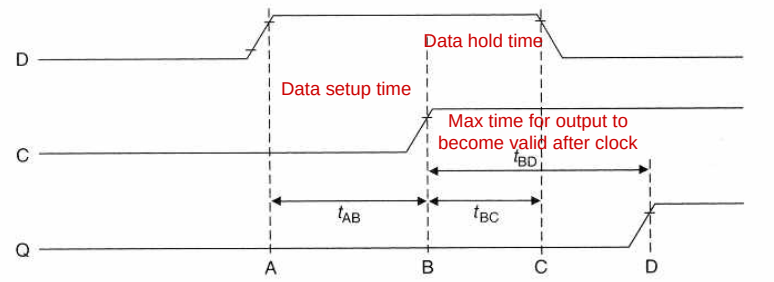
The 68000 Read Cycle

Timing Diagram of a Simple Flip-Flop

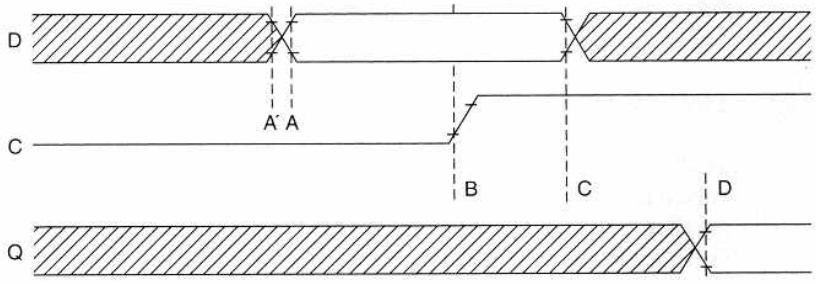
Idealized form of the timing diagram



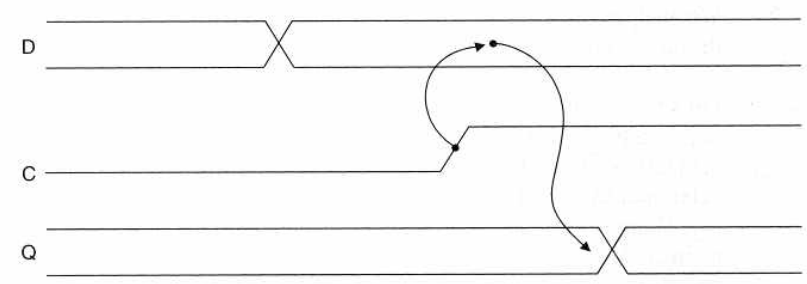
Actual behavior of a D flip-flop



General form of the timing diagram

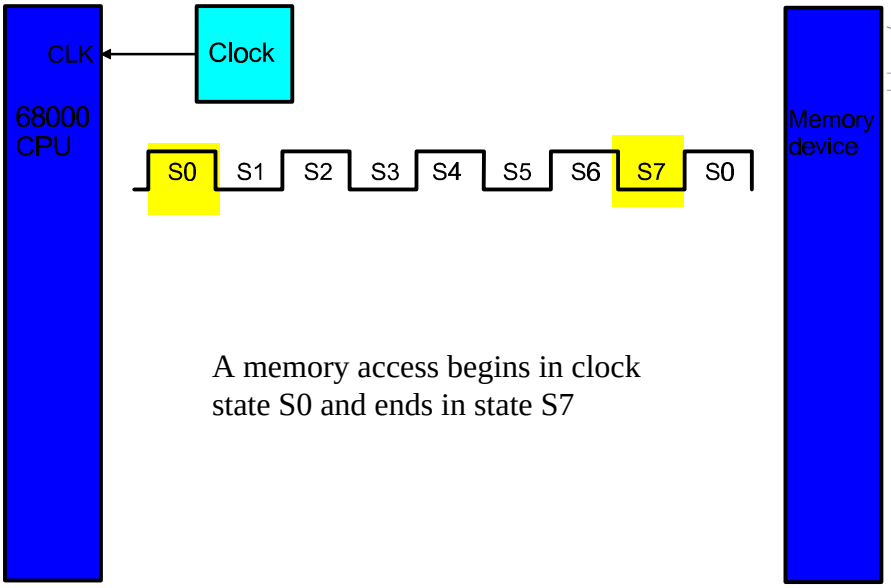


An alternative form of the timing diagram

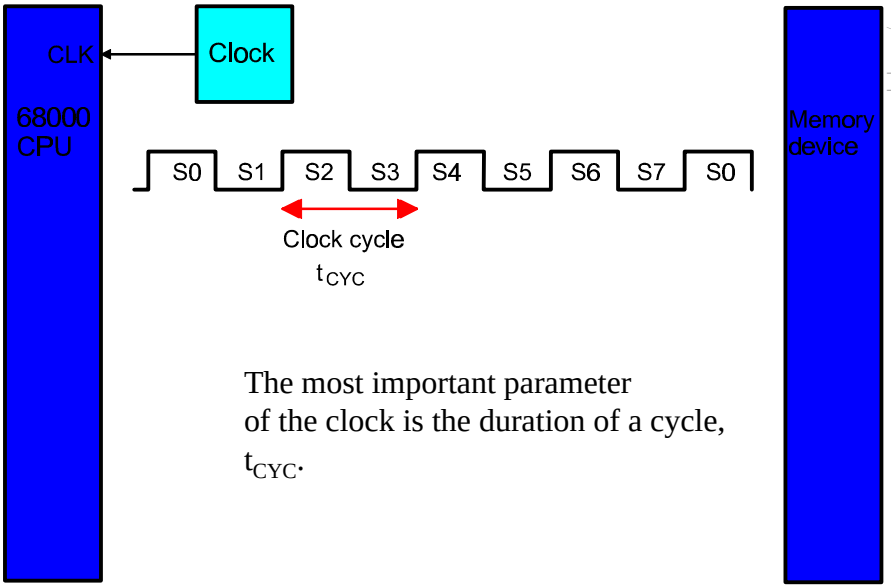


The Clock

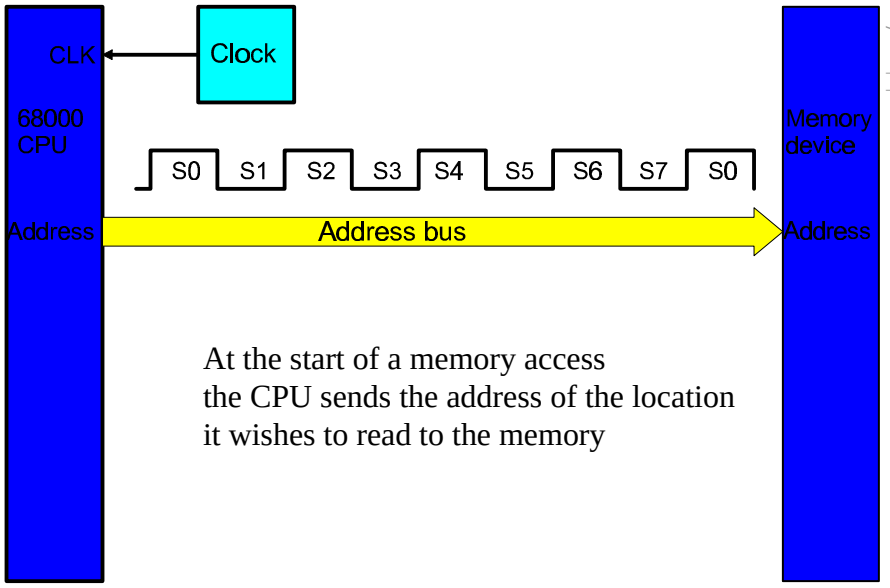
- A microprocessor requires a clock that provides a stream of timing pulses to control its internal operations
- A 68000 memory access takes a minimum of eight clock states numbered from clock state S0 to clock state S7



A memory access begins in clock state S0 and ends in state S7



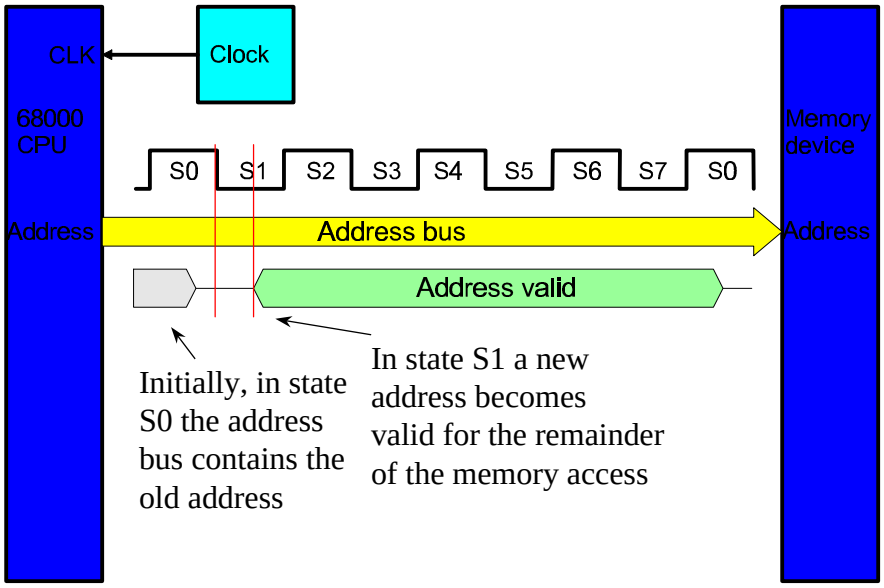
The most important parameter of the clock is the duration of a cycle, t_{CYC}.

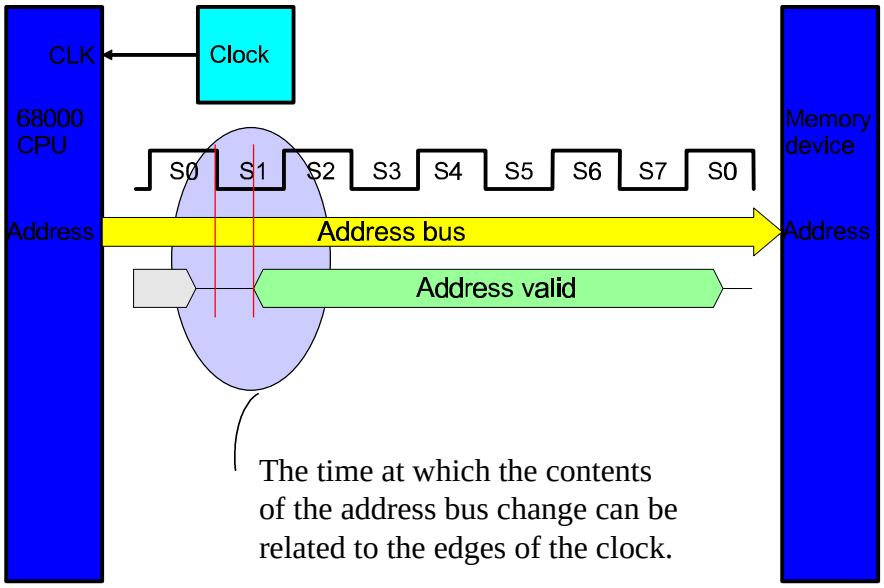


At the start of a memory access the CPU sends the address of the location it wishes to read to the memory

Address Timing

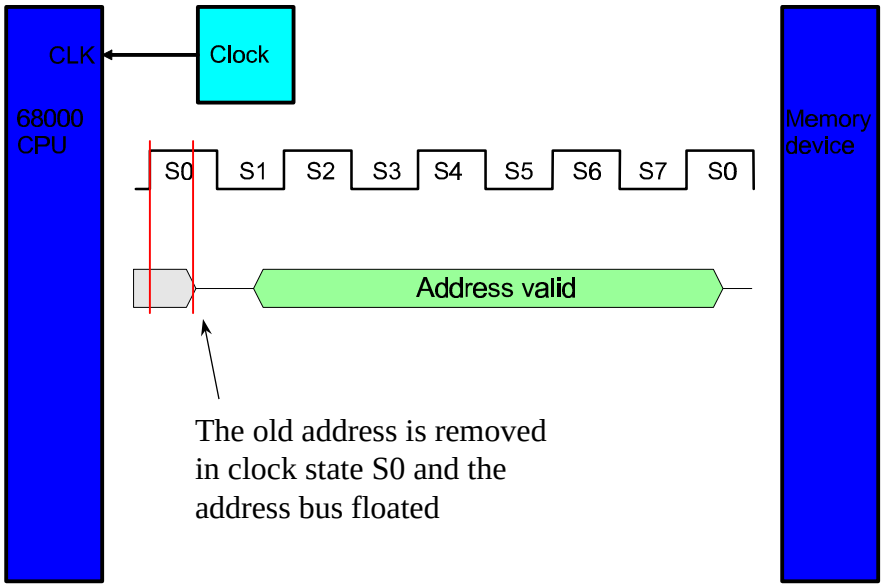
- We are interested in when the 68000 generates a new address for use in the current memory access
- The next slide shows the relationship between the new address and the state of the 68000's clock



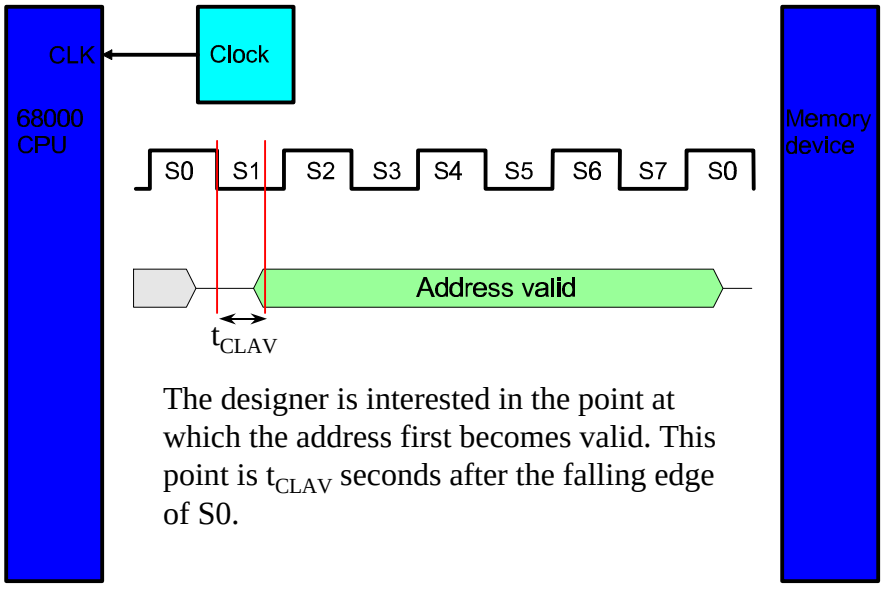


Address Timing

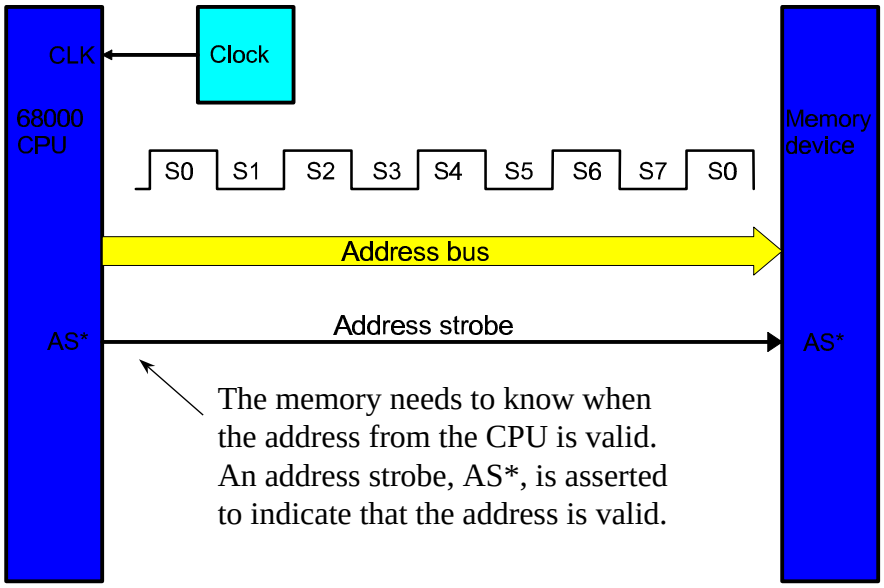
- Let's look at the sequence of events that govern the timing of the address bus
- The "old" address is removed in state S0
- The address bus is floated for a short time, and the CPU puts out a new address in state S1



The old address is removed in clock state S0 and the address bus floated

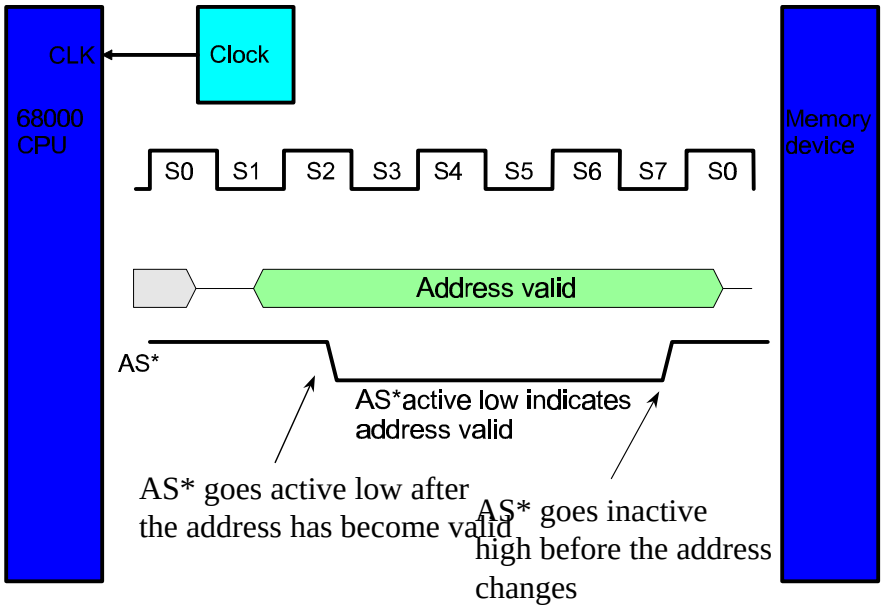


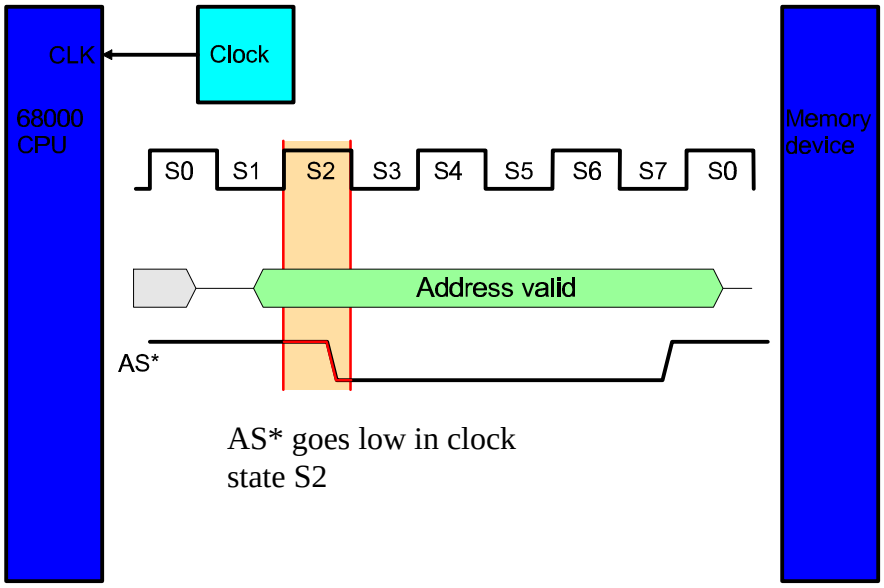
The designer is interested in the point at which the address first becomes valid. This point is t_{CLAV} seconds after the falling edge of S0.



Address and Address Strobe

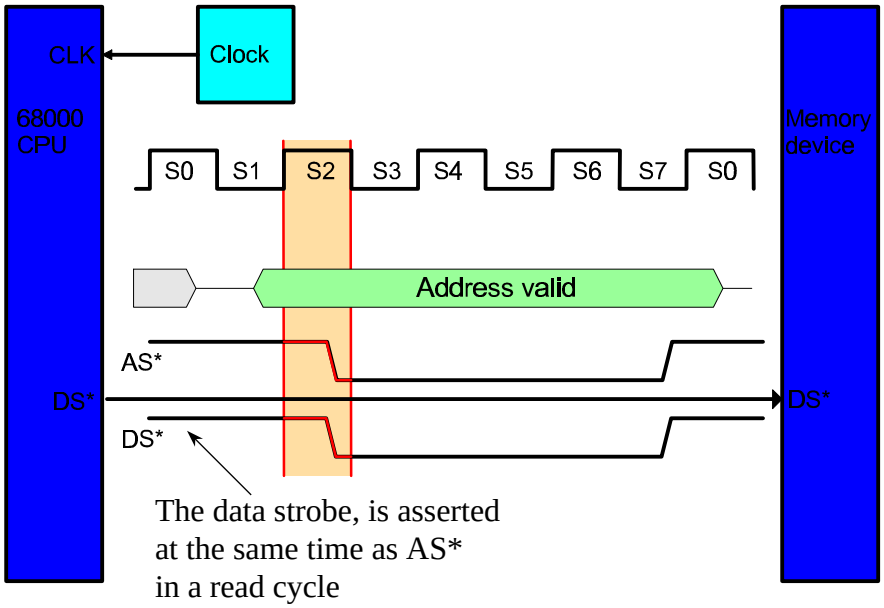
- We are interested in the relationship between the time at which the address is valid and the time at which the address strobe, AS*, is asserted
- When AS* is *active-low* it indicates that the address is valid
- We now look at the timing of the clock, the address, and the address strobe


CLK
Clock
68000
CPU
Memory
device
S0
S1
S2
S3
S4
S5
S6
S7
S0
Address valid
AS*
AS*active low indicates
address valid
AS* goes active low after
the address has become valid
AS* goes inactive
high before the address
changes


CLK
Clock
68000
CPU
Memory
device
S0
S1
S2
S3
S4
S5
S6
S7
S0
Address valid
AS*
AS* goes low in clock
state S2

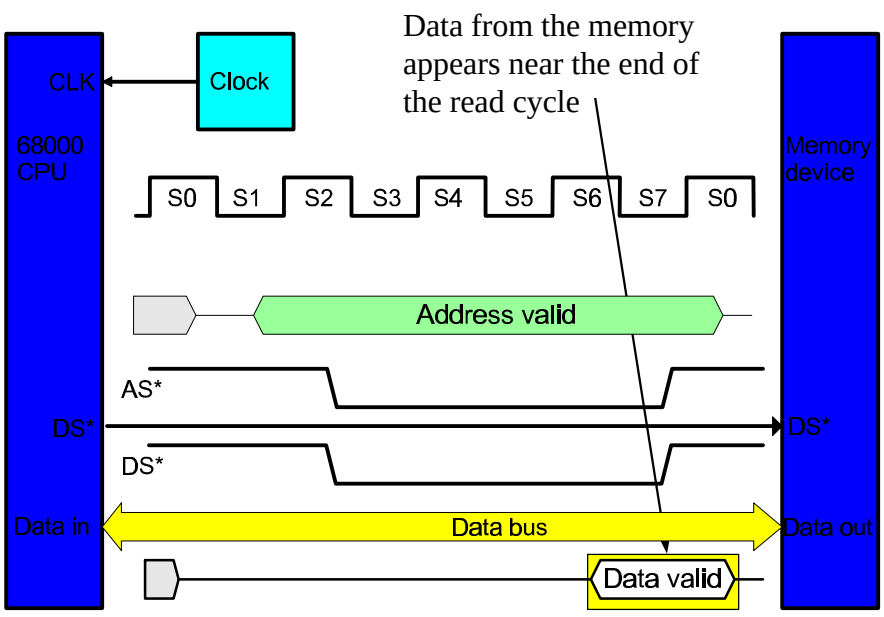
The Data Strobes

- The 68000 has two data strobes LDS* and UDS*. These select the lower byte or the upper byte of a word during a memory access
- To keep things simple, we will use a single data strobe, DS*
- The timing of DS* in a read cycle is the same as the address strobe, AS*



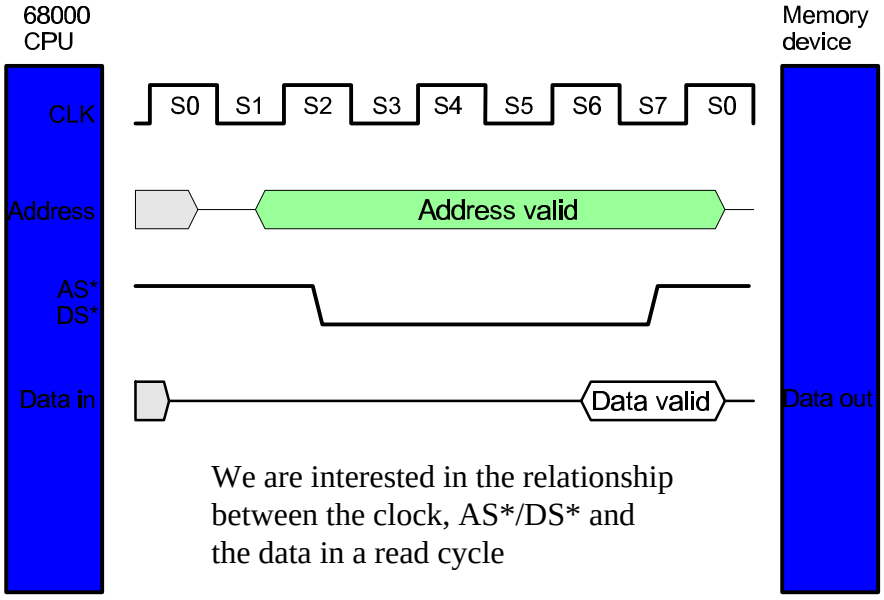
The Data Bus

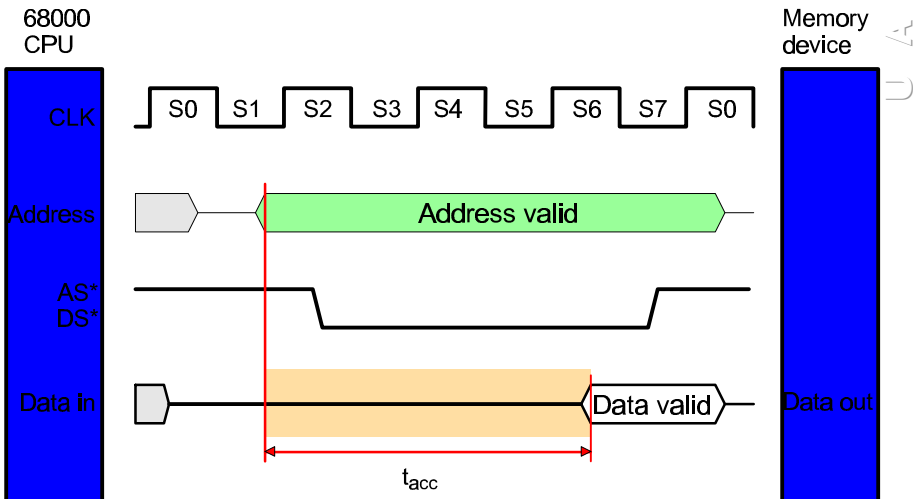
- During a read cycle the memory provides the CPU with data
- The next slide shows the data bus and the timing of the data signal
- Note that valid data does not appear on the data bus until near the end of the read cycle



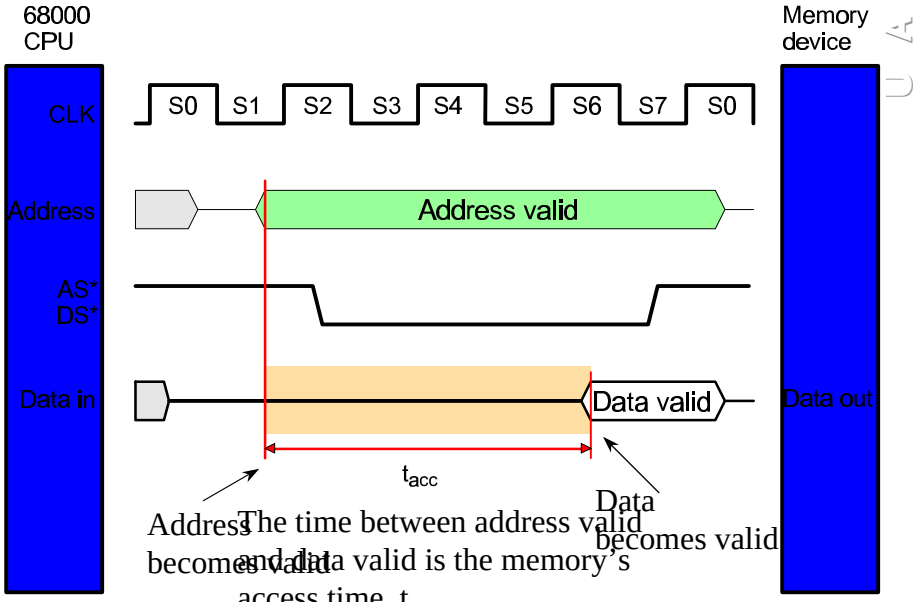
Analyzing the Timing Diagram

- We are going to redraw the timing diagram to remove clutter
- We aren't interested in the signal paths themselves, only in the relationship between the signals





The earliest time at which the memory can begin to access data is measured from the point at which the address is first valid



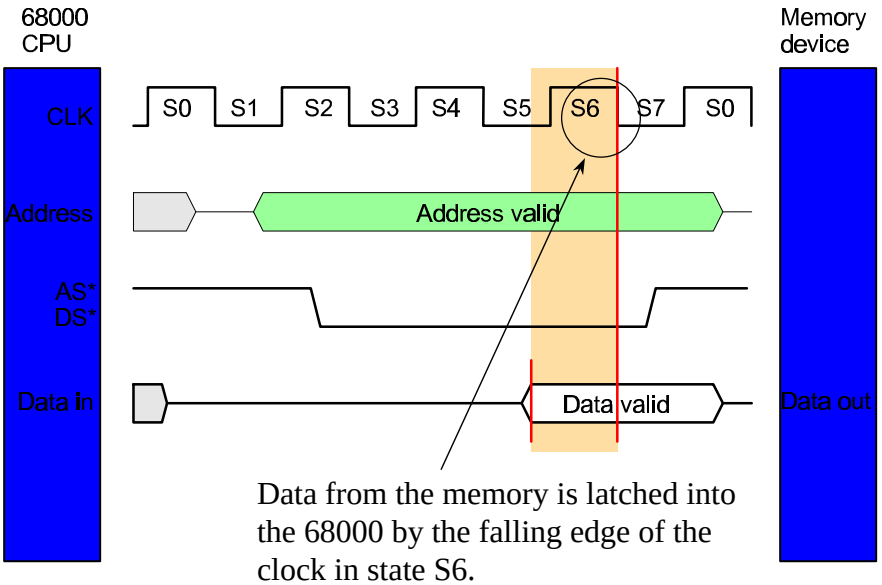
Address becomes valid

The time between address valid and data valid is the memory's access time, t_{acc}

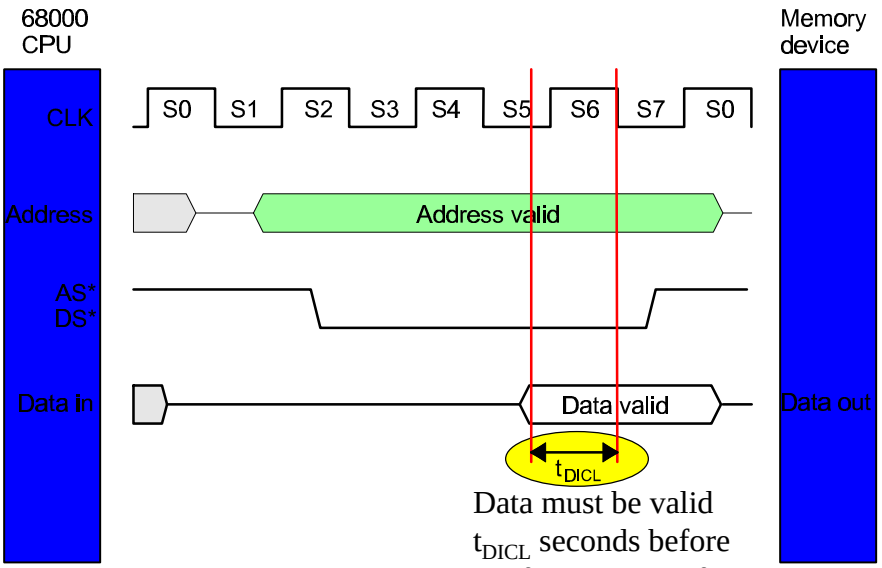
Data becomes valid

Calculating the Access Time

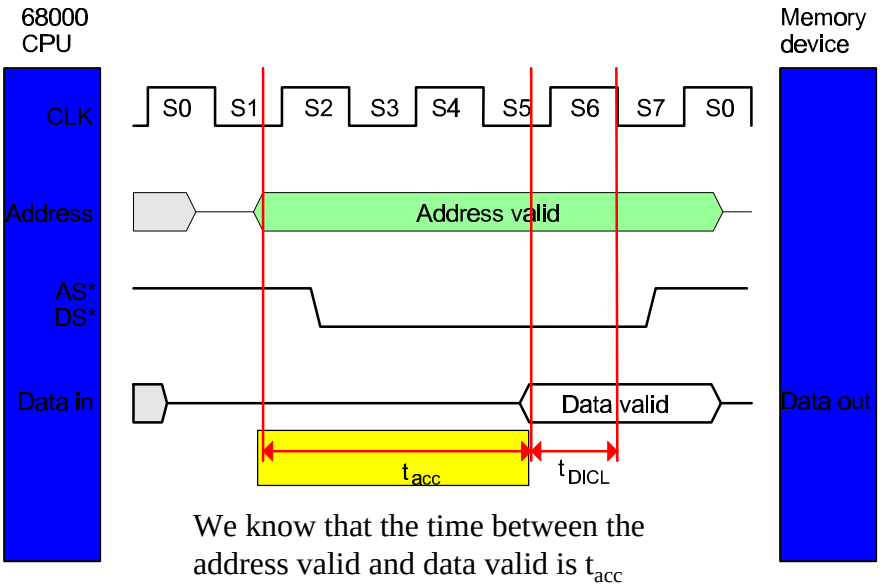
- We need to calculate the memory's access time
- By knowing the access time, we can use the appropriate memory component
- Equally, if we select a given memory component, we can calculate whether its access time is adequate for a particular system



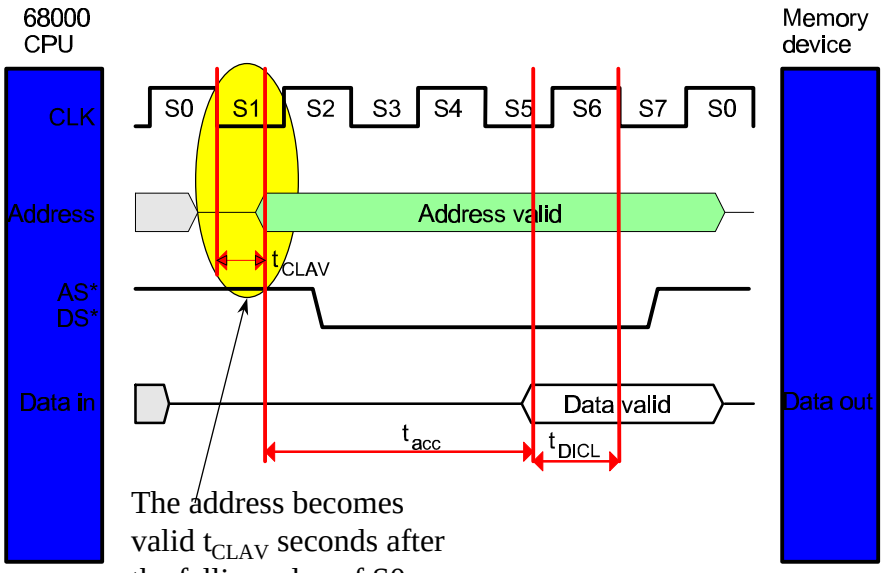
Data from the memory is latched into the 68000 by the falling edge of the clock in state S6.



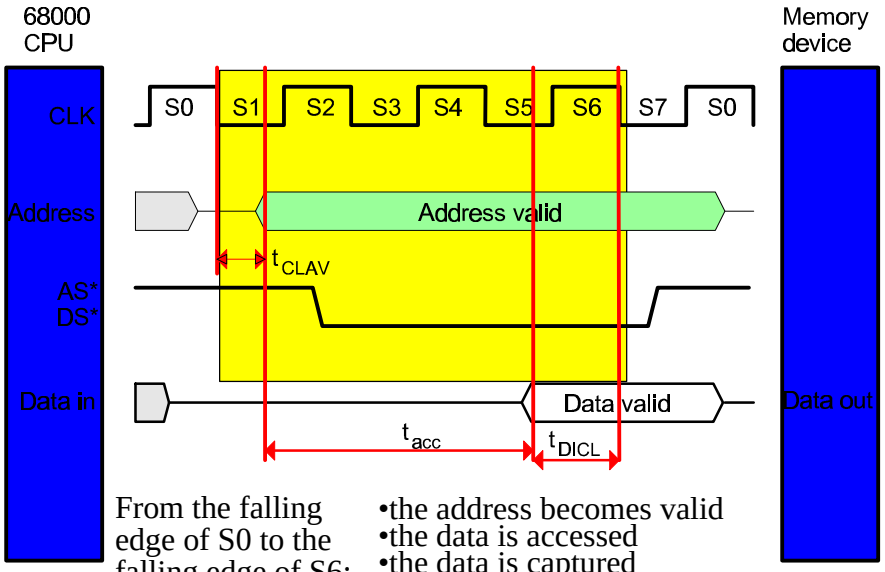
Data must be valid t_{DICL} seconds before the falling edge of S6



We know that the time between the address valid and data valid is t_{acc}

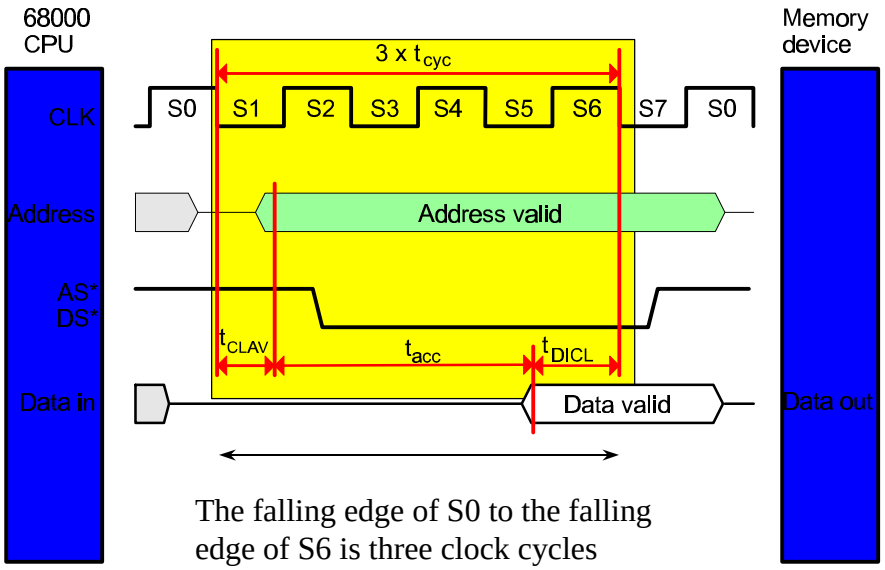


The address becomes valid t_{CLAV} seconds after the falling edge of S0

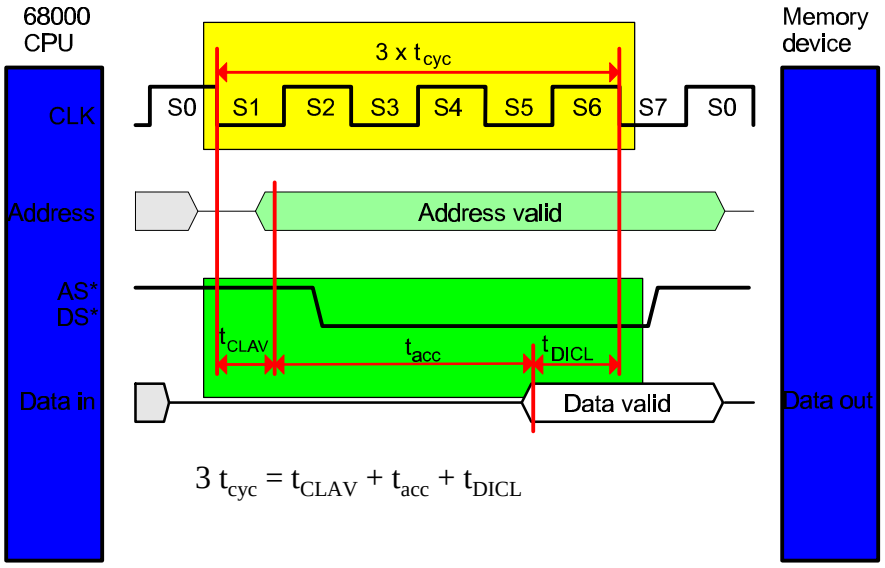


From the falling edge of S0 to the falling edge of S6:

- the address becomes valid
- the data is accessed
- the data is captured



The falling edge of S0 to the falling edge of S6 is three clock cycles



$3\ t_{cyc} = t_{CLAV} + t_{acc} + t_{DICL}$

Timing Example

- 68000 clock 8 MHz t_{CYC} = 125 ns
- 68000 CPU t_{CLAV} = 70 ns
- 68000 CPU t_{DICL} = 15 ns
- What is the minimum t_{acc}?
- 3 $t_{CYC} = t_{CLAV} + t_{acc} + t_{DICL}$
- 375 = 70 + t_{acc} + 15
- t_{acc} = 290 ns