# HD Starlight Sensor

## FEATURES

- Best-in-class low-light performance
- True single exposure wide dynamic range operation (25000:1) to avoid motion artifacts
- Type 1/1.2-inch CMOS sensor
- Support both Rolling Shutter mode and Global Shutter mode
- High resolution imaging array: 1920(H) x 1080(V)
- Up to 100 fps @1080P in Rolling Shutter mode and 50 fps in Global Shutter mode
- Low noise: 1.2 e- RMS @ 30 fps in Rolling Shutter mode, 6.5 e- RMS @ 30 fps in Global Shutter mode
- 6.5μm by 6.5μm 5T active pixels
- Peak quantum efficiency > 50% at 600nm
- Protection against black-sun artifacts
- Low power consumption ( <0.4 W @ 30 fps)

## APPLICATIONS

- Video surveillance that demands low light performance as well as motion artifacts free high dynamic range imaging

## DESCRIPTION

Vimicro's VC0201 is a high resolution, low-noise CMOS image sensor intended for video surveillance requiring high frame rate operation as well as high dynamic range capability at very low light levels. The device features an array of 5T pixels on a 6.5 μm pitch with an active imaging area of 1920(H) x 1080(V) pixels with support for both Rolling Shutter and Global Shutter readout modes. The sensor supports user-programmable row and column start/stop control in region of interest (ROI) readout mode. The sensor supports full frame readout up to 100 fps in Rolling Shutter mode and 50 fps in Global Shutter mode.

## General

| Parameter | Typical value |
|---|---|
| Active array size | 2048 (H) x 1144 (V) |
| Pixel size | 6.5 μm x 6.5 μm |
| Dimensions of active area | 13311.6 microns (H) x 7435.6 microns (V) |
| Dimensions of die | 15675 microns (H) x 14829.8 microns (V) |
| Distance from die center to center of active area | 3187.68 microns |
| Shutter type | Rolling Shutter, Global Shutter (snapshot). ROI readout capabilities for both shutter types. |
| Maximum frame rate | 100 fps (Rolling Shutter) (@ 283MHz clock rate) 50 fps (Global Shutter) |
| Number of readout ports | 1 |
| Maximum line rate | 114kHz (8.7 μs/line) |
| Maximum pixel rate | 234 MHz (3.5ns/pixel, and 2048 pixels/line, + ADC dead time) |
| ADC resolution | 2 x 11-bit |
| Column level amplifier gain | 1x or 2x (low gain output) 10x or 30x (high gain output) |
| Power consumption | 0.8W dual channel @100fps, 0.3W in Low-Gain only @50fps |
| I/O interface | 1.8V LVCMOS and 1.8V HSTL |

## Electrical-optical Specifications

| Parameter | Specification | Notes |
|---|---|---|
| Intra-frame dynamic range | 30000:1.2 => 25000:1 | |
| PRNU | < 3% RMS | at 75% of max output |
| Dark current | < 35 e-/pixel/sec | at 20ºC |
| Dark current non-uniformity | < 65 e-/pixel/sec RMS | at 20ºC |
| Fixed pattern noise (FPN) | < 2% RMS uncorrected | of the max output |
| Conversion gain (DN/e-) | High gain output − 1.7 at 30x − 0.55 at 10x Low gain output − 0.12 at 2x − 0.055 at 1x | w/1.4V ADC input range (ADC input range is user programmable from 0.8V to 2V) (30x: 1.3DN/e- w/1.85V ADC default input range) |
| Full well capacity (FWC) | > 30,000 e- | |
| Lag | < 0.1% | of maximum output |
| Non-linearity | < 1% | |
| Fill factor with microlens | > 0.9 | |
| Microlens F-number | 1.5 | |
| Peak QE | > 0.50 | at 600nm |
| MTF | > 0.4 | at 600nm |
| Temporal read noise | < 1.2 e- RMS @ 50 fps Rolling Shutter readout, @T=30ºC | Median value of read noise distribution from high gain output (30x gain) |
| Spectral sensitivity range | 400 – 700nm | See QE plots for spectral sensitivity in the Near IR out to 1100 nm |

## Recommended Operating Condition

| Parameter | Definition | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| AVDD | Analog circuits power supply (avg 90 mA, Peak at 170mA on 5% duty cycle) | 3.135 | 3.3 | 3.465 | V |
| AVDD_PIX | Pixel source follower power supply (10 mA avg) | 3.135 | 3.3 | 3.465 | V |
| AVDD_RST1 | Pixel reset power supply1 (1mA) | 2.50 | 3.00 (RS) or 2.77 (GS) | 3.3 | V |
| AVDD_RST2 | Pixel reset power supply2 (1mA) | 2.50 | 3.0 | 3.3 | V |
| DVDD | Digital circuits power supply (160mA) | 1.71 | 1.8 | 1.89 | V |
| DVDD_IO | I/O circuits power supply (65 mA) (with no terminations on outputs) | 1.71 | 1.8 | 1.89 | V |
| VTX1_POS | TX1 Transfer gate positive power supply (80 mA/ 1µsec pulse in GS, <1mA in RS). | 3.135 | 3.3 | 3.465 | V |
| VTX2_POS | TX2 Transfer gate positive power supply (80 mA/ 1µsec pulse in GS, <1mA in RS) | 3.135 | 3.3 | 3.465 | V |
| VTX1_NEG | TX1 Transfer gate negative power supply (80 mA/ 1µsec pulse in | -1.5 | -0.4 | +0.3 | V |

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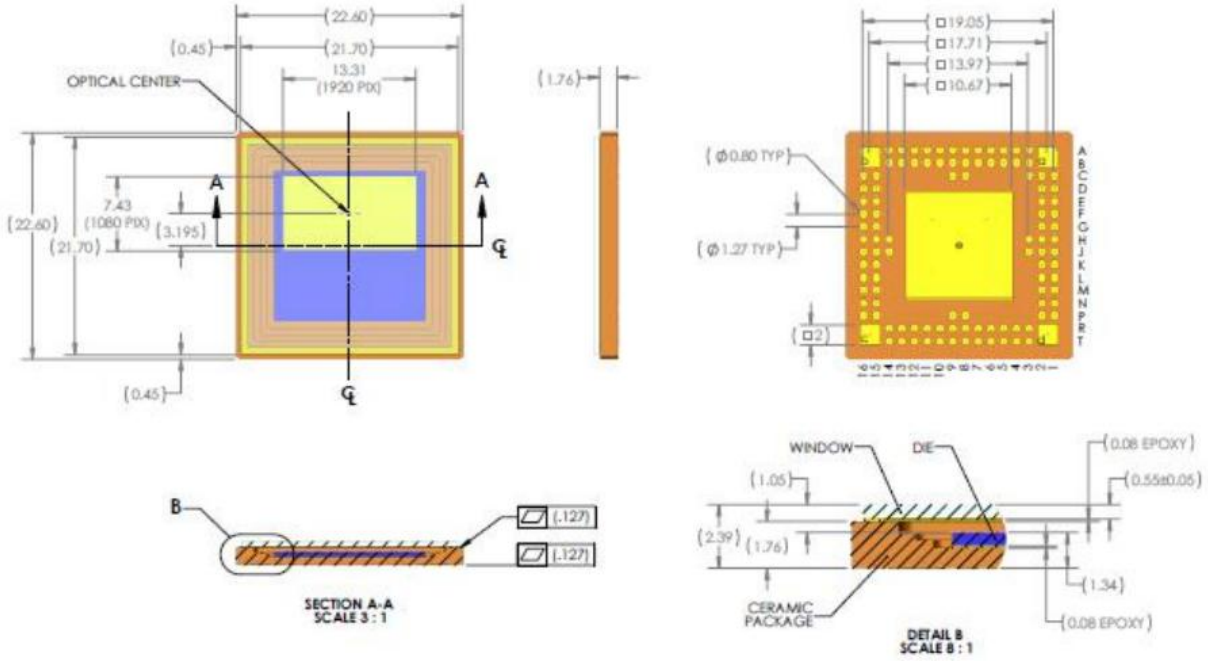
|---|---|---|---|---|---|
| | GS, < 1mA in RS) | | | | |
| VTX2_NEG | TX2 Transfer gate negative power supply (80 mA/ 1µsec pulse in GS, < 1mA in RS) | -1.5 | -0.4 or +0.8 | +0.85 | V |
| $T_{operation}$ | Sensor junction temperature | -40 | 30 | +55 | °C |

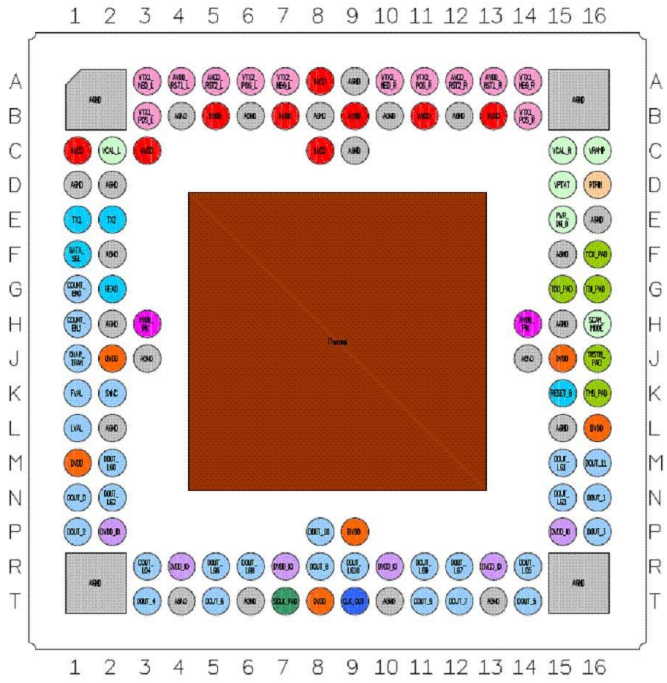
# Package

All the dimensions in the below drawing are in mm.

### Package




## Pad Diagram



## Pad List

The VC0201 Standard package image sensor has 105 pads in a LGA (Land Grid Array) package. The list shown below provides a complete description of the pad names, their functions and electrical requirements. Note the suffix L is appended to pads on left side of the sensor, and the suffix R is appended to pads on right side of the sensor.

| Pad number | Pad name | Pad type | Signal type | Power voltage/current | Pad description |
|---|---|---|---|---|---|
| A3 | VTX1_NEG_L | Power | | 0~-1.5v/80mA max, Ripple < 100μV RMS | TX1 negative supply |
| A4 | AVDD_RST1_L | Power | | 2.7-3.0v/1 mA, Ripple < 10 μV RMS | AVDD_RST1 reset supply |
| A5 | AVDD_RST2_L | Power | | 3.0v/1 mA, Ripple < 10 μV RMS | AVDD_RST2 reset supply |
| A6 | VTX2_POS_L | Power | | 3.3v/80mA max, Ripple < 1 mV RMS | TX2 positive supply |
| A7 | VTX2_NEG_L | Power | | +0.8v to -1.5v/80mA max, Ripple < 1 mV RMS | TX2 negative supply |
| A8 | AVDD | Power | | 3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS | AVDD analog supply |
| A9 | AGND | Ground | | | AGND common ground 0V |
| A10 | VTX2_NEG_R | Power | | +0.8v to -1.5v/80mA max, Ripple < 1 mV RMS | TX2 negative supply |
| A11 | VTX2_POS_R | Power | | 3.3v/80mA max, Ripple < 1 mV RMS | TX2 positive supply |
| A12 | AVDD_RST2_R | Power | | 3.0v/1 mA, Ripple < 10 μV RMS | AVDD_RST2 reset supply |
| A13 | AVDD_RST1_R | Power | | 2.7-3.0v/1 mA, Ripple < 10 μV RMS | AVDD_RST1 reset supply |
| A14 | VTX1_NEG_R | Power | | 0~-1.5v/80mA max, Ripple < 100μV RMS | TX1 negative supply |
| B3 | VTX1_POS_L | Power | | 3.3v/80mA max, Ripple < 1 mV RMS | TX1 positive supply |
| B4 | AGND | Ground | | | AGND common ground 0V |
| B5 | AVDD | Power | | 3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS | AVDD analog supply |
| B6 | AGND | Ground | | | AGND common ground 0V |
| B7 | AVDD | Power | | 3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS | AVDD analog supply |
| B8 | AGND | Ground | | | AGND common ground 0V |

| Pad number | Pad name | Pad type | Signal type | Power voltage/current | Pad description |
|---|---|---|---|---|---|
| B9 | AVDD | Power | | 3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS | AVDD analog supply |
| B10 | AGND | Ground | | | AGND common ground 0V |
| B11 | AVDD | Power | | 3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS | AVDD analog supply |
| B12 | AGND | Ground | | | AGND common ground 0V |
| B13 | AVDD | Power | | 3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS | AVDD analog supply |
| B14 | VTX1_POS_R | Power | | 3.3v/80mA max, Ripple < 1 mV RMS | TX1 positive supply |
| C1 | AVDD | Power | | 3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS | AVDD analog supply |
| C2 | VCAL_L | Input | Analog | | Optional column calibration reference voltage. Normally not used and so this pad is left as no connection or tied to ground. When it is used, the user inputs a fixed voltage (2.5V-1.0V, 1mA), when Register 2 bit 18 = 0 (not the default). With this Register setting, VCAL is connected to the column amplifier inputs (instead of the pixel floating diffusion voltages being connected to the column amplifier inputs). |
| C3 | AVDD | Power | | 3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS | AVDD analog supply |
| C8 | AVDD | Power | | 3.3v/90mA average, 170mA peak on 5% duty cycle for each | AVDD analog supply |

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|---|---|---|---|---|---|
| | | | | line time, Ripple < 1mV RMS | |

| Pad number | Pad name | Pad type | Signal type | Power voltage/current | Pad description |
|---|---|---|---|---|---|
| C9 | AGND | Ground | | | AGND common ground 0V |
| C15 | VCAL_R | Input | Analog | | Optional column calibration reference voltage. Normally not used and so this pad is left as no connection or tied to ground. When it is used, the user inputs a fixed voltage (2.5V-1.0V, 1mA), when Register 2 bit 18 = 0 (not the default). With this Register setting, VCAL is connected to the column amplifier inputs (instead of the pixel floating diffusion voltages being connected to the column amplifier inputs). |
| C16 | VRAMP | Input | Analog | | Optional external VRAMP voltage that can be used in place of the internally provided VRAMP. Normally this pad is not used and can be left as a no connection or tied to ground. If it is used, the user inputs the ADC ramp voltage (from 1.0V to 2.5V, 20mA) using timing signals from COUNT_EN[1:0]. |
| D1 | AGND | Ground | | | AGND common ground 0V |
| D2 | AGND | Ground | | | AGND common ground 0V |

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| D15 | VPTAT | Output | Analog | | Temperature sensor Output. This pad will output a voltage of slightly over 2 Volts at room temperature that will change linearly with temperature with a slope of 5 to 7 mV per degree Celsius. The exact calibration of offset and slope for VPTAT must be performed by the user with a reference temperature sensor (e.g. a thermocouple). |
| D16 | RTRIM | Output | Analog | | External current reference resistor pad. This pad must have a 12.2 kΩ resistor attached to this pad at one end and tied to ground at the other end. Providing this pad with a path to ground through a 12.2 kΩ resistor is necessary for the functioning of the column amplifiers. |
| E1 | TX1 | Input | 1.8v lvcmos | | Global TX1 Charge transfer control, rise/fall time < 500ns, Skew < 100ns, Ripple < 100μV RMS |

| Pad number | Pad name | Pad type | Signal type | Power voltage/current | Pad description |
|---|---|---|---|---|---|
| E2 | TX2 | Input | 1.8v lvcmos | | Global TX2 Charge dump control, rise/fall time < 500ns, Skew < 100ns, Ripple < 1mV RMS |
| E15 | PWR_DN_B | Input | 1.8v lvcmos | | Power Down Input (active low). Setting this pad to logic 0 has the same effect as setting Register 2 bit 25 to 1. It enables the low power control register, Register 12. |
| E16 | AGND | Ground | | | AGND common ground 0V |

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| F1 | DATA_SEL | Input | 1.8v lvcmos | | DATA_SEL = 0 selects wavetable A for sensor readout and wavetable B for read/write access. DATA_SEL = 1 selects wavetable B for sensor readout and wavetable A for read/write access. Typically, for Rolling Shutter operation, wavetable A is always used fro sensor readout, so DATA_SEL = 0 (fixed). For Global Shutter operation, DATA_SEL = 0 selects wavetable A (the GS Reset frame) and DATA_SEL = 1 selects wavetable B (the GS Data frame) so DATA_SEL is constantly switching between 0 and 1. |
| F2 | AGND | Ground | | | AGND common ground 0V |
| F15 | AGND | Ground | | | AGND common ground 0V |
| F16 | TCK_PAD | Input | 1.8v lvcmos | | SPI clock (clk) This clock must be 25 MHz or less. |
| G1 | COUNT_EN0 | Output | 1.8v hstl | | External count and external VRAMP synchronization Output, bit 0. Normally ignored unless the external VRAMP (pad C16) is being used (which it typically is not). |
| G2 | READ | Input | 1.8v lvcmos | | External start/pause row counter and readout activities control Input from pad |
| G15 | TDO_PAD | Output | 1.8v hstl | | SPI serial data Output (so) |
| G16 | TDI_PAD | Input | 1.8v lvcmos | | SPI serial data Input (si) |
| H1 | COUNT_EN1 | Output | 1.8v hstl | | External count and external VRAMP synchronization Output, bit 1. Normally ignored unless the external VRAMP (pad C16) is being used (which it typically is not). |
| H2 | AGND | Ground | | | AGND common ground 0V |

| Pad number | Pad name | Pad type | Signal type | Power voltage/current | Pad description |
|---|---|---|---|---|---|
| H3 | AVDD_PIX | Power | | 3.3v/10mA avg, Ripple < 100 µV RMS | Pixel source follower supply |
| H14 | AVDD_PIX | Power | | 3.3v/10mA avg, Ripple < 100 µV RMS | Pixel source follower supply |
| H15 | AGND | Ground | | | AGND common ground 0V |
| H16 | SCAN_MODE | Input | 1.8v lvcmos | | Input switch to put the sensor into “Scan Mode” when logic 1 is input. SCAN_MODE is an internal BAE test so the customer should always tie this pad to ground. |
| J1 | CHARGE_TRANS | Output | 1.8v hstl | | Marker pulse indicating when data sampling of the floating node voltage is occurring for the selected row. This signal comes directly from the wavetable without any modification. In Global Shutter, the user must supply TX1, TX2, and DATA_SEL inputs on external pads, and the timing of these signals should (usually) be correlated with CHARGE_TRANS. |
| J2 | DVDD | Power | | 1.8v/160 mA max, Ripple < 25 mV RMS | DVDD digital core supply |
| J3 | AGND | Ground | | | AGND common ground 0V |
| J14 | AGND | Ground | | | AGND common ground 0V |
| J15 | DVDD | Power | | 1.8v/160 mA max, Ripple < 25 mV RMS | DVDD digital core supply |
| J16 | TRSTB_PAD | Input | 1.8v lvcmos | | Optional SPI Reset This pad is optional but it is still functional in that a logic 0 on this pad will put the SPI controller in a reset state that prevents the other SPI pads from working. Therefore, in SPI mode, this pad should be tied to logic 1. |

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| K1 | FVAL | Output | 1.8v hstl | | Frame valid Output, also called F_VALID. Will be high when data from the physical array (i.e. active imager rows and dark rows, but not pre-scan rows) is being output on the DOUT/DOUT_LG pads. |
| K2 | SYNC | Output | 1.8v hstl | | Marker pulse for line or frame. This signal comes from the wavetable and will pulse once at the beginning of each line (if Register 11 bit 14 = 0, the default) or once at the beginning of |

| Pad number | Pad name | Pad type | Signal type | Power voltage/current | Pad description |
|---|---|---|---|---|---|
| | | | | | each frame (if Register 11 bit 14 = 1). |
| K15 | RESET_B | Input | 1.8v lvcmos | | Active low reset to the chip. RESET_B = 0 will reset all state machines and reload default values to the registers. The effect of a RESETB = 0 on the chip is equivalent to power cycling the chip. |
| K16 | TMS_PAD | Input | 1.8v lvcmos | | SPI active low chip enable (ceb) |
| L1 | LVAL | Output | 1.8v hstl | | Line valid Output, also called L_VALID. Will be high once each line during the period each line time when data is appearing on the DOUT/DOUT_LG pads. |
| L2 | AGND | Ground | | | AGND common ground 0V |
| L15 | AGND | Ground | | | AGND common ground 0V |
| L16 | DVDD | Power | | 1.8v/160 mA max, Ripple < 25 mV RMS | DVDD digital core supply |
| M1 | DVDD | Power | | 1.8v/160 mA max, Ripple < 25 mV RMS | DVDD digital core supply |
| M2 | DOUT_LG0 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 0. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If |

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| | | | | | Register 2 bit 20 = 1, this pad is forced to 0. |
| M15 | DOUT_LG1 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 1. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0. |
| M16 | DOUT_11 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is always 0 because the DOUT[10:0] pads will only output data from the High gain channel. If Register 2 bit 20 = 1, data multiplexing for the DOUT pads is enabled, and this Output will be logic 0 when DOUT[10:0] is High gain data and this Output will be logic 1 when DOUT[10:0] is Low gain data. |
| N1 | DOUT_0 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 0. The DOUT[10:0] pad data is in Gray code and must be converted to binary |

| Pad number | Pad name | Pad type | Signal type | Power voltage/current | Pad description |
|---|---|---|---|---|---|
| | | | | | off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 0. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on |

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| | | | | | DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip. |
| N2 | DOUT_LG2 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 2. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0. |
| N15 | DOUT_LG3 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 3. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0. |
| N16 | DOUT_1 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 1. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 1. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip. |

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| P1 | DOUT_2 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 2. The DOUT[10:0] pad data is in Gray code |

| Pad number | Pad name | Pad type | Signal type | Power voltage/current | Pad description |
|---|---|---|---|---|---|
| | | | | | and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 2. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip. |
| P2 | DVDD_IO | Power | | 1.8v/65 mA max, Ripple < 1 mV RMS | DVDD digital core supply |
| P8 | DOUT_10 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 10. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 10. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. |

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| | | | | | Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip. |
| P9 | DVDD | Power | | 1.8v/160 mA max, Ripple < 25 mV RMS | DVDD digital core supply |
| P15 | DVDD_IO | Power | | 1.8v/65 mA max, Ripple < 1 mV RMS | DVDD digital core supply |
| P16 | DOUT_3 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 3. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High |

| Pad number | Pad name | Pad type | Signal type | Power voltage/current | Pad description |
|---|---|---|---|---|---|
| | | | | | gain of ADC Output bit 3. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip. |
| R3 | DOUT_LG4 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 4. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0. |
| R4 | DVDD_IO | Power | | 1.8v/65 mA max, | DVDD digital core |

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| | | | | Ripple < 1 mV RMS | supply |
| R5 | DOUT_LG6 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 6. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0. |
| R6 | DOUT_LG8 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 8. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0. |
| R7 | DVDD_IO | Power | | 1.8v/65 mA max, Ripple < 1 mV RMS | DVDD digital core supply |
| R8 | DOUT_8 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 8. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 8. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], |

| Pad number | Pad name | Pad type | Signal type | Power voltage/current | Pad description |
|---|---|---|---|---|---|
| | | | | | including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip. |

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|---|---|---|---|---|---|
| R9 | DOUT_LG10 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 10. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0. |
| R10 | DVDD_IO | Power | | 1.8v/65 mA max, Ripple < 1 mV RMS | DVDD digital core supply |
| R11 | DOUT_LG9 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 9. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0. |
| R12 | DOUT_LG7 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 7. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0. |
| R13 | DVDD_IO | Power | | 1.8v/65 mA max, Ripple < 1 mV RMS | DVDD digital core supply |
| R14 | DOUT_LG5 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 5. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0. |
| T3 | DOUT_4 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 4. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | ADC Output bit 4. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], |

| Pad number | Pad name | Pad type | Signal type | Power voltage/current | Pad description |
|---|---|---|---|---|---|
| | | | | | including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip. |
| T4 | AGND | Ground | | | AGND common ground 0V |
| T5 | DOUT_6 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 6. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 6. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip. |
| T6 | AGND | Ground | | | AGND common ground 0V |
| T7 | SCLK_PAD | Input | 1.8v hstl | | System clock. Input frequency should be between 30 MHz and 283 MHz. |
| T8 | DVDD | Power | | 1.8v/160 mA max, Ripple < 25 mV RMS | DVDD digital core supply |

| | | | | | |
|---|---|---|---|---|---|
| T9 | CLK_OUT | Output | 1.8v hstl | | Clock to synchronize the data Output. This output clock is from the user-supplied input clock SCLK. CLK_OUT may have some phase shift relative to SCLK but it will be of the same frequency. The phase of the data on the DOUT and DOUT_LG pads is aligned to the phase of CLK_OUT. |
| T10 | AGND | Ground | | | AGND common ground 0V |
| T11 | DOUT_9 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 9. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 9. If the binary value of the High gain channel is less |

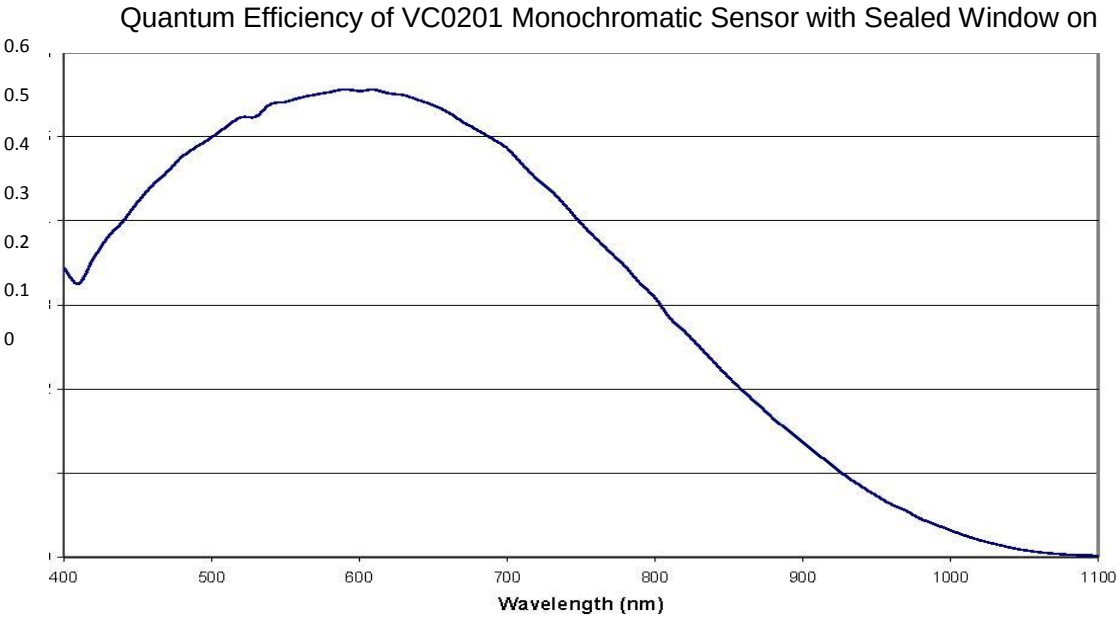
| Pad number | Pad name | Pad type | Signal type | Power voltage/current | Pad description |
|---|---|---|---|---|---|
| | | | | | than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip. |

| | | | | | |
|---|---|---|---|---|---|
| T12 | DOUT_7 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 7. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 7. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip. |
| T13 | AGND | Ground | | | AGND common ground 0V |
| T14 | DOUT_5 | Output | 1.8v hstl | | If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 5. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 5. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | DOUT[10:0] is in Gray code and must be converted to binary off-chip. |

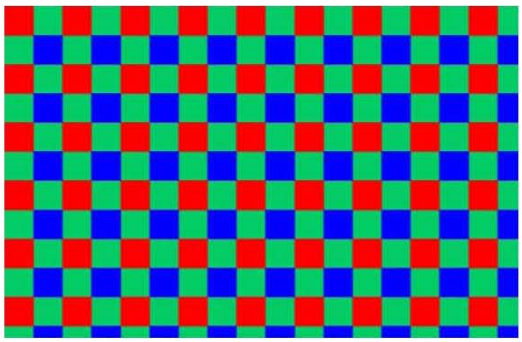
## Monochromatic Quantum Efficiency

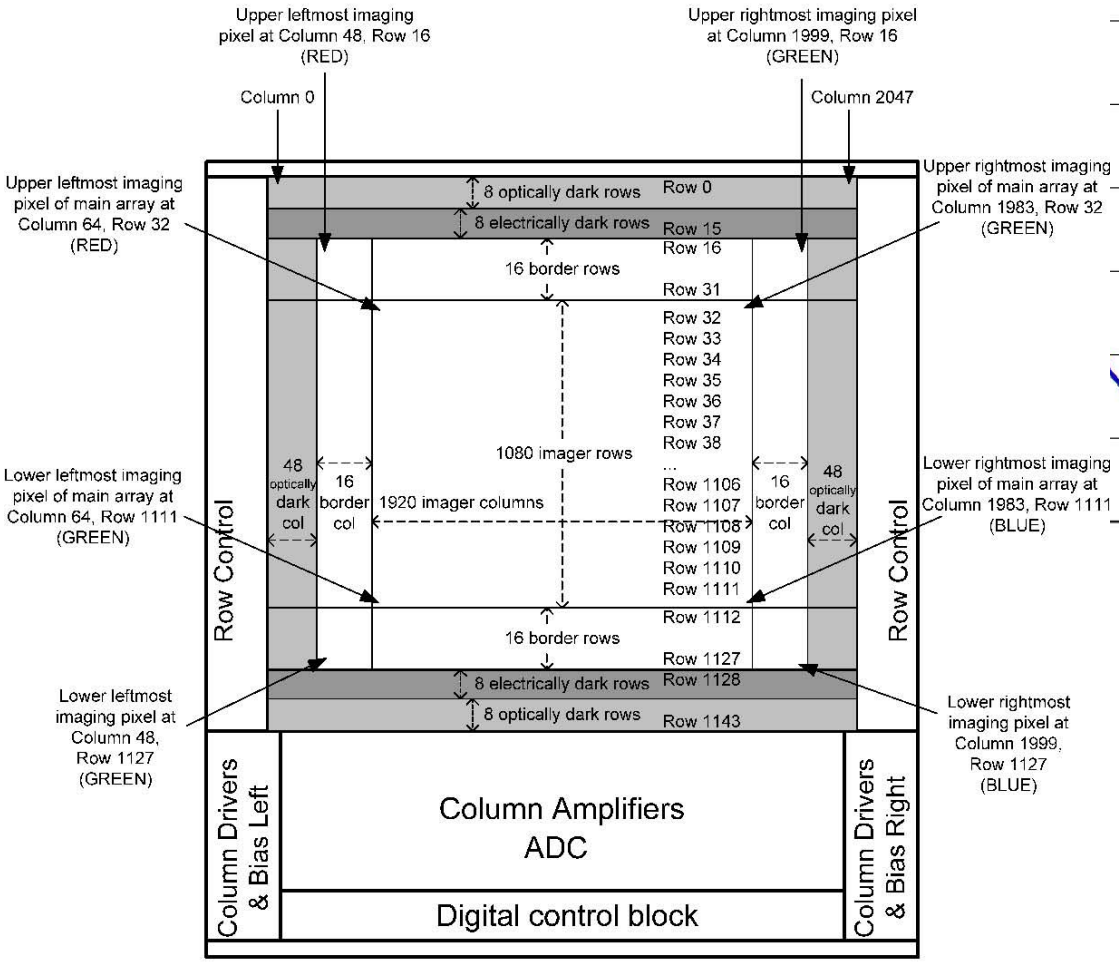
This datasheet assumes the VC0201 sensor is monochromatic (i.e. it has no color filter), and a QE curve for the monochromatic sensor is shown as below




## Color Filter Array (CFA)

## Option






The Bayer pattern RGB Color Filter Array (CFA) covers the 1952 (H) x 1112 (V) imaging pixels and extends 2 pixels deep into the dark pixels region on all 4 sides. Even numbered rows are Red/Green, with even columns Red and odd columns Green. Odd numbered rows are Green/Blue, with even columns Green and odd columns Blue

The QE curves for the RGB filters are shown as below

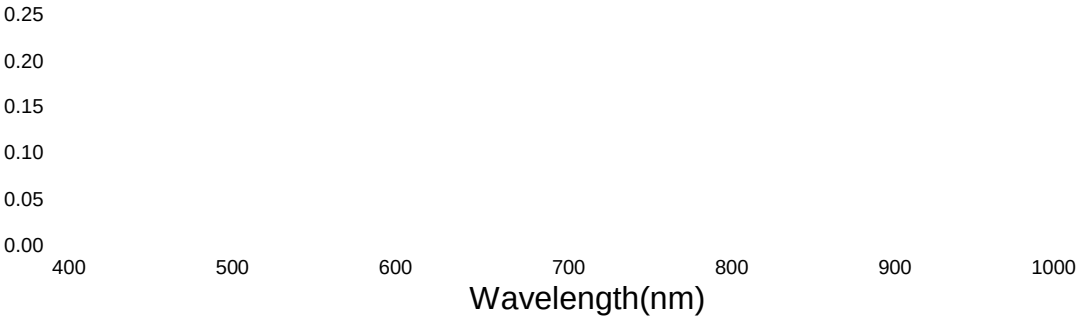
Quantum Efficiency of VC0201 RGB Color Sensor with Sealed Window on

0.45

0.40

0.35

0.30




## Cosmetic Specification

| Defect classification | Criteria | Maximum Count | Comments |
|---|---|---|---|
| Hot Pixels in Dark Frame | ± 6 sigma from the mean | 2000 | Low gain only |
| Cold/Warm Pixels in Light Frame – Minor Defects | > 15% from the mean | 2000 | Low gain only |
| Cold/Warm Pixels in Light Frame – Major Defects | > 50% from the mean | 25 | Low gain only |
| Small Cluster in Light Frame – Qty Allowed | ± 6 sigma from the mean 2 < Size <= 20pix | 50 | Low gain only |
| Large Cluster in Light Frame– Qty Allowed | ± 6 sigma from the mean Size > 20pix | 0 | Low gain only |
| Column --Qty Allowed | ± 10% gain variation from the mean | 0 | Low gain only, Light frame – dark frame |
| Row --Qty Allowed | ± 10% gain variation from the mean | 0 | Low gain only, Light frame – dark frame |

## Test conditions

Blemish tests are performed in Rolling Shutter mode; light frame captured at 50% of saturation. Dark frame captured at 91 ms integration time.

Defect measurements are performed on the full active pixel array