Features

- 2nd Generation EE Complex Programmable Logic Devices
  - 3.0V to 3.6V Operating Range with 5V Tolerant I/Os
  - 32 - 512 Macrocells with Enhanced Features
  - Pin-compatible with Industry-standard Devices
  - Speeds to 4.5 ns Maximum Pin-to-pin Delay
  - Registered Operation to 225 MHz
- Enhanced Macrocells with Logic Doubling™ Features
  - Bury Either Register or COM while Using the Other for Output
  - Dual Independent Feedback Allows Multiple Latch Functions per Macrocell
  - 5 Product Terms per Macrocell, Expandable to 40 per Macrocell with Cascade Logic, Plus 15 More with Foldback Logic
  - D/T/Latch Configurable Flip-flops plus Transparent Latches
  - Global and/or per Macrocell Register Control Signals
  - Global and/or per Macrocell Output Enable
  - Programmable Output Slew Rate per Macrocell
  - Programmable Output Open Collector Option per Macrocell
  - Fast Registered Input from Product Term
- Enhanced Connectivity
  - Single Level Switch Matrix for Maximum Routing Options
  - Up to 40 Inputs per Logic Block
- Advanced Power Management Features
  - ITD (Input Transition Detection) Available Individually on Global Clocks, Inputs and I/O for µA Level Standby Current on “L” versions
  - Pin-controlled 1 mA Standby Mode
  - Reduced-power Option per Macrocell
  - Automatic Power Down of Unused Macrocells
  - Programmable Pin-keeper Inputs and I/Os
- Available in Commercial and Industrial Temperature Ranges
- Available in All Popular Packages Including PLCC, PQFP, TQFP and BGA
- EE Technology
  - 100% Tested
  - Completely Reprogrammable
  - 10,000 Program/Erase Cycles
  - 20 Year Data Retention
  - 2000V ESD Protection
  - 200 mA Latch-up Immunity
- JTAG Boundary-scan Testing Port per IEEE 1149.1-1990 and 1149.1a-1993
  - Pull-up Option on JTAG Pins TMS and TDI
- IEEE 1532 Compatibility for Fast In-System Programmability (ISP) via JTAG
- PCI-compliant
- Security Fuse Feature

ATF15xxAE Family Datasheet

ATF1502AE(L)
ATF1504AE(L)
ATF1508AE(L)
ATF1516AE(L)
ATF1532AE(L)

Preliminary

Rev. 2398E–12/01

General Description

Beginning with the introduction of the 100% connected ATF1500 with 32 enhanced macrocells in 1996, Atmel's CPLD products have delivered extra IO connectivity and logic reusability. Atmel's commitment to efficient, flexible architecture has continued with the current Atmel ATF15xx Family of industry-standard, pin-compatible CPLDs. Atmel's Logic Doubling architecture consists of wider fan-in, additional routing and clock options, combined with sophisticated, proprietary device fitters, extend CPLD place and route efficiency. Atmel enhanced macrocell includes double independent buried feedback that allows designers to pack more logic (particularly shifters and latches) into a smaller CPLD or leave spare room for later revisions. The Atmel ATF15xx family delivers enhanced functionality and flexibility with no additional design effort and is highly cost effective.

The Atmel ATF15xx Family includes all popular configurations and speeds.

Table 1. ATF15xxAE Family Device Features

Feature	ATF1502AE(L)	ATF1504AE(L)	ATF1508AE(L)	ATF1516AE(L)	ATF1532AE(L)
Usable Gates	750	1500	3000	6000	12000
Macrocells	32	64	128	256	512
Logic Blocks	2	4	8	16	32
Max. # Pins	44	100	256	256	256
Max. User I/Os	36	68	100	164	212
T_{PD} Grades (ns)	4, 7, 10(15)	4, 7, 10(15)	5, 7, 10(15)	5, 7, 10(15)	5, 7, 12(15)

The Atmel ATF15xxAE Family includes pin-compatible products in all popular packages.

Table 2. ATF15xxAE Family Device Packages and Number of Signal Pins[1][2]

Packages	ATF1502AE(L)	ATF1504AE(L)	ATF1508AE(L)	ATF1516AE(L)	ATF1532AE(L)
44-pin PLCC	36	36			
44-pin TQFP	36	36			
49-ball BGA		41			
84-pin PLCC			68		
100-pin TQFP		68	84	84	
100-ball BGA		68	84	84	
144-pin TQFP			100	120	120
169-ball BGA			100		
208-pin PQFP				164	176
256-ball BGA			100	164	212

Notes: 1. Contact Atmel for up-to-date information on device and package availability.
2. When the JTAG port is used for In System Programming (ISP) or Boundary-scan Testing (BST), the four associated pins become JTAG pins and are unavailable for user I/O.

Functional Description

The ATF15xxAE Family of 3.3 Volt supply, high-performance, high-density complex programmable logic devices (CPLDs) utilizes Atmel's proven electrically-erasable technology. With up to 512 macrocells, they easily integrate logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF15xxAE Family's enhanced macrocell architecture, switch matrices and routing increase usable gate count for new designs and increase odds of successful pin-locked design modifications while maintaining pin-compatibility with industry-standard CPLDs.

The ATF15xxAE Family devices have four dedicated input pins and depending on the type of device and package, up to 208 bi-directional I/O pins. Each dedicated input pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell. Each input and I/O pin also feeds into the global bus.

The macrocells are organized into groups of sixteen called logic blocks. The switch matrix in each logic block selects 40 individual signals from the global bus. Macrocells within a given logic block may share their sixteen foldback signals on a regional foldback bus. Cascade logic between macrocells in the Logic Block allows fast, efficient generation of complex logic functions. All macrocells are capable of being I/Os; however, the actual number of I/O pins depends on the device and package type. The ATF15xxAE Family members contain two, four, eight, sixteen or thirty-two such logic blocks, each capable of creating sum term logic with a fan-in of 40 inputs from the switch matrix having access to up to 80 product terms.

Unused macrocells are automatically disabled by the fitter software to decrease power consumption. A security fuse, when programmed, protects the contents of the other fuses. Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF15xxAE Family devices are In-System Programmable (ISP) devices. They use the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and are fully-compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Global Bus/Switch Matrix

The global bus (Figure 1) contains all input and I/O pin signals as well as the buried feedback signals from all macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Up to 40 of these signals can be selected as inputs to the individual logic blocks by the fitter software. Atmel's ATF15xx Family of CPLDs use a single level switch matrix signal distribution structure, where each logic block input has access to the same number of global bus inputs, maximizing the number of possible ways to route a global bus signal. This single level structure is in contrast with split switch matrix structures used by others in which routing a particular global bus input to a particular logic block input makes that signal unavailable to some other logic blocks, thus greatly limiting the available opportunities to route.

The ATF15xxAE Family macrocell, shown in Figure 2, consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, foldback bus, a flip-flop and output buffer. Extra fan-in and signal routing are provided throughout. Each macrocell can generate a foldback logic term from the product term mux and a buried feedback with extra routing that go to the global bus.

Figure 1. ATF15xxAE Family Typical Block Diagram

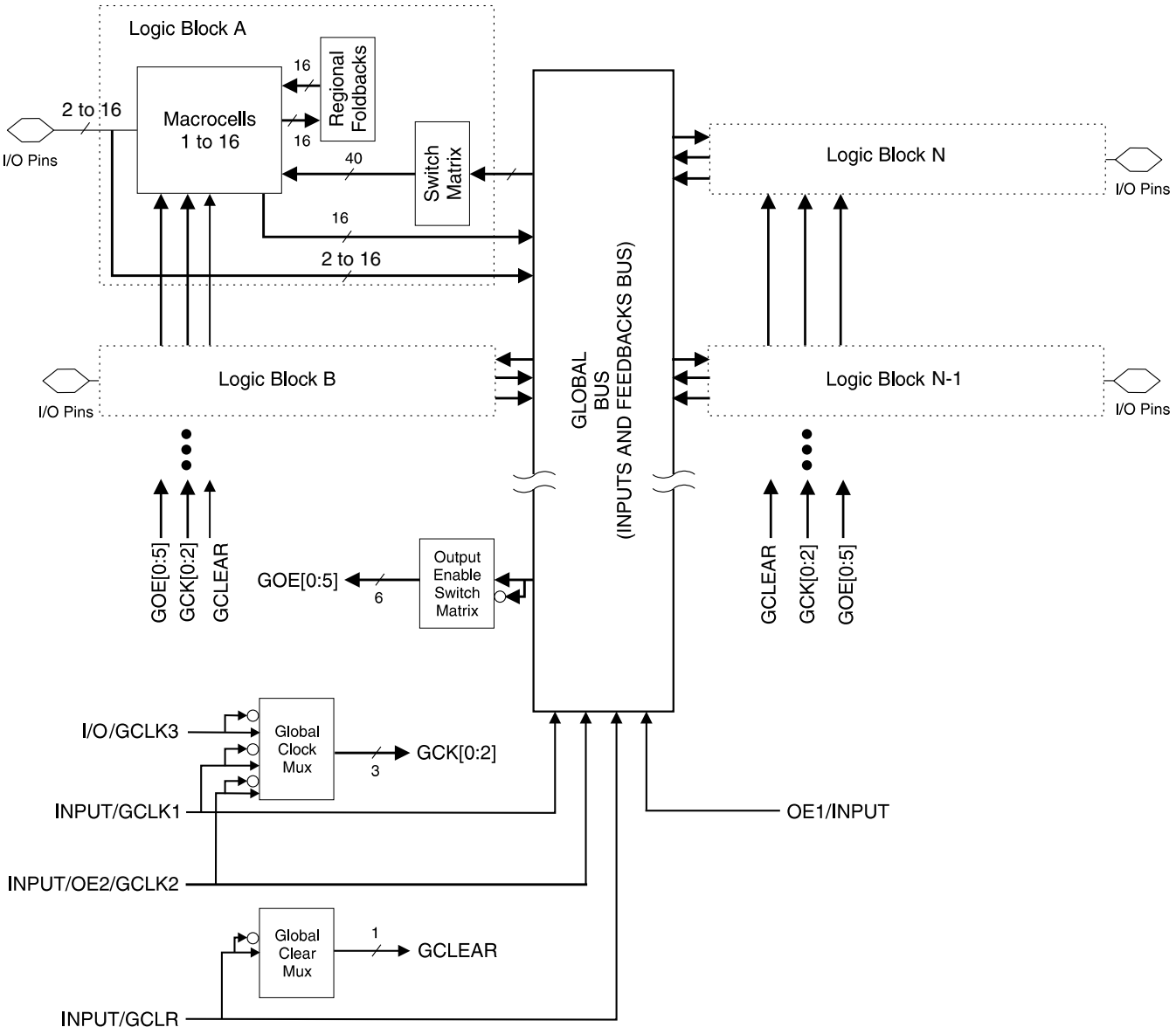
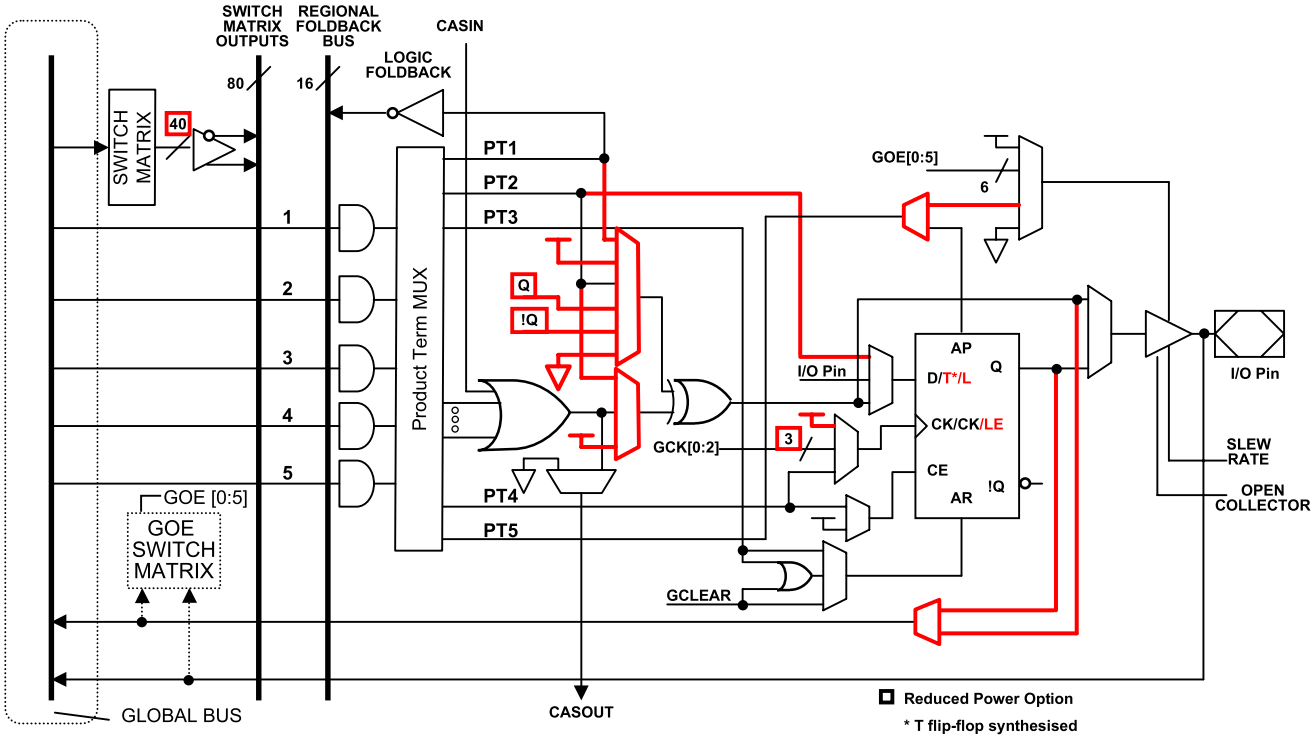


Figure 2. ATF15xxAE Family Macrocell with Enhanced Features In Red



Product Terms and Select Mux

Within each macrocell are five product terms. Each product term may receive as its inputs any combination of the signals from the switch matrix or regional foldback bus. The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the fitter software, which selects the optimum macrocell configuration.

OR/XOR/ CASCADE Logic

Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with little additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high- or low-level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate may be fed from the flip-flop output to emulate T- and JK-type flip-flops, or fed to the buried feedback to synthesize an extra latch.

Foldback Bus

Each macrocell can also generate a foldback product term. This signal goes to the regional bus and is available to the 16 macrocells in a given logic block. The foldback is an inverse polarity of one of the macrocell's product terms. Although Cascade Logic is the preferred method for expanding the number of macrocell inputs to as many as 40, the 16 foldback terms in each region can also generate additional fan-in sum terms with nominal additional delay.

Flip-flop

The ATF15xxAE Family's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output or vice-versa. (This enhanced function is automatically implemented by the fitter software). The flip-flop can be configured for D, T, JK and SR operation, and changes state on the clock's rising edge. It can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

When a GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop has asynchronous reset and preset. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

Output Buffer

The ATF15xxAE Family macrocell output can be selected as registered or combinatorial. The extra buried feedback signal can be either combinatorial or registered signal regardless of whether the output is combinatorial or registered. (This enhanced function is automatically implemented by the fitter software) Feedback of a buried combinatorial output allows the creation of a second latch within a macrocell.

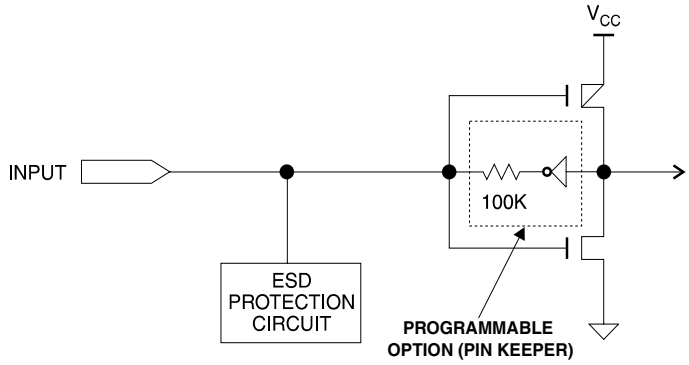
The output enable multiplexer (MOE) controls the output enable signals. Any buffer can be permanently enabled for simple output operation. Buffers can also be permanently disabled to allow use of the pin as an input. In this configuration, all the macrocell resources are still available, including the buried feedback, expander and CASCADE logic. The output enable for each macrocell can be selected as one of six global OE signals or a product term. In addition, some product term feedbacks can generate one of the global output enables.

The buffer has a fast/slow slew rate option to control EMI and an open-collector option which enables the device to provide control signals such as an interrupt that can be asserted by any of the several devices.

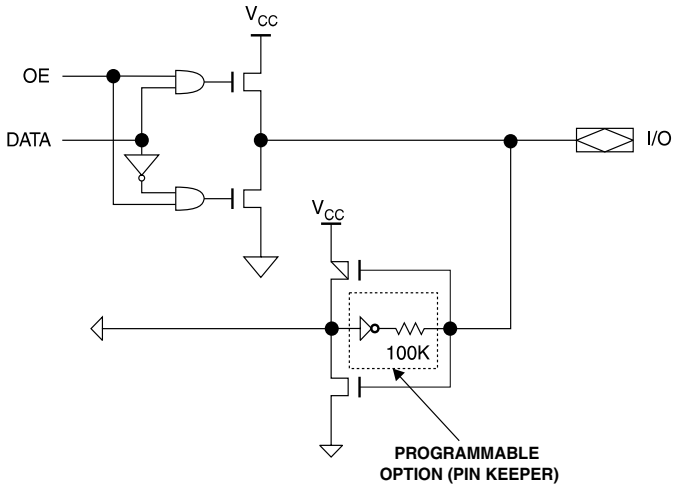
Programmable Pin-keeper Option for Inputs and I/Os

The ATF15xxAE Family offers the option of programming all input and I/O pins with pin-keeper circuits enabled. When any pin is driven high or low and then subsequently left floating, the pin keeper circuit will hold it at that previous high or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The pin-keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Input Diagram



I/O Diagram



Speed/Power Management

The ATF15xxAE Family has several speed and power management features.

Multiple Power Supplies, Power Sequencing and Hot-Socketing

Because the ATF15xxAE Family can be used in a system with mixture of power supply voltages, it has been designed to function with the V_{CCINT} and V_{CCIO} power supplies applied in any sequence. Also, until the power up sequence completes, the input/output buffers are kept in a high impedance state, and so may be driven but do not drive power out.

Power-on Reset

The ATF15xx Family devices are designed with a power-on reset, a feature critical for state machine initialization. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be initialized, and the state of each output will depend on the polarity of its buffer. However, due to the asynchronous nature of reset and uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and,
3. The clock must remain stable during T_D.

The ATF15xx Family has two options for the hysteresis about the reset level, V_{RST}, Small and Large. To ensure a robust operating environment in applications where the device is operated near 3.0V, Atmel recommends that during the fitting process users configure the device with the Power-on Reset hysteresis set to Large.

Power Down of Unused Macrocells

To conserve power, Atmel fitters automatically power down all unused macrocells.

Input Transition Detection/ Automatic Power Down

The ATF15xxAEL versions provide automatic power down to µA level standby power (the "L" suffix indicates "low" power) through Atmel's patented Input Transition Detection (ITD) circuitry on Global Clocks, Inputs and I/O. These ITD circuits automatically put the device into a low-power standby mode when no logic transitions are occurring. This reduces power consumption during inactive periods, and so provides proportional power-savings for most applications running at system speeds below $f_{critical}$ (~5 MHz).

In clocked applications where the device is operated at a frequency high enough to keep the device from going into standby (above $f_{critical}$), the device will perform at the faster speeds given in the next faster speed column. These higher speeds can be achieved in combinatorial designs as well, as long as, once activated by an initial input transition, the device continues to receive input transitions often enough to keep the device from going into standby mode again. That is, the time between input transitions is less than $1/f_{critical}$.

Reduced-Power per Macrocell

To further reduce power, each ATF15xx Family macrocell has a reduced-power bit feature. With this feature the designer can reduce power by 50% or more for logic that does not need to operate at the maximum switching speed. The reduced-power bit may be activated by changing the default OFF to ON for any or all macrocells. For macrocells in reduced-power mode (reduced-power bit turned on), the reduced- power adder, t_{RPA}, must be added to the AC parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH} and t_{SEXP}. All power-down AC characteristic parameters are computed from external input or I/O pins, with the reduced-power bit turned on.

Slew Rate Control

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching. The slew rate option is selected in the design source file.

Pin Controlled Power-down

All ATF15xx Family devices also have an optional pin-controlled power-down mode. When activated, one or both of two pins, PD1 and PD2, can act as power-down pins. The device goes into power-down when either PD1 or PD2 pins (or both) are high, and the device supply current is reduced to less than 1 mA. Also, all internal logic signals are latched and held, as are any enabled outputs. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. Input and I/O hold

latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled for PD1 or PD2, that pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals. The power-down option is selected in the design source file.

Power Consumption Estimates

An estimate of power consumption can be made based on typical designs and operation conditions, but because it is sensitive to these factors, power consumption must be verified with actual pattern and operation conditions. The equations given below are based on a pattern of 16-bit up/down counters in each logic block and may be used to estimate power consumption for both operating modes.

Standby Power

1. $P_{standby} = I_{ccstandby} \times V_{supply}$

Where:

$I_{ccstandby}$ = the standby current given for the particular device and standby mode (e.g., pin controlled Power Down)

V_{supply}= the power supply voltage

Active Power

2. $P_{active} = P_{internal} + P_{load} = I_{ccinternal} \times V_{supply} + P_{load}$

Where:

$I_{ccinternal}$ = the internal current estimated from equation 3 below

V_{supply}= the power supply voltage

P_{load} = depends on the device output load capacitance and switching frequency on each output pin.

P_{load} and additional power savings at low frequencies using Atmel Input Transition Detection ("L" versions) can be estimated according to the methods discussed in the Atmel Application Note "Saving Power with Atmel PLDs"

3. $I_{ccinternal} = [K_1 \times (MC_{inuse} - MC_{reducedpower})] + (K_2 \times MC_{reducedpower}) + (K_3 \times MC_{inuse} \times f_{op} \times NS)$

Where:

$MC_{reducedpower}$ = the number of macrocells operating at reduced power (from fitter report file)

MC_{inuse}= the number of macrocells in use (from fitter report file. Unused macrocells are powered down.)

NS = the proportion of logic nodes switching (typically 10-20%)

f_{op} = the switching frequency

K_1, K_2, and K_3 = device constants given in the table below.

Device	K_1	K_2	K_3
ATF1502AE	0.6	0.3	0.015
ATF1504AE	0.6	0.3	0.015
ATF1508AE	0.6	0.3	0.015
ATF1516AE	0.6	0.3	0.015
ATF1532AE	0.6	0.3	0.015

Note: Shaded data is preliminary and subject to change without notice.

Design Software

Atmel ATF15xx Family fitters allow logic synthesis using a variety of high-level description languages and formats. ATF15xx Family designs are supported by Atmel specific design tools as well as by several third-party tools. Free conversion software is also offered for industry standard devices. Check the Atmel web site or contact your authorized Atmel sales representative for up-to-date design software information.

Programming

ATF15xx Family devices can be programmed using standard third-party programmers. With third-party programmers, the JTAG ISP port can be disabled thereby allowing four additional I/O pins to be used for logic. Check the Atmel web site, contact your authorized Atmel sales representative or Atmel PLD Applications for details of third-party programmers.

ATF15xx Family devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes. Atmel provides ISP hardware and software to allow programming of the ATF15xx Family via the PC. ISP is performed by using either a download cable, a compatible board tester or a simple microprocessor interface.

It is most common to devote the JTAG pins to ISP, but it is possible to use ISP to program the part through the JTAG pins, and set these four pins I/O pins. However, this will effectively disable further ISP and the device will need to be erased on a programmer to re-enable ISP. Contact Atmel PLD Applications by e-mail at pld@atmel.com or call our Hotline at (408) 436-4333 for details.

To allow ISP programming support by the Automated Test Equipment (ATE) vendors, Serial Vector Format (SVF) files can be created by the Atmel ISP software. Conversion to other ATE tester formats is also possible. Check the Atmel web site for up-to-date programming and software support information.

ISP Programming Protection

The ATF15xx Family also incorporates a protection feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin-keeper option preserves the former state during device programming.

All ATF15xx Family devices are initially shipped in the erased state thereby making them ready to use for ISP.

For more information refer to the “Designing for In-System Programmability with Atmel CPLDs” application note.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF15xx Family fuse patterns. Once programmed, fuse verify is inhibited. However, the User Signature and device ID remain accessible.

JTAG-BST Overview

The JTAG-BST (JTAG boundary-scan testing) is controlled by the Test Access Port (TAP) controller. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own Boundary-scan Cell (BSC) in order to support boundary-scan testing. The ATF15xxAE Family does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The ATF15xx Family implements six BST instructions, and seven Atmel-defined In System Programming (ISP) instructions. All ATF15xx Family BST and ISP instructions have a length of 10 bits.

JTAG BST Instructions	Description
SAMPLE/PRELOAD	Captures signals at the device pins for later examination, or loads a data pattern prior to an EXTEST instruction.
EXTEST	Allows testing of off-chip circuitry and interconnections by forcing a pattern on the output pins or capturing signals from the input pins.
BYPASS	Places a single shift register stage between TDI and TDO, allowing test BST data to pass through a particular device in a chain of devices.
IDCODE	Places the 32-bit IDCODE register between TDI and TDO, allowing the IDCODE data to be shifted out of TDO.
UESCODE	Places the 16-bit user electronic signature register between TDI and TDO, allowing the UESCODE data to be shifted out of TDO.
HIGHZ	Places the BYPASS register between TDI and TDO in a high impedance mode, protecting the device from damage from externally applied test signals.
7 ISP instructions	These seven instructions allow in-system programming via the four JTAG pins.

The ATF15xx Family BST implementation complies with the Boundary-scan Definition Language (BSDL) described in the JTAG specification (IEEE Standard 1149.1). Any third-party tool that supports the BSDL format can be used to perform BST on the ATF15xx Family.

The ATF15xx Family also has the option of using four JTAG-standard I/O pins for in-system programming (ISP). The ATF15xx Family is programmable through the four JTAG pins using programming-compatible with the IEEE JTAG Standard 1149.1. Programming is performed by using 5V TTL-level programming signals from the JTAG ISP interface. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins. Refer to Atmel Application Note “Designing for In-System Programmability with Atmel CPLDs for more details.

JTAG Boundary-scan Cell (BSC) Testing

The ATF15xx Family has four dedicated input pins and a number of I/O pins depending on the device type and package type selected. Each input pin and I/O pin has a boundary-scan cell (BSC) which supports boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the (BST) capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller.

Device	Boundary-Scan Register Length	IDCODE MSB LSB
ATF1502AE	96	0000,0001,0101,0100,0010,0000,0011,1111
ATF1504AE	192	0000,0001,0101,0100,0100,0000,0011,1111
ATF1508AE	352	0000,0001,0101,0100,1000,0000,0011,1111
ATF1516AE	672	0000,0001,0101,0101,0000,0000,0011,1111
ATF1532AE	1232	0000,0001,0101,0110,0000,0000,0011,1111

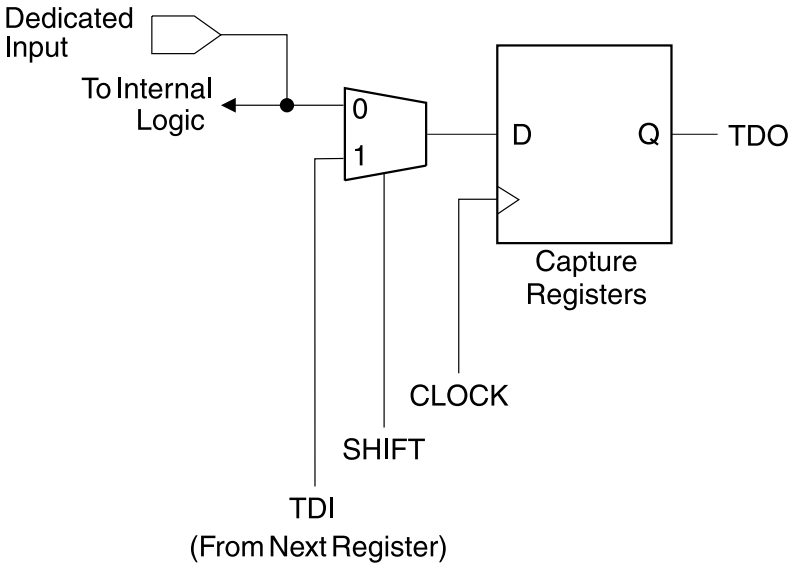
Note: Shaded data is preliminary and subject to change without notice.

Boundary-scan Definition Language (BSDL) Models

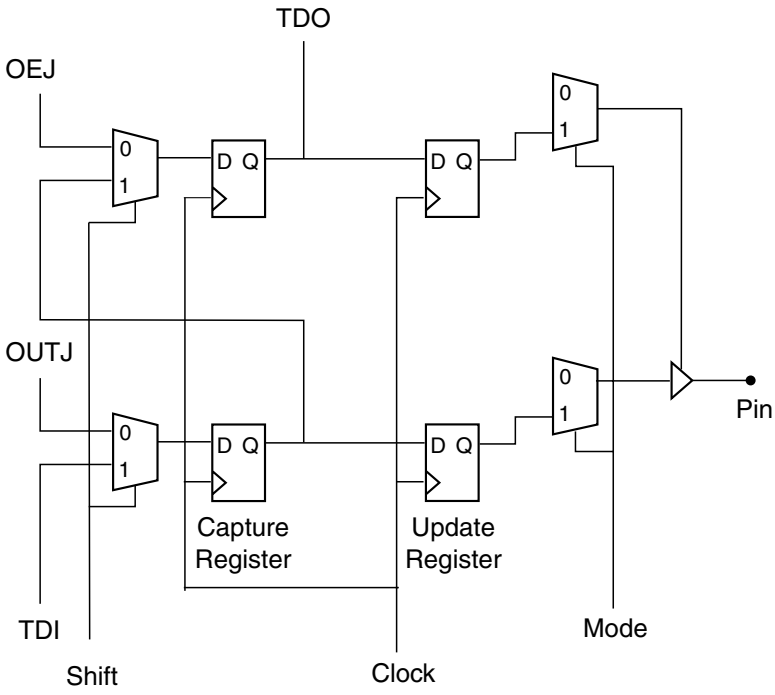
These are now available in all package types via the Atmel web site. These models conform to the IEEE 1149.1 standard and can be used for Boundary-scan Test Operation of the ATF15xx Family.

The BSC configuration for the input and I/O pins and macrocells are shown below.

BSC Configuration for Pins (Except JTAG TAP Pins)



BSC Configuration for Macrocell

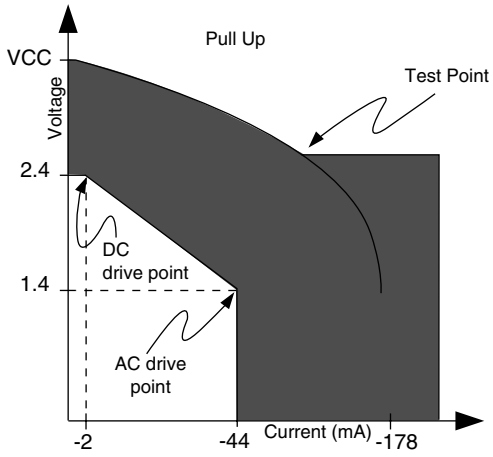


Macrocell BSC

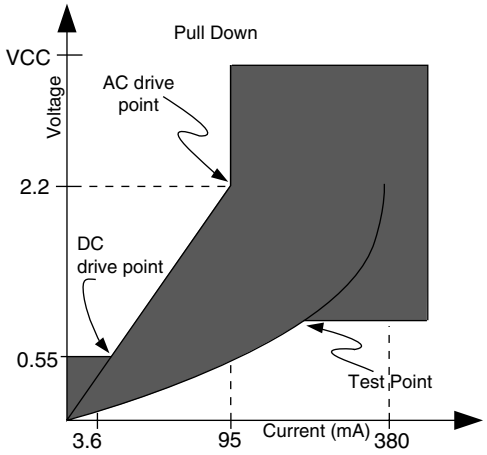
PCI Compliance

The ATF15xx Family also supports peripheral component interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers, which are much larger than the traditional TTL drivers.

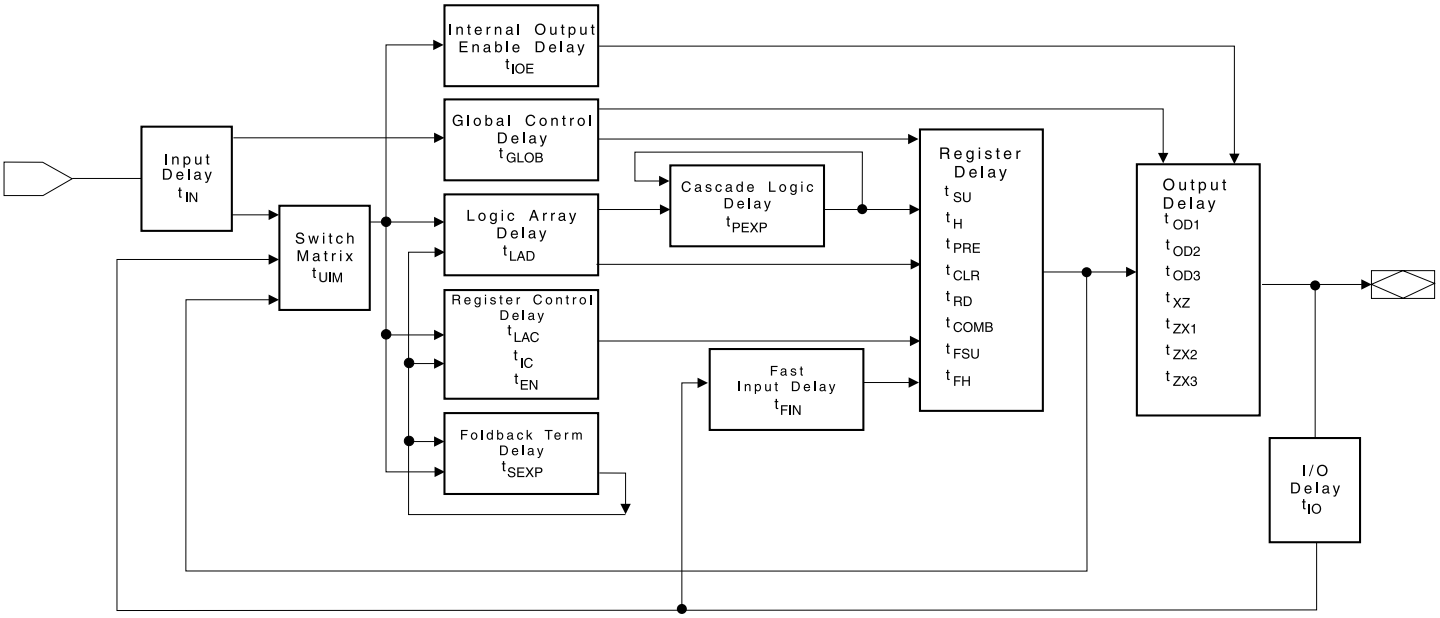
PCI Voltage-to-current Curves for +5V Signaling in Pull-up Mode



PCI Voltage-to-current Curves for +5V Signaling in Pull-down Mode



Timing Model

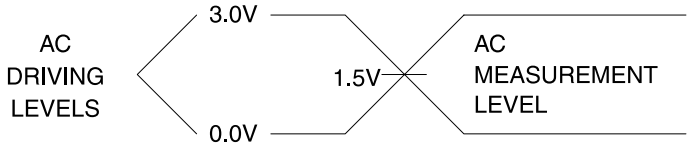


Pin Capacitance

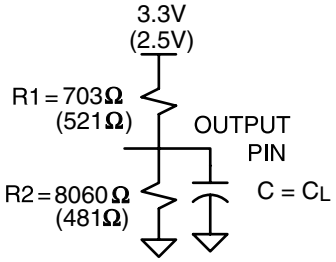
	Typ[1]	Max	Units	Condition
C_{IN}		8	pF	V_{IN} = 0V; f = 1.0 MHz
$C_{I/O}$		8	pF	V_{OUT} = 0V; f = 1.0 MHz

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested. The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

Input Test Waveforms and Measurement Levels



Output AC Test Loads



Absolute Maximum Ratings*

Ambient Temperature Under Bias	-65°C to +135°C
Storage Temperature	-65°C to +150°C
Junction Temperature	$150°C_{(MAX)}$
Voltage on Any Pin with Respect to Ground	-2.0V to +5.75V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)
DC Output Current per Pin	-25 to +25 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. For currents less than 100 mA, minimum voltage is -0.6 VDC and maximum voltage is V_{CC} + 0.75 VDC. Pulses of less than 20µs may undershoot to -2.0V or overshoot to 5.75V.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient), T_A	0°C - 70°C	-40°C - 85°C
Junction Temperature, T_J(1)	–	–
V_{CCINT} (3.3V) Power Supply	3.0V - 3.6V	3.0V - 3.6V
V_{CCIO} (3.3V) Power Supply	3.0V - 3.6V	3.0V - 3.6V
V_{CCIO} (2.5V) Power Supply	2.3V - 2.7V	2.3V - 2.7V
V_I Input Voltage	-0.5V - 5.75V	-0.5V - 5.75V
V_O Output Voltage	0 - V_{CCIO}	0 - V_{CCIO}
t_R Input Rise Time	40 ns Max	40 ns Max
t_F Input Fall Time	40 ns Max	40 ns Max

Note: 1. Junction temperature is package and device dependant and can be calculated as follows: $T_{J(MAX)} = T_{A(MAX)} + (\theta_{JA}|_{Air\ Flow\ =\ 0} * P_{(MAX)})$. For more information, see "Thermal Characteristic's of Atmel Packages"

DC Characteristics[1]

Symbol	Parameter	Condition			Min	Typ	Min	Unit
I_I	Input Leakage Current	$V_{IN} = V_{CCINT}$ or Ground			-10		10	µA
I_{OZ}	Tri-State Output Off-State Current	$V_O = V_{CCINT}$ or GND			-10		10	µA
I_{CC1}	Power Supply Current, Standby	V_{CCINT} = Max, V_{IN} = 0, V_{CCINT}	Std Mode	Com.		Note 3		mA
				Ind.		Note 3		mA
			"ITD" Mode	Com.		1		mA
				Ind.		1		mA
I_{CC2}	Power Supply Current, Power-down Mode	V_{CCINT} = Max, V_{IN} = 0, V_{CCINT}	PD Mode			0.1	1	mA
I_{CC3}[2]	Reduced-power Mode Supply Current, Standby	V_{CCINT} = Max, V_{IN} = 0, V_{CCINT}	Std Mode	Com.		Note 3		mA
				Ind.		Note 3		mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				1.7		5.75	V
V_{OL}	3.3V Output Low Voltage (TTL)	V_{CCIO} = 3.0V, I_{OL} = 8 mA		Com.			0.45	V
				Ind.			0.45	V
	3.3V Output Low Voltage (CMOS)	V_{CCIO} = 3.0V, I_{OL} = 0.1 mA		Com.			0.2	V
				Ind.			0.2	V
	2.5V Low Voltage	I_{OL} = 100 µA, V_{CCIO} = 2.3V					.2	V
		I_{OL} = 1 mA, V_{CCIO} = 2.3V					.4	V
		I_{OL} = 2 mA, V_{CCIO} = 2.3V					.7	V
V_{OH}	Output High Voltage -3.3V (TTL)	V_{CCIO} = 3.0V, I_{OH} = -2.0 mA			2.4			V
	Output High Voltage -3.3V (CMOS)	$V_{IN} = V_{IH}$ or V_{IL}, V_{CCIO} = 3.0V, I_{OH} = -0.1 mA			V_{CCIO} -0.2			V
	2.5V High Voltage	I_{OH} = -100 µA, V_{CCIO} = 2.3V			2.1			V
		I_{OH} = -1 mA, V_{CCIO} = 2.3V			2.0			V
		I_{OH} = -2 mA, V_{CCIO} = 2.3V			1.7			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. I_{CC3} refers to the current in the reduced-power mode when macrocell reduced-power is turned ON.
3. See Characterization Curves for each device.

Power-down AC Characteristics[1]

		-4, -5		-7		-10		-12		-15		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{IVDH}	Valid 1, I/O before PD High	4.5		7.5		10		12		15		ns
t_{GVDH}	Valid 1, OE[2] before PD High	4.5		7.5		10		12		15		ns
t_{CVDH}	Valid 1, Clock[2] before PD High	4.5		7.5		10		12		15		ns
t_{DHIX}	I, I/O Don't Care after PD High		9.0		15		20		22		25	ns
t_{DHGX}	OE[2] Don't Care after PD High		9.0		15		20		22		25	ns
t_{DHCX}	Clock[2] Don't Care after PD High		9.0		15		20		22		25	ns
t_{DLIV}	PD Low to Valid I, I/O		1.0		1.0		1.0		1.0		1.0	µs

Power-down AC Characteristics[1]

Symbol	Parameter	-4, -5		-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{DLGV}	PD Low to Valid OE, (Pin or Term)		1.0		1.0		1.0		1.0		1.0	µs
t_{DLCV}	PD Low to Valid Clock, (Pin or Term)		1.0		1.0		1.0		1.0		1.0	µs
t_{DLOV}	PD Low to Valid Output		1.0		1.0		1.0		1.0		1.0	µs

Notes: 1. For slow slew outputs, add t_{SSO}.
2. Pin or product term.

AC Characteristics ATF1502AE(L)[1]

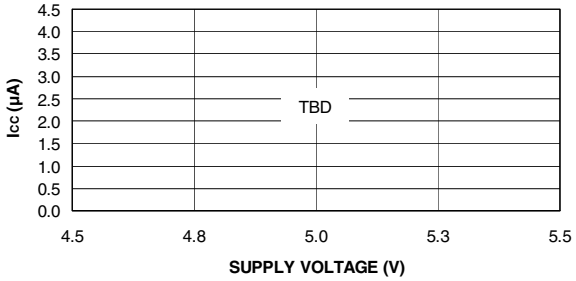
Symbol	Parameter	AE -4		AE -7		AE -10		AEL-15[6]		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		4.5		7.5		10		15	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		4.5		7.5		10		12	ns
t_{SU}	Global Clock Setup Time	2.9		4.7		6.3		11		ns
t_{H}	Global Clock Hold Time	0.0		0.0		0.0		0.0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	2.5		3.0		3.0		3.0		ns
t_{FH}	Global Clock Hold of Fast Input	0.0		0.0		0.0		1.0		MHz
t_{COP}	Global Clock to Output Delay	1.0	3.0	1.0	5.0	1.0	6.7	1.0	8.0	ns
t_{CH}	Global Clock High Time	2.0		3.0		4.0		5.0		ns
t_{CL}	Global Clock Low Time	2.0		3.0		4.0		5.0		ns
t_{ASU}	Array Clock Setup Time	1.6		2.5		3.6		4.0		ns
t_{AH}	Array Clock Hold Time	0.3		0.5		0.5		4.0		ns
t_{ACOP}	Array Clock Output Delay	1.0	4.3	1.0	7.2	1.0	9.4	1.0	15	ns
t_{ACH}	Array Clock High Time	2.0		3.0		4.0		6.0		ns
t_{ACL}	Array Clock Low Time	2.0		3.0		4.1		6.0		ns
t_{CNT}	Minimum Clock Global Period		4.4		7.2		9.7		13	ns
f_{CNT}[3]	Maximum Internal Global Clock Frequency	225		133		100		77		MHz
t_{ACNT}	Minimum Array Clock Period		4.4		7.2		9.7		13	ns
f_{ACNT}[4]	Maximum Internal Array Clock Frequency	225		133		100		77		MHz
f_{MAX}[5]	Maximum Clock Frequency	230		140		100		77		MHz
t_{IN}	Input Pad and Buffer Delay		0.7		1.2		1.5		2.0	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.7		1.2		1.5		2.0	ns
t_{FIN}	Fast Input Delay		2.3		2.8		3.4		2.0	ns
t_{SEXP}	Foldback Term Delay		1.9		3.1		4.0		8.0	ns
t_{PEXP}	Cascade Logic Delay		0.5		0.8		1.0		1.0	ns
t_{LAD}	Logic Array Delay		1.5		2.5		3.3		6.0	ns
t_{LAC}	Logic Control Delay		0.6		1.0		1.2		3.5	ns
t_{IOE}	Internal Output Enable Delay		0.0		0.0		00		3.0	ns

AC Characteristics ATF1502AE(L)[1] (Continued)

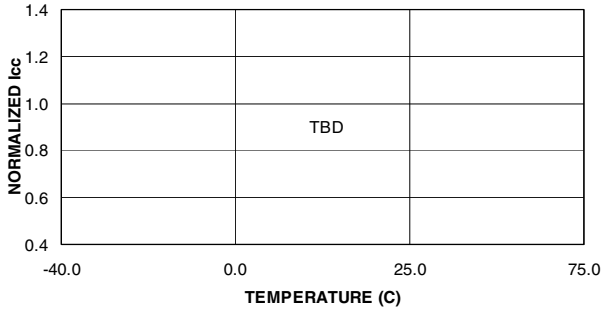
Symbol	Parameter	AE -4		AE -7		AE -10		AEL-15[6]		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{OD1}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35pF)		0.8		1.3		1.8		3.0	ns
t_{OD2}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35pF)		1.3		1.8		2.3		3.0	ns
t_{OD3}	Output Buffer and Pad Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35pF)		5.8		6.3		6.8		5.0	ns
t_{ZX1}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35pF)		4.0		4.0		5.0		7.0	ns
t_{ZX2}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35pF)		4.5		4.5		5.5		7.0	ns
t_{ZX3}	Output Buffer Enable Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35pF)		9.0		9.0		10.0		10	ns
t_{XZ}	Output Buffer Disable Delay (C_L= 5pF)		4.0		4.0		5.0		6.0	ns
t_{SU}	Register Setup Time	1.3		2.0		2.8		4.0		ns
t_H	Register Hold Time	0.6		1.0		1.3		4.0		ns
t_{FSU}	Register Setup Time of Fast Input	1.0		1.5		1.5		2.0		ns
t_{FH}	Register Hold Time of Fast Input	1.5		1.5		1.5		2.0		ns
t_{RD}	Register Delay		0.7		1.2		1.5		2.0	ns
t_{COMB}	Combinatorial Delay		0.6		1.0		1.3		2.0	ns
t_{IC}	Array Clock Delay		1.2		2.0		2.5		7.0	ns
t_{EN}	Register Enable Time		0.6		1.0		1.2		7.0	ns
t_{GLOB}	Global Control Delay		0.8		1.3		1.9		1.0	ns
t_{PRE}	Register Preset Time		1.2		1.9		2.6		5.0	ns
t_{CLR}	Register Clear Time		1.2		1.9		2.6		5.0	ns
t_{UIM}	Switch Matrix Delay		0.9		1.5		2.1		2.0	ns
t_{RPA}[2]	Reduced Power Adder		2.5		4.0		5.0		14	ns

Notes:
1. See ordering Information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL} and t_{SEXP} parameters for macrocells running in the reduced-power mode.
3. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells). f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
4. f_{ACNT} is the fastest 16-bit counter frequency available, using the internal array clock, local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells).
5. f_{MAX} is the fastest available frequency for pipeline data.
6. For clocked applications and frequencies above $f_{critical}$, OR, non-clocked applications with dormant times less that $1/f_{critical}$, the device will achieve the speeds of the -10 column. (See “ITD/automatic power down.”)

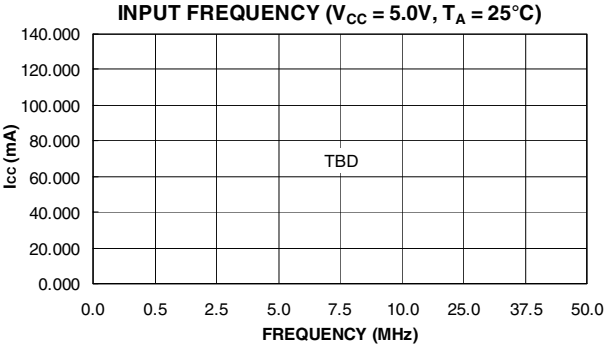
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



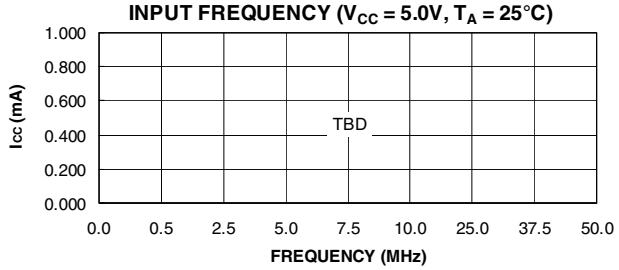
NORMALIZED I_{CC} VS. TEMP



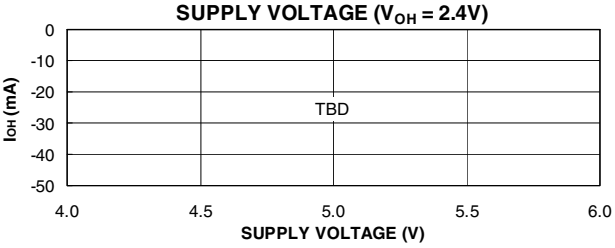
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



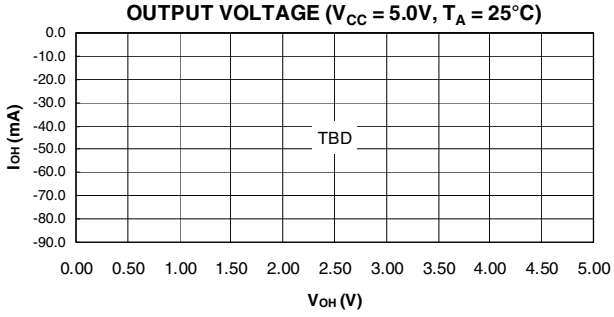
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



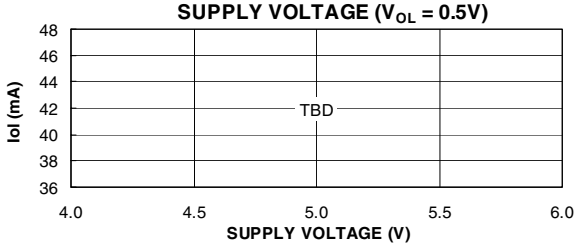
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



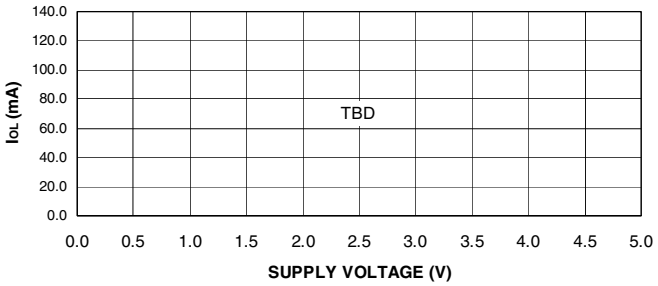
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



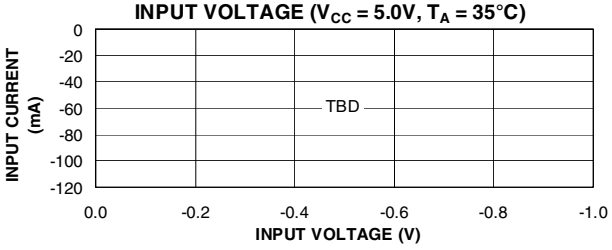
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



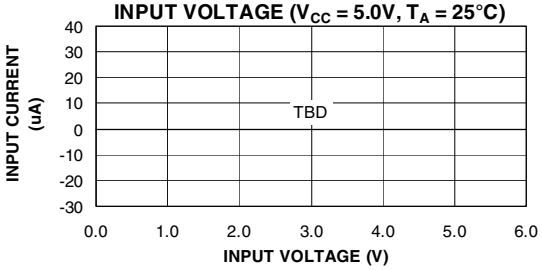
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



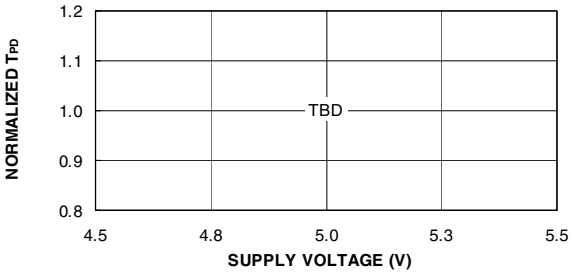
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



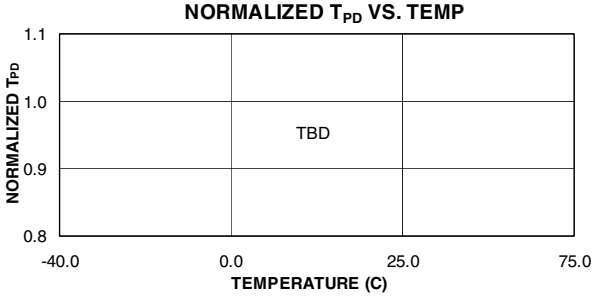
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



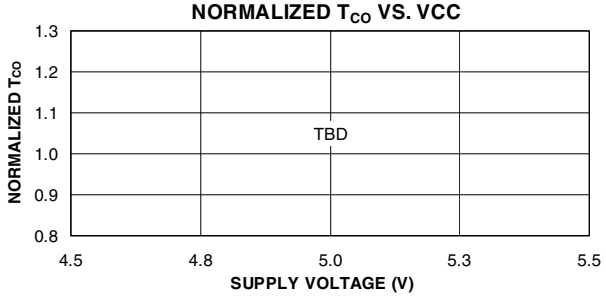
NORMALIZED T_{PD} VS. VCC



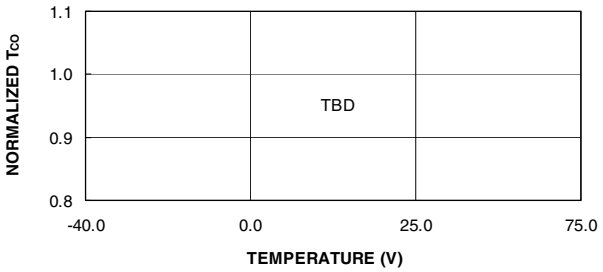
NORMALIZED T_{PD} VS. TEMP



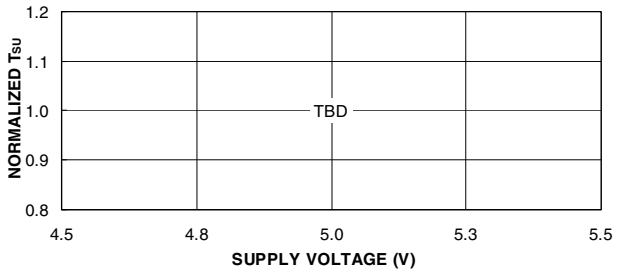
NORMALIZED T_{CO} VS. VCC



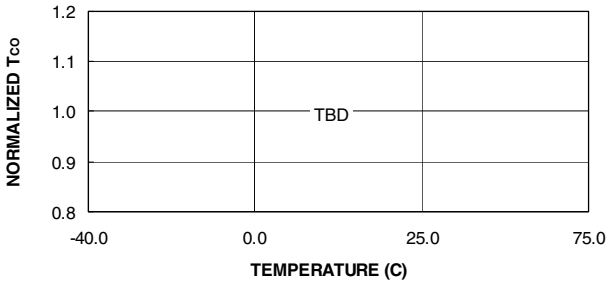
NORMALIZED T_{CO} VS. TEMP

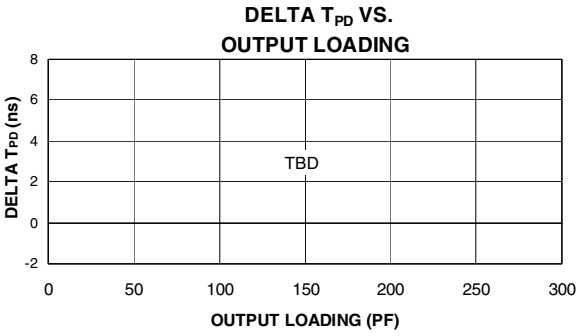


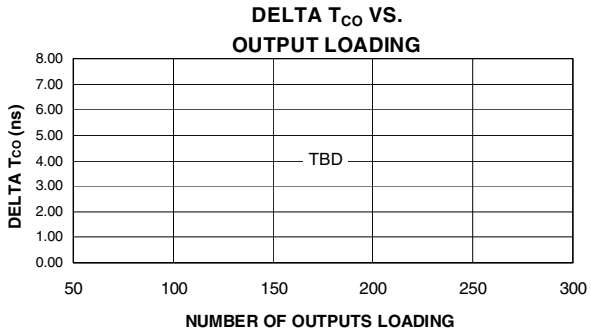
NORMALIZED T_{SU} VS. VCC

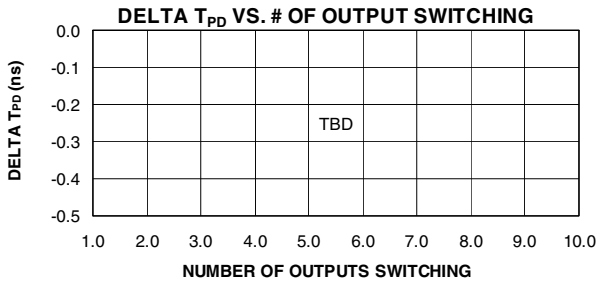


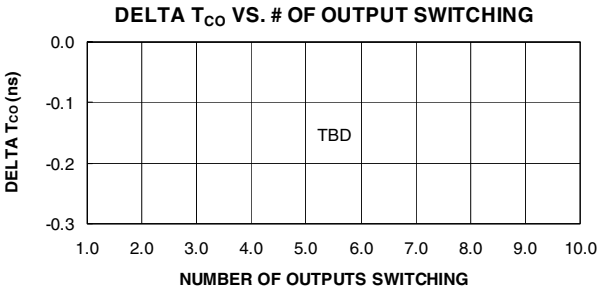
NORMALIZED T_{SU} VS. TEMP




DELTA T_{PD} VS.
OUTPUT LOADING
DELTA T_{PD} (ns)
8
6
4
2
0
-2
TBD
0
50
100
150
200
250
300
OUTPUT LOADING (PF)

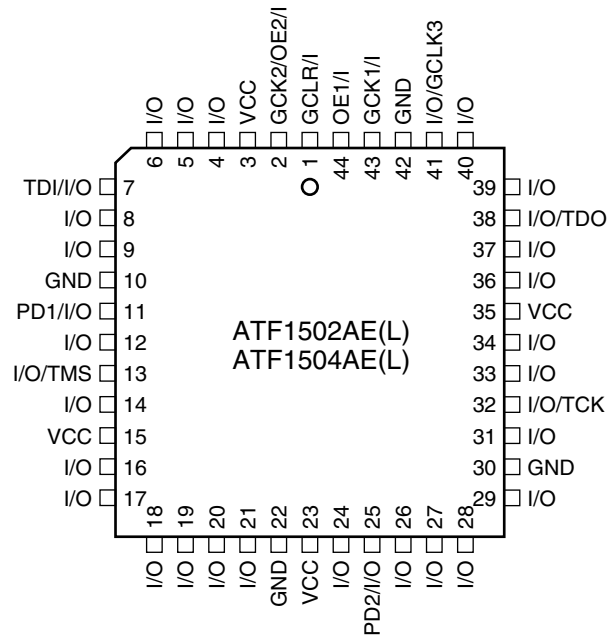

DELTA T_{CO} VS.
OUTPUT LOADING
DELTA T_{CO} (ns)
8.00
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
TBD
50
100
150
200
250
300
NUMBER OF OUTPUTS LOADING


DELTA T_{PD} VS. # OF OUTPUT SWITCHING
DELTA T_{PD} (ns)
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
TBD
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
NUMBER OF OUTPUTS SWITCHING

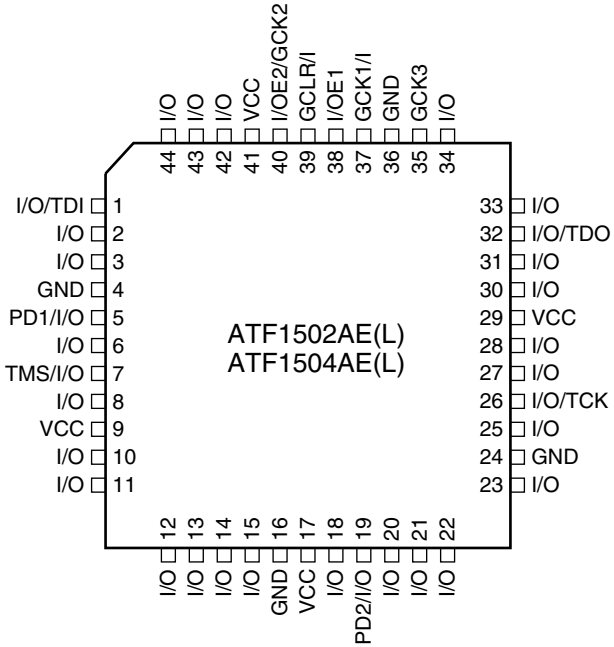

DELTA T_{CO} VS. # OF OUTPUT SWITCHING
DELTA T_{CO} (ns)
0.0
-0.1
-0.2
-0.3
TBD
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
NUMBER OF OUTPUTS SWITCHING

ATF1502AE(L) Pinouts

44-lead PLCC



44-lead TQFP



ATF1502AE(L) Dedicated Pinouts

Dedicated Pin	44-lead J-lead	44-lead TQFP
INPUT/OE2/GCLK2	2	40
INPUT/GCLR	1	39
INPUT/OE1	44	38
INPUT/GCLK1	43	37
I/O/GCLK3	41	35
I/O/PD (1,2)	11, 25	5, 19
I/O/TDI (JTAG)	7	1
I/O/TMS (JTAG)	13	7
I/O/TCK (JTAG)	32	26
I/O/TDO (JTAG)	38	32
GNDINT	22, 42	16, 36
GNDIO	10, 30	4, 24
VCCINT	3, 23	17, 41
VCCIO	15, 35	9, 29
# of Signal Pins	36	36
# User I/O Pins	32	32

OE (1, 2) Global OE pins
GCLR Global Clear pin
GCLK (1, 2, 3) Global Clock pins
PD (1, 2) Power-down pins
TDI, TMS, TCK, TDO JTAG pins used for boundary-scan testing or in-system programming
GNDINT Ground pins for the internal device logic
GNDIO Ground pins for the I/O drivers
VCCINT VCC pins for the internal device logic (+3.3V)
VCCIO VCC for the I/O drivers

ATF1502AE(L) I/O Pinouts

MC	PLC	44-lead PLCC	44-lead TQFP
1	A	4	42
2	A	5	43
3	A	6	44
4/**TDI**	A	7	1
5	A	8	2
6	A	9	3
7/**PD1**	A	11	5
8	A	12	6
9/**TMS**	A	13	7
10	A	14	8
11	A	16	10
12	A	17	11
13	A	18	12
14	A	19	13
15	A	20	14
16	A	21	15
17	B	41	35
18	B	40	34
19	B	39	33
20/**TDO**	B	38	32
21	B	37	31
22	B	36	30
23	B	34	28
24	B	33	27
25/**TCK**	B	32	26
26	B	31	25
27	B	29	23
28	B	28	22
29	B	27	21
30	B	26	20
31/**PD2**	B	25	19
32	B	24	18

ATF1502AE(L) Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	F_{MAX} (MHz)	Ordering Code	Package	Operation Range
4.5	3.0	230	ATF1502AE-4 AC44 ATF1502AE-4 JC44	44A 44J	Commercial (0°C to 70°C)
7.5	5.0	140	ATF1502AE-7 AC44 ATF1502AE-7 JC44	44A 44J	Commercial (0°C to 70°C)
			ATF1502AE-7 AI44 ATF1502AE-7 JI44	44A 44J	Industrial (-40°C to +85°C)
10.0	6.7	100	ATF1502AE-10 AC44 ATF1502AE-10 JC44	44A 44J	Commercial (0°C to 70°C)
			ATF1502AE-10 AI44 ATF1502AE-10 JI44	44A 44J	Industrial (-40°C to +85°C)
15.0	8.0	77	ATF1502AEL-15 AC44 ATF1502AEL-15 JC44	44A 44J	Commercial (0°C to 70°C)

Using “C” Product for Industrial

There is very little risk in using “C” devices for industrial applications because the V_{CC} conditions for 3.3V products are the same for commercial and industrial (there is only 15°C difference at the high end of the temperature range). To use commercial product for industrial temperature ranges, de-rate I_{CC} by 15%.

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)

AC Characteristics ATF1504AE(L) (1)

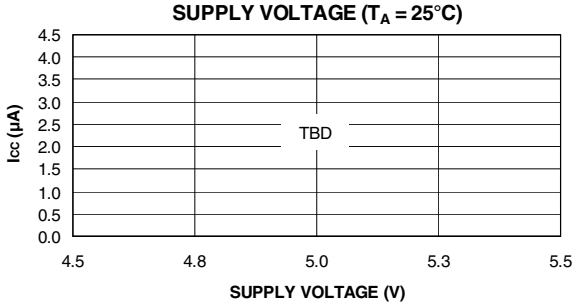
Symbol	Parameter	AE -4		AE -7		AE -10		AEL -15(6)		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		4.5		7.5		10		15	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		4.5		7.5		10		12	ns
t_{SU}	Global Clock Setup Time	2.8		4.7		6.2		11		ns
t_{H}	Global Clock Hold Time	0.0		0.0		0.0		0.0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	2.5		3.0		3.0		3.0		ns
t_{FH}	Global Clock Hold of Fast Input	0.0		0.0		0.0		1.0		MHz
t_{COP}	Global Clock to Output Delay	1.0	3.1	1.0	5.1	1.0	7.0	1.0	9.0	ns
t_{CH}	Global Clock High Time	2.0		3.0		4.0		5.0		ns
t_{CL}	Global Clock Low Time	2.0		3.0		4.0		5.0		ns
t_{ASU}	Array Clock Setup Time	1.6		2.6		3.6		5.0		ns
t_{AH}	Array Clock Hold Time	0.3		0.4		0.6		4.0		ns
t_{ACOP}	Array Clock Output Delay	1.0	4.3	1.0	7.2	1.0	9.6	1.0	15	ns
t_{ACH}	Array Clock High Time	2.0		3.0		4.0		6.0		ns
t_{ACL}	Array Clock Low Time	2.0		3.0		4.0		6.0		ns
t_{CNT}	Minimum Clock Global Period		4.5		7.4		10		13	ns
f_{CNT}(3)	Maximum Internal Global Clock Frequency	225		133		100		77		MHz
t_{ACNT}	Minimum Array Clock Period		4.5		7.4		10		13	ns
f_{ACNT}(4)	Maximum Internal Array Clock Frequency	225		133		100		77		MHz
f_{MAX}(5)	Maximum Clock Frequency	230		140		100		77		MHz
t_{IN}	Input Pad and Buffer Delay		0.6		1.1		1.4		2.0	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.6		1.1		1.4		2.0	ns
t_{FIN}	Fast Input Delay		2.5		3.0		3.7		2.0	ns
t_{SEXP}	Foldback Term Delay		1.8		3.0		3.9		8.0	ns
t_{PEXP}	Cascade Logic Delay		0.4		0.7		0.9		1.0	ns
t_{LAD}	Logic Array Delay		1.5		2.5		3.2		6.0	ns
t_{LAC}	Logic Control Delay		0.6		1.0		1.2		3.5	ns
t_{IOE}	Internal Output Enable Delay		0.0		0.0		00		3.0	ns
t_{OD1}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35pF)		0.8		1.3		1.8		3.0	ns
t_{OD2}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35pF)		1.3		1.8		2.3		3.0	ns
t_{OD3}	Output Buffer and Pad Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35pF)		5.8		6.3		6.8		5.0	ns
t_{ZX1}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35pF)		4.0		4.0		5.0		7.0	ns

AC Characteristics ATF1504AE(L) (Continued)[1]

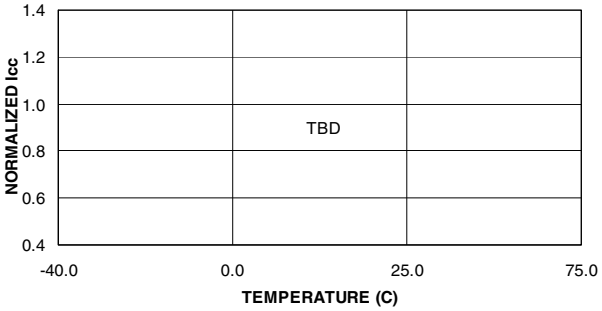
Symbol	Parameter	AE -4		AE -7		AE -10		AEL -15[6]		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZX2}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35pF)		4.5		4.5		5.5		7.0	ns
t_{ZX3}	Output Buffer Enable Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35pF)		9.0		9.0		10.0		10	ns
t_{XZ}	Output Buffer Disable Delay (C_L= 5pF)		4.0		4.0		5.0		6.0	ns
t_{SU}	Register Setup Time	1.3		2.0		2.9		5.0		ns
t_H	Register Hold Time	0.6		1.0		1.3		4.0		ns
t_{FSU}	Register Setup Time of Fast Input	1.0		1.5		1.5		2.0		ns
t_{FH}	Register Hold Time of Fast Input	1.5		1.5		1.5		2.0		ns
t_{RD}	Register Delay		0.7		1.2		1.6		2.0	ns
t_{COMB}	Combinatorial Delay		0.6		0.9		1.3		2.0	ns
t_{IC}	Array Clock Delay		1.2		1.9		2.5		6.0	ns
t_{EN}	Register Enable Time		0.6		1.0		1.2		6.0	ns
t_{GLOB}	Global Control Delay		1.0		1.5		2.2		2.0	ns
t_{PRE}	Register Preset Time		1.3		2.1		2.9		4.0	ns
t_{CLR}	Register Clear Time		1.3		2.1		2.9		4.0	ns
t_{UIM}	Switch Matrix Delay		1.0		1.7		2.3		2.0	ns
t_{RPA}[2]	Reduced Power Adder		3.5		4.0		5.0		10	ns

Notes:
1. See ordering Information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL} and t_{SEXP} parameters for macrocells running in the reduced-power mode.
3. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells). f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
4. f_{ACNT} is the fastest 16-bit counter frequency available, using the internal array clock, local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells).
5. f_{MAX} is the fastest available frequency for pipeline data.
6. For clocked applications and frequencies above $f_{critical}$, OR, non-clocked applications with dormant times less that $1/f_{critical}$, the device will achieve the speeds of the -10 column. (See “ITD/automatic power down.”)

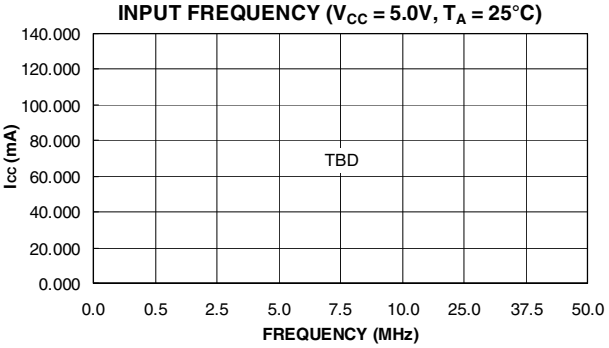
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



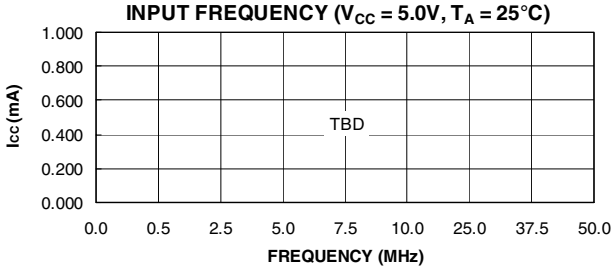
NORMALIZED I_{CC} VS. TEMP



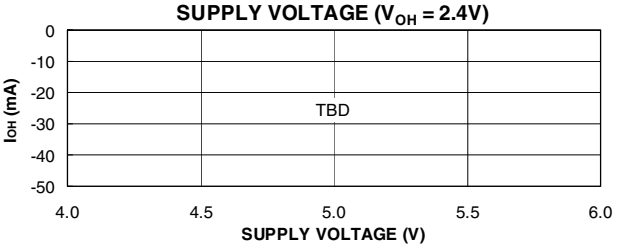
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



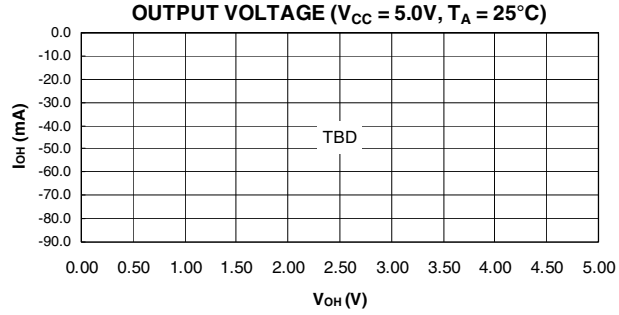
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



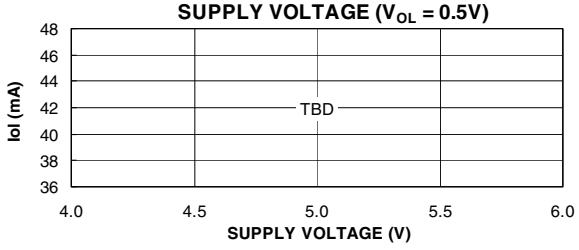
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



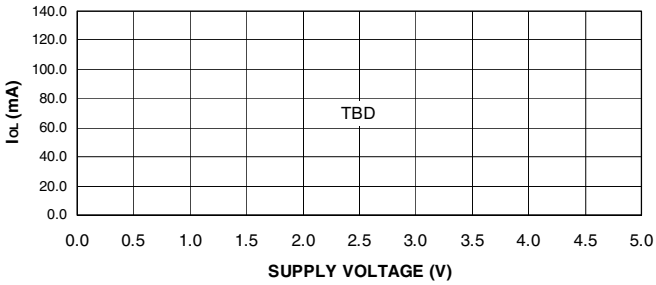
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



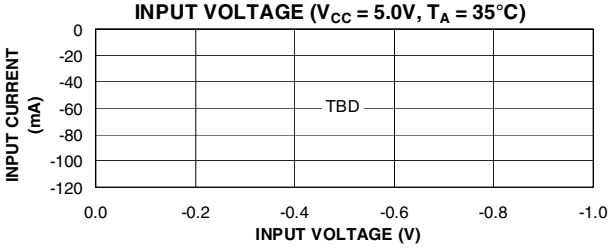
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



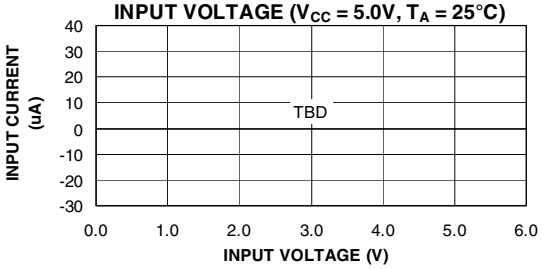
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



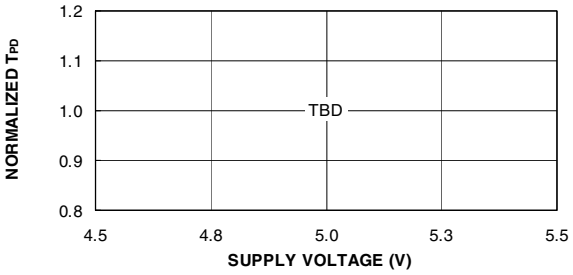
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



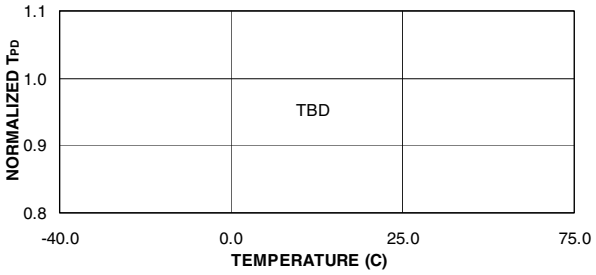
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



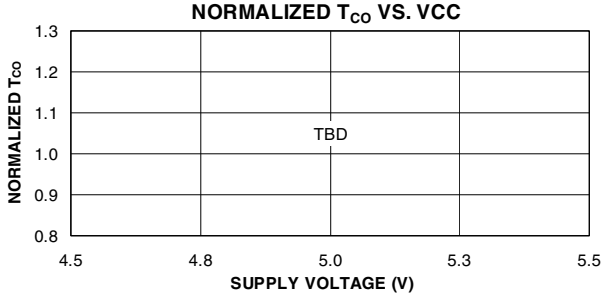
NORMALIZED T_{PD} VS. VCC



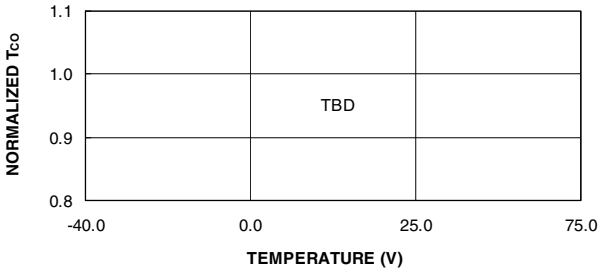
NORMALIZED T_{PD} VS. TEMP



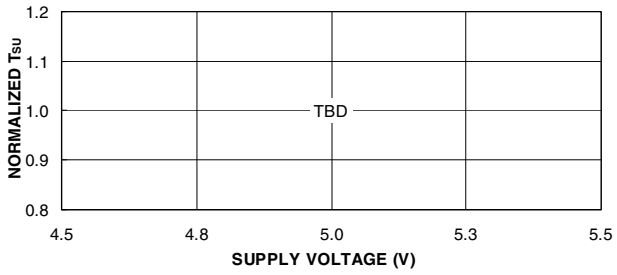
NORMALIZED T_{CO} VS. VCC



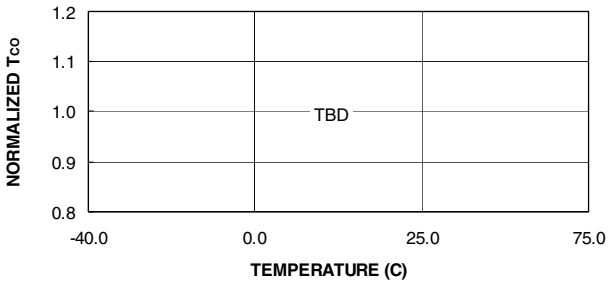
NORMALIZED T_{CO} VS. TEMP

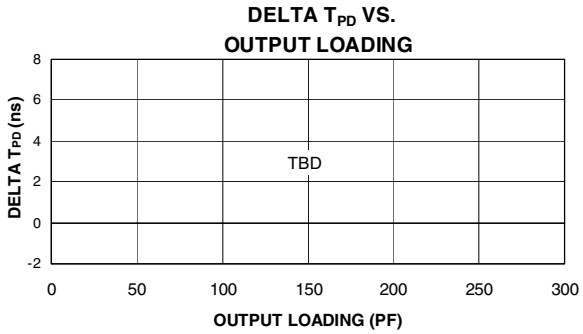


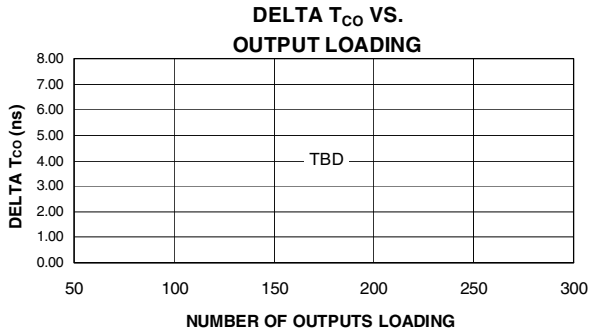
NORMALIZED T_{SU} VS. VCC

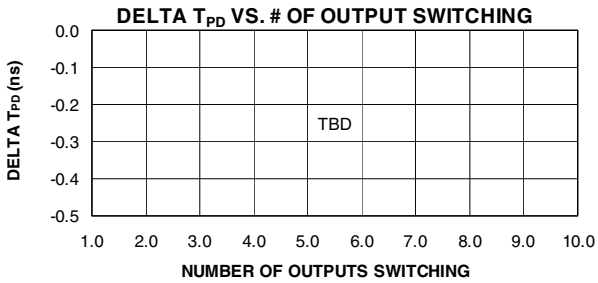


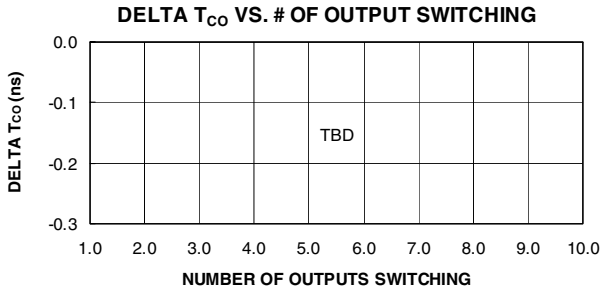
NORMALIZED T_{SU} VS. TEMP




DELTA T_{PD} VS.
OUTPUT LOADING
DELTA T_{PD} (ns)
8
6
4
2
0
-2
TBD
0
50
100
150
200
250
300
OUTPUT LOADING (PF)

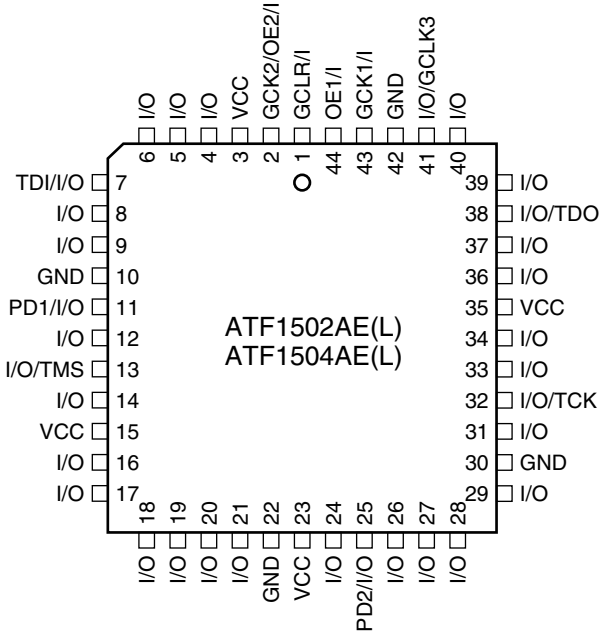

DELTA T_{CO} VS.
OUTPUT LOADING
DELTA T_{CO} (ns)
8.00
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
TBD
50
100
150
200
250
300
NUMBER OF OUTPUTS LOADING


DELTA T_{PD} VS. # OF OUTPUT SWITCHING
DELTA T_{PD} (ns)
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
TBD
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
NUMBER OF OUTPUTS SWITCHING

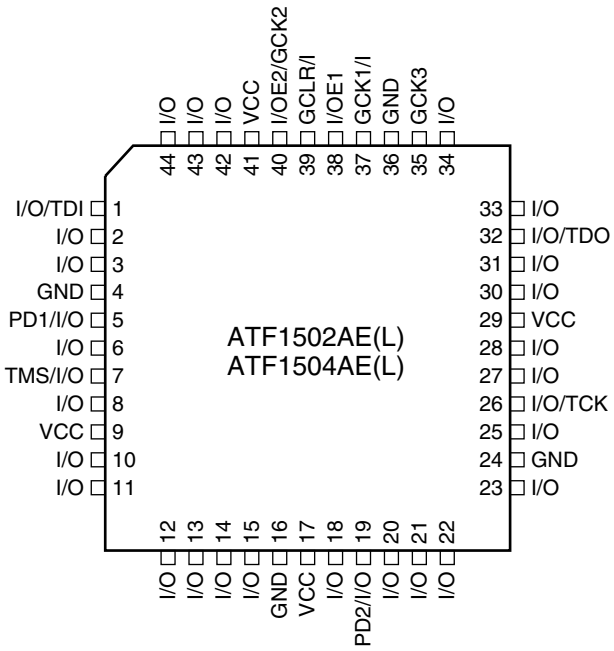

DELTA T_{CO} VS. # OF OUTPUT SWITCHING
DELTA T_{CO} (ns)
0.0
-0.1
-0.2
-0.3
TBD
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
NUMBER OF OUTPUTS SWITCHING

ATF1504AE(L) Pinouts

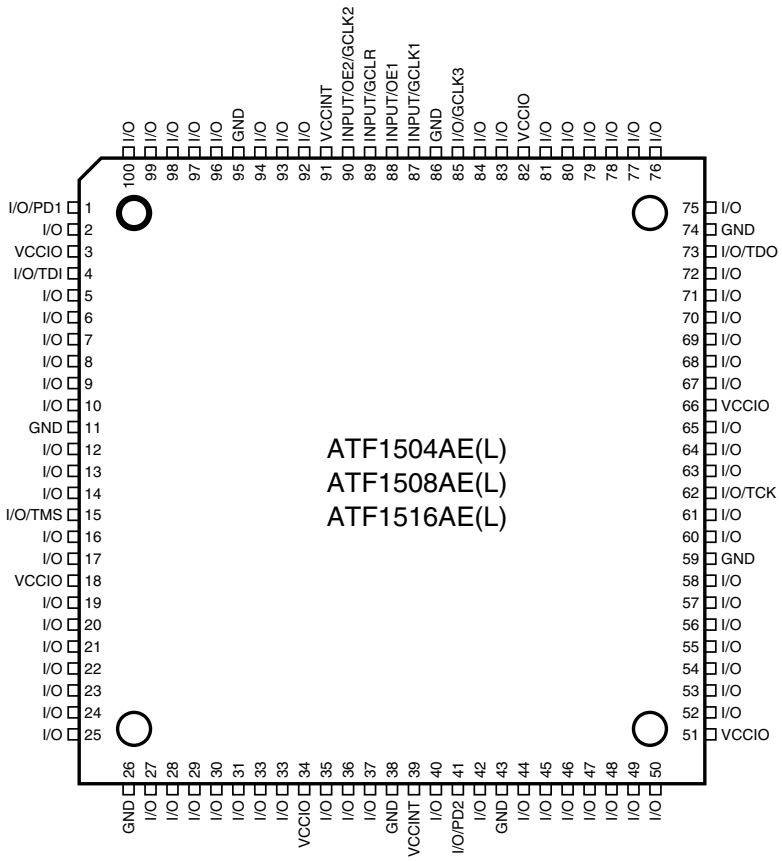
44-lead PLCC – Top View



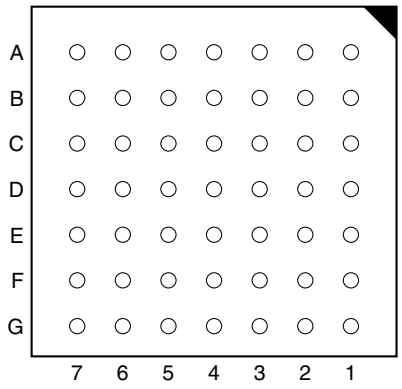
44-lead TQFP – Top View



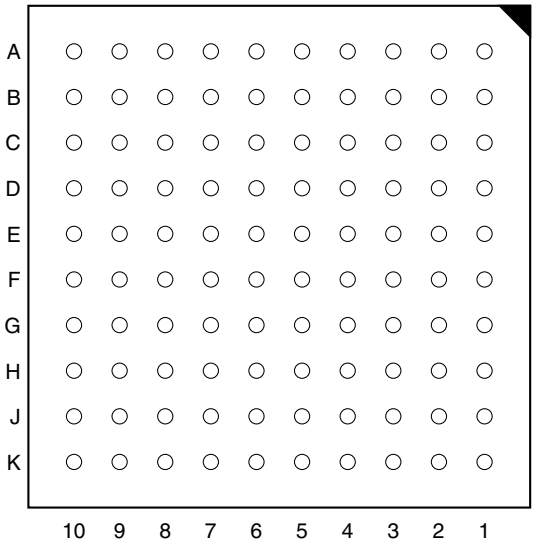
100-lead TQFP



ATF1504AE(L)
49-ball 0.8 mm Pitch
Bottom View



ATF1504AE(L)
ATF1508AE(L)
ATF1516AE(L)
100-ball 1.0 mm Pitch
Bottom View



ATF1504AE(L) Dedicated Pinouts

Dedicated Pin	44-lead TQFP	44-lead J-lead	49-ball BGA	100-ball BGA	100-lead TQFP
INPUT/OE2/GCLK2	40	2	B4	A5	90
INPUT/GCLR	39	1	A3	B5	89
INPUT/OE1	38	44	A4	B6	88
INPUT/GCLK1	37	43	A5	A6	87
I/O /GCLK3	35	41	C4	C6	85
I/O/PD (1,2)	5, 19	11, 25	D1, G5	E1, H6	12, 42
I/O/TDI (JTAG)	1	7	B1	A1	4
I/O/TMS (JTAG)	7	13	F1	F3	15
I/O/TCK (JTAG)	26	32	F7	F8	62
I/O/TDO (JTAG)	32	38	B7	A10	73
GNDINT	16, 36	22, 44	C2, E6	C3, D6, D7, E5, F6, G4, G5, H8	38, 86
GNDIO	4, 24	10, 30	B5, F4	–	11, 26, 43, 59, 74, 95
VCCINT	17, 41	3, 23	B3, E4	D5, G6	39, 91
VCCIO	9, 29	15, 35	C6, E2	C8, D4, E6, F5, G7, H3	3, 18, 34, 51, 66, 82
N/C	-	-	-	B1, B10, C1, C9, C10, D8, E3, E4, H1, H9, H10, J1, J2, J10, K1, K9	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78
# of Signal Pins	36	36	41	68	68
# User I/O Pins	32	32	37	64	64

OE (1, 2) Global OE pins
GCLR Global Clear pin
GCLK (1, 2, 3) Global Clock pins
PD (1, 2) Power-down pins
TDI, TMS, TCK, TDO JTAG pins used for boundary-scan testing or in-system programming
GNDINT Ground pins for the internal device logic
GNDIO Ground pins for the I/O pins
VCCINT VCC pins for the internal device logic
VCCIO VCC for the I/O drivers

ATF1504AE(L) I/O Pinouts

MC	PLC	44-lead PLCC	44-lead TQFP	49-ball BGA	84-lead PLCC	100-ball BGA	100-lead TQFP	MC	PLC	44-lead PLCC	44-lead TQFP	49-ball BGA	84-lead PLCC	100-ball BGA	100-lead TQFP
1	A	12	6	D2	22	F4	14	33	C	24	18	E5	44	K6	40
2	A	-	-	-	21	E2	13	34	C	-	-	-	45	J6	41
3	A/ **PD1**	11	5	D1	20	E1	12	35	C/ **PD2**	25	19	G5	46	H6	42
4	A	9	3	D4	18	D2	10	36	C	26	20	F5	48	K7	44
5	A	8	2	C1	17	D1	9	37	C	27	21	G6	49	J7	45
6	A	-	-	-	16	D3	8	38	C	-	-	-	50	H7	46
7	A	-	-	-	15	C2	6	39	C	-	-	G7	51	J8	47
8/ **TDI**	A	7	1	B1	14	A1	4	40	C	28	22	F6	52	K8	48
9	A	-	-	B2	12	B2	100	41	C	29	23	D5	54	K10	52
10	A	-	-	-	11	A2	99	42	C	-	-	-	55	J9	54
11	A	6	44	A1	10	A3	98	43	C	-	-	-	56	G9	56
12	A	-	-	-	9	B3	97	44	C	-	-	-	57	G10	57
13	A	-	-	-	8	A4	96	45	C	-	-	-	58	G8	58
14	A	5	43	A2	6	B4	94	46	C	31	25	E7	60	F9	60
15	A	-	-	-	5	C4	93	47	C	-	-	-	61	F10	61
16	A	4	42	C3	4	C5	92	48/ **TCK**	C	32	26	F7	62	F8	62
17	B	21	15	G4	41	K5	37	49	D	33	27	D7	63	F7	63
18	B	-	-	E3	40	J5	36	50	D	-	-	-	64	E9	64
19	B	20	14	G3	39	H5	35	51	D	34	28	D6	65	E10	65
20	B	19	13	F3	37	K4	33	52	D	36	30	C7	67	E8	67
21	B	18	12	G2	36	J4	32	53	D	37	31	B6	68	E7	68
22	B	-	-	G1	35	H4	31	54	D	-	-	-	69	D9	69
23	B	-	-	-	34	J3	30	55	D	-	-	-	70	D10	71
24	B	17	11	F2	33	K3	29	56/ **TDO**	D	38	32	B7	71	A10	73
25	B	16	10	D3	31	K2	25	57	D	39	33	A7	73	B9	75
26	B	-	-	-	30	H2	23	58	D	-	-	-	74	A9	76
27	B	-	-	-	29	G2	21	59	D	-	-	A6	75	A8	79
28	B	-	-	-	28	G1	20	60	D	-	-	-	76	B8	80
29	B	-	-	-	27	G3	19	61	D	-	-	-	77	A7	81
30	B	14	8	E1	25	F2	17	62	D	40	34	C5	79	B7	83
31	B	-	-	-	24	F1	16	63	D	-	-	-	80	C7	84
32/ **TMS**	B	13	7	F1	23	F3	15	64	D/ **GCLK3**	41	35	C4	81	C6	85

ATF1504AE(L) Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
4.5	3.1	225	ATF1504AE-4 AC44 ATF1504AE-4 JC44 ATF1504AE-4 CC49 ATF1504AE-4 AC100 ATF1504AE-4 CTC100	44A 44J 49C1 100A 100CT1	Commercial (0°C to 70°C)
7.5	5.1	133	ATF1504AE-7 AC44 ATF1504AE-7 JC44 ATF1504AE-7 CC49 ATF1504AE-7 AC100 ATF1504AE-7 CTC100	44A 44J 49C1 100A 100CT1	Commercial (0°C to 70°C)
			ATF1504AE-7 AI44 ATF1504AE-7 JI44 ATF1504AE-7 CI49 ATF1504AE-7 AI100 ATF1504AE-7 CTI100	44A 44J 49C1 100A 100CT1	Industrial (-40°C to +85°C)
10.0	7.0	100	ATF1504AE-10 AC44 ATF1504AE-10 JC44 ATF1504AE-10 CC49 ATF1504AE-10 AC100 ATF1504AE-10 CTC100	44A 44J 49C1 100A 100CT1	Commercial (0°C to 70°C)
			ATF1504AE-10 AI44 ATF1504AE-10 JI44 ATF1504AE-10 CI49 ATF1504AE-10 AI100 ATF1504AE-10 CTI100	44A 44J 49C1 100A 100CT1	Industrial (-40°C to +85°C)
15.0	9.0	77	ATF1504AEL-15 AC44 ATF1504AEL-15 JC44 ATF1504AEL-15 CC49 ATF1504AEL-15 AC100 ATF1504AEL-15CTC100	44A 44J 49C1 100A 100CT1	Commercial (0°C to 70°C)

Using “C” Product for Industrial

There is very little risk in using “C” devices for industrial applications because the V_{CC} conditions for 3.3V products are the same for commercial and industrial (there is only 15°C difference at the high end of the temperature range). To use commercial product for industrial temperature ranges, de-rate I_{CC} by 15%.

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
49C1	49-lead, Chip Scale Ball Grid Array (CBGA) 0.8 mm pitch
100A	100-lead, Very Thin Plastic Gull Wing Quad Flatpack (TQFP)
100CT1	100-lead, Tape Ball Grid Array (TBGA) 1.0 mm pitch

AC Characteristics ATF1508AE(L) (1)

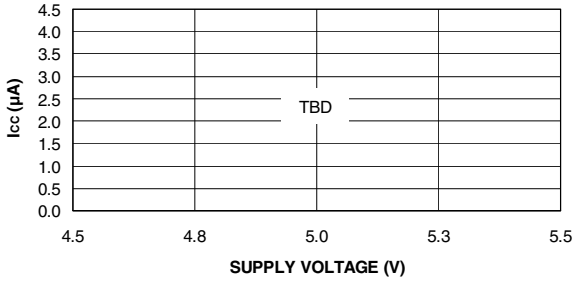
Symbol	Parameter	AE -5		AE -7		AE -10		AEL -15(6)		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		5		7.5		10	3		ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		5		7.5		10	3		ns
t_{SU}	Global Clock Setup Time	3.3		4.9		6.6		11		ns
t_{H}	Global Clock Hold Time	0		0		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	2.5		3		3		3		ns
t_{FH}	Global Clock Hold of Fast Input	0		0		0		1		MHz
t_{COP}	Global Clock to Output Delay	1	3.4	1	5	1	6.6		9	ns
t_{CH}	Global Clock High Time	2		3		4		5		ns
t_{CL}	Global Clock Low Time	2		3		4		5		ns
t_{ASU}	Array Clock Setup Time	1.8		2.8		3.8		5		ns
t_{AH}	Array Clock Hold Time	0.2		0.3		0.3		4		ns
t_{ACOP}	Array Clock Output Delay	1	4.9	1	7.1	1	9.4		15	ns
t_{ACH}	Array Clock High Time	2		3		4		6		ns
t_{ACL}	Array Clock Low Time	2		3		4		6		ns
t_{CNT}	Minimum Clock Global Period		5.2		7.7		10.2		13	ns
f_{CNT}(3)	Maximum Internal Global Clock Frequency	193		130		100		77		MHz
t_{ACNT}	Minimum Array Clock Period		5.2		7.7		10.2		13	ns
f_{ACNT}(4)	Maximum Internal Array Clock Frequency	193		130		100		77		MHz
f_{MAX}(5)	Maximum Clock Frequency	200		133		100		77		MHz
t_{IN}	Input Pad and Buffer Delay		0.7		1		1.4		2	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.7		1		1.4		2	ns
t_{FIN}	Fast Input Delay		2.5		3		3.4		2	ns
t_{SEXP}	Foldback Term Delay		2		2.9		3.8		8	ns
t_{PEXP}	Cascade Logic Delay		0.4		0.7		0.9		1	ns
t_{LAD}	Logic Array Delay		1.6		2.4		3.1		6	ns
t_{LAC}	Logic Control Delay		0.7		1		1.3		3.5	ns
t_{IOE}	Internal Output Enable Delay		0		0		0		3	ns
t_{OD1}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35pF)		0.8		1.2		1.6		3	ns
t_{OD2}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35pF)		1.3		1.7		2.1		3	ns
t_{OD3}	Output Buffer and Pad Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35pF)		5.8		6.2		6.6		5	ns
t_{ZX1}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35pF)		4		4		5		7	ns

AC Characteristics ATF1508AE(L) (Continued)[1]

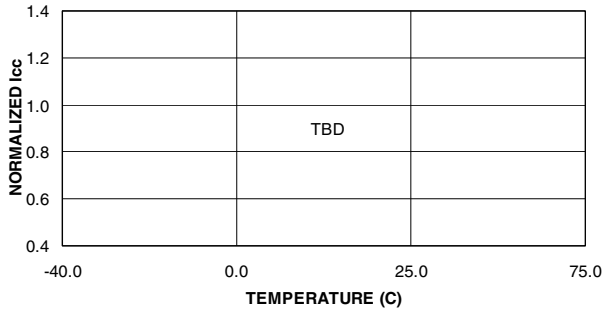
Symbol	Parameter	AE -5		AE -7		AE -10		AEL -15[6]		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZX2}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35pF)		4.5		4.5		5.5		7	ns
t_{ZX3}	Output Buffer Enable Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35pF)		9		9		10		10	ns
t_{XZ}	Output Buffer Disable Delay (C_L= 5pF)		4		4		5		6	ns
t_{SU}	Register Setup Time	1.4		2.1		2.9		5		ns
t_H	Register Hold Time	0.6		1		1.3		4		ns
t_{FSU}	Register Setup Time of Fast Input	1.1		1.6		1.6		2		ns
t_{FH}	Register Hold Time of Fast Input	1.4		1.4		1.4		2		ns
t_{RD}	Register Delay		0.8		1.2		1.6		2	ns
t_{COMB}	Combinatorial Delay		0.5		0.9		1.3		2	ns
t_{IC}	Array Clock Delay		1.2		1.7		2.2		6	ns
t_{EN}	Register Enable Time		0.7		1		1.3		6	ns
t_{GLOB}	Global Control Delay		1.1		1.6		2		2	ns
t_{PRE}	Register Preset Time		1.4		2		2.7		4	ns
t_{CLR}	Register Clear Time		1.4		2		2.7		4	ns
t_{UIM}	Switch Matrix Delay		1.4		2		2.6		2	ns
t_{RPA}[2]	Reduced Power Adder		4.0		4.0		5		10	ns

Notes:
1. See ordering Information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL} and t_{SEXP} parameters for macrocells running in the reduced-power mode.
3. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells). f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
4. f_{ACNT} is the fastest 16-bit counter frequency available, using the internal array clock, local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells).
5. f_{MAX} is the fastest available frequency for pipeline data.
6. For clocked applications and frequencies above $f_{critical}$, OR, non-clocked applications with dormant times less that $1/f_{critical}$, the device will achieve the speeds of the -10 column. (See “ITD/automatic power down.”)

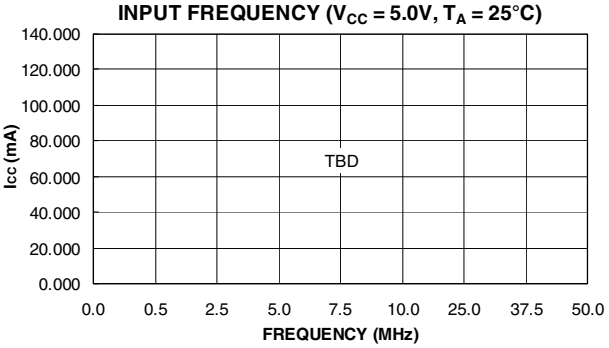
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



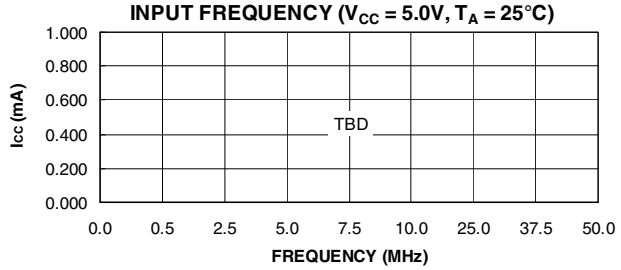
NORMALIZED I_{CC} VS. TEMP



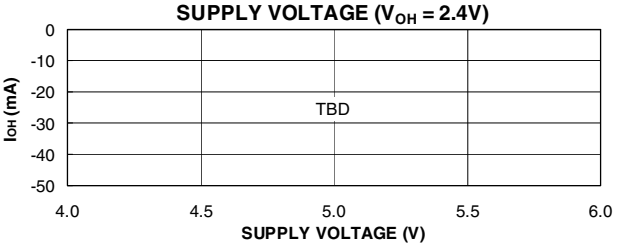
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



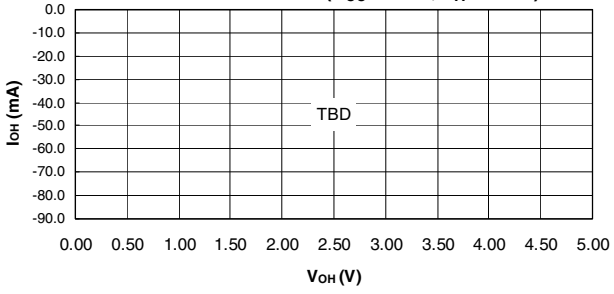
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



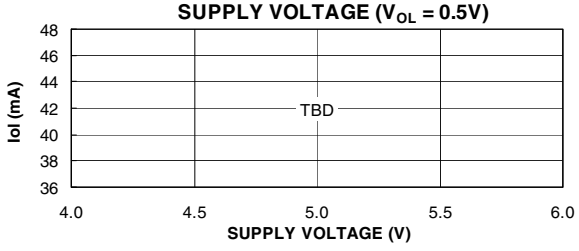
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



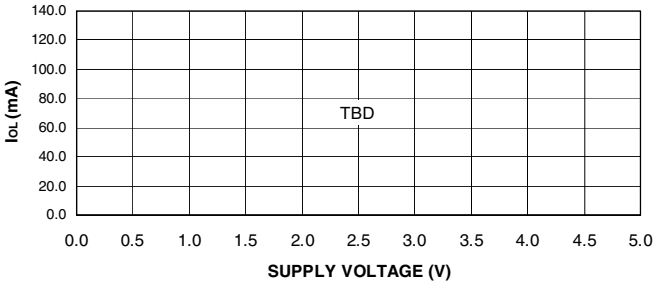
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



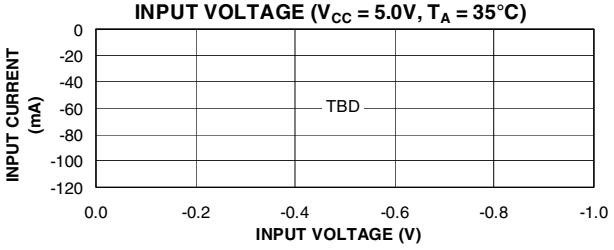
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



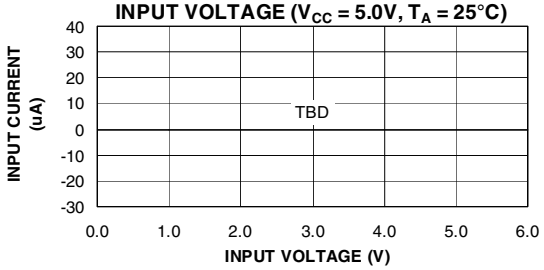
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



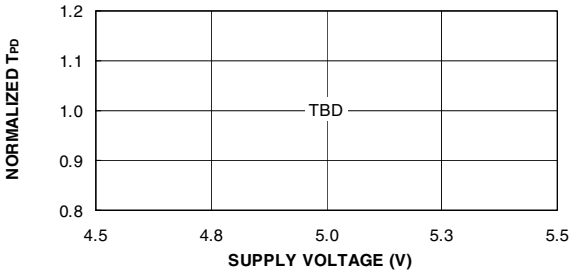
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



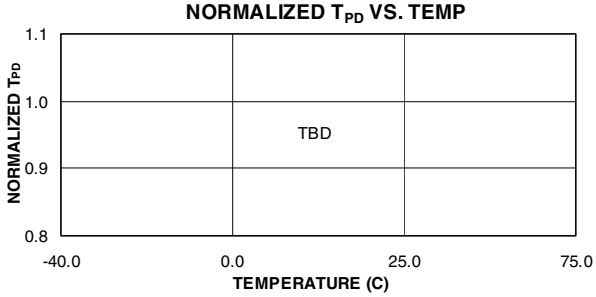
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



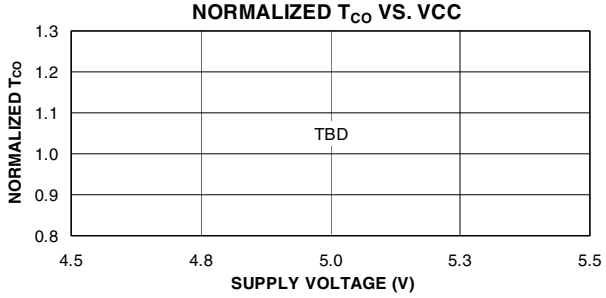
NORMALIZED T_{PD} VS. VCC



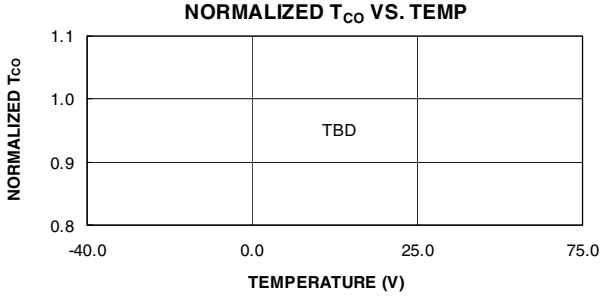
NORMALIZED T_{PD} VS. TEMP



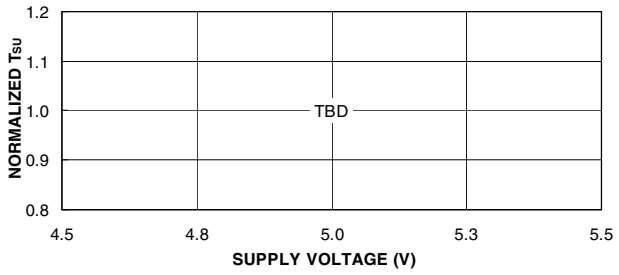
NORMALIZED T_{CO} VS. VCC



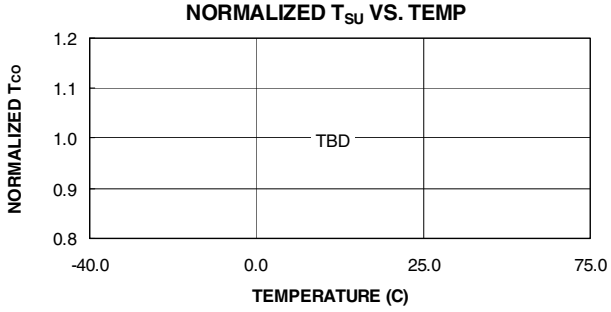
NORMALIZED T_{CO} VS. TEMP



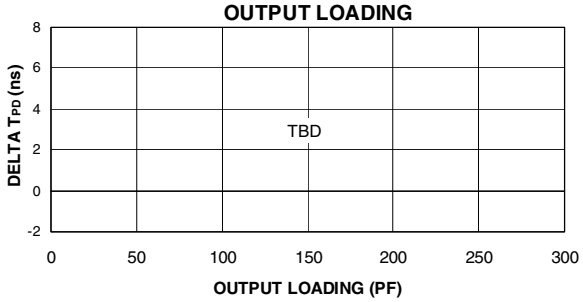
NORMALIZED T_{SU} VS. VCC



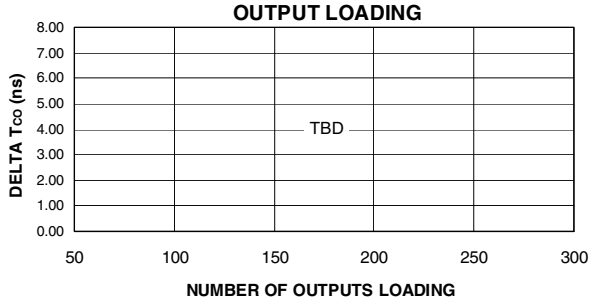
NORMALIZED T_{SU} VS. TEMP



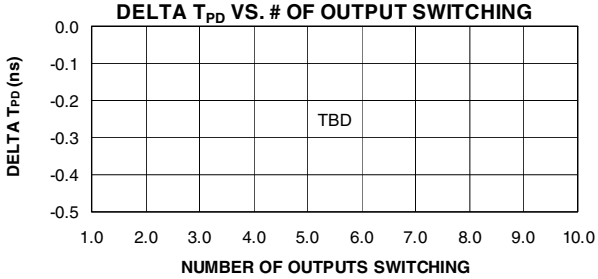
DELTA T_{PD} VS. OUTPUT LOADING



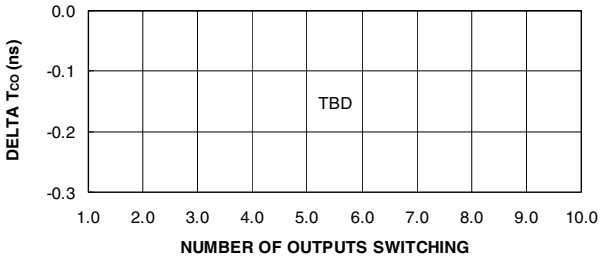
DELTA T_{CO} VS. OUTPUT LOADING



DELTA T_{PD} VS. # OF OUTPUT SWITCHING

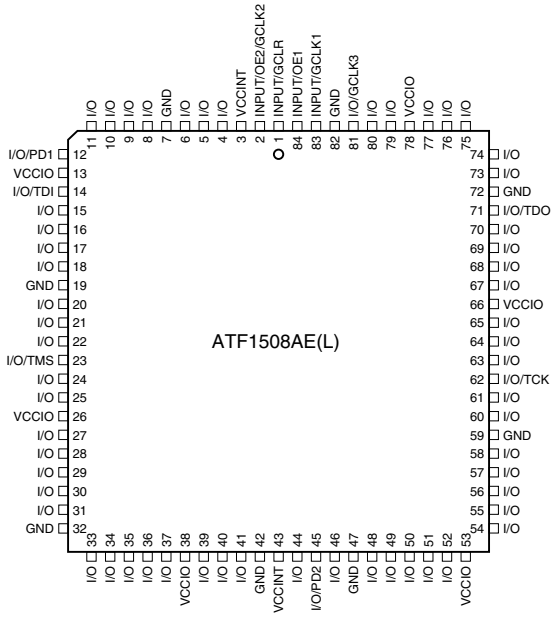


DELTA T_{CO} VS. # OF OUTPUT SWITCHING

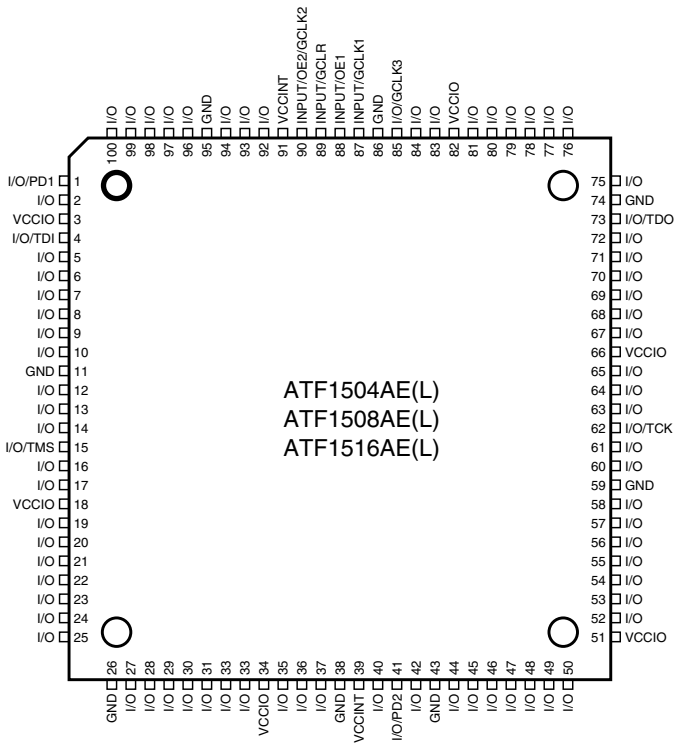


ATF1508AE(L) Pinouts

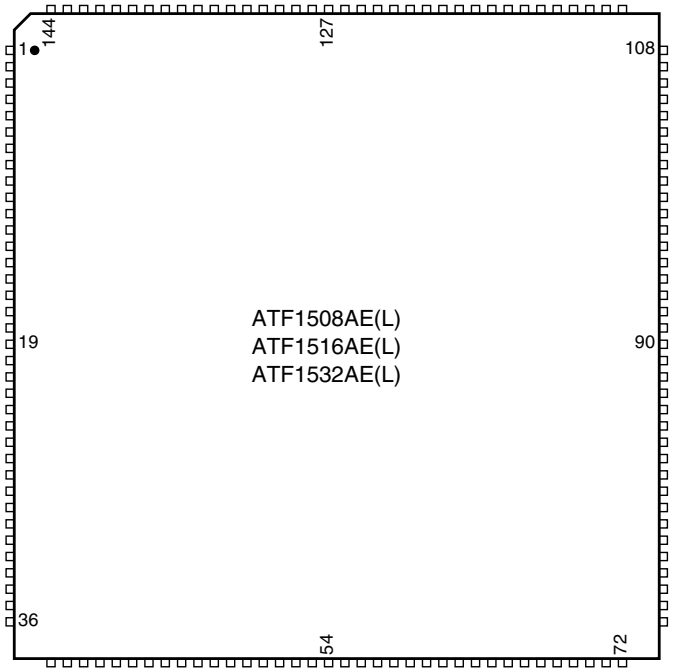
84-lead PLCC – Top View



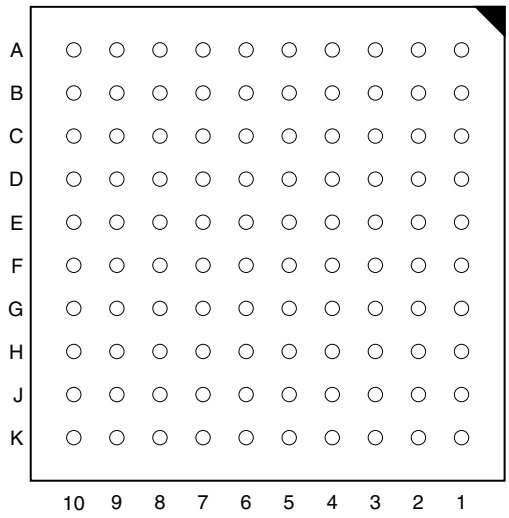
100-lead TQFP – Top View



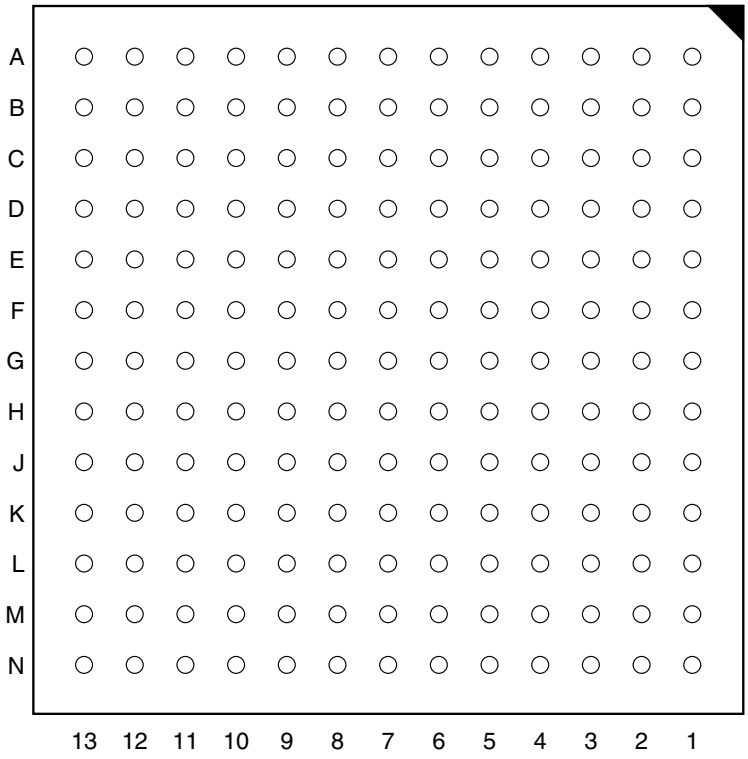
144-lead TQFP – Top View



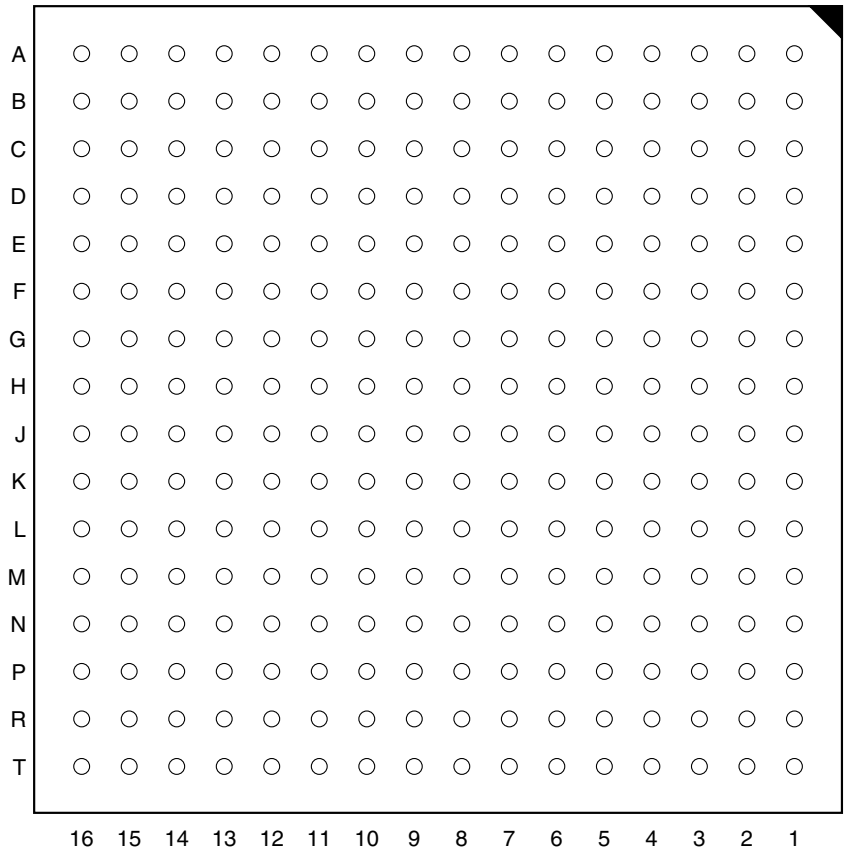
ATF1504AE(L)
ATF1508AE(L)
ATF1516AE(L)
100-ball 1.0 mm Pitch
Bottom View



ATF1508AE(L)
169-ball 0.8 mm Pitch
Bottom View



ATF1508AE(L)
ATF1516AE(L)
ATF1532AE(L)
256-ball 1.0 mm Pitch
Bottom View



ATF1508AE(L) Dedicated Pinouts

Dedicated Pin	84-pin J-Lead	100-pin TQFP	100-ball BGA	144-pin TQFP	169-ball BGA	256-ball BGA
INPUT/GCLK1	83	87	A6	125	D8	D9
INPUT/GCLR	1	89	B5	127	D6	E8
INPUT/OE1	84	88	B6	126	D7	E9
INPUT/OE2/GCK2	2	90	A5	128	E7	D8
I/O/GCLK3	81	85	C6	119	A8	F9
I/O PD (1,2)	12, 45	1,41	B1, J6	142, 61	D4, H8	E4, M9
TDI (JTAG)	14	4	A1	4	E4	D4
TMS (JTAG)	23	15	F3	20	J4	J6
TCK (JTAG)	62	62	F8	89	J10	J11
TDO (JTAG)	71	73	A10	104	E10	D13
GNDINT	42, 82	38,86	D6, G5	52, 57, 124, 129	A7, E8, J7, N7	A8, C9, G9, K8, P9
GNDIO	7, 19, 32, 47, 59, 72	11, 26, 43, 59, 74, 95	C3, D7, E5, F6, G4, H8	3, 13, 17, 33, 59, 64, 85, 105, 135	A3, A12, E1, F5, F13, H1, H9, J13, N2, N11	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT	3, 43	39, 91	D5, G6	51, 58, 123, 130	B7, E6, H7, M7	B9, C8, G8, K9, P8
VCCIO	13, 26, 38, 53, 66, 78	3, 18, 34, 51, 66, 82	C8, D4, E6, F5, G7, H3	24, 50, 73, 76, 95, 115, 144	A2, A11, E13, F1, F9, H5, H13, J1, N3, N12	B3, B5, C14, E15, F11, G3, G7, G15, H9, J8, K10, L3, L6, M15, P14, T2, T3
No Connect	-	-	-	1, 2, 12, 19, 34, 35, 36, 43, 46, 47, 48, 49, 66, 75, 90, 103, 108, 120, 121, 122	B5, B6, B8, B9, C5, C6, C7, C8, C9, C10, E2, E3, E11, E12, F2, F3, F11, F12, G1, G3, G11, G12, H2, H3, H11, H12, J2, J3, J11, J12, L4, L5, L6, L7, L8, L9, M5, M6, M8, M9	A1, A2, A4, A5, A6, A7, A9, A10, A11, A12, A13, A14, A15, A16, B1, B2, B4, B6, B7, B8, B11, B12, B13, B14, B15, B16, C1, C3, C4, C6, C11, C13, C15, C16, D1, D2, D3, D15, D16, E1, E2, E3, E14, E16, F1, F2, F15, F16, G1, G2, G14, G16, H1, H2, H15, H16, J1, J2, J15, J16, K1, K2, K3, K14, K15, K16, L1, L2, L15, L16, M1, M14, M16, N1, N2, N3, N14, N15, N16, P1, P2, P3, P4, P12, P13, P15, P16, R1, R4, R5, R6, R7, R8, R9, R11, R12, R13, R14, R15, R16, T4, T5, T6, T8, T9, T10, T11, T12, T13, T14, T16
# of Signal pins	68	84	84	100	100	100
# of User I/O pins	64	80	80	96	96	96

OE (1,2) Global OE pins.
GCLR Global Clear pin.
GCLK (1,2,3) Global Clock pins.
TDI, TMS, TCK, TDO JTAG pins used for In System Programming or Boundary-scan Testing.
GNDINT Ground pins for the internal device logic.
GNDIO Ground pins for the I/O drivers.
VCCINT VCC pins for the internal device logic.
VCCIO VCC pins for the I/O drivers.

ATF1508AE(L) I/O Pinouts

MC	PLB	84-pin J-Lead	100-pin TQFP	100-ball BGA	144-pin TQFP	169-ball BGA	256-ball BGA	MC	PLB	84-pin J-Lead	100-pin TQFP	100-ball BGA	144-pin TQFP	169-ball BGA	256-ball BGA
1	A	-	2	C1	143	E5	F4	33	C	-	25	K1	32	K4	N4
2	A	-	-	-	-	-	-	34	C	-	-	-	-	-	-
3/**PD1**	A	12	1	B1	142	D4	E4	35	C	31	24	J1	31	J5	M4
4	A	-	-	-	141	B2	C5	36	C	-	-	-	30	N1	M2
5	A	11	100	B2	140	B3	E5	37	C	30	23	H1	29	M1	L4
6	A	10	99	A2	139	C3	D5	38	C	29	22	H2	28	L1	L5
7	A	-	-	-	-	-	-	39	C	-	-	-	-	-	-
8	A	9	98	A3	138	C4	D6	40	C	28	21	G2	27	L2	K5
9	A	-	97	B3	137	B4	E6	41	C	-	20	G1	26	K3	K4
10	A	-	-	-	-	-	-	42	C	-	-	-	-	-	-
11	A	8	96	A4	136	A4	D7	43	C	27	19	G3	25	G6	K6
12	A	-	-	-	134	D5	C7	44	C	-	-	-	23	K2	J3
13	A	6	94	B4	133	A5	E7	45	C	25	17	F2	22	H4	J5
14	A	5	93	C4	132	F6	F7	46	C	24	16	F1	21	K1	J4
15	A	-	-	-	-	-	-	47	C	-	-	-	-	-	-
16	A	4	92	C5	131	A6	F8	48/ **TMS**	C	23	15	F3	20	J4	J6
17	B	22	14	F4	18	D1	J7	49	D	41	37	K5	56	N6	N8
18	B	-	-	-	-	-	-	50	D	-	-	-	-	-	-
19	B	21	13	E2	16	G5	H5	51	D	40	36	J5	55	K7	M8
20	B	-	-	-	15	D2	H3	52	D	-	-	-	54	N5	P7
21	B	20	12	E1	14	G4	H4	53	D	39	35	H5	53	H6	L8
22	B	-	10	E3	11	D3	H6	54	D	-	33	K4	45	N4	N7
23	B	-	-	-	-	-	-	55	D	-	-	-	-	-	-
24	B	18	9	E4	10	C1	H7	56	D	37	32	J4	44	K6	M7
25	B	17	8	D2	9	C2	G5	57	D	36	31	H4	42	M4	L7
26	B	-	-	-	-	-	-	58	D	-	-	-	-	-	-
27	B	16	7	D1	8	G7	G4	59	D	35	30	J3	41	J6	M6
28	B	-	-	-	7	B1	F3	60	D	-	-	-	40	M3	P5
29	B	15	6	D3	6	F4	G6	61	D	34	29	K3	39	L3	N6
30	B	-	5	C2	5	A1	F5	62	D	-	28	J2	38	M2	M5
31	B	-	-	-	-	-	-	63	D	-	-	-	-	-	-
32/ **TDI**	B	14	4	A1	4	E4	D4	64	D	33	27	K2	37	K5	N5

ATF1508AE(L) I/O Pinouts

MC	PLB	84-pin J-Lead	100-pin TQFP	100-ball BGA	144-pin TQFP	169-ball BGA	256-ball BGA	MC	PLB	84-pin J-Lead	100-pin TQFP	100-ball BGA	144-pin TQFP	169-ball BGA	256-ball BGA
65	E	44	40	K6	60	L10	N9	97	G	63	63	F7	91	G13	J10
66	E	-	-	-	-	-	-	98	G	-	-	-	-	-	-
67/ **PD2**	E	45	41	J6	61	H8	M9	99	G	64	64	E9	92	G10	H12
68	E	-	-	-	62	N8	R10	100	G	-	-	-	93	D13	H14
69	E	46	42	H6	63	K8	L9	101	G	65	65	E10	94	G9	H13
70	E	-	44	K7	65	N9	N10	102	G	-	67	E8	96	D12	H11
71	E	-	-	-	-	-	-	103	G	-	-	-	-	-	-
72	E	48	45	J7	67	J8	M10	104	G	67	68	E7	97	D11	H10
73	E	49	46	H7	68	M10	L10	105	G	68	69	D9	98	C13	G12
74	E	-	-	-	-	-	-	106	G	-	-	-	-	-	-
75	E	50	47	J8	69	K9	M11	107	G	69	70	D10	99	F10	G13
76	E	-	-	-	70	N10	P11	108	G	-	-	-	100	C12	F14
77	E	51	48	K8	71	K10	N11	109	G	70	71	D8	101	E9	G11
78	E	-	49	K9	72	L11	N12	110	G	-	72	C9	102	B13	F12
79	E	-	-	-	-	-	-	111	G	-	-	-	-	-	-
80	E	52	50	K10	74	M11	N13	112/ **TDO**	G	71	73	A10	104	E10	D13
81	F	-	52	J10	77	M12	M13	113	H	-	75	C10	106	A13	F13
82	F	-	-	-	-	-	-	114	H	-	-	-	-	-	-
83	F	54	53	H10	78	J9	L13	115	H	73	76	B10	107	D10	E13
84	F	-	-	-	79	N13	L14	116	H	-	-	-	109	B12	C12
85	F	55	54	H9	80	M13	L12	117	H	74	77	B9	110	D9	E12
86	F	56	55	J9	81	L13	M12	118	H	75	78	A9	111	C11	D12
87	F	-	-	-	-	-	-	119	H	-	-	-	-	-	-
88	F	57	56	G9	82	L12	K12	120	H	76	79	A8	112	B11	D11
89	F	-	57	G10	83	K13	K13	121	H	-	80	B8	113	B10	E11
90	F	-	-	-	-	-	-	122	H	-	-	-	-	-	-
91	F	58	58	G8	84	G8	K11	123	H	77	81	A7	114	F8	D10
92	F	-	-	-	86	K12	J14	124	H	-	-	-	116	A10	C10
93	F	60	60	F9	87	H10	J12	125	H	79	83	B7	117	F7	E10
94	F	61	61	F10	88	K11	J13	126	H	80	84	C7	118	A9	F10
95	F	-	-	-	-	-	-	127	H	-	-	-	-	-	-
96/ **TCK**	F	62	62	F8	89	J10	J11	128/ **GCLK3**	H	81	85	C6	119	A8	F9

ATF1508AE(L) Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
5.0	3.4	200	ATF1508AE-5 JC84 ATF1508AE-5 AC100 ATF1508AE-5 CTC100 ATF1508AE-5 AAC144 ATF1508AE-5 CC169 ATF1508AE-5 CTC256	84J 100A 100CT1 144AA 169C1 256CT1	Commercial (0°C to 70°C)
7.5	5.0	133	ATF1508AE-7 JC84 ATF1508AE-7 AC100 ATF1508AE-7 CTC100 ATF1508AE-7 AAC144 ATF1508AE-7 CC169 ATF1508AE-7 CTC256	84J 100A 100CT1 144AA 169C1 256CT1	Commercial (0°C to 70°C)
			ATF1508AE-7 JI84 ATF1508AE-7 AI100 ATF1508AE-7 CTI100 ATF1508AE-7 AAI144 ATF1508AE-7 CI169 ATF1508AE-7 CTI256	84J 100A 100CT1 144AA 169C1 256CT1	Industrial (-40°C to +85°C)
10.0	6.6	100	ATF1508AE-10 JC84 ATF1508AE-10 AC100 ATF1508AE-10 CTC100 ATF1508AE-10 AAC144 ATF1508AE-15 CC169 ATF1508AE-10 CTC256	84J 100A 100CT1 144AA 169C1 256CT1	Commercial (0°C to 70°C)
			ATF1508AE-10 JI84 ATF1508AE-10 AI100 ATF1508AE-10 CTI100 ATF1508AE-10 AAI144 ATF1508AE-10 CI169 ATF1508AE-10 CTI256	84J 100A 100CT1 144AA 169C1 256CT1	Industrial (-40°C to +85°C)
15.0	9.0	77	ATF1508AEL-15 JC84 ATF1508AEL-15 AC100 ATF1508AEL-15 CTC100 ATF1508AEL-15 AAC144 ATF1508AEL-15 CC169 ATF1508AEL-15 CTC256	84J 100A 100CT1 144AA 169C1 256CT1	Commercial (0°C to 70°C)

Using “C” Product for Industrial

There is very little risk in using “C” devices for industrial applications because the V_{CC} conditions for 3.3V products are the same for commercial and industrial (there is only 15°C difference at the high end of the temperature range). To use commercial product for industrial temperature ranges, de-rate I_{CC} by 15%.

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100A	100-lead, Very Thin Plastic Gull Wing Quad Flatpack (TQFP)
100CT1	100-lead, Tape Ball Grid Array (TBGA) 1.0 mm pitch
144AA	144-lead, Low Profile Plastic Gull Wing Quad Flatpack (TQFP)
169C1	169-lead, Chip Scale Ball Grid Array (CBGA) 0.8 mm pitch
256CT1	256-lead, Tape Ball Grid Array (TBGA) 1.0 mm pitch

AC Characteristics ATF1516AE(L) (1)

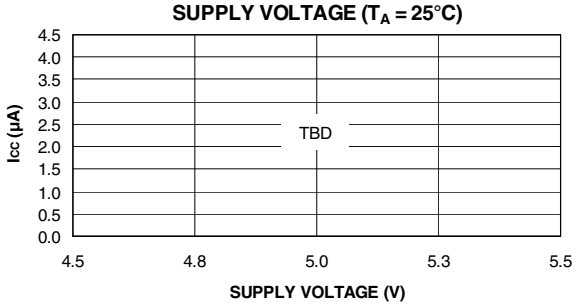
Symbol	Parameter	AE -5		AE -7		AE -10		AEL -15(6)		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		5.5		7.5		10		15	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		5.5		7.5		10		12	ns
t_{SU}	Global Clock Setup Time	3.9		5.2		6.9		11		ns
t_{H}	Global Clock Hold Time	0		0		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	2.5		3		3		3		ns
t_{FH}	Global Clock Hold of Fast Input	0		0		0		1		MHz
t_{COP}	Global Clock to Output Delay	1	3.5	1	4.8	1	6.4		9	ns
t_{CH}	Global Clock High Time	2		3		4		5		ns
t_{CL}	Global Clock Low Time	2		3		4		5		ns
t_{ASU}	Array Clock Setup Time	2.0		2.7		3.6		5		ns
t_{AH}	Array Clock Hold Time	0.2		0.3		0.5		4		ns
t_{ACOP}	Array Clock Output Delay	1	5.4	1	7.3	1	9.7		15	ns
t_{ACH}	Array Clock High Time	2		3		4		6		ns
t_{ACL}	Array Clock Low Time	2		3		4		6		ns
t_{CNT}	Minimum Clock Global Period		5.8		7.9		10.5		13	ns
f_{CNT}(3)	Maximum Internal Global Clock Frequency	175		125		100		77		MHz
t_{ACNT}	Minimum Array Clock Period		5.8		7.9		10.5		13	ns
f_{ACNT}(4)	Maximum Internal Array Clock Frequency	175		125		100		77		MHz
f_{MAX}(5)	Maximum Clock Frequency	200		133		100		77		MHz
t_{IN}	Input Pad and Buffer Delay		0.7		0.9		1.2		2	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.7		0.9		1.2		2	ns
t_{FIN}	Fast Input Delay		2.4		2.9		3.4		2	ns
t_{SEXP}	Foldback Term Delay		2.1		2.8		3.7		8	ns
t_{PEXP}	Cascade Logic Delay		0.3		0.5		0.6		1	ns
t_{LAD}	Logic Array Delay		1.7		2.2		2.8		6	ns
t_{LAC}	Logic Control Delay		0.8		1.0		1.3		3.5	ns
t_{IOE}	Internal Output Enable Delay		0		0		0		3	ns
t_{OD1}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35pF)		0.9		1.2		1.6		3	ns
t_{OD2}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35pF)		1.4		1.7		2.1		3	ns
t_{OD3}	Output Buffer and Pad Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35pF)		5.9		6.2		6.6		5	ns

AC Characteristics ATF1516AE(L) (Continued)[1]

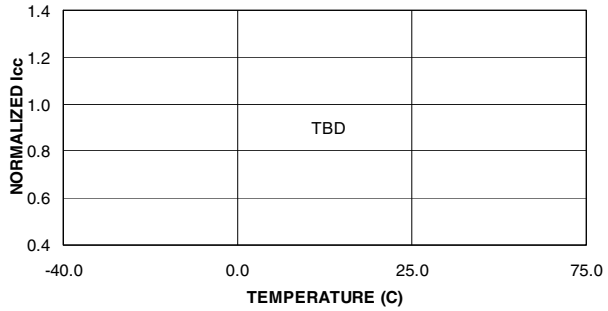
Symbol	Parameter	AE -5		AE -7		AE -10		AEL -15[6]		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZX1}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35pF)		4.0		4.0		5.0		7	ns
t_{ZX2}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35pF)		4.5		4.5		5.5		7	ns
t_{ZX3}	Output Buffer Enable Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35pF)		9		9		10		10	ns
t_{XZ}	Output Buffer Disable Delay (C_L= 5pF)		4		4		5		6	ns
t_{SU}	Register Setup Time	1.5		2.1		2.9		5		ns
t_H	Register Hold Time	0.7		0.9		1.2		4		ns
t_{FSU}	Register Setup Time of Fast Input	1.1		1.6		1.6		2		ns
t_{FH}	Register Hold Time of Fast Input	1.4		1.4		1.4		2		ns
t_{RD}	Register Delay		0.9		1.2		1.6		2	ns
t_{COMB}	Combinatorial Delay		0.5		0.8		1.2		2	ns
t_{IC}	Array Clock Delay		1.2		1.6		2.1		6	ns
t_{EN}	Register Enable Time		0.8		1.0		1.3		6	ns
t_{GLOB}	Global Control Delay		1.0		1.5		2.1		2	ns
t_{PRE}	Register Preset Time		1.6		2.3		3.0		4	ns
t_{CLR}	Register Clear Time		1.6		2.3		3.0		4	ns
t_{UIM}	Switch Matrix Delay		1.7		2.4		3.2		2	ns
t_{RPA}	Reduced Power Adder[2]		4.0		4.0		5.0		10	ns

Notes:
1. See ordering Information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL} and t_{SEXP} parameters for macrocells running in the reduced-power mode.
3. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells). f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
4. f_{ACNT} is the fastest 16-bit counter frequency available, using the internal array clock, local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells).
5. f_{MAX} is the fastest available frequency for pipeline data.
6. For clocked applications and frequencies above $f_{critical}$, OR, non-clocked applications with dormant times less that $1/f_{critical}$, the device will achieve the speeds of the -10 column. (See “ITD/automatic power down.”)

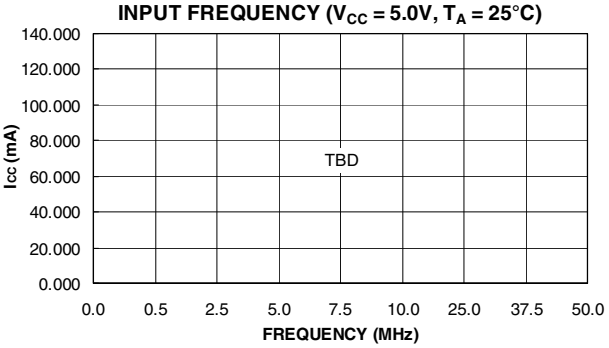
STAND-BY I_{CC} VS. SUPPLY VOLTAGE (T_A = 25°C)



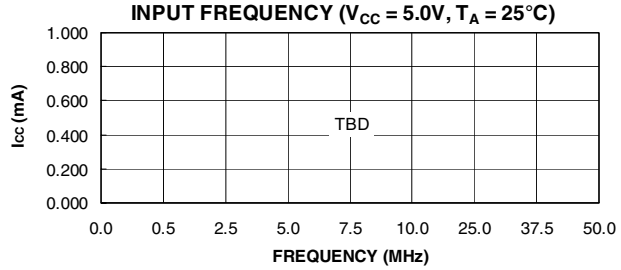
NORMALIZED I_{CC} VS. TEMP



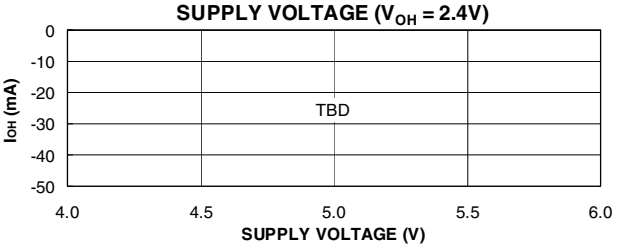
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



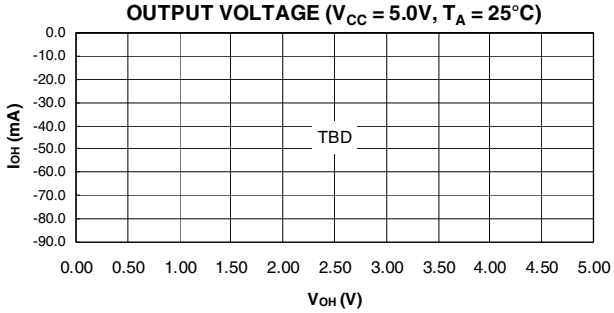
SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



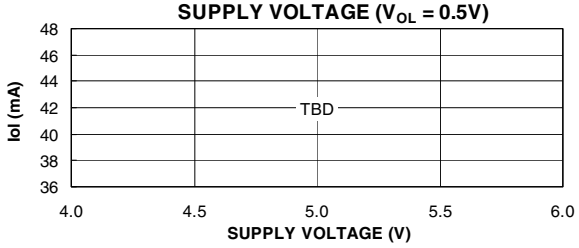
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



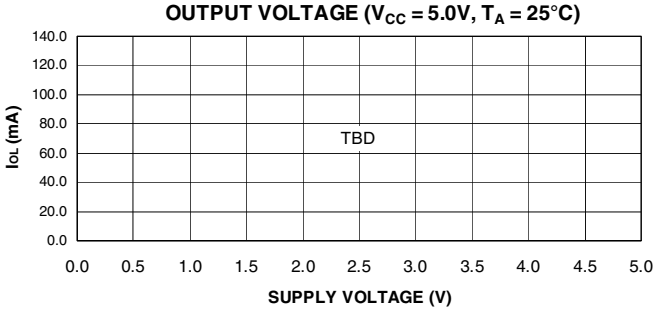
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



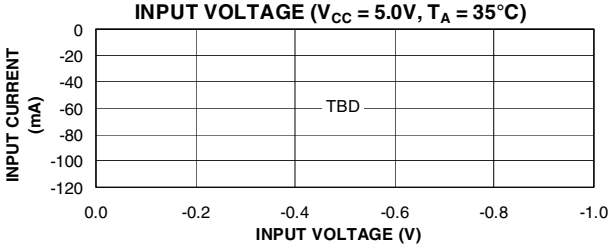
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



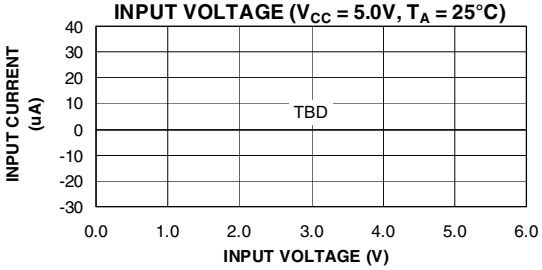
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



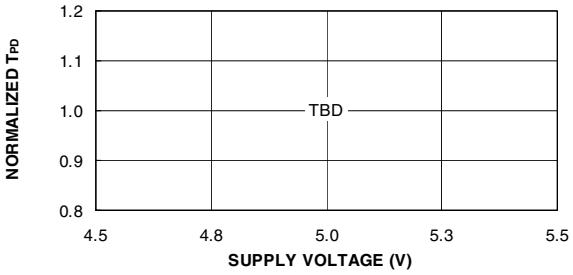
INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 35°C)



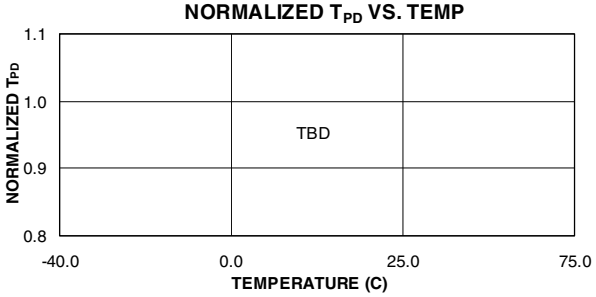
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



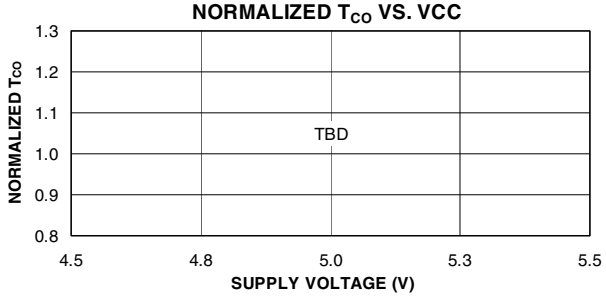
NORMALIZED T_{PD} VS. VCC



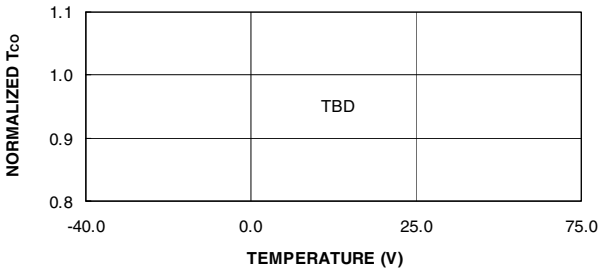
NORMALIZED T_{PD} VS. TEMP



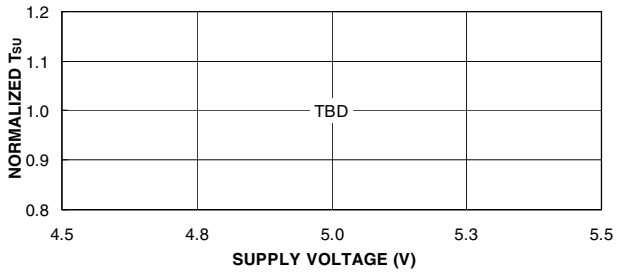
NORMALIZED T_{CO} VS. VCC



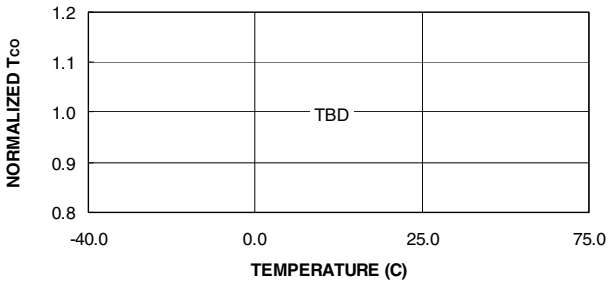
NORMALIZED T_{CO} VS. TEMP



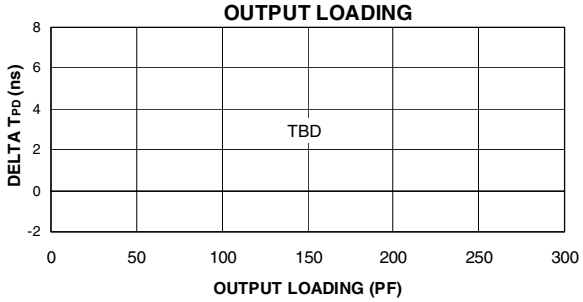
NORMALIZED T_{SU} VS. VCC



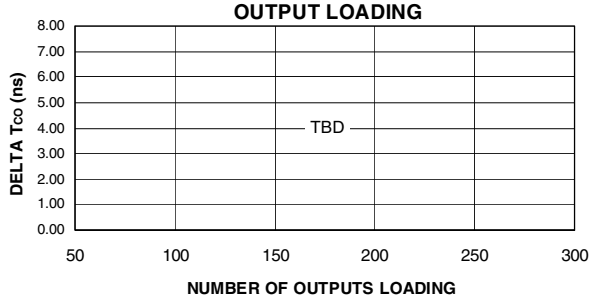
NORMALIZED T_{SU} VS. TEMP



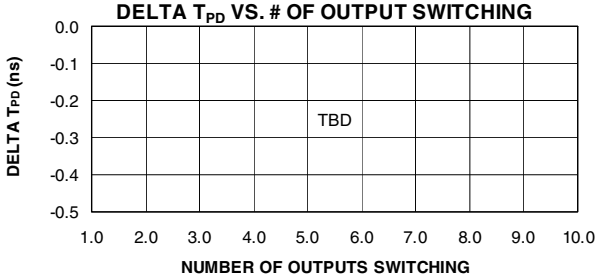
DELTA T_{PD} VS. OUTPUT LOADING



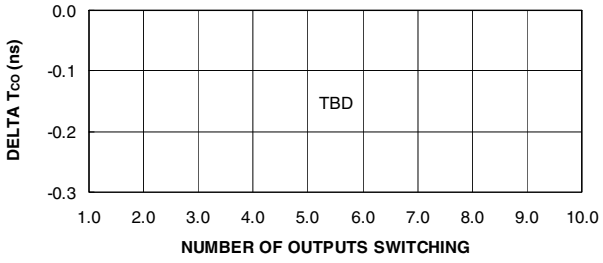
DELTA T_{CO} VS. OUTPUT LOADING



DELTA T_{PD} VS. # OF OUTPUT SWITCHING

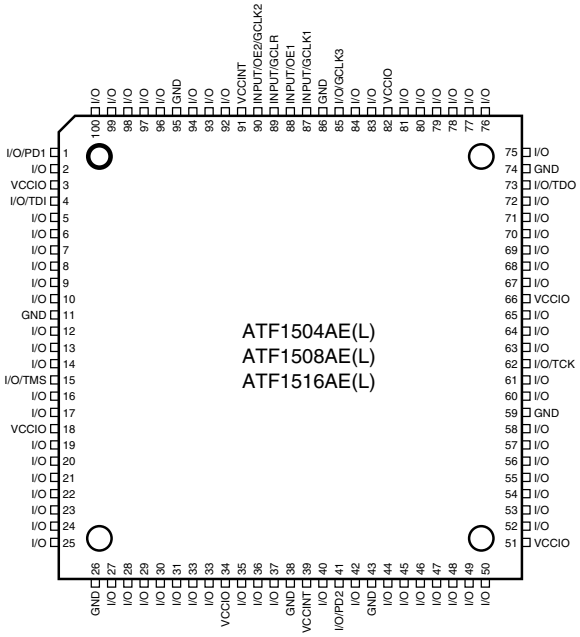


DELTA T_{CO} VS. # OF OUTPUT SWITCHING

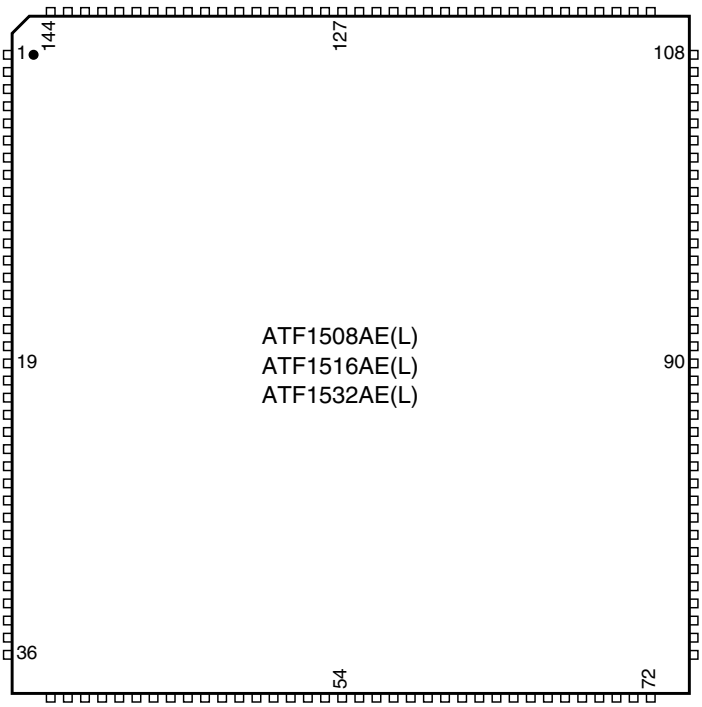


ATF1516AE(L) Pinouts

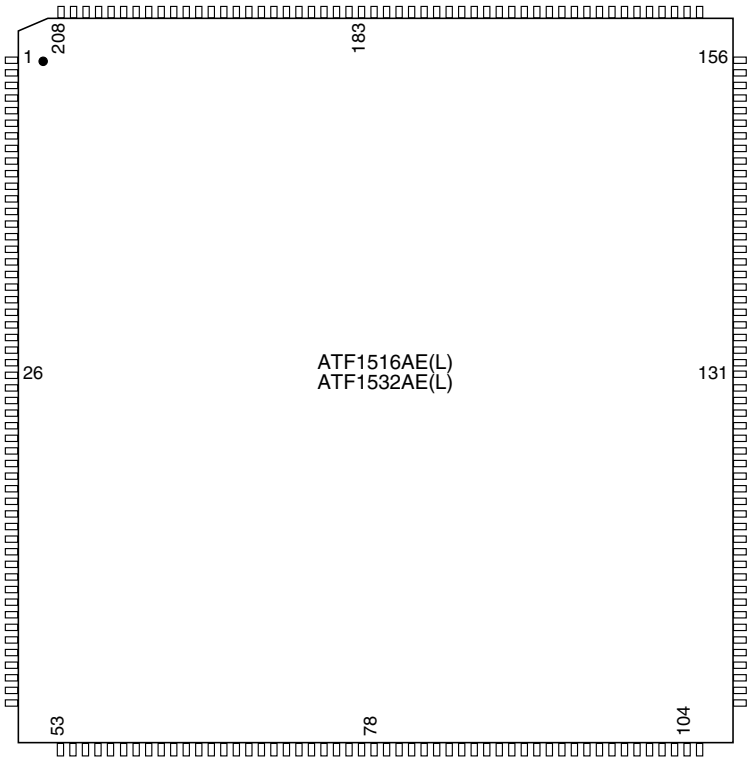
100-lead TQFP – Top View



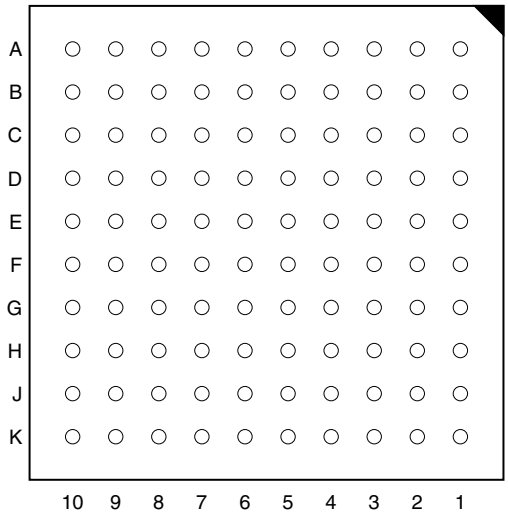
144-lead TQFP – Top View



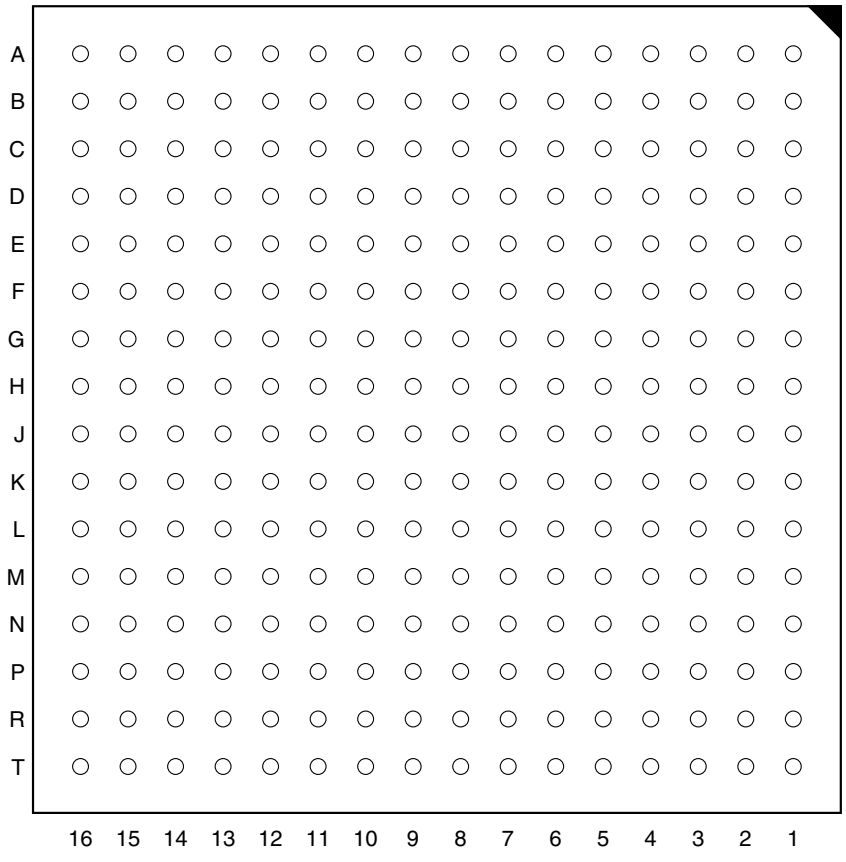
208-lead PQFP – Top View



ATF1504AE(L)
ATF1508AE(L)
ATF1516AE(L)
100-ball 1.0 mm Pitch – Bottom View



ATF1508AE(L)
ATF1516AE(L)
ATF1532AE(L)
256-ball 1.0 mm Pitch – Bottom View



ATF1516AE(L) Dedicated Pinouts

Dedicated Pin	100-pin TQFP	100-ball BGA	144-pin TQFP	208-pin PQFP	256-ball BGA
INPUT/GCLK1	87	A6	125	184	D9
INPUT/GCLR	89	B5	127	182	E8
INPUT/OE1	88	B6	126	183	E9
INPUT/OE2/GCK2	90	A5	128	181	D8
I/O/GCLK3	TBD	TBD	TBD	TBD	TBD
I/O PD (1,2)	TBD	TBD	TBD	TBD	TBD
TDI (JTAG)	4	A1	4	176	D4
TMS (JTAG)	15	F3	20	127	J6
TCK (JTAG)	62	F8	89	30	J11
TDO (JTAG)	73	A10	104	189	D13
GNDINT	38, 86	D6, G5	52, 57, 124, 129	75, 82, 180, 185	A8, C9, G9, K8, P9
GNDIO	11, 26, 43, 59, 74, 95	C3, D7, E5, F6, G4, H8	3, 13, 17, 33, 59, 64, 85, 105, 135	14, 32, 50, 72, 94, 116, 134, 152, 174, 200	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT	39, 91	D5, G6,	51, 58, 123, 130	74, 83, 179, 186	B9, C8, G8, K9, P8
VCCIO	3, 18, 34, 51, 66, 82	C8, D4, E6, F5, G7, H3	24, 50, 73, 76, 95, 115, 144	5, 23, 41, 63, 85, 107, 125, 143, 165, 191	B3, B5, C14, E15, F11, G3, G7, G15, H9, J8, K10, L3, L6, M15, P14, T2, T3
No Connect	-	-	-	1,2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208	A1, A2, A6, A12, A13, A14, A15, A16, B1, B2, B15, B16, C1, C15, C16, D1, D3, D15, D16, G1, G16, H15, H16, J1, K1, L1, L2, M1, M16, N1, N16, P1, P2, P15, P16, R1, R14, R15, R16, T7, T8, T10, T11, T14, T16
# of Signal pins	84	84	120	164	164
# of User I/O pins	80	80	116	160	160

OE (1,2) Global OE pins.
GCLR Global Clear pin.
GCLK (1,2,3) Global Clock pins.
TDI, TMS, TCK, TDO JTAG pins used for In System Programming or Boundary-scan Testing.
GNDINT Ground pins for the internal device logic.
GNDIO Ground pins for the I/O drivers.
VCCINT VCC pins for the internal device logic.
VCCIO VCC pins for the I/O drivers.

ATF1516AE(L) I/O Pinouts

MC	PLB	100-pin TQFP	100-ball BGA	144-pin TQFP	208-pin PQFP	256-ball BGA	MC	PLB	100-pin TQFP	100-ball BGA	144-pin TQFP	208-pin PQFP	256-ball BGA
1	A	-	C1	-	153	C3	33	C	-	-	36	108	N4
2	A	-	-	-	-	-	34	C	-	-	-	-	-
3	A	-	-	2	154	C4	35	C	-	-	35	109	P3
4	A	-	-	-	-	-	36	C	-	-	-	-	-
5	A	-	B1	1	159	E5	37	C	-	-	34	110	N3
6	A	-	-	143	160	D5	38	C	-	-	-	111	M4
7	A	-	-	-	-	-	39	C	-	-	-	-	-
8	A	2	-	-	161	C5	40	C	25	K1	32	112	M2
9	A	1	-	-	162	B4	41	C	24	J1	31	113	L4
10	A	-	-	-	-	-	42	C	-	-	-	-	-
11	A	100	B2	142	163	A4	43	C	23	H1	30	114	L5
12	A	-	-	-	-	-	44	C	-	-	-	-	-
13	A	-	-	141	164	A5	45	C	22	H2	29	115	K6
14	A	99	A2	140	166	D6	46	C	-	-	-	117	K5
15	A	-	-	-	-	-	47	C	-	-	-	-	-
16	A	98	A3	139	167	C6	48	C	21	G2	28	118	K4
17	B	-	-	-	141	F5	49	D	31	H4	44	92	N6
18	B	-	-	-	-	-	50	D	-	-	-	-	-
19	B	-	-	10	142	F2	51	D	30	J3	43	93	T5
20	B	-	-	-	-	-	52	D	-	-	-	-	-
21	B	-	-	9	144	E1	53	D	29	K3	42	95	M6
22	B	-	-	-	145	F4	54	D	28	J2	41	96	R5
23	B	-	-	-	-	-	55	D	-	-	-	-	-
24	B	8	D2	8	146	F3	56	D	-	-	40	97	M5
25	B	7	D1	7	147	E2	57	D	-	-	-	98	P5
26	B	-	-	-	-	-	58	D	-	-	-	-	-
27	B	6	D3	6	148	D2	59	D	-	-	39	99	N5
28	B	-	-	-	-	-	60	D	-	-	-	-	-
29	B	5	C2	5	149	E3	61	D	-	-	38	100	T4
30	B	-	-	-	150	E4	62	D	-	-	-	101	R4
31	B	-	-	-	-	-	63	D	-	-	-	-	-
32	B	4	A1	4	151	D4	64	D	27	K2	37	102	P4

ATF1516AE(L) I/O Pinouts

MC	PLB	100-pin TQFP	100-ball BGA	144-pin TQFP	208-pin PQFP	256-ball BGA	MC	PLB	100-pin TQFP	100-ball BGA	144-pin TQFP	208-pin PQFP	256-ball BGA
65	E	-	-	-	168	B6	97	G	-	-	-	119	K3
66	E	-	-	-	-	-	98	G	-	-	-	-	-
67	E	-	-	-	169	E6	99	G	-	-	27	120	K2
68	E	-	-	-	-	-	100	G	-	-	-	-	-
69	E	-	-	138	170	F7	101	G	-	-	26	121	J7
70	E	-	-	-	171	E7	102	G	-	-	-	122	H7
71	E	-	-	-	-	-	103	G	-	-	-	-	-
72	E	97	B3	137	172	D7	104	G	20	G1	25	123	J5
73	E	96	A4	136	173	C7	105	G	19	G3	23	124	J2
74	E	-	-	-	-	-	106	G	-	-	-	-	-
75	E	94	B4	134	175	B7	107	G	17	F2	22	126	J3
76	E	-	-	-	-	-	108	G	-	-	-	-	-
77	E	93	C4	133	176	A7	109	G	16	F1	21	127	J4
78	E	-	-	132	177	F8	110	G	-	-	-	128	H6
79	E	-	-	-	-	-	111	G	-	-	-	-	-
80	E	92	C5	131	178	B8	112	G	15	F3	20	129	J6
81	F	-	-	-	130	H5	113	H	37	K5	-	79	M8
82	F	-	-	-	-	-	114	H	-	-	-	-	-
83	F	-	-	19	131	H1	115	H	36	J5	54	80	N8
84	F	-	-	-	-	-	116	H	-	-	-	-	-
85	F	-	-	18	132	H2	117	H	-	-	53	81	L8
86	F	-	-	-	133	H3	118	H	35	H5	-	84	R7
87	F	-	-	-	-	-	119	H	-	-	-	-	-
88	F	14	F4	16	135	H4	120	H	-	-	49	86	P7
89	F	13	E2	15	136	G6	121	H	-	-	48	87	N7
90	F	-	-	-	-	-	122	H	-	-	-	-	-
91	F	12	E1	14	137	G5	123	H	-	-	47	88	M7
92	F	-	-	-	-	-	124	H	-	-	-	-	-
93	F	10	E3	12	138	G2	125	H	33	K4	46	89	L7
94	F	-	-	-	139	G4	126	H	-	-	-	90	T6
95	F	-	-	-	-	-	127	H	-	-	-	-	-
96	F	9	E4	11	140	F1	128	H	32	J4	45	91	R6

ATF1516AE(L) I/O Pinouts

MC	PLB	100-pin TQFP	100-ball BGA	144-pin TQFP	208-pin PQFP	256-ball BGA	MC	PLB	100-ball TQFP	100-pin BGA	144-pin TQFP	208-pin PQFP	256-ball BGA
129	I	80	B8	114	197	C11	161	K	-	-	-	38	K11
130	I	-	-	-	-	-	162	K	-	-	-	-	-
131	I	81	A7	116	196	B11	163	K	57	G10	82	37	K12
132	I	-	-	-	-	-	164	K	-	-	-	-	-
133	I	-	-	117	195	A11	165	K	-	-	83	36	K14
134	I	-	-	-	194	F10	166	K	-	-	-	35	K13
135	I	-	-	-	-	-	167	K	-	-	-	-	-
136	I	-	-	118	193	E10	168	K	58	G8	84	34	K15
137	I	-	-	119	192	A10	169	K	-	-	86	33	K16
138	I	-	-	-	-	-	170	K	-	-	-	-	-
139	I	83	B7	120	190	C10	171	K	60	F9	87	31	J13
140	I	-	-	-	-	-	172	K	-	-	-	-	-
141	I	84	C7	121	189	D10	173	K	61	F10	88	30	J14
142	I	-	-	-	188	F9	174	K	-	-	-	29	J12
143	I	-	-	-	-	-	175	K	-	-	-	-	-
144	I	85	C6	122	187	A9	176	K	62	F8	89	28	J11
145	J	63	F7	-	27	J15	177	L	-	-	-	78	R8
146	J	-	-	-	-	-	178	L	-	-	-	-	-
147	J	64	E9	90	26	J16	179	L	-	-	55	77	T9
148	J	-	-	-	-	-	180	L	-	-	-	-	-
149	J	65	E10	91	25	J10	181	L	-	-	56	76	R9
150	J	-	-	-	24	H14	182	L	-	-	-	73	N9
151	J	-	-	-	-	-	183	L	-	-	-	-	-
152	J	-	-	92	22	H13	184	L	40	K6	60	71	M9
153	J	-	-	93	21	H12	185	L	41	J6	61	70	L9
154	J	-	-	-	-	-	186	L	-	-	-	-	-
155	J	67	E8	94	20	H11	187	L	42	H6	62	69	R10
156	J	-	-	-	-	-	188	L	-	-	-	-	-
157	J	-	-	96	19	H10	189	L	44	K7	63	68	N10
158	J	-	-	-	18	G11	190	L	-	-	-	67	M10
159	J	-	-	-	-	-	191	L	-	-	-	-	-
160	J	68	E7	97	17	G14	192	L	45	J7	65	66	L10

ATF1516AE(L) I/O Pinouts

MC	PLB	100-pin TQFP	100-ball BGA	144-pin TQFP	208-pin PQFP	256-ball BGA	MC	PLB	100-pin TQFP	100-ball BGA	144-pin TQFP	208-pin PQFP	256-ball BGA
193	M	-	-	106	4	B14	225	O	-	-	-	49	R13
194	M	-	-	-	-	-	226	O	-	-	-	-	-
195	M	75	C10	107	3	C13	227	O	-	-	74	48	P13
196	M	-	-	-	-	-	228	O	-	-	-	-	-
197	M	-	-	108	206	B13	229	O	-	-	75	47	N13
198	M	-	-	-	205	F12	230	O	-	-	-	46	M14
199	M	-	-	-	-	-	231	O	-	-	-	-	-
200	M	-	-	109	204	E12	232	O	52	J10	77	45	M13
201	M	76	B10	110	203	D12	233	O	53	H10	78	44	L13
202	M	-	-	-	-	-	234	O	-	-	-	-	-
203	M	77	B9	111	202	C12	235	O	54	H9	79	43	L14
204	M	-	-	-	-	-	236	O	-	-	-	-	-
205	M	-	-	-	201	B12	237	O	55	J9	80	42	L12
206	M	78	A9	112	199	E11	238	O	-	-	-	40	L15
207	M	-	-	-	-	-	239	O	-	-	-	-	-
208	M	79	A8	113	198	D11	240	O	56	G9	81	39	L16
209	N	-	-	-	16	G13	241	P	46	H7	66	65	R11
210	N	-	-	-	-	-	242	P	-	-	-	-	-
211	N	69	D9	98	15	G12	243	P	47	J8	67	64	P11
212	N	-	-	-	-	-	244	P	-	-	-	-	-
213	N	-	-	99	13	F16	245	P	48	K8	68	62	N11
214	N	-	-	-	12	F15	246	P	49	K9	69	61	M11
215	N	-	-	-	-	-	247	P	-	-	-	-	-
216	N	70	D10	100	11	F13	248	P	-	-	-	60	T12
217	N	-	-	101	10	F14	249	P	-	-	70	59	R12
218	N	-	-	-	-	-	250	P	-	-	-	-	-
219	N	71	D8	102	9	E16	251	P	-	-	-	58	M12
220	N	-	-	-	-	-	252	P	-	-	-	-	-
221	N	72	C9	103	8	E14	253	P	-	-	71	57	P12
222	N	-	-	-	7	E13	254	P	-	-	-	56	N12
223	N	-	-	-	-	-	255	P	-	-	-	-	-
224	N	73	A10	104	6	D13	256	P	50	K10	72	55	T13

ATF1516AE(L) Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
5.5	3.5	200	ATF1516AE-5 AC100 ATF1516AE-5 CTC100 ATF1516AE-5 AAC144 ATF1516AE-5 QC208 ATF1516AE-5 CTC256	100A 100CT1 144AA 208Q1 256CT1	Commercial (0°C to 70°C)
7.5	4.8	133	ATF1516AE-7 AC100 ATF1516AE-7 CTC100 ATF1516AE-7 AAC144 ATF1516AE-7 QC208 ATF1516AE-7 CTC256	100A 100CT1 144AA 208Q1 256CT1	Commercial (0°C to 70°C)
			ATF1516AE-7 AI100 ATF1516AE-7 CTI100 ATF1516AE-7 AAI144 ATF1516AE-7 QI208 ATF1516AE-7 CTI256	100A 100CT1 144AA 208Q1 256CT1	Industrial (-40°C to +85°C)
10.0	6.4	100	ATF1516AE-10 AC100 ATF1516AE-10 CTC100 ATF1516AE-10 AAC144 ATF1516AE-10 QC208 ATF1516AE-10 CTC256	100A 100CT1 144AA 208Q1 256CT1	Commercial (0°C to 70°C)
			ATF1516AE-10 AI100 ATF1516AE-10 CTI100 ATF1516AE-10 AAI144 ATF1516AE-10 QI208 ATF1516AE-10 CTI256	100A 100CT1 144AA 208Q1 256CT1	Industrial (-40°C to +85°C)
15.0	9.0	77	ATF1508AEL-15 AC100 ATF1508AEL-15 CTC100 ATF1508AEL-15 AAC144 ATF1508AEL-15 QC208 ATF1508AEL-15 CTC256	100A 100CT1 144AA 208Q1 256CT1	Commercial (0°C to 70°C)

Using “C” Product for Industrial

There is very little risk in using “C” devices for industrial applications because the V_{CC} conditions for 3.3V products are the same for commercial and industrial (there is only 15°C difference at the high end of the temperature range). To use commercial product for industrial temperature ranges, de-rate I_{CC} by 15%.

Package Type	
100A	100-lead, Very Thin Plastic Gull Wing Quad Flatpack (TQFP)
100CT1	100-ball, Tape Ball Grid Array (TBGA) 1.0 mm pitch
144AA	144-lead, Low Profile Plastic Gull Wing Quad Flatpack (TQFP)
208Q1	208-lead, Plastic Quad Flatpack (PQFP)
256CT1	256-ball, Tape Ball Grid Array (TBGA) 1.0 mm pitch

AC Characteristics ATF1532AE(L) (1)

Symbol	Parameter	AE -7		AE -10		AE -12		AEL -15(6)		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		7.5		10		12		15	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		7.5		10		12		12	ns
t_{SU}	Global Clock Setup Time	5.6		7.6		9.1		11		ns
t_{H}	Global Clock Hold Time	0		0		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		3		3		ns
t_{FH}	Global Clock Hold of Fast Input	0		0		0		1		MHz
t_{COP}	Global Clock to Output Delay	1	4.7	1	6.3	1	7.5		9	ns
t_{CH}	Global Clock High Time	3		4		5		5		ns
t_{CL}	Global Clock Low Time	3		4		5		5		ns
t_{ASU}	Array Clock Setup Time	2.5		3.5		4.1		5		ns
t_{AH}	Array Clock Hold Time	0.2		0.3		0.4		4		ns
t_{ACOP}	Array Clock Output Delay	1	7.8	1	10.4	1	12.5		15	ns
t_{ACH}	Array Clock High Time	3		4		5		6		ns
t_{ACL}	Array Clock Low Time	3		4		5		6		ns
t_{CNT}	Minimum Clock Global Period		8.6		11.5		13.9		13	ns
f_{CNT}(3)	Maximum Internal Global Clock Frequency	120		90		75		70		MHz
t_{ACNT}	Minimum Array Clock Period		8.6		11.5		13.9		13	ns
f_{ACNT}(4)	Maximum Internal Array Clock Frequency	120		90		75		70		MHz
f_{MAX}(5)	Maximum Clock Frequency	133		100		80		66		MHz
t_{IN}	Input Pad and Buffer Delay		0.7		0.9		1.0		2	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.7		0.9		1.0		2	ns
t_{FIN}	Fast Input Delay		3.1		3.6		4.1		2	ns
t_{SEXP}	Foldback Term Delay		2.7		3.5		4.4		8	ns
t_{PEXP}	Cascade Logic Delay		0.4		0.5		0.6		1	ns
t_{LAD}	Logic Array Delay		2.2		2.8		3.5		6	ns
t_{LAC}	Logic Control Delay		1.0		1.3		3.5		3.5	ns
t_{IOE}	Internal Output Enable Delay		0		0		0		3	ns
t_{OD1}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35pF)		1.0		1.5		1.7		3	ns
t_{OD2}	Output Buffer and Pad Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35pF)		1.5		2.0		2.2		3	ns
t_{OD3}	Output Buffer and Pad Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35pF)		6.0		6.5		6.7		5	ns
t_{ZX1}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 5V; C_L= 35pF)		4		5		5		7	ns

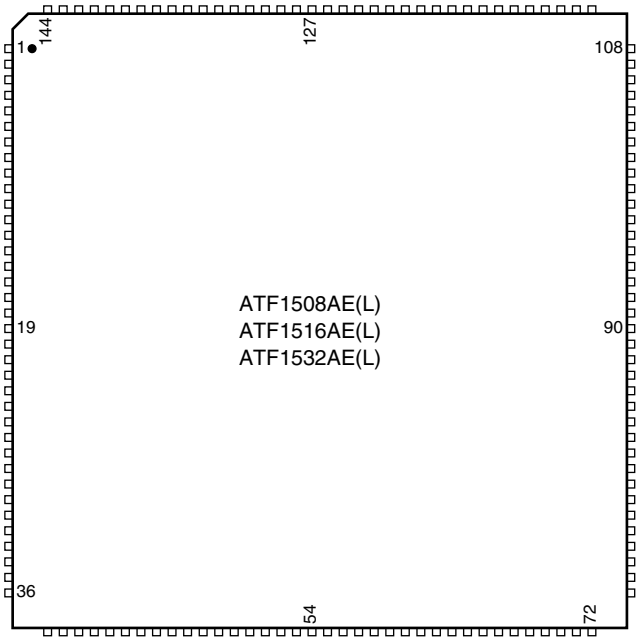
AC Characteristics ATF1532AE(L) (Continued)[1]

Symbol	Parameter	AE -7		AE -10		AE -12		AEL -15[6]		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZX2}	Output Buffer Enable Delay (slow slew rate = OFF; V_{CCIO} = 3.3V; C_L= 35pF)		4.5		5.5		5.5		7	ns
t_{ZX3}	Output Buffer Enable Delay (slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L= 35pF)		9		10		10		10	ns
t_{XZ}	Output Buffer Disable Delay (C_L= 5pF)		4		5		5		6	ns
t_{SU}	Register Setup Time	2.1		3.0		3.5		5		ns
t_H	Register Hold Time	0.6		0.8		1.0		4		ns
t_{FSU}	Register Setup Time of Fast Input	1.6		1.6		1.6		2		ns
t_{FH}	Register Hold Time of Fast Input	1.4		1.4		1.4		2		ns
t_{RD}	Register Delay		1.3		1.7		2.1		2	ns
t_{COMB}	Combinatorial Delay		0.6		0.8		1.0		2	ns
t_{IC}	Array Clock Delay		1.8		2.3		2.9		6	ns
t_{EN}	Register Enable Time		1.0		1.3		1.7		6	ns
t_{GLOB}	Global Control Delay		1.7		2.2		2.7		2	ns
t_{PRE}	Register Preset Time		1.0		1.4		1.7		4	ns
t_{CLR}	Register Clear Time		1.0		1.4		4.8		4	ns
t_{UIM}	Switch Matrix Delay		3.0		4.0		4.8		2	ns
t_{RPA}[2]	Reduced Power Adder		4.5		5.0		5.0		10	ns

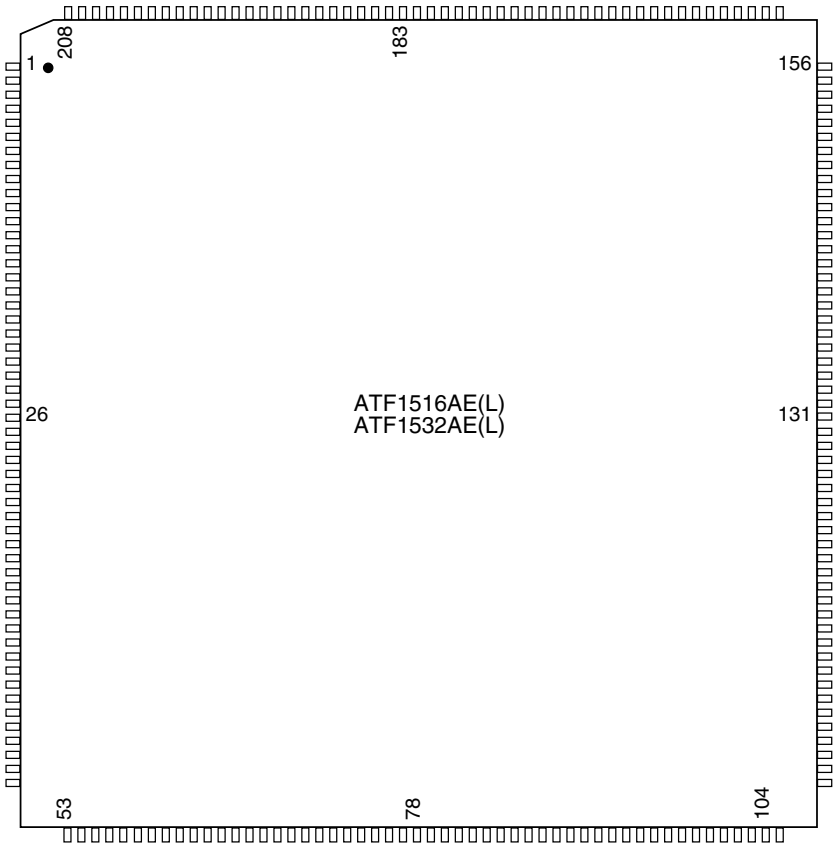
Notes:
1. See ordering Information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL} and t_{SEXP} parameters for macrocells running in the reduced-power mode.
3. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells). f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
4. f_{ACNT} is the fastest 16-bit counter frequency available, using the internal array clock, local feedback when applicable, and a PIA fan-out of one logic block (16 macrocells).
5. f_{MAX} is the fastest available frequency for pipeline data.
6. For clocked applications and frequencies above $f_{critical}$, OR, non-clocked applications with dormant times less that $1/f_{critical}$, the device will achieve the speeds of the -10 column. (See “ITD/automatic power down.”)

ATF1532AE(L) Pinouts

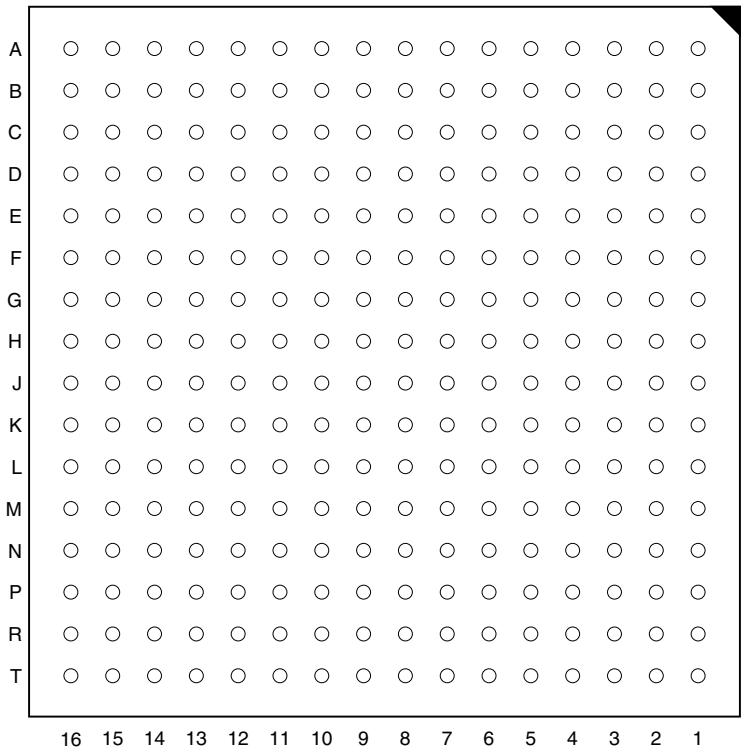
144-lead TQFP – Top View



208-lead PQFP – Top View



ATF1532AE(L)
256-ball 1.0 mm Pitch
Bottom View



ATF1532AE(L) Dedicated Pinouts

Dedicated Pin	144-pin TQFP	208-pin PQFP	256-ball BGA
INPUT/GCLK1	125	184	D9
INPUT/GCLR	127	182	E8
INPUT/OE1	126	183	E9
INPUT/OE2/GCK2	128	181	D8
I/O/GCLK3	TBD	TBD	TBD
I/O PD (1,2)	TBD	TBD	TBD
TDI (JTAG)	4	176	D4
TMS (JTAG)	20	127	J6
TCK (JTAG)	89	30	J11
TDO (JTAG)	104	189	D13
GNDINT	52, 57, 124, 129	75, 82, 180, 185	A8, C9, G9, K8, P9
GNDIO	3, 13, 17, 33, 59, 64, 85, 105, 135	14, 32, 50, 51, 94, 116, 134, 152, 158, 200	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT	51, 58, 123, 130	74, 83, 179, 186	B9, C8, G8, K9, P8
VCCIO	24, 50, 73, 76, 95, 115, 144	5, 23, 41, 63, 85, 105, 107, 125, 143, 165, 191, 207	B3, B5, C14, E15, F11, G3, G7, G15, H9, J8, K10, L3, L6, M15, P14, T2, T3
No Connect	-	-	-
# of Signal pins	120	176	212
# of User I/O pins	116	172	206

OE (1,2) Global OE pins.
GCLR Global Clear pin.
GCLK (1,2,3) Global Clock pins.
TDI, TMS, TCK, TDO JTAG pins used for In System Programming or Boundary-scan Testing.
GNDINT Ground pins for the internal device logic.
GNDIO Ground pins for the I/O drivers.
VCCINT VCC pins for the internal device logic.
VCCIO VCC pins for the I/O drivers.

ATF1532AE(L) I/O Pinouts

MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA	MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA
1	A	134	173	D7	33	C	142	163	E4
2	A	-	-	-	34	C	-	-	-
3	A	-	-	-	35	C	-	-	-
4	A	-	-	-	36	C	-	-	-
5	A	-	-	C7	37	C	141	164	C5
6	A	-	-	-	38	C	-	-	-
7	A	-	-	-	39	C	-	-	-
8	A	-	-	-	40	C	-	-	-
9	A	-	175	B7	41	C	140	166	A5
10	A	-	-	-	42	C	-	-	-
11	A	133	176	A7	43	C	-	167	D5
12	A	-	-	-	44	C	-	-	-
13	A	-	-	-	45	C	-	-	-
14	A	132	177	F8	46	C	139	168	E5
15	A	-	-	-	47	C	-	-	-
16	A	131	178	B8	48	C	-	-	E6
17	B	-	169	D6	49	D	2	-	B2
18	B	-	-	-	50	D	-	-	-
19	B	-	-	-	51	D	-	-	-
20	B	-	-	-	52	D	-	-	-
21	B	138	170	C6	53	D	1	-	A2
22	B	-	-	-	54	D	-	-	-
23	B	-	-	-	55	D	-	-	-
24	B	-	-	-	56	D	-	-	-
25	B	137	171	B6	57	D	-	159	B4
26	B	-	-	-	58	D	-	-	-
27	B	136	172	A6	59	D	-	160	A4
28	B	-	-	-	60	D	-	-	-
29	B	-	-	-	61	D	-	-	-
30	B	-	-	F7	62	D	-	161	C4
31	B	-	-	-	63	D	-	-	-
32	B	-	-	E7	64	D	143	162	C3

ATF1532AE(L) I/O Pinouts

MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA	MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA
65	E	-	-	E3	97	G	-	-	H6
66	E	-	-	-	98	G	-	-	-
67	E	7	153	C1	99	G	15	141	G5
68	E	-	-	-	100	G	-	-	-
69	E	-	-	B1	101	G	14	142	G4
70	E	-	-	-	102	G	-	-	-
71	E	-	-	-	103	G	-	-	-
72	E	-	-	-	104	G	-	-	-
73	E	-	154	A1	105	G	-	144	G4
74	E	-	-	-	106	G	-	-	-
75	E	6	155	D2	107	G	-	145	G1
76	E	-	-	-	108	G	-	-	-
77	E	-	-	-	109	G	-	-	-
78	E	5	156	D3	110	G	12	146	G6
79	E	-	-	-	111	G	-	-	-
80	E	4	157	D4	112	G	-	-	F5
81	F	-	147	F2	113	H	19	135	J1
82	F	-	-	-	114	H	-	-	-
83	F	-	148	F3	115	H	-	136	H7
84	F	-	-	-	116	H	-	-	-
85	F	11	149	F1	117	H	18	137	H5
86	F	-	-	-	118	H	-	-	-
87	F	-	-	-	119	H	-	-	-
88	F	-	-	-	120	H	-	-	-
89	F	-	-	F4	121	H	-	-	H2
90	F	-	-	-	122	H	-	-	-
91	F	10	150	E1	123	H	-	138	H3
92	F	-	-	-	124	H	-	-	-
93	F	-	-	-	125	H	-	-	-
94	F	9	151	D1	126	H	-	139	H1
95	F	-	-	-	127	H	-	-	-
96	F	8	-	E2	128	H	16	140	H4

ATF1532AE(L) I/O Pinouts

MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA	MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA
129	I	-	-	K1	161	K	29	115	N4
130	I	-	-	-	162	K	-	-	-
131	I	-	129	J7	163	K	-	117	M2
132	I	-	-	-	164	K	-	-	-
133	I	20	130	J6	165	K	-	118	M1
134	I	-	-	-	166	K	-	-	-
135	I	-	-	-	167	K	-	-	-
136	I	-	-	-	168	K	-	-	-
137	I	-	131	J5	169	K	28	119	M4
138	I	-	-	-	170	K	-	-	-
139	I	-	-	J4	171	K	-	-	M5
140	I	-	-	-	172	K	-	-	-
141	I	-	-	-	173	K	-	-	-
142	I	-	132	J3	174	K	-	120	L5
143	I	-	-	-	175	K	-	-	-
144	I	-	133	J2	176	K	27	121	L4
145	J	-	122	L2	177	L	34	109	R1
146	J	-	-	-	178	L	-	-	-
147	J	-	-	L1	179	L	-	-	-
148	J	-	-	-	180	L	-	-	-
149	J	26	123	K6	181	L	32	110	P2
150	J	-	-	-	182	L	-	-	-
151	J	-	-	-	183	L	-	-	-
152	J	-	-	-	184	L	-	-	-
153	J	25	124	K5	185	L	-	111	N3
154	J	-	-	-	186	L	-	-	-
155	J	23	126	K4	187	L	-	112	N2
156	J	-	-	-	188	L	-	-	-
157	J	-	-	-	189	L	-	-	-
158	J	22	127	K3	190	L	31	113	P1
159	J	-	-	-	191	L	-	-	-
160	J	21	128	K2	192	L	30	114	N1

ATF1532AE(L) I/O Pinouts

MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA	MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA
193	M	-	101	P5	225	O	47	88	R7
194	M	-	-	-	226	O	-	-	-
195	M	-	-	-	227	O	46	89	P7
196	M	-	-	-	228	O	-	-	-
197	M	-	102	N5	229	O	45	90	T7
198	M	-	-	-	230	O	-	-	-
199	M	-	-	-	231	O	-	-	-
200	M	-	-	-	232	O	-	-	-
201	M	37	103	T4	233	O	-	91	L8
202	M	-	-	-	234	O	-	-	-
203	M	-	104	R4	235	O	44	92	N7
204	M	-	-	-	236	O	-	-	-
205	M	-	-	-	237	O	-	-	-
206	M	36	106	P4	238	O	-	-	M7
207	M	-	-	-	239	O	-	-	-
208	M	35	108	P3	240	O	43	93	L7
209	N	42	95	R6	241	P	54	79	M9
210	N	-	-	-	242	P	-	-	-
211	N	-	-	-	243	P	-	-	-
212	N	-	-	-	244	P	-	-	-
213	N	41	96	T6	245	P	-	80	L9
214	N	-	-	-	246	P	-	-	-
215	N	-	-	-	247	P	-	-	-
216	N	-	-	-	248	P	-	-	-
217	N	40	97	N6	249	P	53	81	R8
218	N	-	-	-	250	P	-	-	-
219	N	39	98	M6	251	P	-	84	T8
220	N	-	-	-	252	P	-	-	-
221	N	-	-	-	253	P	-	-	-
222	N	-	99	R5	254	P	49	86	N8
223	N	-	-	-	255	P	-	-	-
224	N	38	100	T5	256	P	48	87	M8

ATF1532AE(L) I/O Pinouts

MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA	MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA
257	Q	55	78	N9	289	S	66	62	K11
258	Q	-	-	-	290	S	-	-	-
259	Q	-	-	-	291	S	-	-	-
260	Q	-	-	-	292	S	-	-	-
261	Q	-	77	T9	293	S	67	61	M12
262	Q	-	-	-	294	S	-	-	-
263	Q	-	-	-	295	S	-	-	-
264	Q	-	-	-	296	S	-	-	-
265	Q	56	76	R9	297	S	68	60	N12
266	Q	-	-	-	298	S	-	-	-
267	Q	-	73	L10	299	S	69	59	T12
268	Q	-	-	-	300	S	-	-	-
269	Q	-	-	-	301	S	-	-	-
270	Q	60	71	M10	302	S	-	58	R12
271	Q	-	-	-	303	S	-	-	-
272	Q	61	70	N10	304	S	70	57	T13
273	R	62	69	R10	305	T	-	56	P12
274	R	-	-	-	306	T	-	-	-
275	R	63	68	T10	307	T	-	-	-
276	R	-	-	-	308	T	-	-	-
277	R	-	67	M11	309	T	-	55	T14
278	R	-	-	-	310	T	-	-	-
279	R	-	-	-	311	T	-	-	-
280	R	-	-	-	312	T	-	-	-
281	R	-	66	N11	313	T	71	54	P13
282	R	-	-	-	314	T	-	-	-
283	R	65	65	P11	315	T	72	53	R13
284	R	-	-	-	316	T	-	-	-
285	R	-	-	-	317	T	-	-	-
286	R	-	-	R11	318	T	-	52	R14
287	R	-	-	-	319	T	-	-	-
288	R	-	64	T11	320	T	74	49	R15

ATF1532AE(L) I/O Pinouts

MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA	MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA
321	U	75	48	P15	353	W	82	35	L16
322	U	-	-	-	354	W	-	-	-
323	U	-	-	-	355	W	-	-	L13
324	U	-	-	-	356	W	-	-	-
325	U	-	47	N15	357	W	83	34	L12
326	U	-	-	-	358	W	-	-	-
327	U	-	-	-	359	W	-	-	-
328	U	-	-	-	360	W	-	-	-
329	U	-	46	T16	361	W	84	33	K12
330	U	-	-	-	362	W	-	-	-
331	U	-	45	R16	363	W	86	31	K14
332	U	-	-	-	364	W	-	-	-
333	U	-	-	-	365	W	-	-	-
334	U	77	44	P16	366	W	87	30	K15
335	U	-	-	-	367	W	-	-	-
336	U	78	43	N14	368	W	88	29	K16
337	V	79	42	N16	369	X	89		J11
338	V	-	-	-	370	X	-	-	-
339	V	80	40	M14	371	X	-	28	J12
340	V	-	-	-	372	X	-	-	-
341	V	-	39	N13	373	X	-	27	J13
342	V	-	-	-	374	X	-	-	-
343	V	-	-	-	375	X	-	-	-
344	V	-	-	-	376	X	-	-	-
345	V	81	38	M16	377	X	-	26	J14
346	V	-	-	-	378	X	-	-	-
347	V	-	-	M13	379	X	-	-	J15
348	V	-	-	-	380	X	-	-	-
349	V	-	-	-	381	X	-	-	-
350	V	-	37	L14	382	X	-	25	K13
351	V	-	-	-	383	X	-	-	-
352	V	-	36	L15	384	X	90	24	J16

ATF1532AE(L) I/O Pinouts

MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA	MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA
385	Y	91	22	H10	417	AA	-	10	F14
386	Y	-	-	-	418	AA	-	-	-
387	Y	-	21	H11	419	AA	-	9	F15
388	Y	-	-	-	420	AA	-	-	-
389	Y	92	20	H12	421	AA	98	8	F16
390	Y	-	-	-	422	AA	-	-	-
391	Y	-	-	-	423	AA	-	-	-
392	Y	-	-	-	424	AA	-	-	-
393	Y	-	-	H15	425	AA	-	-	E12
394	Y	-	-	-	426	AA	-	-	-
395	Y	-	19	H16	427	AA	99	7	E13
396	Y	-	-	-	428	AA	-	-	-
397	Y	-	-	-	429	AA	-	-	-
398	Y	-	18	H14	430	AA	100	6	E14
399	Y	-	-	-	431	AA	-	-	-
400	Y	93	17	H13	432	AA	101	-	E16
401	Z	-	-	G12	433	BB	-	-	D16
402	Z	-	-	-	434	BB	-	-	-
403	Z	-	16	G13	435	BB	102	4	C16
404	Z	-	-	-	436	BB	-	-	-
405	Z	94	15	G14	437	BB	-	-	B16
406	Z	-	-	-	438	BB	-	-	-
407	Z	-	-	-	439	BB	-	-	-
408	Z	-	-	-	440	BB	-	-	-
409	Z	96	13	G16	441	BB	-	3	A16
410	Z	-	-	-	442	BB	-	-	-
411	Z	-	12	G11	443	BB	103	2	D15
412	Z	-	-	-	444	BB	-	-	-
413	Z	-	-	-	445	BB	-	-	-
414	Z	97	11	F12	446	BB	104	1	D13
415	Z	-	-	-	447	BB	-	-	-
416	Z	-	-	F13	448	BB	106	208	C15

ATF1532AE(L) I/O Pinouts

MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA	MC	PLB	144-pin TQFP	208-pin PQFP	256-ball BGA
449	CC	-	-	B15	481	EE	-	196	D11
450	CC	-	-	-	482	EE	-	-	-
451	CC	-	-	-	483	EE	-	-	-
452	CC	-	-	-	484	EE	-	-	-
453	CC	107	-	A15	485	EE	113	195	C11
454	CC	-	-	-	486	EE	-	-	-
455	CC	-	-	-	487	EE	-	-	-
456	CC	-	-	-	488	EE	-	-	-
457	CC	108	206	B14	489	EE	114	194	A11
458	CC	-	-	-	490	EE	-	-	-
459	CC	-	205	A14	491	EE	116	193	B11
460	CC	-	-	-	492	EE	-	-	-
461	CC	-	-	-	493	EE	-	-	-
462	CC	-	204	B13	494	EE	117	-	F10
463	CC	-	-	-	495	EE	-	-	-
464	CC	109	203	A13	496	EE	-	-	E10
465	DD	-	202	C13	497	FF	118	192	D10
466	DD	-	-	-	498	FF	-	-	-
467	DD	-	-	-	499	FF	-	-	-
468	DD	-	-	-	500	FF	-	-	-
469	DD	110	201	D12	501	FF	-	-	C10
470	DD	-	-	-	502	FF	-	-	-
471	DD	-	-	-	503	FF	-	-	-
472	DD	-	-	-	504	FF	-	-	-
473	DD	111	199	C12	505	FF	119	190	A10
474	DD	-	-	-	506	FF	-	-	-
475	DD	-	198	B12	507	FF	120	189	J10
476	DD	-	-	-	508	FF	-	-	-
477	DD	-	-	-	509	FF	-	-	-
478	DD	112	197	A12	510	FF	121	188	F9
479	DD	-	-	-	511	FF	-	-	-
480	DD	-	-	E11	512	FF	122	187	A9

ATF1532AE(L) Ordering Information

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
7.5	4.7	133	ATF1532AE-7 AAC144 ATF1532AE-7 QC208 ATF1532AE-7 CTC256	144AA 208Q1 256CT1	Commercial (0°C to 70°C)
10.0	6.3	100	ATF1532AE-10 AAC144 ATF1532AE-10 QC208 ATF1532AE-10 CTC256	144AA 208Q1 256CT1	Commercial (0°C to 70°C)
			ATF1532AE-10 AAI144 ATF1532AE-10 QI208 ATF1532AE-10 CTI256	144AA 208Q1 256CT1	Industrial (-40°C to +85°C)
12.0	7.5	80	ATF1532AE-12 AAC144 ATF1532AE-12 QC208 ATF1532AE-12 CTC256	144AA 208Q1 256CT1	Commercial (0°C to 70°C)
			ATF1532AE-12 AAI144 ATF1532AE-12 QI208 ATF1532AE-12 CTI256	144AA 208Q1 256CT1	Industrial (-40°C to +85°C)
15.0	9.0	66	ATF1508AEL-15 AAC144 ATF1508AEL-15 CC208 ATF1508AEL-15 CTC256	144AA 169Q1 256CT1	Commercial (0°C to 70°C)

Using “C” Product for Industrial

There is very little risk in using “C” devices for industrial applications because the V_{CC} conditions for 3.3V products are the same for commercial and industrial (there is only 15°C difference at the high end of the temperature range). To use commercial product for industrial temperature ranges, de-rate I_{CC} by 15%.

Package Type	
144AA	144-lead, Very Thin Plastic Gull Wing Quad Flatpack (TQFP)
208Q1	208-ball, Plastic Quad Flatpack (PQFP)
256CT1	256-lead, Tape Ball Grid Array (TBGA) 1.0 mm pitch

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