

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
- Data Sheet Describes Mode 0 Operation
- Low-voltage Operation
 - 1.8 ($V_{CC} = 1.8V$ to $5.5V$)
- 20 MHz Clock Rate (4.5 – 5.5V)
- 128-byte Page Mode and Byte Write Operation Supported
- Block Write Protection
 - Protect 1/4, 1/2, or Entire Array
- Write Protect (\overline{WP}) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-timed Write Cycle (5 ms Max)
- High-reliability
 - Endurance: 1 Million Write Cycles
 - Data Retention: >40 Years
- Lead-free/Halogen-free Devices
- 8-lead JEDEC SOIC, 8-lead TSSOP and 8-lead SAP Packages
- Die Sales: Wafer Form, Waffle Pack, and Bumped Die

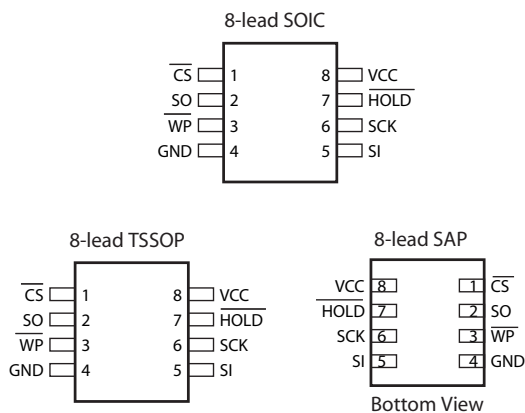
Description

The AT25512 provides 524,288 bits of serial electrically-erasable programmable read only memory (EEPROM) organized as 65,536 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space saving 8-lead JEDEC SOIC, 8-lead TSSOP and 8-lead SAP packages. In addition, the entire family is available in 1.8V (1.8V to 5.5V) versions.

The AT25512 is enabled through the Chip Select pin (\overline{CS}) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate Erase cycle is required before Write.

Table 0-1. Pin Configurations

| Pin Name | Function |
|-------------------|-----------------------|
| \overline{CS} | Chip Select |
| SCK | Serial Data Clock |
| SI | Serial Data Input |
| SO | Serial Data Output |
| GND | Ground |
| VCC | Power Supply |
| \overline{WP} | Write Protect |
| \overline{HOLD} | Suspends Serial Input |
| NC | No Connect |



SPI Serial EEPROM

512K (65,536 x 8)

AT25512

Block Write protection is enabled by programming the status register with top ¼, top ½ or entire array of write protection. Separate Program Enable and Program Disable instructions are provided for additional data protection. Hardware data protection is provided via the \overline{WP} pin to protect against inadvertent write attempts to the status register. The \overline{HOLD} pin may be used to suspend any serial communication without resetting the serial sequence.

1. Absolute Maximum Ratings*

| | |
|----------------------------------------------------|-------------------|
| Operating Temperature..... | -55° C to +125° C |
| Storage Temperature | -65° C to +150° C |
| Voltage on Any Pin with Respect to Ground | -1.0V to +7.0V |
| Maximum Operating Voltage | 4.3V |
| DC Output Current..... | 5.0 mA |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1-1. Block Diagram

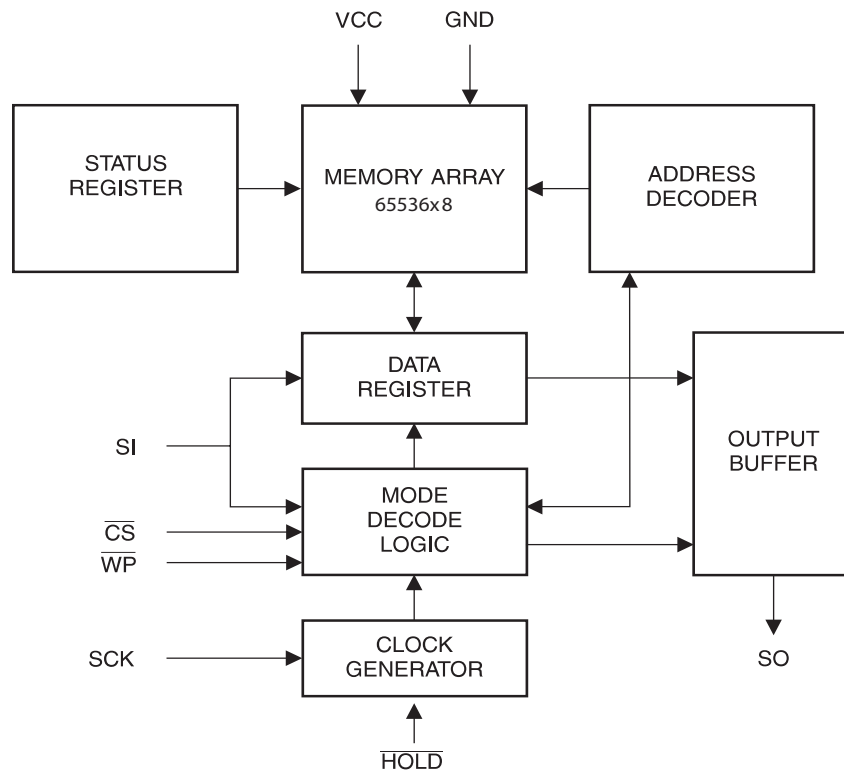


Table 1-1. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = +5.0\text{V}$ (unless otherwise noted)

| Symbol | Test Conditions | Max | Units | Conditions |
|-----------|------------------------------------------------------------------------|-----|-------|-----------------------|
| C_{OUT} | Output Capacitance (SO) | 8 | pF | $V_{OUT} = 0\text{V}$ |
| C_{IN} | Input Capacitance (\overline{CS} , SCK, SI, \overline{WP} , HOLD) | 6 | pF | $V_{IN} = 0\text{V}$ |

Note: 1. This parameter is characterized and is not 100% tested.

Table 1-2. DC Characteristics

Applicable over recommended operating range from $T_{AI} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$,

$V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$ (unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|----------------|---------------------|-------------------------------------------------------------------------------------|---------------------|------------------------------|---------------------|---------------|
| V_{CC1} | Supply Voltage | | 1.8 | | 5.5 | V |
| V_{CC2} | Supply Voltage | | 2.7 | | 5.5 | V |
| V_{CC3} | Supply Voltage | | 4.5 | | 5.5 | V |
| I_{CC1} | Supply Current | $V_{CC} = 5.0\text{V}$ at 20 MHz, SO = Open, Read | | 9.0 | 10.0 | mA |
| I_{CC2} | Supply Current | $V_{CC} = 5.0\text{V}$ at 10 MHz, SO = Open, Read, Write | | 5.0 | 7.0 | mA |
| I_{CC3} | Supply Current | $V_{CC} = 5.0\text{V}$ at 1 MHz, SO = Open, Read, Write | | 2.2 | 3.5 | mA |
| I_{SB1} | Standby Current | $V_{CC} = 1.8\text{V}$, $\overline{CS} = V_{CC}$ | | 0.2 | 3.0 | μA |
| I_{SB2} | Standby Current | $V_{CC} = 2.7\text{V}$, $\overline{CS} = V_{CC}$ | | 0.5 | 3.0 | μA |
| I_{SB3} | Standby Current | $V_{CC} = 5.0\text{V}$, $\overline{CS} = V_{CC}$ | | 2.0 | 5.0 | μA |
| I_{IL} | Input Leakage | $V_{IN} = 0\text{V}$ to V_{CC} | -3.0 | | 3.0 | μA |
| I_{OL} | Output Leakage | $V_{IN} = 0\text{V}$ to V_{CC} , $T_{AC} = 0^\circ\text{C}$ to 70°C | -3.0 | | 3.0 | μA |
| $V_{IL}^{(1)}$ | Input Low-voltage | | -1.0 | | $V_{CC} \times 0.3$ | V |
| $V_{IH}^{(1)}$ | Input High-voltage | | $V_{CC} \times 0.7$ | | $V_{CC} + 0.5$ | V |
| V_{OL1} | Output Low-voltage | $3.6 \leq V_{CC} \leq 5.5\text{V}$ | | $I_{OL} = 3.0\text{ mA}$ | 0.4 | V |
| V_{OH1} | Output High-voltage | | | $I_{OH} = -1.6\text{ mA}$ | $V_{CC} - 0.8$ | V |
| V_{OL2} | Output Low-voltage | $1.8\text{V} \leq V_{CC} \leq 3.6\text{V}$ | | $I_{OL} = 0.15\text{ mA}$ | 0.2 | V |
| V_{OH2} | Output High-voltage | | | $I_{OH} = -100\ \mu\text{A}$ | $V_{CC} - 0.2$ | V |

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.



Table 1-3. AC Characteristics

Applicable over recommended operating range from $T_{AI} = -40^{\circ}C$ to $+85^{\circ}C$, $V_{CC} = As Specified$,
 $CL = 1$ TTL Gate and 30 pF (unless otherwise noted)

| Symbol | Parameter | Voltage | Min | Max | Units |
|-----------|-----------------------------------|---------|-----|-----|---------|
| f_{SCK} | SCK Clock Frequency | 4.5–5.5 | 0 | 20 | MHz |
| | | 2.7–5.5 | 0 | 10 | |
| | | 1.8–5.5 | 0 | 5 | |
| t_{RI} | Input Rise Time | 4.5–5.5 | | 2 | μs |
| | | 2.7–5.5 | | 2 | |
| | | 1.8–5.5 | | 2 | |
| t_{FI} | Input Fall Time | 4.5–5.5 | | 2 | μs |
| | | 2.7–5.5 | | 2 | |
| | | 1.8–5.5 | | 2 | |
| t_{WH} | SCK High Time | 4.5–5.5 | 20 | | ns |
| | | 2.7–5.5 | 40 | | |
| | | 1.8–5.5 | 80 | | |
| t_{WL} | SCK Low Time | 4.5–5.5 | 20 | | ns |
| | | 2.7–5.5 | 40 | | |
| | | 1.8–5.5 | 80 | | |
| t_{CS} | \overline{CS} High Time | 4.5–5.5 | 100 | | ns |
| | | 2.7–5.5 | 100 | | |
| | | 1.8–5.5 | 200 | | |
| t_{CSS} | \overline{CS} Setup Time | 4.5–5.5 | 100 | | ns |
| | | 2.7–5.5 | 100 | | |
| | | 1.8–5.5 | 200 | | |
| t_{CSH} | \overline{CS} Hold Time | 4.5–5.5 | 100 | | ns |
| | | 2.7–5.5 | 100 | | |
| | | 1.8–5.5 | 200 | | |
| t_{SU} | Data In Setup Time | 4.5–5.5 | 5 | | ns |
| | | 2.7–5.5 | 10 | | |
| | | 1.8–5.5 | 20 | | |
| t_H | Data In Hold Time | 4.5–5.5 | 5 | | ns |
| | | 2.7–5.5 | 10 | | |
| | | 1.8–5.5 | 20 | | |
| t_{HD} | \overline{Hold} Setup Time | 4.5–5.5 | 5 | | ns |
| | | 2.7–5.5 | 10 | | |
| | | 1.8–5.5 | 20 | | |
| t_{CD} | \overline{Hold} Hold Time | 4.5–5.5 | 5 | | ns |
| | | 2.7–5.5 | 10 | | |
| | | 1.8–5.5 | 20 | | |
| t_V | Output Valid | 4.5–5.5 | 0 | 20 | ns |
| | | 2.7–5.5 | 0 | 40 | |
| | | 1.8–5.5 | 0 | 80 | |
| t_{HO} | Output Hold Time | 4.5–5.5 | 0 | | ns |
| | | 2.7–5.5 | 0 | | |
| | | 1.8–5.5 | 0 | | |
| t_{LZ} | \overline{Hold} to Output Low Z | 4.5–5.5 | 0 | 25 | ns |
| | | 2.7–5.5 | 0 | 50 | |
| | | 1.8–5.5 | 0 | 100 | |

Table 1-3. AC Characteristics (Continued)

Applicable over recommended operating range from $T_{AI} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = \text{As Specified}$, $CL = 1\text{ TTL Gate and }30\text{ pF}$ (unless otherwise noted)

| Symbol | Parameter | Voltage | Min | Max | Units |
|--------------------------|-------------------------------------------|---------|-----|-----|--------------|
| t_{HZ} | $\overline{\text{Hold}}$ to Output High Z | 4.5–5.5 | | 25 | ns |
| | | 2.7–5.5 | | 50 | |
| | | 1.8–5.5 | | 100 | |
| t_{DIS} | Output Disable Time | 4.5–5.5 | | 25 | ns |
| | | 2.7–5.5 | | 50 | |
| | | 1.8–5.5 | | 100 | |
| t_{WC} | Write Cycle Time | 4.5–5.5 | | 5 | ms |
| | | 2.7–5.5 | | 5 | |
| | | 1.8–5.5 | | 5 | |
| Endurance ⁽¹⁾ | 5.0V, 25 $^{\circ}$ C, Page Mode | | 1M | | Write Cycles |

Notes: 1. This parameter is characterized and is not 100% tested. Contact Atmel for further information.

2. Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the serial clock pin (SCK) is always an input, the AT25512 always operates as a slave.

TRANSMITTER/RECEIVER: The AT25512 has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with $\overline{\text{CS}}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25512, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{\text{CS}}$ is detected again. This will reinitialize the serial communication.

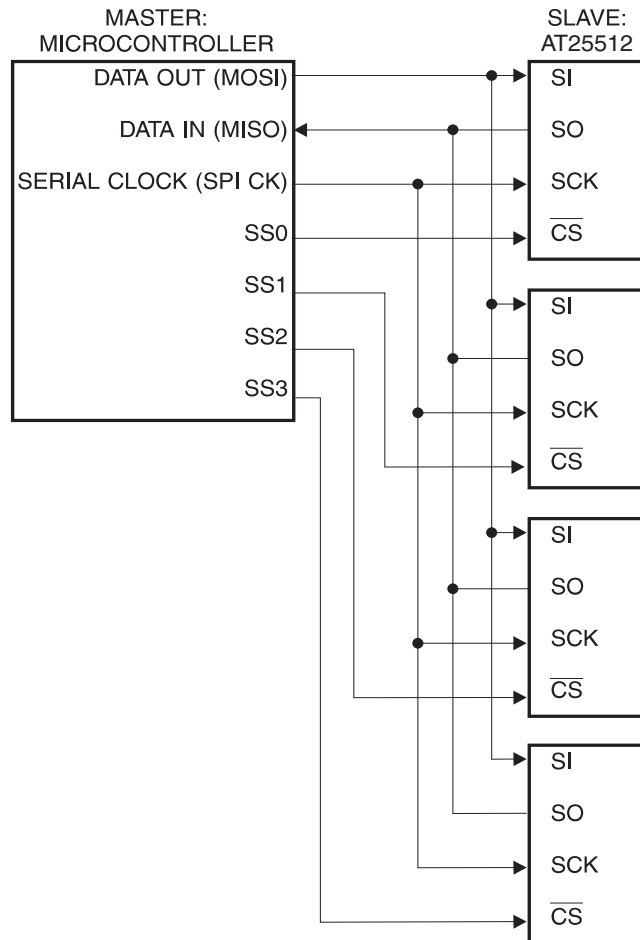
CHIP SELECT: The AT25512 is selected when the $\overline{\text{CS}}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The $\overline{\text{HOLD}}$ pin is used in conjunction with the $\overline{\text{CS}}$ pin to select the AT25512. When the device is selected and a serial sequence is underway, $\overline{\text{HOLD}}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{\text{HOLD}}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{\text{HOLD}}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{\text{HOLD}}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The write protect pin ($\overline{\text{WP}}$) will allow normal read/write operations when held high. When the $\overline{\text{WP}}$ pin is brought low and WPEN bit is “1”, all write operations to the status register are inhibited. $\overline{\text{WP}}$ going low while $\overline{\text{CS}}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{\text{WP}}$ going low will have no effect on any write operation to the status register. The $\overline{\text{WP}}$ pin function is blocked when the WPEN bit in the status register is “0”. This will allow the user to install the AT25512 in a system with the $\overline{\text{WP}}$ pin tied to

ground and still be able to write to the status register. All \overline{WP} pin functions are enabled when the WPEN bit is set to "1".

Figure 2-1. SPI Serial Interface



3. Functional Description

The AT25512 is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6800 type series of microcontrollers.

The AT25512 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in see [Table 4-3](#). All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low \overline{CS} transition.

Table 3-1. Instruction Set for the AT25512

| Instruction Name | Instruction Format | Operation |
|------------------|--------------------|-----------------------------|
| WREN | 0000 X110 | Set Write Enable Latch |
| WRDI | 0000 X100 | Reset Write Enable Latch |
| RDSR | 0000 X101 | Read Status Register |
| WRSR | 0000 X001 | Write Status Register |
| READ | 0000 X011 | Read Data from Memory Array |
| WRITE | 0000 X010 | Write Data to Memory Array |

WRITE ENABLE (WREN): The device will power-up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the \overline{WP} pin.

READ STATUS REGISTER (RDSR): The Read Status Register instruction provides access to the status register. The Ready/Busy and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 3-2. Status Register Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|------------------|
| WPEN | X | X | X | BP1 | BP0 | WEN | \overline{RDY} |

Table 3-3. Read Status Register Bit Definition

| Bit | Definition |
|-----------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|
| Bit 0 (\overline{RDY}) | Bit 0 = "0" (\overline{RDY}) indicates the device is ready. Bit 0 = "1" indicates the write cycle is in progress. |
| Bit 1 (WEN) | Bit 1 = 0 indicates the device <i>is not</i> write enabled. Bit 1 = "1" indicates the device is write enabled. |
| Bit 2 (BP0) | See Table 3-4 on page 8 . |
| Bit 3 (BP1) | See Table 3-4 on page 8 . |
| Bits 4 –6 are 0s when device is not in an internal write cycle. | |
| Bit 7 (WPEN) | See Table 3-5 on page 8 . |
| Bits 0 –7 are "1"s during an internal write cycle. | |

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25512 is divided into four array segments. Top quarter (1/4), top half (1/2), or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read only. The block write protection levels and corresponding status register control bits are shown in [Table 3-4](#).

The three bits, BP0, BP1, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g. WREN, t_{WC} , RDSR).

Table 3-4. Block Write Protect Bits

| Level | Status Register Bits | | Array Addresses Protected |
|--------|----------------------|-----|---------------------------|
| | BP1 | BP0 | AT25512 |
| 0 | 0 | 0 | None |
| 1(1/4) | 0 | 1 | C000 – FFFF |
| 2(1/2) | 1 | 0 | 8000 – FFFF |
| 3(All) | 1 | 1 | 0000 – FFFF |

The WRSR instruction also allows the user to enable or disable the write protect (\overline{WP}) pin through the use of the write protect enable (WPEN) bit. Hardware write protection is enabled when the \overline{WP} pin is low and the WPEN bit is “1”. Hardware write protection is disabled when *either* the \overline{WP} pin is high or the WPEN bit is “0”. When the device is hardware write protected, writes to the Status Register, including the Block Protect bits and the WPEN bit, and the block-protected sections in the memory array are disabled. Writes are only allowed to sections of the memory which are not block-protected.

NOTE: When the WPEN bit is hardware write protected, it cannot be changed back to “0”, as long as the \overline{WP} pin is held low.

Table 3-5. WPEN Operation

| WPEN | WP | WEN | Protected Blocks | Unprotected Blocks | Status Register |
|------|------|-----|------------------|--------------------|-----------------|
| 0 | X | 0 | Protected | Protected | Protected |
| 0 | X | 1 | Protected | Writable | Writable |
| 1 | Low | 0 | Protected | Protected | Protected |
| 1 | Low | 1 | Protected | Writable | Protected |
| X | High | 0 | Protected | Protected | Protected |
| X | High | 1 | Protected | Writable | Writable |

READ SEQUENCE (READ): Reading the AT25512 via the SO pin requires the following sequence. After the \overline{CS} line is pulled low to select a device, the Read op-code is transmitted via the SI line followed by the byte address to be read (see [Table 3-6 on page 9](#)). Upon completion, any data on the SI line will be ignored. The data (D7 – D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the \overline{CS} line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous read cycle.

WRITE SEQUENCE (WRITE): In order to program the AT25512, two separate instructions must be executed. First, the device *must be write enabled* via the Write Enable (WREN) Instruction. Then a Write instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write

Protection Level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write Instruction requires the following sequence. After the \overline{CS} line is pulled low to select the device, the Write op-code is transmitted via the SI line followed by the byte address and the data (D7 – D0) to be programmed (see Table 3-6). Programming will start after the \overline{CS} pin is brought high. (The Low-to-High transition of the \overline{CS} pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The Ready/Busy status of the device can be determined by initiating a Read Status Register (RDSR) Instruction. If Bit 0 = 1, the Write cycle is still in progress. If Bit 0 = 0, the Write cycle has ended. Only the Read Status Register instruction is enabled during the Write programming cycle.

The AT25512 is capable of a 128-byte Page Write operation. After each byte of data is received, the seven low order address bits are internally incremented by one; the high order bits of the address will remain constant. If more than 128 bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25512 is automatically returned to the write disable state at the completion of a Write cycle.

NOTE: If the device is not write enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when \overline{CS} is brought high. A new CS falling edge is required to re-initiate the serial communication.

Table 3-6. Address Key

| Address | AT25512 |
|---------|----------------|
| A_N | $A_{15} - A_0$ |

4. Timing Diagrams (for SPI Mode 0 (0, 0))

Figure 4-1. Synchronous Data Timing

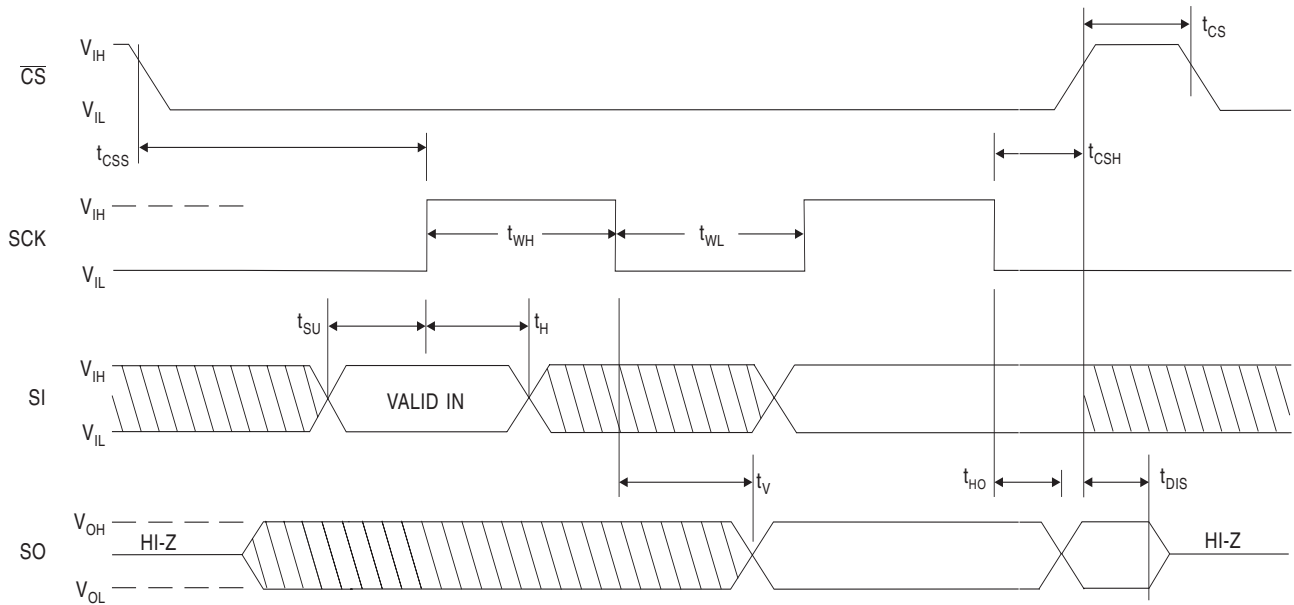


Figure 4-2. WREN Timing

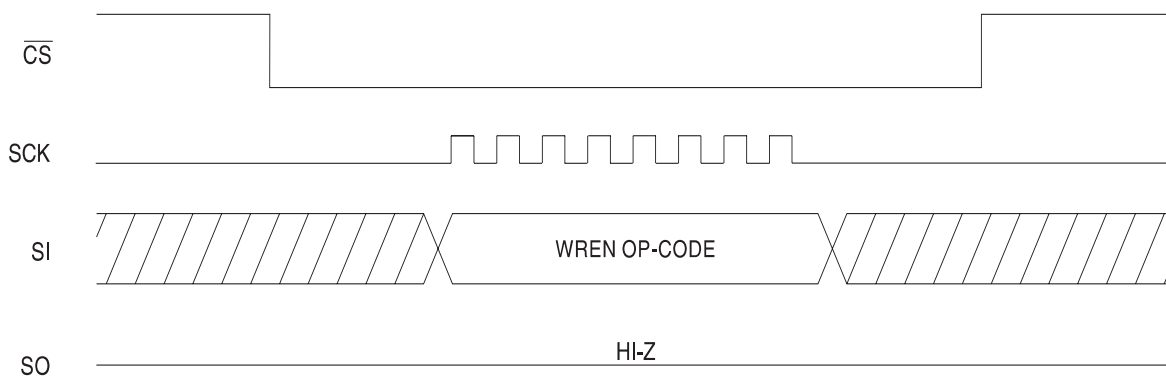


Figure 4-3. WRDI Timing

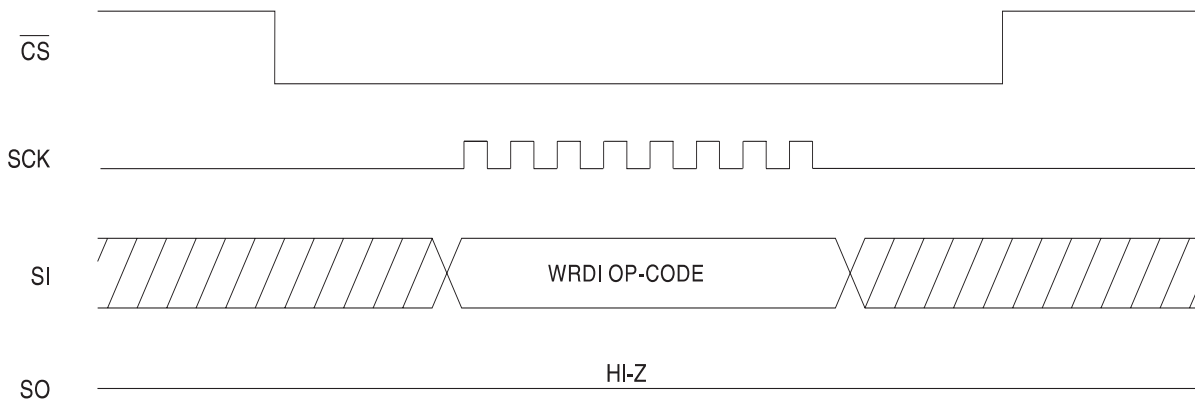


Figure 4-4. RDSR Timing

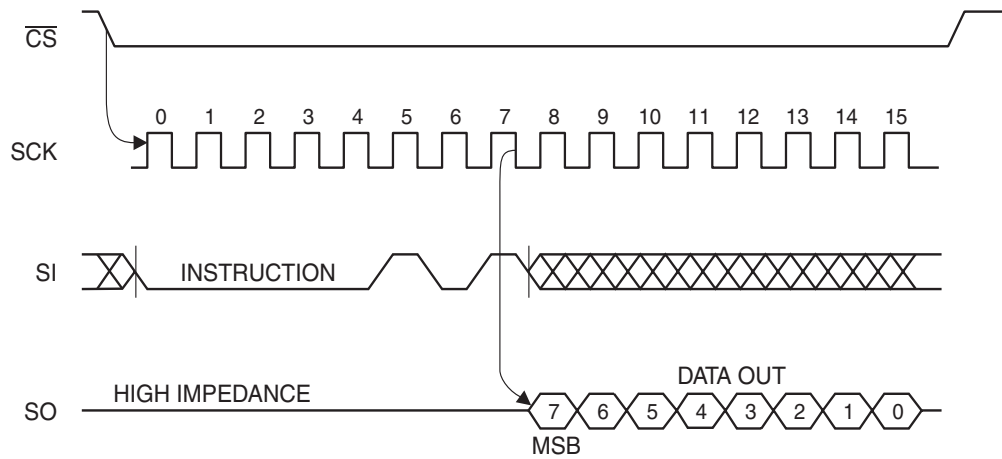


Figure 4-5. WRSR Timing

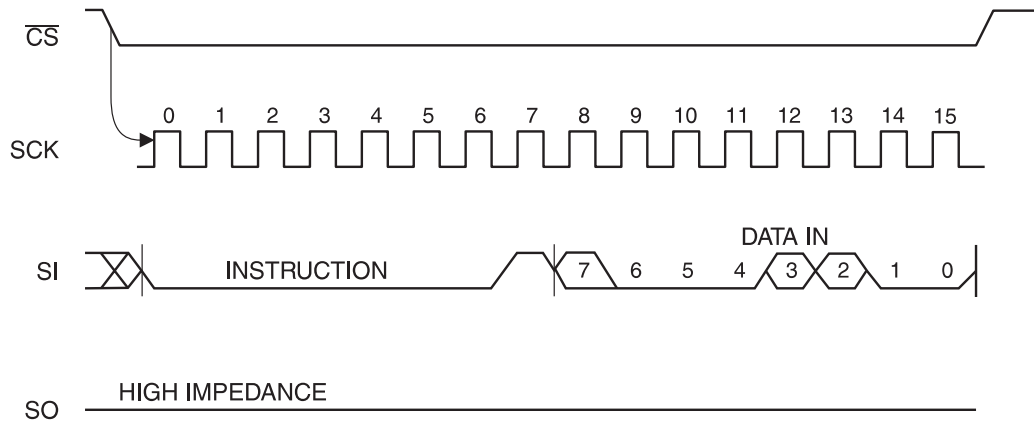


Figure 4-6. READ Timing

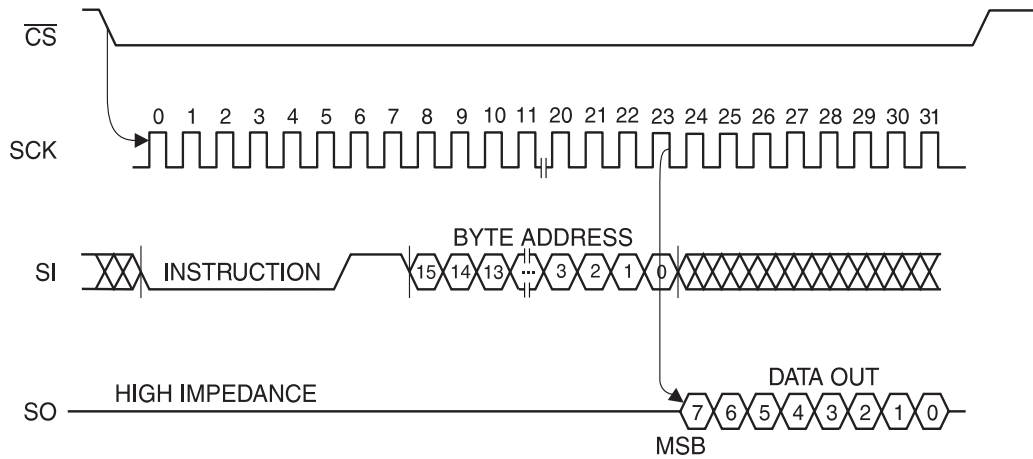


Figure 4-7. WRITE Timing

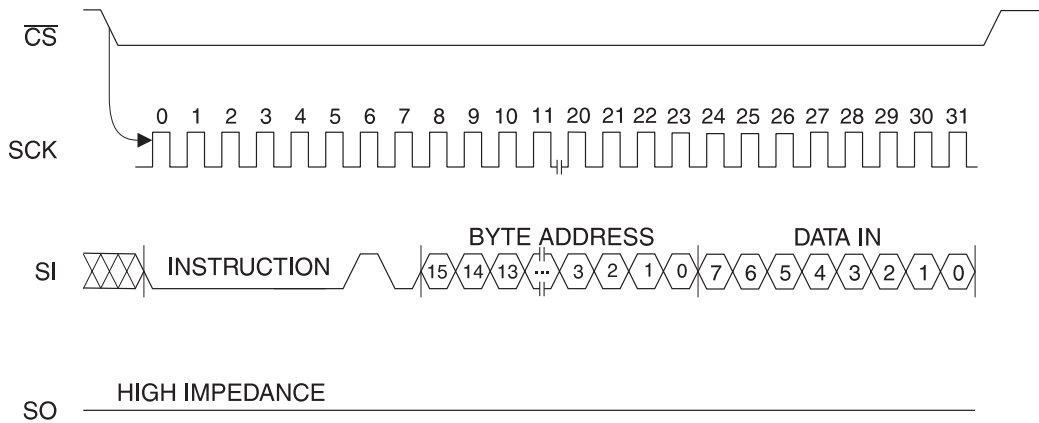
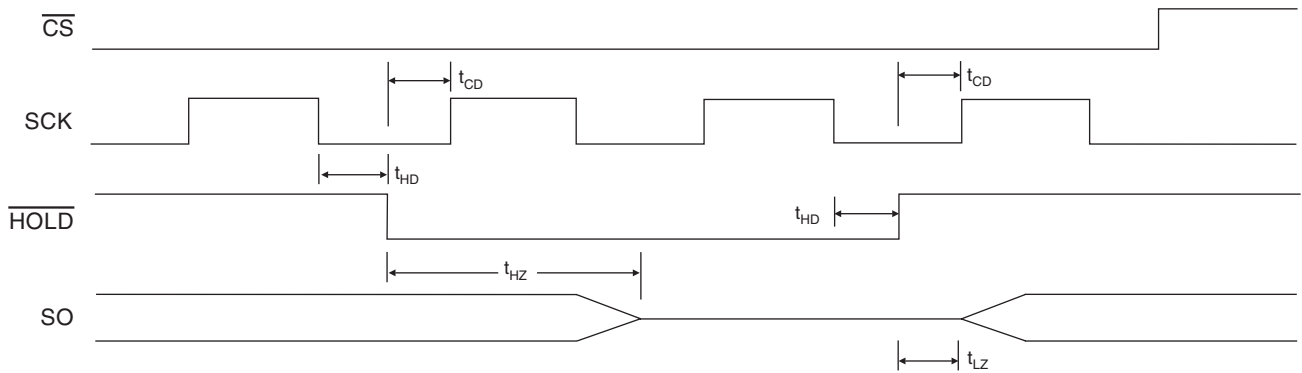


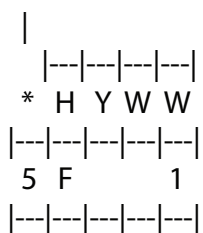
Figure 4-8. HOLD Timing



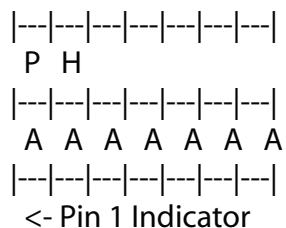
5. Part Marking Scheme

TOP MARK

Pin 1 Indicator (Dot)



BOTTOM MARK



Y = SEAL YEAR WW = SEAL WEEK

6:2006 0:2010 02 = Week 2

7:2007 1:2011 04 = Week 4

8:2008 2:2012 :::::

9:2009 3:2013 :::::

50 = Week 50

52 = Week 52



AT25512N-SH-B/T



Y = SEAL YEAR WW = SEAL WEEK

6:2006 0:2010 02 = Week 2

7:2007 1:2011 04 = Week 4

8:2008 2:2012 :::::

9:2009 3:2013 :::::

50 = Week 50

52 = Week 52

Lot Number to Use ALL Characters in Marking

BOTTOM MARK

No Bottom Mark



AT25512Y7-YH-T



Y = SEAL YEAR WW = SEAL WEEK
 6: 2006 0: 2010 02 = Week 2
 7: 2007 1: 2011 04 = Week 4
 8: 2008 2: 2012 :::::
 9: 2009 3: 2013 :::::
 50 = Week 50
 52 = Week 52

Lot Number to Use ALL Characters in Marking

BOTTOM MARK

No Bottom Mark



6. AT25512 Ordering Information

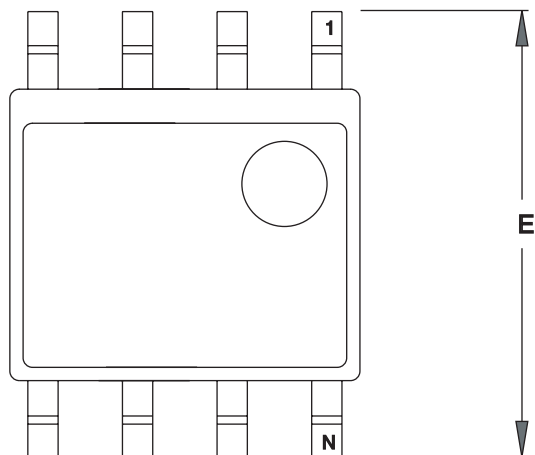
| Ordering Code | Voltage | Package | Operation Range |
|-------------------------------|---------|----------|----------------------------------------------------------------------------------------------|
| AT25512N-SH-B ⁽¹⁾ | 1.8 | 8S1 | Lead-free/Halogen-free NiPD Au Lead Finish Industrial Temperature (-40° C to 85° C) |
| AT25512N-SH-T ⁽²⁾ | 1.8 | 8S1 | |
| AT25512-TH-B ⁽¹⁾ | 1.8 | 8A2 | |
| AT25512-TH-T ⁽²⁾ | 1.8 | 8A2 | |
| AT25512Y7-YH-T ⁽²⁾ | 1.8 | 8Y7 | |
| AT25512-W-11 ⁽³⁾ | 1.8 | Die Sale | Industrial Temperature (-40° C to 85° C) |

- Notes:
1. "-B" denotes bulk.
 2. "-T" denotes tape and reel. SOIC = 4K per reel. TSSOP = 5K per reel. SAP = 3K per reel.
 3. Available in waffle pack, tape and reel, and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

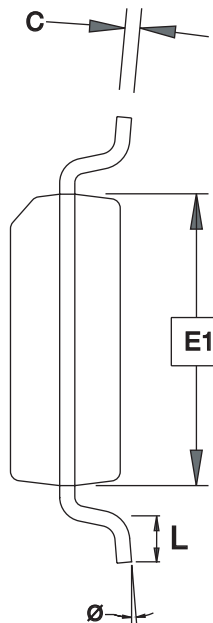
| Package Type | |
|--------------|-------------------------------------------------------------------------------------------------|
| 8S1 | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| 8A2 | 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP) |
| 8Y7 | 8-lead, 6.00mm x 4.90mm Body, Ultra Thin, Dual Footprint, Non-leaded, Small Array Package (SAP) |
| Options | |
| -1.8 | Low-voltage (1.8V to 5.5V) |

7. Packaging Information

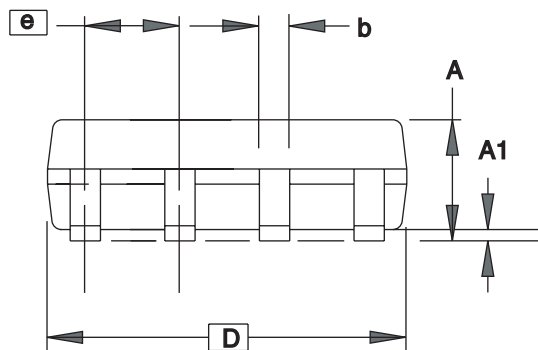
8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-----|------|------|
| A | 1.35 | – | 1.75 | |
| A1 | 0.10 | – | 0.25 | |
| b | 0.31 | – | 0.51 | |
| C | 0.17 | – | 0.25 | |
| D | 4.80 | – | 5.05 | |
| E1 | 3.81 | – | 3.99 | |
| E | 5.79 | – | 6.20 | |
| e | 1.27 BSC | | | |
| L | 0.40 | – | 1.27 | |
| θ | 0° | – | 8° | |

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

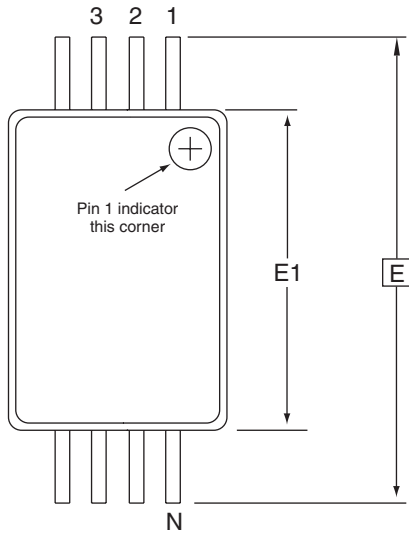
3/17/05

AMEL 1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906

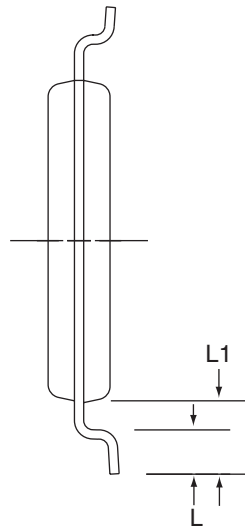
TITLE
8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing
Small Outline (JEDEC SOIC)

| | |
|--------------------|-------------|
| DRAWING NO. | REV. |
| 8S1 | C |

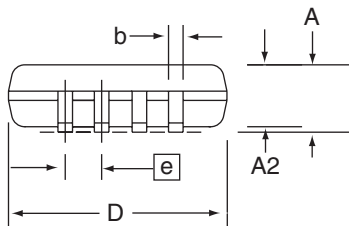
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|------|------|------|
| D | 2.90 | 3.00 | 3.10 | 2, 5 |
| E | 6.40 BSC | | | |
| E1 | 4.30 | 4.40 | 4.50 | 3, 5 |
| A | – | – | 1.20 | |
| A2 | 0.80 | 1.00 | 1.05 | |
| b | 0.19 | – | 0.30 | 4 |
| e | 0.65 BSC | | | |
| L | 0.45 | 0.60 | 0.75 | |
| L1 | 1.00 REF | | | |

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
 2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
 3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
 4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
 5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02

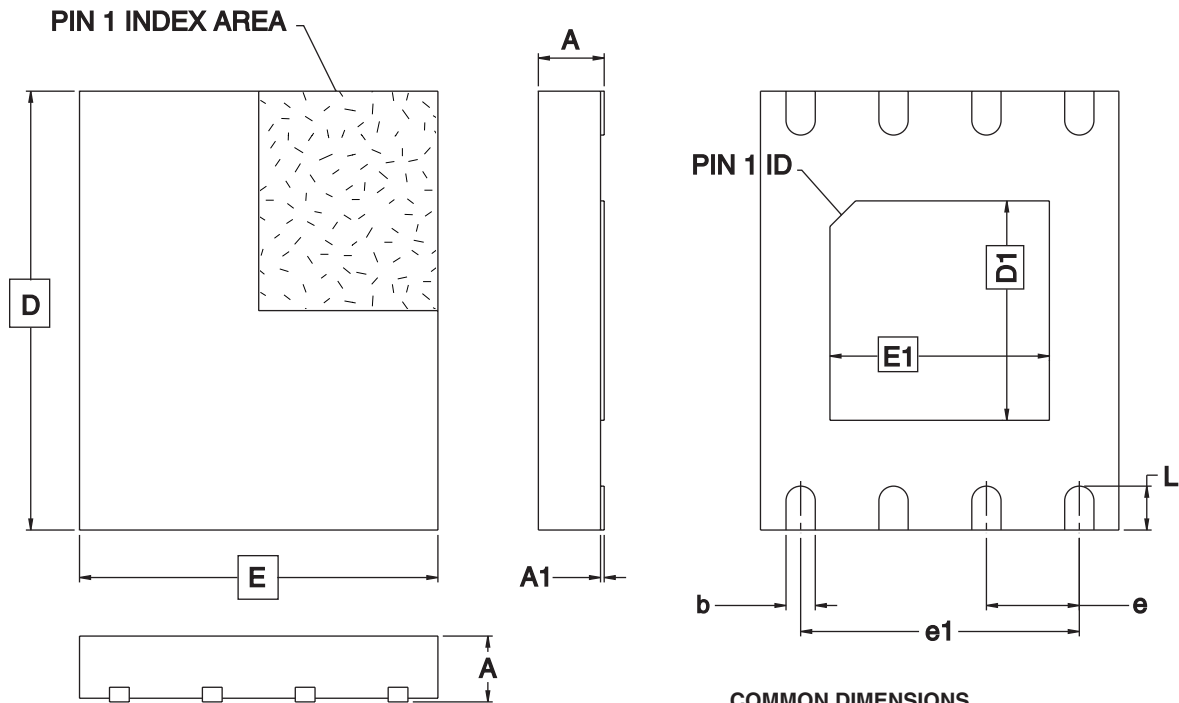
2325 Orchard Parkway
San Jose, CA 95131

TITLE
8A2, 8-lead, 4.4 mm Body, Plastic
Thin Shrink Small Outline Package (TSSOP)

DRAWING NO.
8A2

REV.
B

8Y7 - SAP



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|------|------|------|
| A | - | - | 0.60 | |
| A1 | 0.00 | - | 0.05 | |
| D | 5.80 | 6.00 | 6.20 | |
| E | 4.70 | 4.90 | 5.10 | |
| D1 | 3.30 | 3.40 | 3.50 | |
| E1 | 3.90 | 4.00 | 4.10 | |
| b | 0.35 | 0.40 | 0.45 | |
| e | 1.27 TYP | | | |
| e1 | 3.81 REF | | | |
| L | 0.50 | 0.60 | 0.70 | |

10/13/05



1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906

TITLE

8Y7, 8-lead (6.00 x 4.90 mm Body) Ultra-Thin SOIC Array Package (UTSAP) Y7

DRAWING NO.

8Y7

REV.

B



8. Revision History

| Doc. Rev. | Date | Comments |
|-----------|--------|-------------------------------------------------------------------------------------------------------------------|
| 5165E | 8/2008 | Updated for 1.8V - 5.5V operation |
| 5165D | 5/2008 | Added part marking diagram information |
| 5165C | 8/2007 | Changed address bit number to seven on page 9 Removed Preliminary status |
| 5165B | 6/2007 | Changed spacing on table notes Reworked figure 4-8 Updated to new template Changed status to Preliminary |
| 5165A | 1/2007 | Initial document release. |



Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
s_eeeprom@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

Disclaimer: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

©2008 Atmel Corporation. All rights reserved. Atmel®, logo and combinations thereof, and others, are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be trademarks of others.