2A Single Input I²C, Standalone Switch-Mode Li-Ion Battery Charger with Power-Path Management

Check for Samples: bq24250, bq24251, bq24253

FEATURES

- High-efficiency Switch-mode Charger with Separate Power Path
- Start up System from Deeply Discharged or Missing Battery
- USB Charging Compliant
  - Selectable Input Current Limit of 100 mA, 500 mA, 900 mA, 1.5 A, and 2 A
- BC1.2 Compatible D+, D– Detection
- In Host Mode (after I²C communication starts and before watchdog timer times out)
  - Programmable Battery Charge Voltage, V_{BATREG}
  - Programmable Charge Current (I_{CHG})
  - Programmable Input Current Limit (I_{LIM})
  - Programmable Input Voltage Based Dynamic Power Management threshold, (V_{IN_DPM})
  - Programmable Input Overvoltage Protection Threshold (V_{OVP})
  - Programmable Safety Timer
- Resistor Programmable Defaults for:
  - I_{CHG} up to 2 A with Current Monitoring Output (ISET)
  - I_{LIM} up to 2 A with Current Monitoring Output (ILIM)
  - V_{IN_DPM} (VDPM)
- Watchdog Timer Disable Bit
- Integrated 4.9 V, 50 mA LDO
- Complete System Level Protection
  - Input UVLO, Input Over-voltage Protection (OVP), Battery OVP, Sleep Mode, VIN_DPM
  - Input Current Limit
  - Charge Current Limit
  - Thermal Regulation
  - Thermal Shutdown
  - Voltage Based, JEITA Compatible NTC Monitoring Input
  - Safety Timer
- 20 V Maximum Input Voltage Rating
- 10.5 V Maximum Operating Input Voltage
- Low $R_{DS(on)}$ Integrated Power FETs for up to 2 A Charging Rate
- Open Drain Status Outputs
- Synchronous Fixed-frequency PWM Controller Operating at 3MHz for Small Inductor Support
- *AnyBoot* Robust Battery Detection Algorithm
- Charge Time Optimizer for improved charge times at any given charge current
- 2.4 x 2.0 mm 30-ball WCSP Package

APPLICATIONS

- Mobile Phones and Smart Phones
- MP3 Players
- Portable Media Players
- Handheld Devices

DESCRIPTION

The bq24250, 1, 3 is a highly integrated single-cell Li-Ion battery charger and system power-path management device targeted for space-limited, portable applications with high capacity batteries. The single cell charger has a single input that operates from either a USB port or AC wall adapter for a versatile solution.

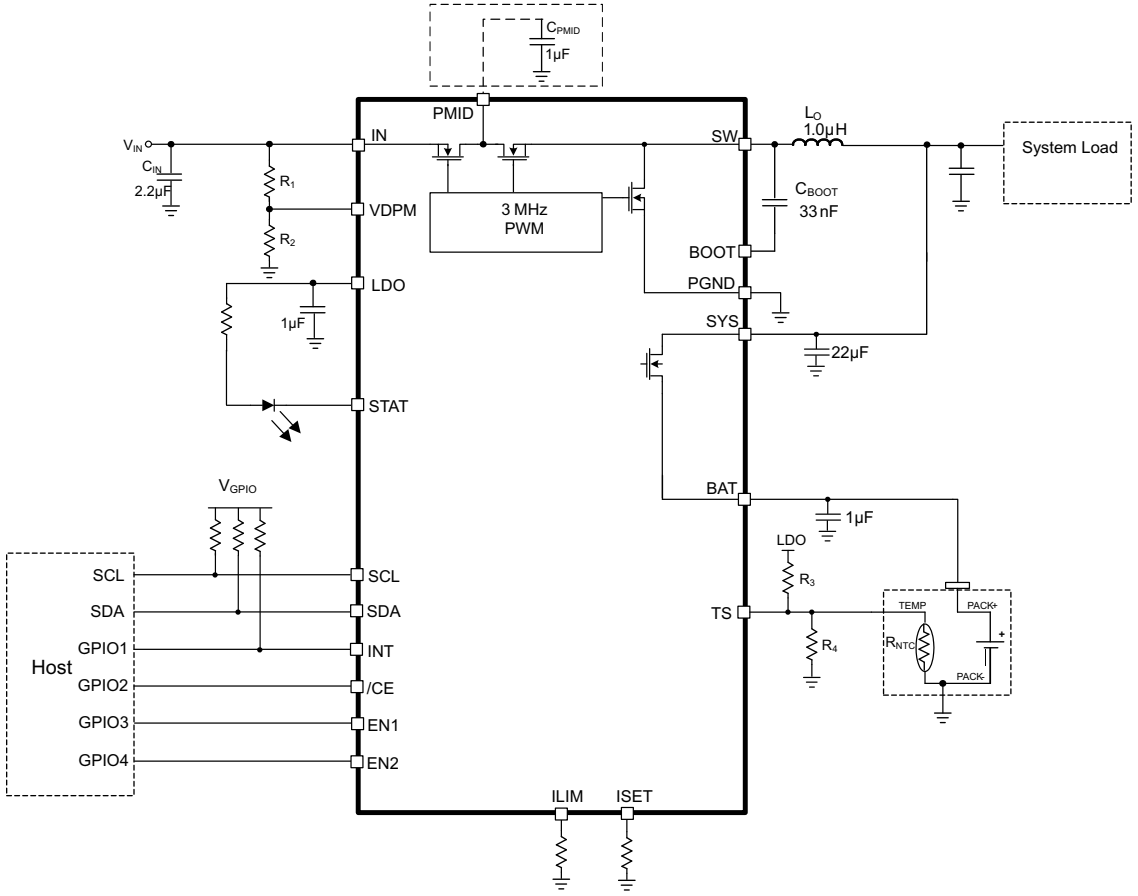
The power path management feature allows the bq24250, 1, 3 to power the system from a high efficiency DC/DC converter while simultaneously and independently charging the battery. The charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit. This allows for proper charge termination and enables the system to run with a defective or absent battery pack. Additionally, this enables instant system turn-on even with a totally discharged battery or no battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. This enables the use of a smaller adapter.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The battery is charged in four phases: trickle charge, pre-charge, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded. Additionally, a voltage-based, JEITA compatible battery pack thermistor monitoring input (TS) is included that monitors battery temperature for safe charging.

Typical Application



AVAILABLE OPTIONS

Device	Default OVP	D+/D- or EN1/EN2	INT or PG	Default V_{OREG}	MINSYS	TS Profile	I^2C or Stand Alone	I^2C Address
bq24250	10.5V	EN1/EN2	INT	4.2V	3.5V	JEITA	I^2C + SA	0x6A
bq24251	10.5V	D+/D-	$\overline{PG}$	4.2V	3.5V	JEITA	I^2C + SA	0x6A
bq24253	10.5V	D+/D- and EN1/EN2	$\overline{PG}$	4.2V	3.5V	JEITA	SA Only	N/A

ORDERING INFORMATION(1)(2)

Part Number	IC Marking	Package	Ordering Number	Quantity
bq24250	bq24250	DSBGA-YFF	bq24250YFFR	3000
		DSBGA-YFF	bq24250YFFT	250
		QFN-RGE	bq24250RGER	3000
		QFN-RGE	bq24250RGET	250
bq24251	bq24251	DSBGA-YFF	bq24251YFFR	3000
		DSBGA-YFF	bq24251YFFT	250
		QFN-RGE	bq24251RGER	3000
		QFN-RGE	bq24251RGET	250
bq24253	bq24253	DSBGA-YFF(3)	bq24253YFFR	3000
		DSBGA-YFF(3)	bq24253YFFT	250
		QFN-RGE	bq24253RGER	3000
		QFN-RGE	bq24253RGET	250

(1) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) Preview

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Pin Voltage Range (with respect to GND)	IN	–0.3	20	V
	SW	–0.7	12	V
	BOOT	–0.3	20	V
	LDO,STAT, INT, /CHG, /PG, EN1, EN2, EN3, /CE, D+, D-, ILIM, ISET, VDPM, TS	–0.3	7	V
	SYS, BAT	–0.3	5	V
BOOT relative to SW		–0.3	7	V
Output Current (Continuous)	IN, SW, SYS, BAT		2	A
Output Sink Current	STAT, /CHG, /PG		5	mA
Operating free-air temperature range		–40	85	°C
Junction temperature, T_J		–40	125	°C
Storage temperature, T_{STG}		–65	150	°C
Input Power	IN		15	W
Lead temperature (soldering, 10 s)			300	°C
ESD Rating(2)	Human body model		2	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

RECOMMENDED OPERATING CONDITIONS

All voltages are with respect to PGND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages

		MIN	MAX	UNITS
V_{IN}	IN voltage range	4.35	18(1)	V
	IN operating voltage range	4.35	10.5	
I_{IN}	Input current		2	A
I_{CHG}	Current in charge mode, BAT		2	A
I_{DISCHG}	Current in discharge mode, BAT		4	A
R_{ISET}	Charge current programming resistor range	75		Ω
R_{ILIM}	Input current limit programming resistor range	105		Ω
P_{IN}	Input Power		12	W
T_J	Operating junction temperature range	0	125	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW pins. Small routing loops for the power nets in layout minimize switching noise.

THERMAL INFORMATION

THERMAL METRIC(1)		bq24250/1/3		UNITS
		YFF	RGE	
θ_{JA}	Junction-to-ambient thermal resistance	76.5	32.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.2	32.8	
θ_{JB}	Junction-to-board thermal resistance	44	10.6	
ψ_{JT}	Junction-to-top characterization parameter	1.6	0.3	
ψ_{JB}	Junction-to-board characterization parameter	43.4	10.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	2.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

$V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = 0ºC-125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{IN}	Supply current from IN	$V_{DPM} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+V_{SLP}$ PWM switching, CE Enable		13		mA
		$V_{DPM} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+V_{SLP}$ PWM switching, CE Disable			5	
		0°C< T_J < 85°C, High-Z Mode		170	225	µA
I_{BAT}	Battery discharge current in high impedance mode, (BAT, SW, SYS)	0°C< T_J < 85°C, VBAT = 4.2 V, VIN = 0V or 5V, High-Z Mode		16	22	µA
	Battery discharge current in SYSOFF mode, (BAT, SW, SYS)	0°C< T_J < 85°C, VBAT = 4.2 V, VIN < UVLO, SYSOFF Mode			1	
POWER-PATH MANAGEMENT						
V_{SYSREG}	System Regulation Voltage	MINSYS stage (no DPM or DPPM)	–1%	3.52	1%	V
		MINSYS stage (DPM or DPPM active)	–1.50%	V_{MINSYS} –200mV	1.50%	
		BATREG stage		V_{BAT} + I_{CHG} R_{on}		
		SYSREG stage	V_{BATREG} +2.1%	V_{BATREG} +3.1%	V_{BATREG} +4.1%	
V_{SPLM}	Enter supplement mode voltage threshold	V_{BAT} = 3.6V		V_{BAT} – 40mV		V
I_{SPLM}	Exit supplement mode current threshold	V_{BAT} = 3.6V		20		mA
$t_{DGL(SC1)}$	Deglitch Time, OUT Short Circuit during Discharge or Supplement Mode	Measured from (V_{BAT} – V_{SYS}) = 300 mV		740		µs
$t_{REC(SC1)}$	Recovery Time, OUT Short Circuit during Discharge or Supplement Mode			64		ms
BATTERY CHARGER						
$R_{ON(BAT-SYS)}$	Internal battery charger MOSFET on-resistance	Measured from BAT to SYS, V_{BAT} = 4.2V (WCSP)		20	30	mΩ
		Measured from BAT to SYS, V_{BAT} = 4.2V (QFN)		30	40	
V_{BATREG}	I^2C host mode	Operating in voltage regulation, Programmable Range	3.5		4.44	V
	SA mode or I^2C default mode			4.2		
	Voltage Regulation Accuracy	T_J = 25°C	–0.5%		0.5%	
		T_J = 0°C to 125°C	–0.75		0.75	
I_{CHG}	Fast Charge Current Range	$V_{LOWV} \le V_{BAT} < V_{BAT(REG)}$	500		2000	mA
	Fast Charge Current Accuracy	I^2C mode	–7%		7%	
$I_{CHG-LOW}$	Low Charge Current Setting	Set via I^2C	297	330	363	mA
K_{ISET}	Programmable Fast Charge Current Factor	$I_{CHG} = \frac{K_{ISET}}{R_{ISET}}$	232.5	250	267.5	AΩ
V_{ISET}	Maximum ISET pin voltage (in regulation)			0.42		V
$R_{ISET-SHORT}$	Short circuit resistance threshold		45	55	75	Ω
V_{LOWV}	Pre-charge to fast charge threshold	Rising	2.9	3	3.1	V
	Hysteresis for V_{LOWV}	Battery voltage falling		100		mV

ELECTRICAL CHARACTERISTICS (continued)

$V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = 0ºC-125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PRECHG}	Pr-charge current ($V_{BATUVLO} < V_{BAT} < V_{LOWV}$)	Ipre-chg is a precentile of the external fast charge settings.	8	10	12	%
$t_{DGL(LOWV)}$	Deglitch time for pre-charge to fast charge transition			32		ms
V_{BAT_UVLO}	Battery Under voltage lockout threshold	V_{BAT} rising	2.37	2.5	2.63	V
	Battery UVLO hysteresis			200		mV
$V_{BATSHRT}$	Trickle charge to pre-charge threshold		1.9	2	2.1	V
	Hysteresis for VBATSHRT	Battery voltage falling		100		mV
$I_{BATSHRT}$	Trickle charge mode charge current ($V_{BAT} < V_{BATSHRT}$)		25	35	50	mA
$t_{DGL(BATSHRT)}$	Deglitch time for trickle charge to pre-charge transition			256		us
I_{TERM}	Termination Current Threshold	Termination current on SA only		10		%ICHG
	Termination Current Threshold Tolerance		–10		10	%
$t_{DGL(TERM)}$	Deglitch time for charge termination	Both rising and falling, 2-mV over-drive, t_{RISE}, t_{FALL} = 100 ns		64		ms
V_{RCH}	Recharge threshold voltage	Below V_{BATREG}	70	115	160	mV
$t_{DGL(RCH)}$	Deglitch time	V_{BAT} falling below V_{RCH}, t_{FALL} = 100 ns		32		ms
BATTERY DETECTION						
V_{BATREG_HI}	Battery Detection High Regulation Voltage	Same as V_{BATREG}		V_{BATREG}		V
V_{BATREG_LO}	Battery Detection Low Regulation Voltage	360 mV offset from V_{BATREG}		V_{BATREG} –480mV		V
$V_{BATDET\ Hi}$	Battery detection comparator	V_{BATREG} = VBATREG_HI		V_{BATREG} –120mV		V
$V_{BATDET\ LO}$	Battery detection comparator	V_{BATREG} = V_{BATREG_LO}		V_{BATREG} +120mV		V
I_{DETECT}	Battery Detection Current Sink	Always on during battery detection		7.5		mA
t_{DETECT}	Battery detection time	For both V_{BATREG_HI} and V_{BATREG_LO}		32		ms
Tsafe	Safety Timer Accuracy		–10		+10	%

ELECTRICAL CHARACTERISTICS (continued)

$V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = 0ºC-125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT PROTECTION						
I_{IN}	Input current limiting	I_{IN_LIMIT} = 100 mA	90	95	100	mA
		I_{IN_LIMIT} = 150 mA	135	142.5	150	
		I_{IN_LIMIT} = 500 mA	450	475	500	
		I_{IN_LIMIT} = 900 mA	810	860	910	
		I_{IN_LIMIT} = 1500 mA	1400	1475	1550	
		I_{IN_LIMIT} = 2000 mA	1850	1950	2050	
		I_{IN_LIMIT} = External	$I_{LIM} = \frac{K_{ILIM}}{R_{ILIM}}$			
I_{LIM}	Maximum input current limit programmable range for IN input		500		2000	mA
K_{ILIM}	Maximum input current factor for IN input	I_{LIM} = 500 mA to 2.0 A	240	270	300	AΩ
V_{ILIM}	Maximum ILIM pin voltage (in regulation)			0.42		V
$R_{ILIM-SHORT}$	Short circuit resistance threshold		65	83	105	Ω
V_{IN_DPM}	V_{IN_DPM} threshold range	SA mode	4.2		10	V
		I^2C mode	4.2		4.76	
	V_{IN_DPM} threshold for USB Input in SA mode	USB100, USB150, USB500, USB900, current limit selected. Also I^2C register default.	4.27	4.36	4.45	
	V_{IN_DPM} threshold with adaptor current limit and VDPM shorted to GND	Must set to external resistor settings via the EN1/EN2 pins or the I^2C register interface.	V_{IN_DPM} –2%	V_{IN_DPM}	V_{IN_DPM} +2%	
	V_{IN_DPM} threshold Accuracy	Both I^2C and SA mode	–2		2	%
V_{REF_DPM}	DPM regulation voltage	External resistor setting only	1.15	1.2	1.25	V
V_{DPM_SHRT}	VIN_DPM short threshold	If VDPM is shorted to ground, V_{IN_DPM} threshold will use internal default value		0.3		V
V_{UVLO}	IC active threshold voltage	V_{IN} rising	3.15	3.35	3.5	V
	IC active hysteresis	V_{IN} falling from above V_{UVLO}		175		mV
V_{SLP}	Sleep-mode entry threshold, $V_{IN-VBAT}$	2.0 V ≤ V_{BAT} ≤ V_{BATREG}, V_{IN} falling	0	50	100	mV
	Sleep-mode exit hysteresis, $V_{IN-VBAT}$	2.0 V ≤ V_{BAT} ≤ V_{BATREG}	40	100	160	mV
$t_{DGL(SLP)}$	Deglitch time for IN rising above VIN+VSLP_EXIT	Rising voltage, 2-mV over drive, t_{RISE} = 100 ns		32		ms
V_{OVP}	Input supply OVP threshold voltage	IN rising	Input OVP –200mV	Input OVP	Input OVP +200mV	V
	VOVP hysteresis	IN falling from V_{OVP}		100		mV
$t_{DGL(OVP)}$	Deglitch time for IN Rising above VOVP	IN rising voltage, t_{RISE} = 100 ns		32		ms
V_{BOVP}	Battery OVP threshold voltage	V_{BAT} threshold over V_{BATREG} to turn off charger during charge	102.5	105	107.5	% V_{BATREG}
	VBOVP hysteresis	Lower limit for V_{BAT} falling from above V_{BOVP}		1		% V_{BATREG}
$t_{DGL(BOVP)}$	BOVP Deglitch	Battery entering/exiting BOVP		1		ms

ELECTRICAL CHARACTERISTICS (continued)

$V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = 0ºC-125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM CONVERTER						
$R_{ON(BLK)}$	Internal blocking MOSFET on-resistance	Measured from IN to PMID (WCSP & QFN)		60	100	mΩ
$R_{ON(HS)}$	Internal high-side MOSFET on-resistance	Measured from PMID to SW (WCSP & QFN)		100	150	mΩ
$R_{ON(LS)}$	Internal low-side MOSFET on-resistance	Measured from SW to PGND (WCSP & QFN)		110	165	mΩ
I_{CbC}	Cycle-by-cycle current limit	VSYS shorted	2.6	3.2	3.8	A
f_{OSC}	Oscillator frequency		2.7	3	3.3	MHz
D_{MAX}	Maximum duty cycle			95%		
D_{MIN}	Minimum duty cycle		0%			
T_{SHTDWN}	Thermal trip			150		°C
	Thermal hysteresis			10		
T_{REG}	Thermal regulation threshold	Charge current begins to cut off		125		
LDO						
V_{LDO}	LDO Output Voltage	V_{IN} = 5.5 V, I_{LDO} = 0 to 50 mA	4.65	4.85	5.04	V
I_{LDO}	Maximum LDO Output Current		50			mA
V_{DO}	LDO Dropout Voltage (V_{IN} – V_{LDO})	V_{IN} = 5.0 V, I_{LDO} = 50 mA		200	300	mV
BATTERY-PACK NTC MONITOR (1)						
V_{HOT}	High temperature threshold	V_{TS} falling	29.6	30	30.4	% V_{LDO}
$V_{HYS(HOT)}$	Hysteresis on high threshold	V_{TS} rising		1		
V_{WARM}	Warm temperature threshold	V_{TS} falling	37.9	38.3	38.7	
$V_{HYS(WARM)}$	Hysteresis on warm temperature threshold	V_{TS} rising		1		
V_{COOL}	Cool temperature threshold	V_{TS} rising	56.1	56.5	56.9	
$V_{HSY(COOL)}$	Hysteresis on cool temperature threshold	V_{TS} falling		1		
V_{COLD}	Low temperature threshold	V_{TS} rising	59.6	60	60.4	
$V_{HYS(COLD)}$	Hysteresis on low threshold	V_{TS} falling		1		
V_{FRZ}	Freeze temperature threshold	V_{TS} rising	62	62.5	63	
$V_{HYS(FRZ)}$	Hysteresis on freeze threshold	V_{TS} falling		1		
V_{TS_DIS}	TS disable threshold		70		73	
$t_{DGL(TS)}$	Deglitch time on TS change			32		ms
INPUTS (EN1, EN2, EN2, $\overline{CE}$, CE1, CE2, BATREG, SCL, SDA, DBP)						
V_{IH}	Input high threshold		1			V
V_{IL}	Input low threshold				0.4	V
STATUS OUTPUTS ($\overline{CHG}$, $\overline{PG}$, STAT, INT, $\overline{BATRDY}$)						
V_{OL}	Low-level output saturation voltage	I_O = 5 mA, sink current			0.4	V
I_{IH}	High-level leakage current	Hi-Z and 5V applies			1	µA
TIMERS						
t_{SAFETY}	45 min safety timer			2700		s
	6 hr safety timer			21600		
	9 hr safety timer			32400		
$t_{WATCH-DOG}$	Watch dog timer			50		s

ELECTRICAL CHARACTERISTICS (continued)

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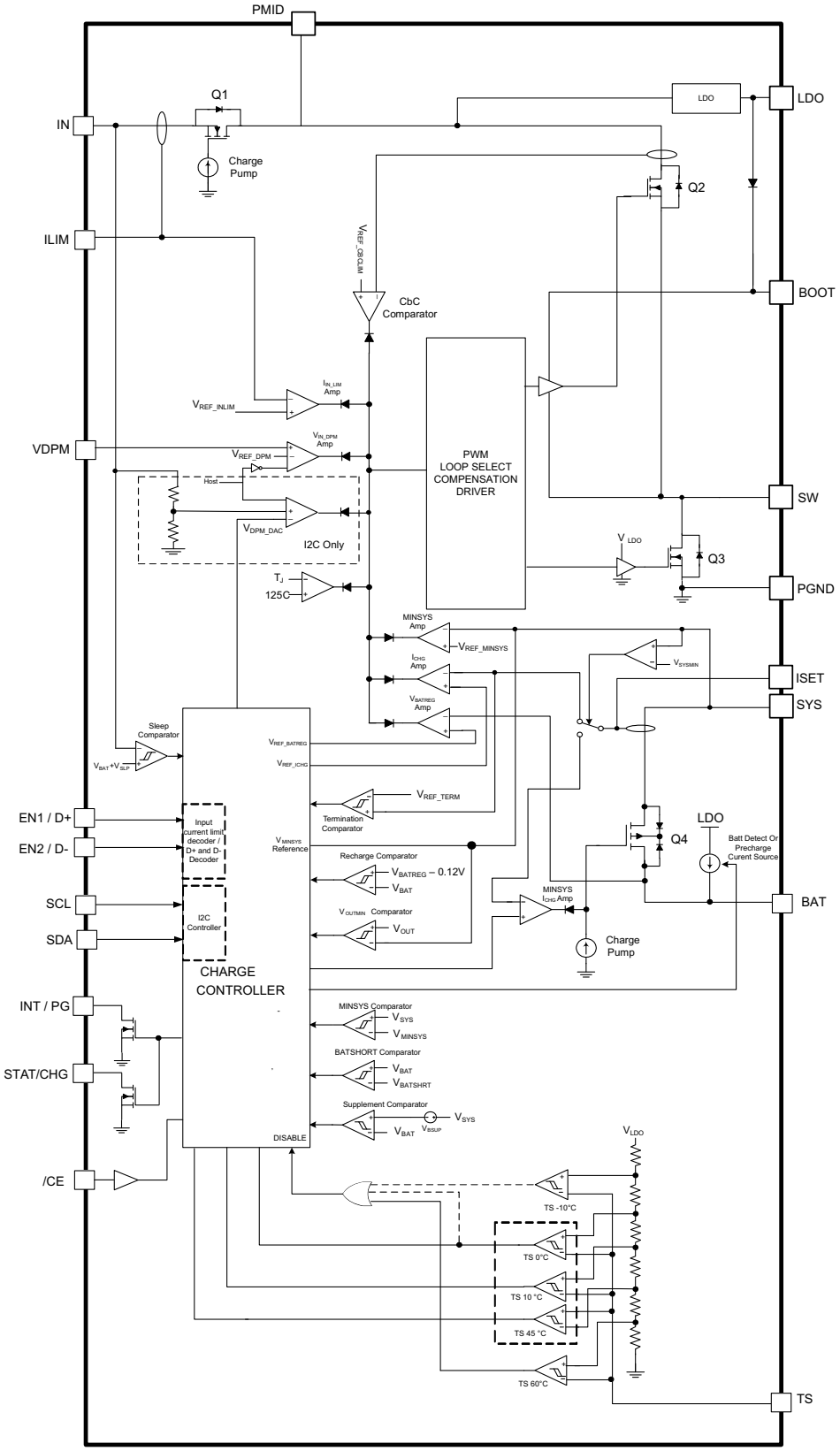
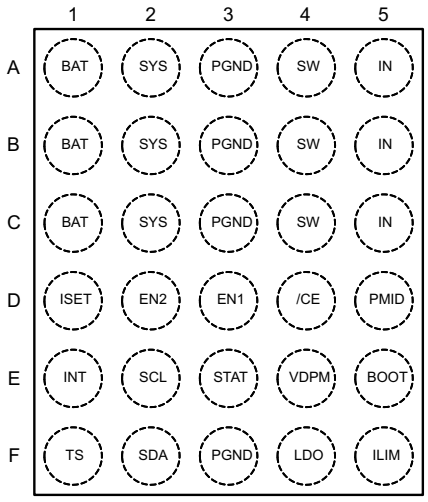
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D+/D– DETECTION						
I_{DP_SRC}	D+ current source for DCD	DCD	7		13	µA
R_{DM_DWN}	D– pull-down resistance for DCD	DCD	14.25		24.8	kΩ
V_{DP_LOW}	D+ low comparator threshold for DCD	DCD	0.85	0.9	0.95	V
V_{DP_SRC}	D+ source voltage for Primary Detection	Primary Detection	0.5	0.6	0.7	V
$I_{DP\_SRC\_PD}$	D+ source voltage output current for Primary Detection	Primary Detection	200			µA
I_{DM_SINK}	D– sink current for Primary Detection	Primary Detection	50	100	150	µA
V_{DAT_REF}	Primary Detection threshold	Primary Detection	250	325	400	mV
V_{LGC}	Primary Detection threshold	Primary Detection	0.85	0.9	0.95	V
V_{DM_SRC}	D- source voltage for Secondary Detection	Secondary Detection	0.5	0.6	0.7	V
$I_{DM\_SRC\_PD}$	D- source voltage output current for Secondary Detection	Secondary Detection	200			µA
I_{DP_SINK}	D+ sink current for Secondary Detection	Secondary Detection	50	100	150	µA
V_{DAT_REF}	Secondary Detection threshold	Secondary Detection	250	325	400	mV
V_{ATT_LO}	Apple/TomTom detection low threshold	Apple/TomTom Detection	1.8	1.85	1.975	V
V_{ATT_HI}	Apple/TomTom detection high threshold	Apple/TomTom Detection	3.2	3.5	4.05	V
C_I	Input Capacitance	D– , switch open		4.5		pF
		D+, switch open		4.5		
I_{D_LKG}	Leakage Current into D+/D–	D–, switch open	–1		1	µA
		D+, switch open	–1		1	

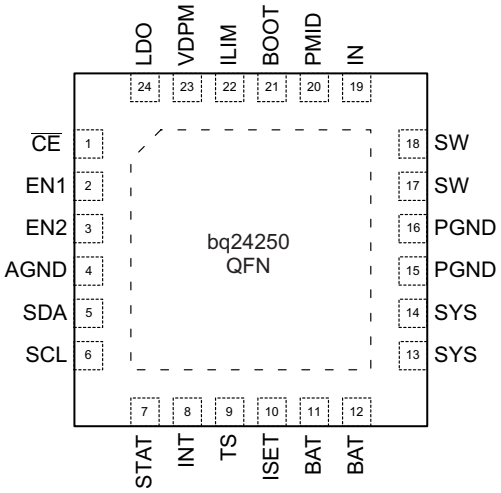
BLOCK DIAGRAM

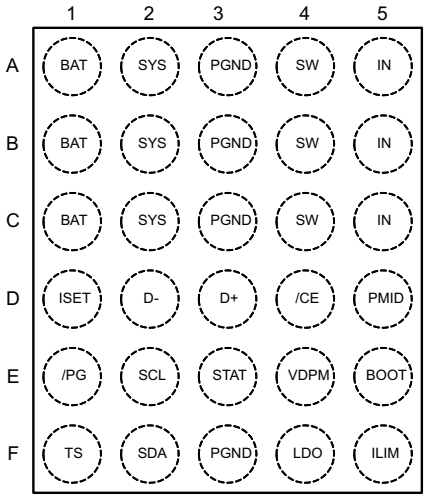


PIN OUTS

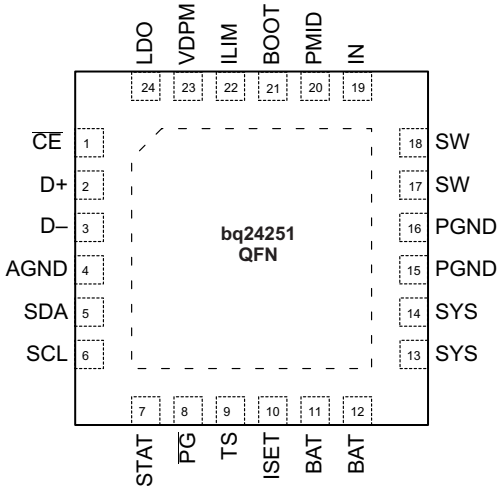


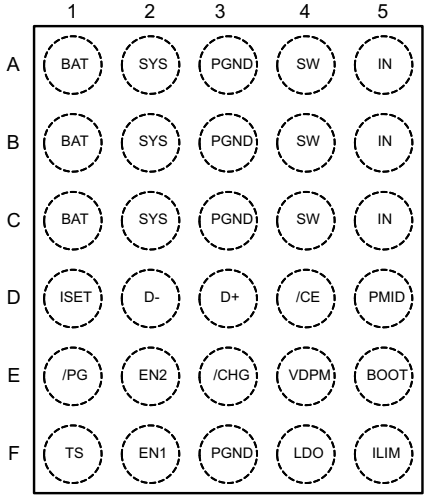
bq24250 WCSP



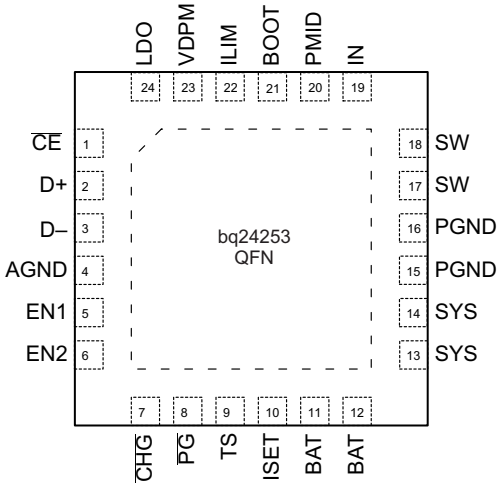


bq24251 WCSP





bq24253 WCSP



PIN DESCRIPTIONS

PIN NAME	bq24250 YFF	bq24250 RGE	bq24251 YFF	bq24251 RGE	bq24253 YFF	bq24253 RGE	I/O	DESCRIPTION
IN	A5,B5,C5	19	A5,B5,C5	19	A5,B5,C5	19	I	Input power supply. IN is connected to the external DC supply (AC adapter or USB port). Bypass IN to PGND with >2µF ceramic capacitor
PMID	D5	20	D5	20	D5	20	I	Connection between blocking FET and high-side FET.
SW	A4, B4, C4	17–18	A4, B4, C4	17–18	A4, B4, C4	17–18	O	Inductor Connection. Connect to the switching side of the external inductor.
BOOT	E5	21	E5	21	E5	21	I	High Side MOSFET Gate Driver Supply. Connect a 0.033µF ceramic capacitor (voltage rating > 15V) from BOOT to SW to supply the gate drive for the high side MOSFETs.
PGND	A3, B3, C3, F3	15–16	A3, B3, C3, F3	15–16	A3, B3, C3, F3	15–16		Ground terminal. Connect to the ground plane of the circuit.
SYS	A2, B2, C2	13–14	A2, B2, C2	13–14	A2, B2, C2	13–14	I	System Voltage Sense and SMPS output filter connection. Connect SYS to the system output at the output bulk capacitors. Bypass SYS locally with >20µF.
BAT	A1, B1, C1	11–12	A1, B1, C1	11–12	A1, B1, C1	11–12	I/O	Battery Connection. Connect to the positive terminal of the battery. Additionally, bypass BAT with a >1µF capacitor.
TS	F1	9	F1	9	F1	9	I	Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from LDO to GND. The NTC is connected from TS to GND. The TS function provides 4 thresholds for JEITA or PSE compatibility. See the *NTC Monitor* section for more details on operation and selecting the resistor values.
VDPM	E4	23	E4	23	E4	23	I	Input DPM Programming Input. Connect a resistor divider between IN and GND with VDPM connected to the center tap to program the Input Voltage based Dynamic Power Management threshold (V_{IN_DPM}). The input current is reduced to maintain the supply voltage at V_{IN_DPM}. The reference for the regulator is 1.23V. Short pin to GND if external resistors are not desired—this sets a default of 4.36V for the input DPM threshold.
ISET	D1	10	D1	10	D1	10	I	Charge Current Programming Input. Connect a resistor from ISET to GND to program the fast charge current. The charge current is programmable from 300mA to 2A.
ILIM	F5	22	F5	22	F5	22	I	Input Current Limit Programming Input. Connect a resistor from ILIM to GND to program the input current limit for IN. The current limit is programmable from 0.5A to 2A. ILIM has no effect on the USB input. If an external resistor is not desired, short to GND for a 2A default setting.
$\overline{CE}$	D4	1	D4	1	D4	1	I	Charge Enable Active-Low Input. Connect CE to a high logic level to place the battery charger in standby mode.
EN1	D3	2	–	–	F2	5	I	Input Current Limit Configuration Inputs. Use EN1, and EN2 to control the maximum input current and enable USB compliance. See Table 1 for programming details.
EN2	D2	3	–	–	E2	6	I	
$\overline{CHG}$	–	–	–	–	E3	7	O	Charge Status Open Drain Output. $\overline{CHG}$ is pulled low when a charge cycle starts and remains low while charging. $\overline{CHG}$ is high impedance when the charging terminates and when no supply exists. $\overline{CHG}$ does not indicate recharge cycles.

PIN DESCRIPTIONS (continued)

PIN NAME	bq24250 YFF	bq24250 RGE	bq24251 YFF	bq24251 RGE	bq24253 YFF	bq24253 RGE	I/O	DESCRIPTION
$\overline{PG}$	–	–	E1	8	E1	8	O	Power Good Open Drain Output. $\overline{PG}$ is pulled low when a valid supply is connected to IN. A valid supply is between $V_{BAT}+V_{SLP}$ and V_{OVP}. If no supply is connected or the supply is out of this range, $\overline{PG}$ is high impedance.
STAT	E3	7	E3	7	–	–	O	Status Output. STAT is an open-drain output that signals charging status and fault interrupts. STAT pulls low during charging. STAT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 256µs pulse is sent out as an interrupt for the host. STAT is enabled/disabled using the EN_STAT bit in the control register. STAT will indicate recharge cycles. Connect STAT to a logic rail using an LED for visual indication or through a 10kΩ resistor to communicate with the host processor.
INT	E1	8	–	–	–	–	O	Status Output. INT is an open-drain output that signals charging status and fault interrupts. INT pulls low during charging. INT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 256µs pulse is sent out as an interrupt for the host. INT will indicate recharge cycles. Connect INT to a logic rail through a 10kΩ resistor to communicate with the host processor.
SCL	E2	6	E2	6	–	–	I	I^2C Interface Clock. Connect SCL to the logic rail through a 10kΩ resistor.
SDA	F2	5	F2	5	–	–	I/O	I^2C Interface Data. Connect SDA to the logic rail through a 10kΩ resistor.
D+	–	–	D3	2	D3	2	I	BC1.2 compatible D+/D– Based Adapter Detection. Detects DCP, SDP, and CDP. Also complies with the unconnected dead battery provision clause. D+ and D- are connected to the D+ and D– outputs of the USB port at power up. Also includes the detection of Apple™ and TomTom™ adapters where a 500mA input current limit is enabled. The $\overline{PG}$ pin will remain low until the detection has completed.
D–	–	–	D2	3	D2	3	I	
LDO	F4	24	F4	24	F4	24	O	LDO output. LDO is regulated to 4.9V and drives up to 50mA. Bypass LDO with a 1µF ceramic Capacitor. LDO is enabled when $V_{UVLO} < V_{IN}$ <18V.
AGND	–	4	–	4	–	4		Analog Ground for QFN only. Connect to the thermal pad and the ground plane of the circuit.

TYPICAL APPLICATION CIRCUITS

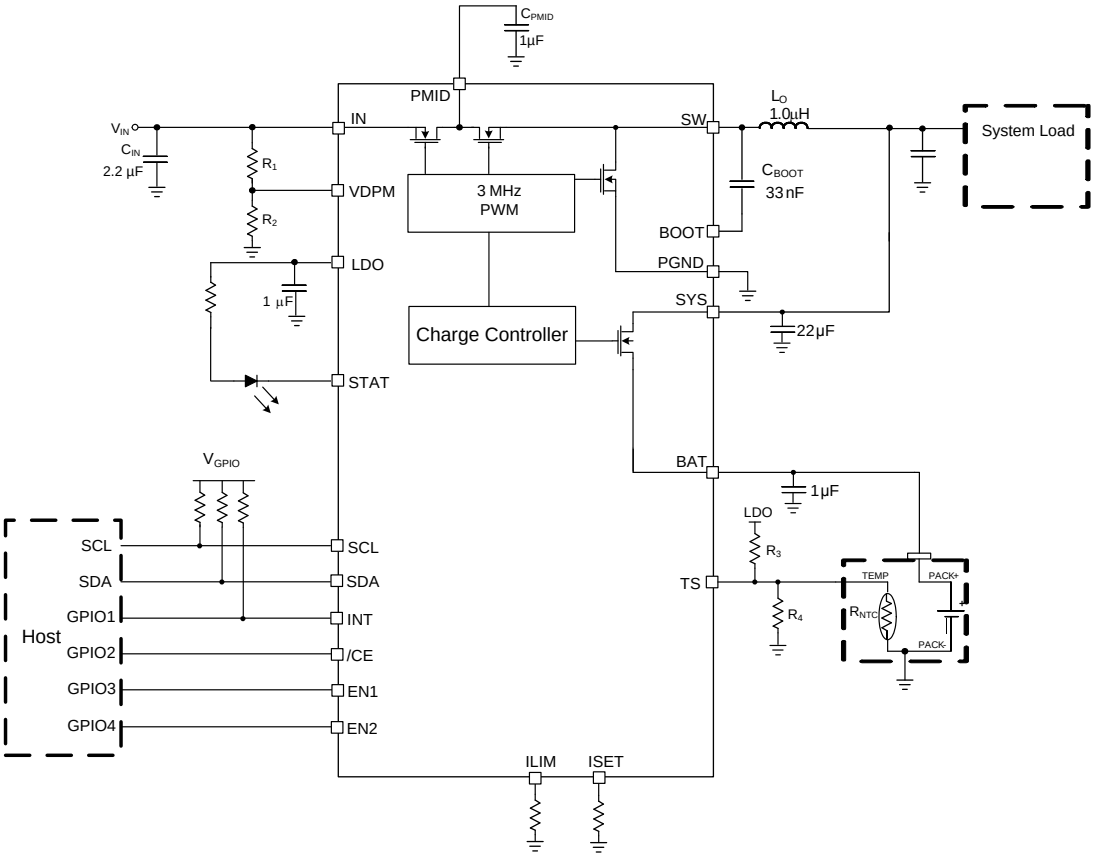


Figure 1. bq24250 Typical Application Circuit

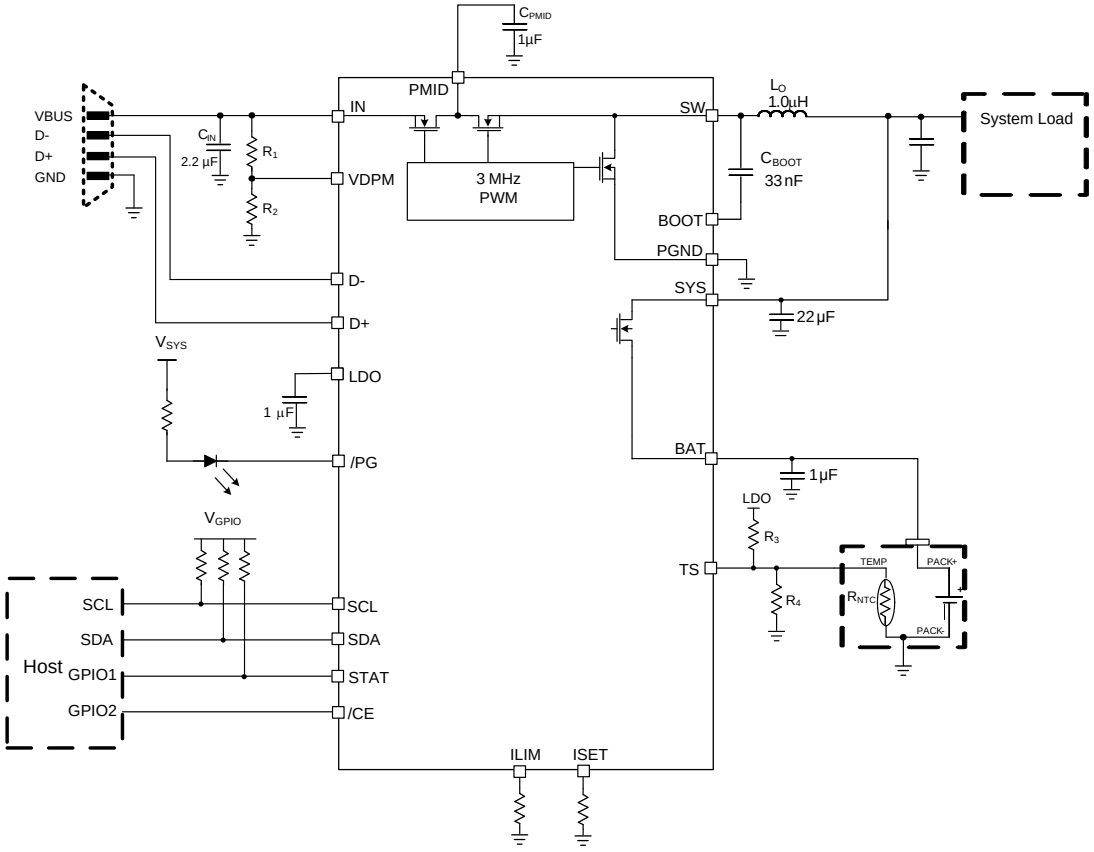


Figure 2. bq24251 Typical Application Circuit

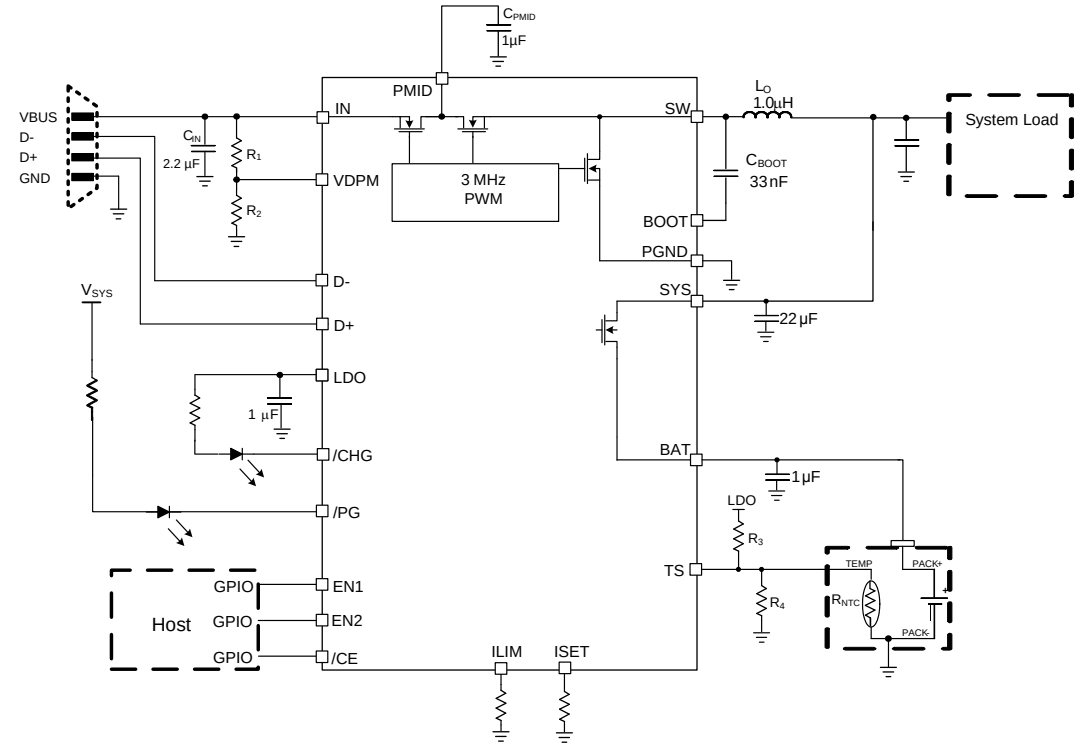


Figure 3. bq24253 Typical Application Circuit

TYPICAL CHARACTERISTICS

Battery Detection

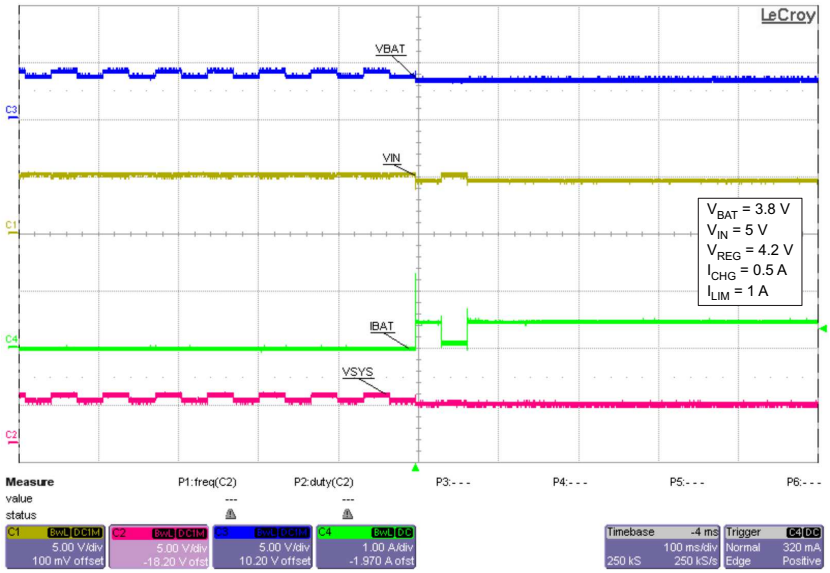


Figure 4.

Battery Removal

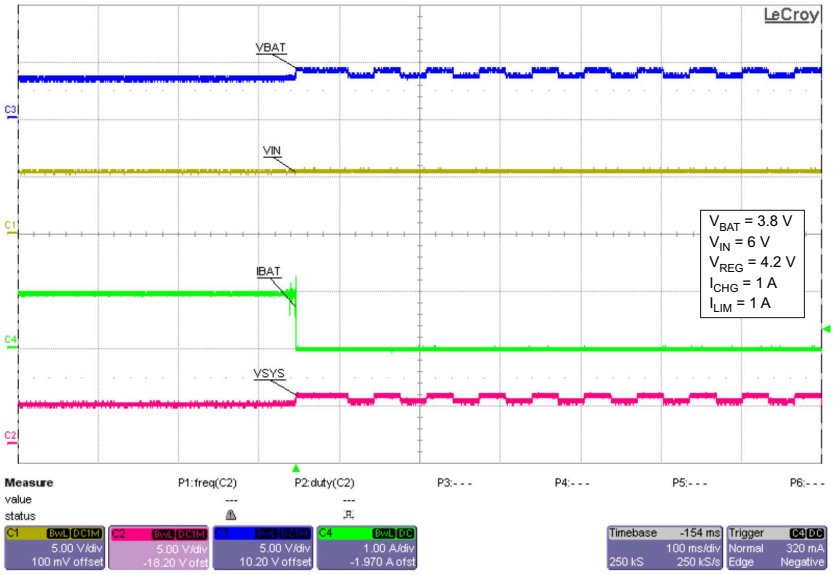


Figure 5.

TYPICAL CHARACTERISTICS (continued)

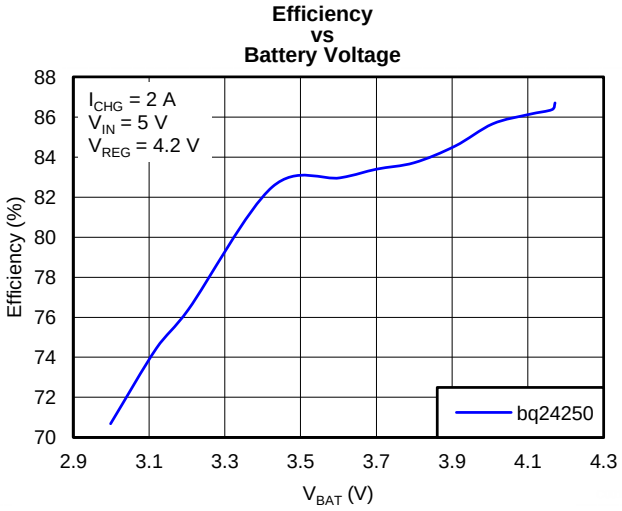


Figure 6.

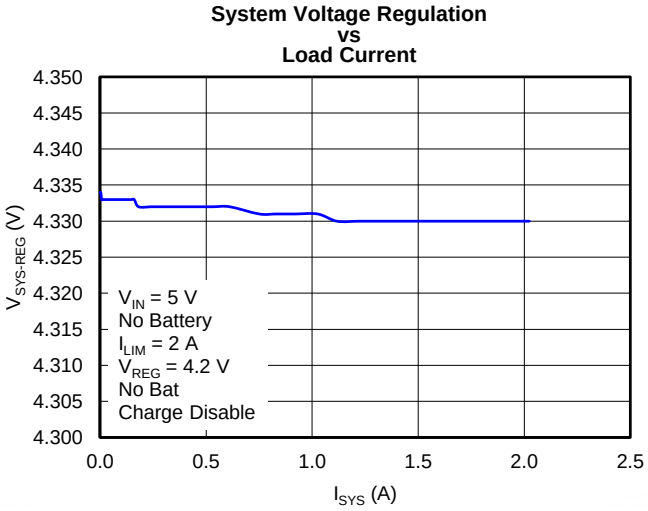


Figure 7.

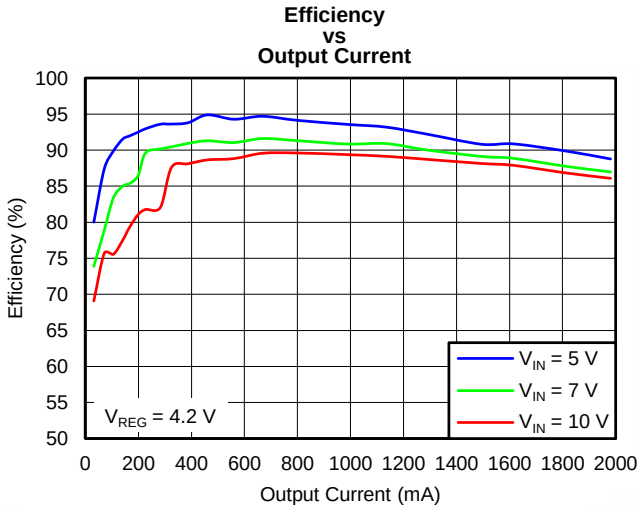


Figure 8.

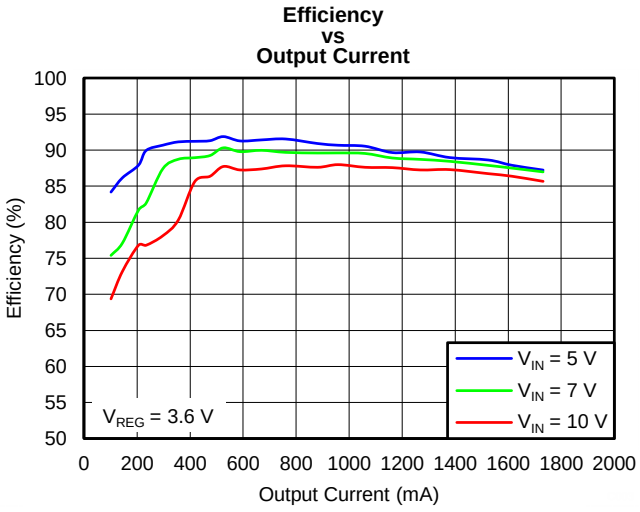


Figure 9.

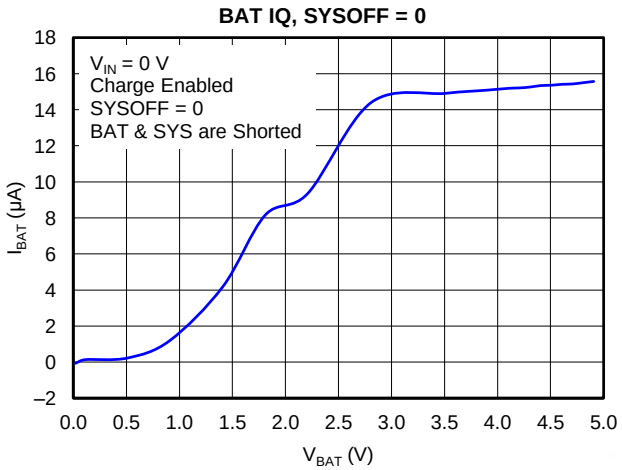


Figure 10.

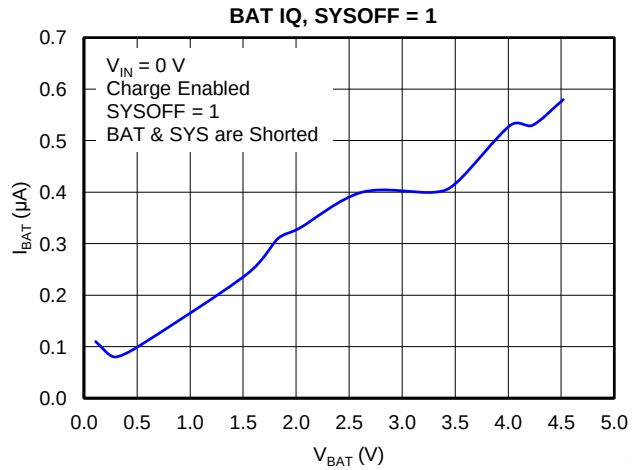


Figure 11.

TYPICAL CHARACTERISTICS (continued)

Input IQ With Charge DIS and EN

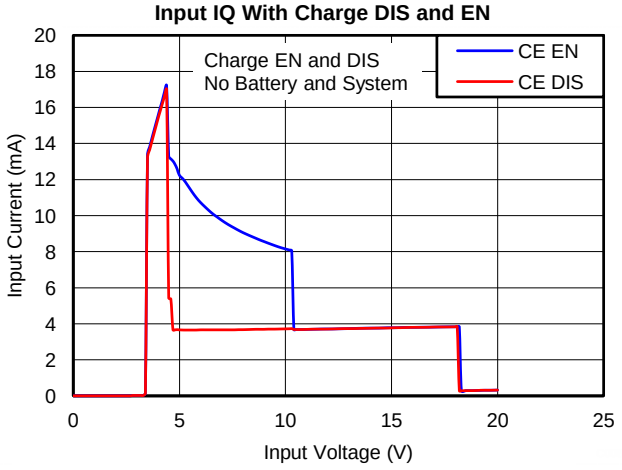


Figure 12.

Input IQ with Charge Enable and Hi-Z

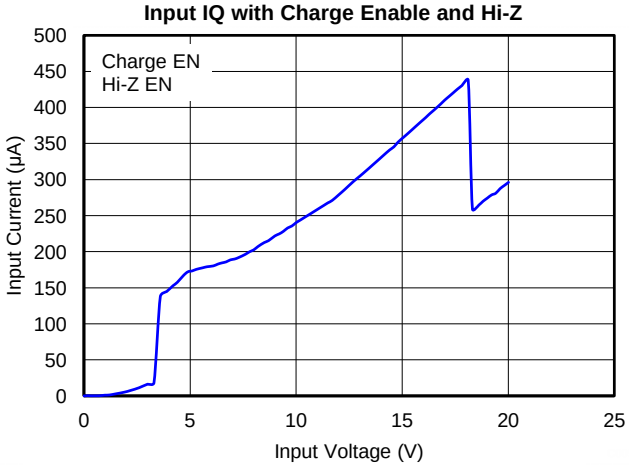


Figure 13.

I_{CHG} Accuracy with Internal Settings, V_{BAT} = 3.3 V

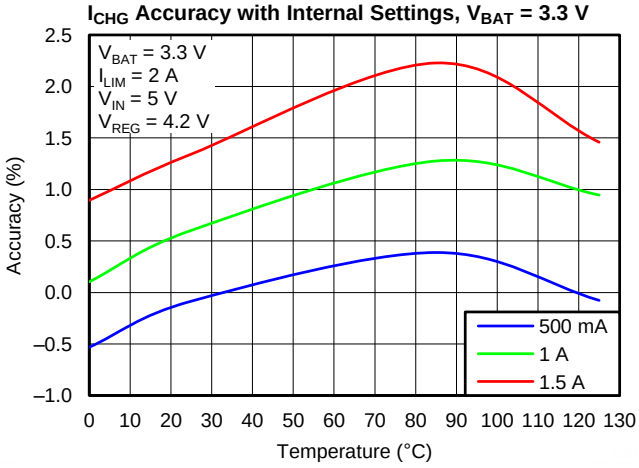


Figure 14.

I_{CHG} Accuracy with Internal Settings, V_{BAT} = 3.8 V

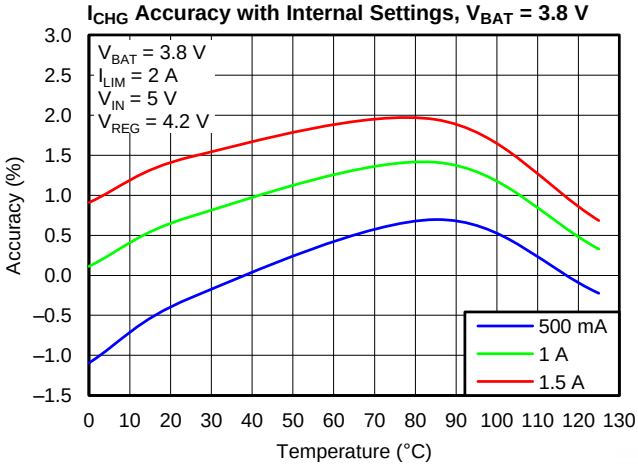


Figure 15.

Startup

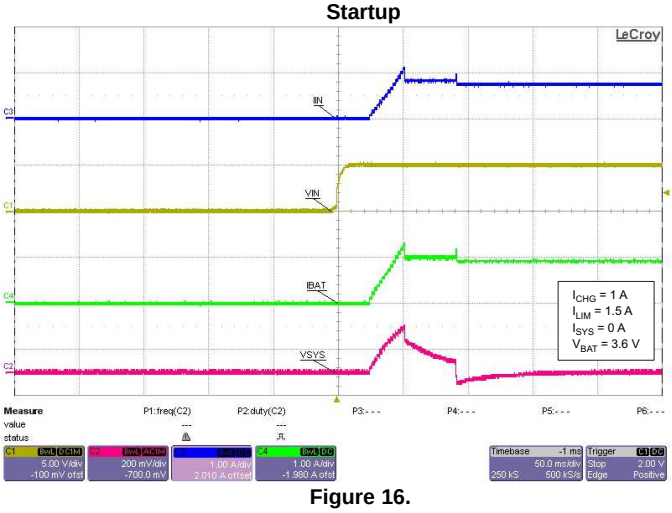


Figure 16.

Input OVP Event with INT

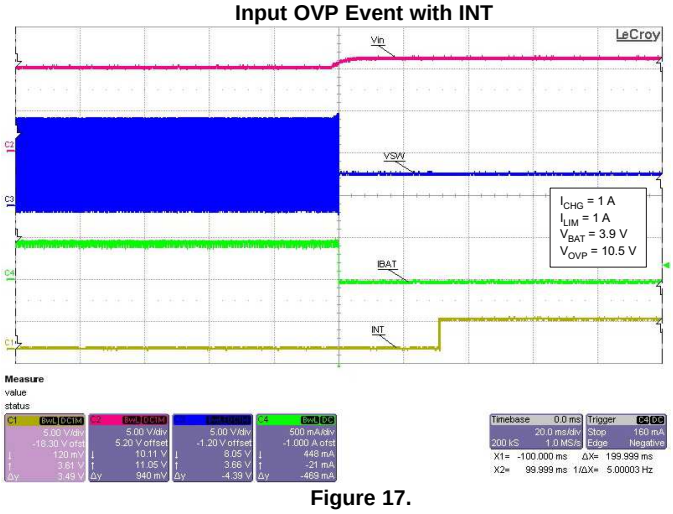


Figure 17.

TYPICAL CHARACTERISTICS (continued)

V_{DPM} Startup, 4.2 V

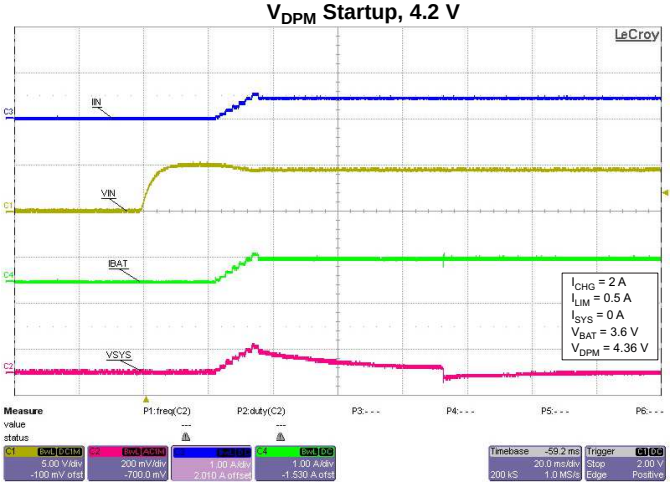


Figure 18.

1.0 µH CCM Operation

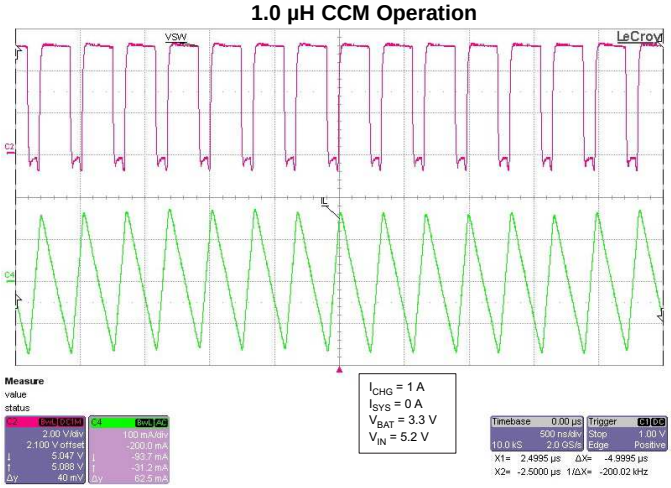


Figure 19.

CHARGE PROFILE

The bq2425x family provides a switch-mode buck regulator with output power path and a charge controller to provide optimum performance over the full battery charge cycle. The control loop for the buck regulator has 7 primary feedback loops that can set the duty cycle:

1. Constant Current (CC)
2. Constant Voltage (CV)
3. Minimum System Voltage (MINSYS)
4. Input Current (I_{ILIM})
5. Input Voltage (V_{IN_DPM})
6. Die Temperature
7. Cycle by Cycle Current

The feedback with the minimum duty cycle will be chosen as the active loop. The bq24250, 1, 3 support a precision Li-Ion or Li-Polymer charging system for single-cell applications. The Dynamic Power Path Management (DPPM) feature regulates the system voltage to a minimum of V_{MINSYS}, so that startup is enabled even with a missing or deeply discharged battery. This provides a much better overall user experience in mobile applications. The figure below illustrates a typical charge profile while also demonstrating the minimum system output voltage regulation.

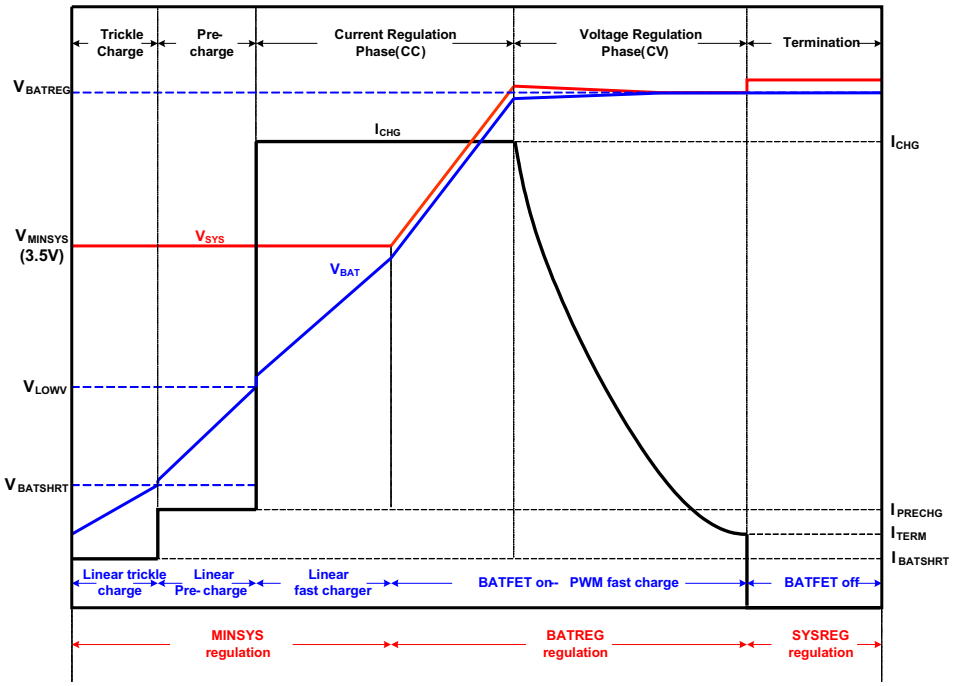


Figure 20 demonstrates a measured charge profile with the bq2425X while charging a 2700mAh Li-Ion battery at a charge rate of 1A.

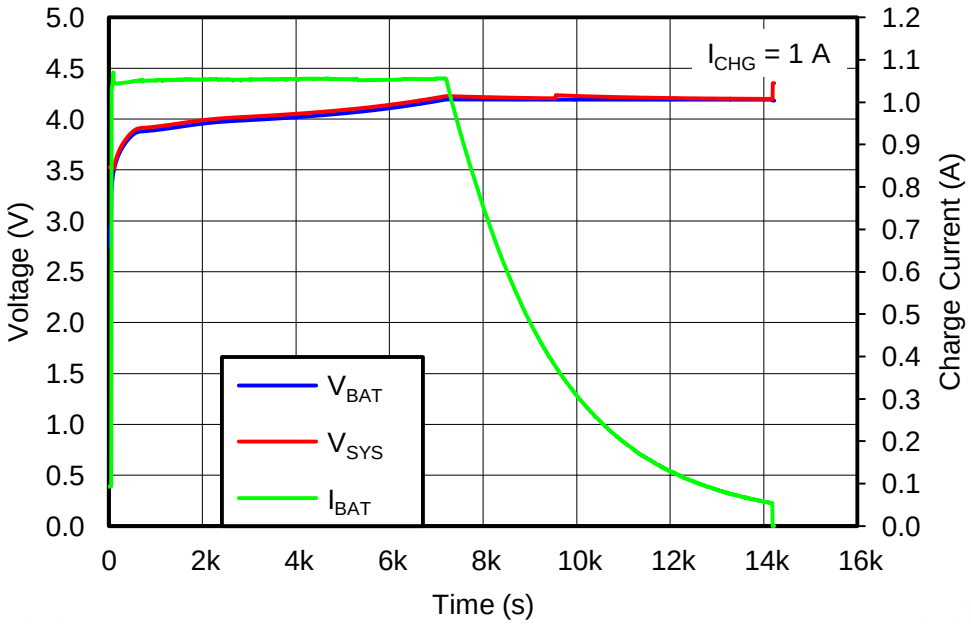


Figure 20. bq24250 Charge Profile while Charging a 2700 mAh Battery at a 1A Charge Rate

Figure 21 illustrates the precharge behavior of the above charge profile by narrowing the time axis to 0 – 120 seconds.

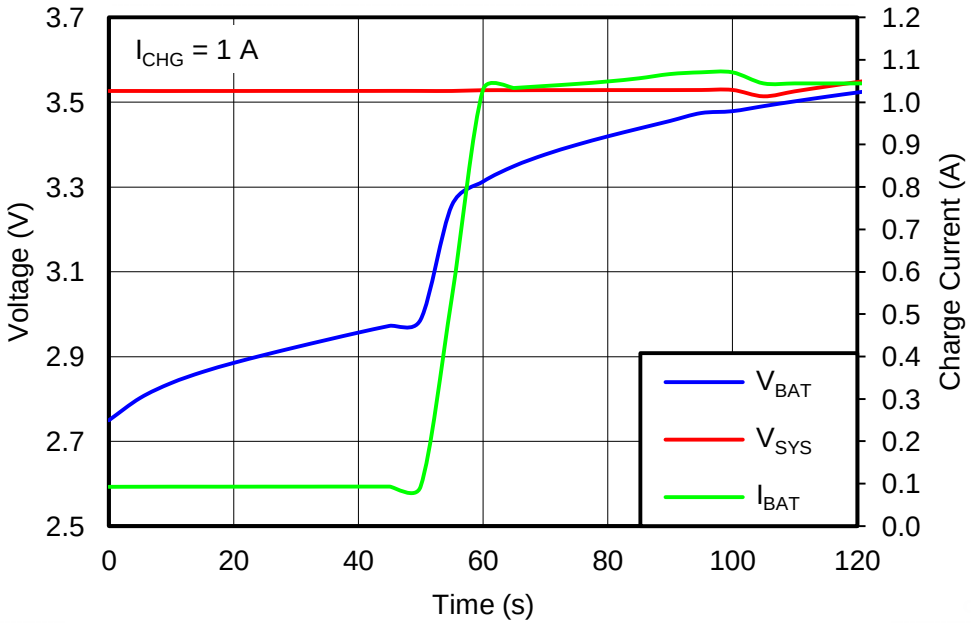


Figure 21. bq24250 Charge Profile While Charging a 2700-mAh Battery at a 1A Charge During Precharge

EN1/EN2 PINS

The bq24250 is I^2C and Stand Alone part. The EN1 and EN2 pins are available in this IC spin to support USB 2.0 compliance. These pins are used for Input Current Limit Configuration I. Set EN1 and EN2 to control the maximum input current and enable USB compliance. See Table 1 below for programming details.

The bq24251 is also an I²C and Stand Alone part. The EN1 and EN2 are not available for this spin but the D+/D- are available to support the BC1.2 D+/D- Based Adapter Detection. It detects DCP, SDP, and CDP. Also it complies with the unconnected dead battery provision clause. D+ and D- pins are connected to the D+ and D- outputs of the USB port at power up. Also includes the detection of Apple™ and TomTom™ adapters where a 500mA input current limit is enabled. The /PG pin will remain high impedance state until the detection is completed.

The bq24253 is only Stand Alone part. Both of the D+/D- and EN1/EN2 are available for this spin. During power up, the device checks first for the D+/D-. The EN1 and EN2 do not take effect until D+/D- detection routine is over and a change on the status of the EN1 and EN2 occurred.

When the input current limit pins change state, the V_{IN_DPM} threshold changes as well. See Table 1 for the detailed truth table:

Table 1. EN1, and EN2 Truth Table(1)

EN2	EN1	Input Current Limit	V_{IN_DPM} Threshold
0	0	500mA	4.36V
0	1	Externally programmed by ILIM (up to 2.0A)	Externally programmed VDPM
1	0	100mA	4.36V
1	1	Input Hi-Z	None

(1) USB3.0 support available. Contact your local TI representative for details.

I²C Operation (Host Mode / Default Mode)

There are two primary modes of operation when interacting with the charge parameters of the bq24250 and bq24251 chargers: 1) *Host mode* operation where the I²C registers set the charge parameters, and 2) *Default mode* where the register defaults set the charge parameters.

Figure 22 illustrates the behavior of the bq24250 when transitioning between host mode and stand alone mode:

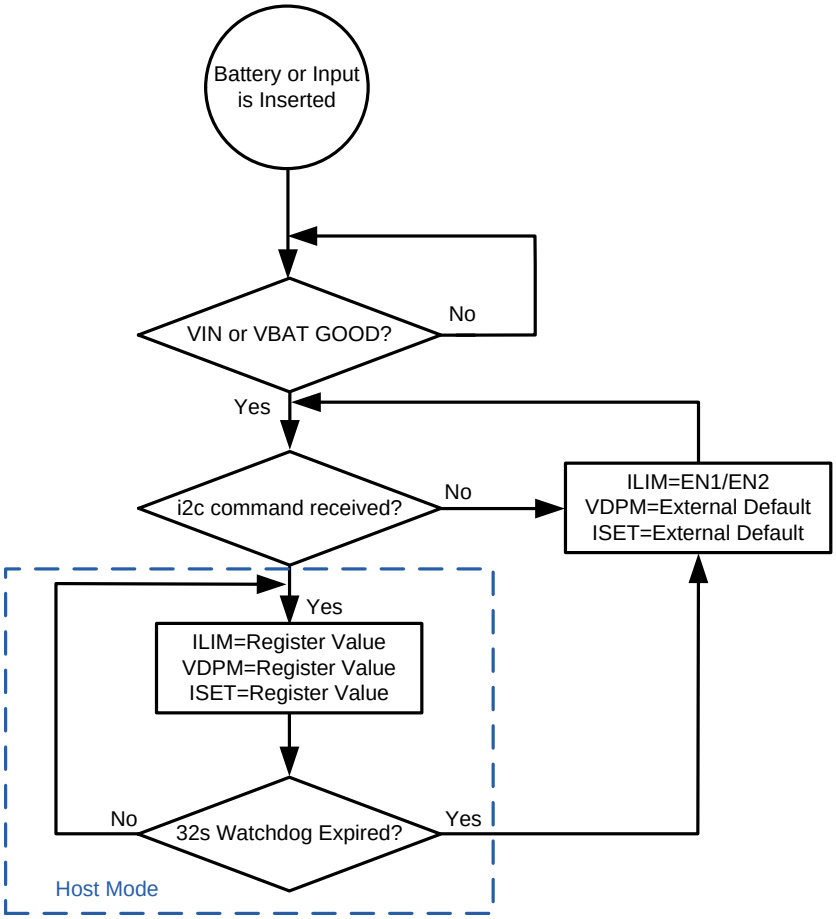


Figure 22. Host Mode and Stand Alone Mode Handoff

Once the battery or input is inserted and above the good thresholds, the device determines if an I^2C command has been received in order to discern whether to operate from the I^2C registers or the internal register defaults. In stand-alone mode the input current limit is set by the EN1/EN2 pins. If the watch dog timer is enabled, the device will enter stand alone operation once the watchdog timer expires and re-initiate the default charge settings.

External Settings: ISET, ILIM and VIN_DPM

If the external resistor settings are used, the following equations can be followed to configure the charge settings.

The fast charge current resistor (R_{ISET}) can be set by using the following formula:

$$R_{ISET} = \frac{K_{ISET}}{I_{FC}} = \frac{250}{I_{FC}} \quad (1)$$

Where I_{FC} is the desired fast charge current setting in Amperes.

The input current limit resistor (R_{ILIM}) can be set by using the following formula:

$$R_{ILIM} = \frac{K_{ILIM}}{I_{IC}} = \frac{270}{I_{IC}} \quad (2)$$

Where I_{IC} is the desired input current limit in Amperes.

Based on the application diagram reference designators, the resistor R1 and R2 can be calculated as follows to set V_{IN_DPM}:

$$V_{IN\_DPM} = V_{REF\_DPM} \times \frac{R_1 + R_2}{R_2} = 1.2V \times \frac{R_1 + R_2}{R_2} \quad (3)$$

V_{IN_DPM} should be chosen first along with R_1. Choosing R_1 first will ensure that R_2 will be greater than the resistance chosen. This is the case since V_{IN_DPM} should be chosen to be greater than 2x V_{REF_DPM}.

If external resistors are not desired in order to reduce the BOM count, the VDPM and the ILIM pins can be shorted to set the internal defaults. The ISET resistor must be floated in order to avoid an internal fault detection. Note that floating the ILIM pin will result in zero charge current if the external ISET is configured via the I^2C register. Table 2 summarizes the settings when the ILIM, ISET, and V_{IN_DPM} pins are shorted to GND:

Table 2. ILIM, VDPM, and ISET Short Behaviors

PIN SHORTED	BEHAVIOR
ILIM	Input current limit = 2A
VDPM	V_{IN_DPM} = 4.36V
ISET	Fault—Charging Suspended

BC1.2 D+/D– Detection

The bq24251 and the bq24253 include a fully BC1.2 compatible D+/D– source detection. This detection supports the following types of ports:

- DCP (dedicated charge port)
- CDP (charging downstream port)
- SDP (standard downstream port)
- Apple™/TomTom™ ports

This D+/D– detection algorithm does not support ACA (accessory charge adapter) identification, but the input current will default to 500mA when a charge port is attached to the ACA and bq24251/3 is connected to the OTG port.

The D+/D– detection algorithm is only active when the device is in standalone mode (e.g. the host is not communicating with the device and the watch dog timer has expired). However, when the device is in host mode (e.g. host is communicating via I^2C to the device) writing a '1' to register 0x04 bit location 4 (DPDM_EN) forces the device to perform a D+/D– detection on the next power port insertion. This allows the D+/D– detection to be enabled in both host mode and default mode.

As described previously, the bq24253 is only a Stand Alone part. Both of the D+/D- and EN1/EN2 are available for this spin. The below flow diagram illustrates the behavior of the bq24253 in D+/D- detection and the effect of the EN1/EN2. During power up, the device checks first for the D+/D-. The EN1 and EN2 do not take effect until D+/D- detection routine is over and a change on the status of the EN1 and EN2 occurred.

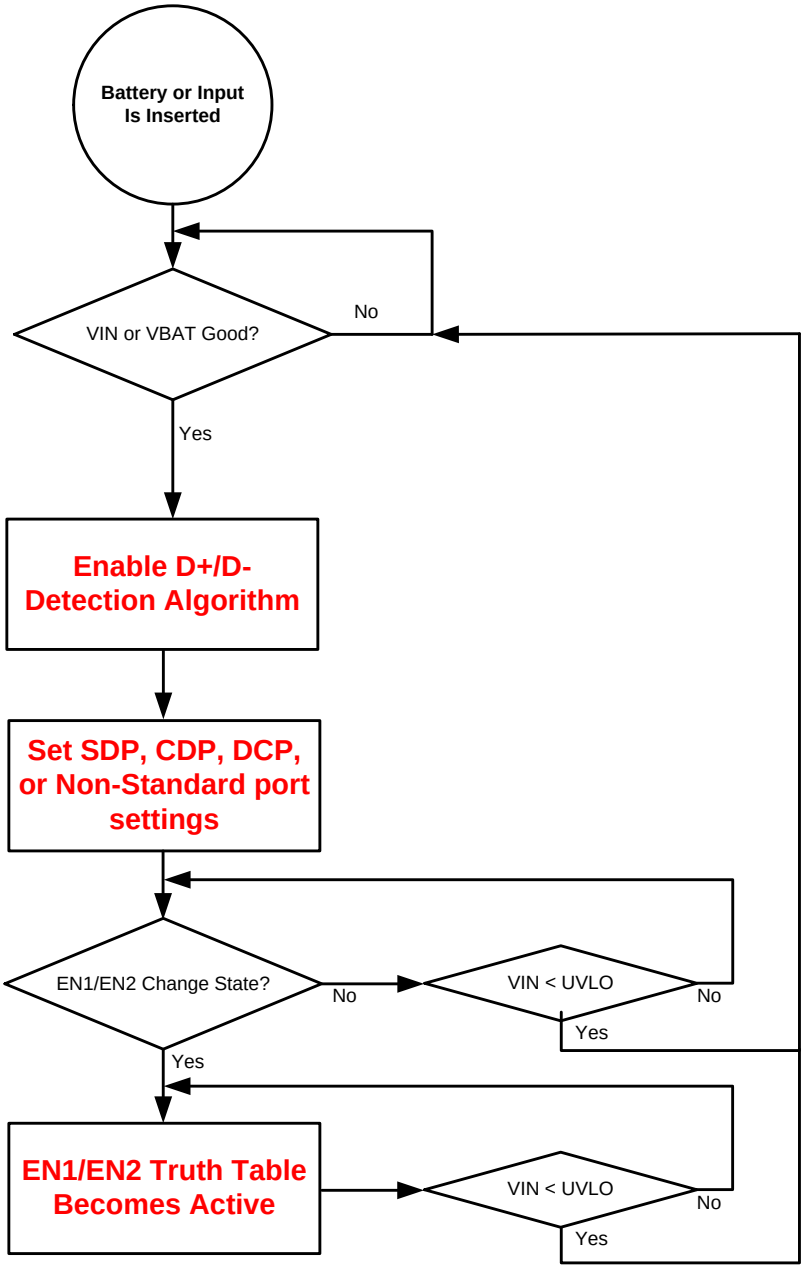


Figure 23. bq24253 D+/D- and EN1/EN2

The D+/D– detection algorithm has 5 primary states. These states are termed the following:

1. Data Contact Detect
2. Primary Detection
3. Secondary Detection
4. Non-standard Adapter Detection (for Apple™ / TomTom™)
5. Detection Configuration

The DCD state determines if the device has properly connected to the D+/D– lines. If the device is not in host mode and VBUS is inserted (or DPDM_EN is true) the device enters the DCD state and enable the appropriate algorithm. If the DCD timer expires, the device enters the Non-standard Adapter Detection (for Apple™ / TomTom™) state. Otherwise it enters the Primary Detection state.

When entering the Primary Detection state, the appropriate algorithm is enabled to determine whether to enter the secondary detection state for DCP and CDP or the secondary detection state for SDP/Non-Standard adaptors.

The non-standard adapter detection state for Apple™ / TomTom™ tests for the unique conditions for these non-standard adapters. If the algorithm passes the unique conditions found with these adapters, it proceeds to the Detection Configuration state. Otherwise it reverts back to the primary detection state.

The secondary detection state determines whether the input port is a DCP, CDP, SDP, or other non-standard adapters. If the Primary Detection state indicated that the input port is either a DCP or CDP, the device enables the appropriate algorithm to differentiate between the two. If the Primary Detection state indicated that the input port is either a SDP or non-standard adapter, the device enables the appropriate algorithm to differentiate between these two ports. Once complete, the device continues to the Detection Configuration state.

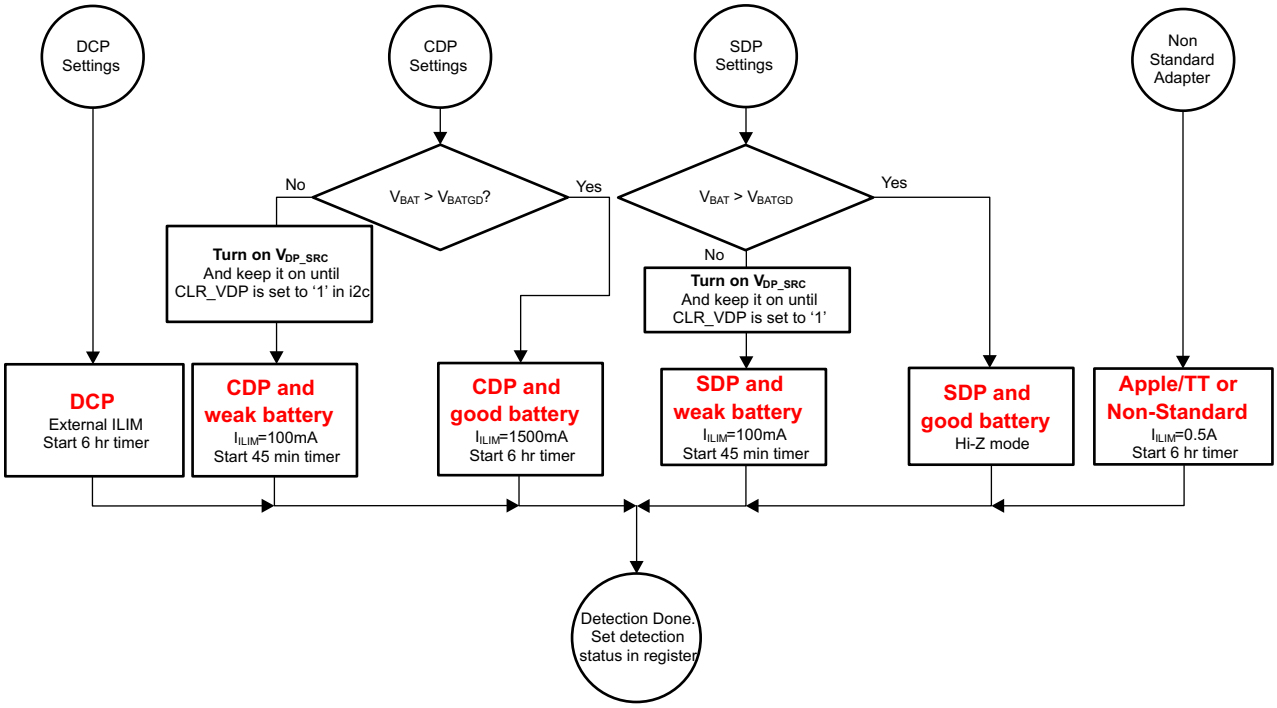


Figure 24. Detection Configuration State

The detection configuration state sets the input current limit of the device along with the charge timer. The exception to the CDP and the SDP settings are due to the Dead Battery Provision (DBP) clause for unconnected devices. This clause states that the device can pull a maximum of 100mA when not connected due to a dead battery. During the battery wakeup time, the device sources a voltage on the D+ pin in order to comply with the DBP clause. Once the battery is good, the system can clear the D+ pin voltage by writing a '1' to address 0x07 bit position 4 (CLR_VDP). The device must connect to the host within 1sec of clearing the D+ pin voltage per the DPB clause.

A summary of the input current limits and timer configurations for each charge port type are found in Table 3.

Table 3. D+/D– Detection Results per Charge Port Type

CHARGE PORT TYPE	INPUT CURRENT LIMIT	CHARGE TIMER
DCP	External ILIM	6 hours
CDP Dead Battery	100 mA	45 minutes
CDP Good Battery	1500 mA	6 hours
SDP Dead Battery	100 mA	45 minutes
SDP Good Battery	Hi-Z	N/A
Non-Standard	500 mA	6 hours

Transient Response

The BQ24250/1/3 includes an advanced hybrid switch mode control architecture. When the device is regulating the charge current (fast-charge), a traditional voltage mode control loop is used with a Type-3 compensation network. However, the BQ24250/1/3 switches to a current mode control loop when the device enters voltage regulation. Voltage regulation occurs in three charging conditions: 1) Minimum system voltage regulation (battery below MINSYS), 2) Battery voltage regulation (I_{BAT} < I_{CHG}), and 3) Charge Done (V_{SYS} = V_{BAT} + 3.5%). This architecture allows for superior transient performance when regulating the voltage due to the simplification of the compensation when using current mode control. The below transient response plot illustrates a 0A to 2A load step with 4.7ms full cycle and 12% duty cycle. A 3.9V Li-Ion battery is used. The input voltage is set to 5V, charge current is set to 0.5A and the input current is limited to 0.5A. Note that a high line impedance input supply was used to indicate a realistic input scenario (adapter and cable). This is illustrated by the change in V_{IN} seen at the input of the IC.

Figure 25 shows a ringing at both the input voltage and the input current. This is caused by the input current limit speed up comparator.

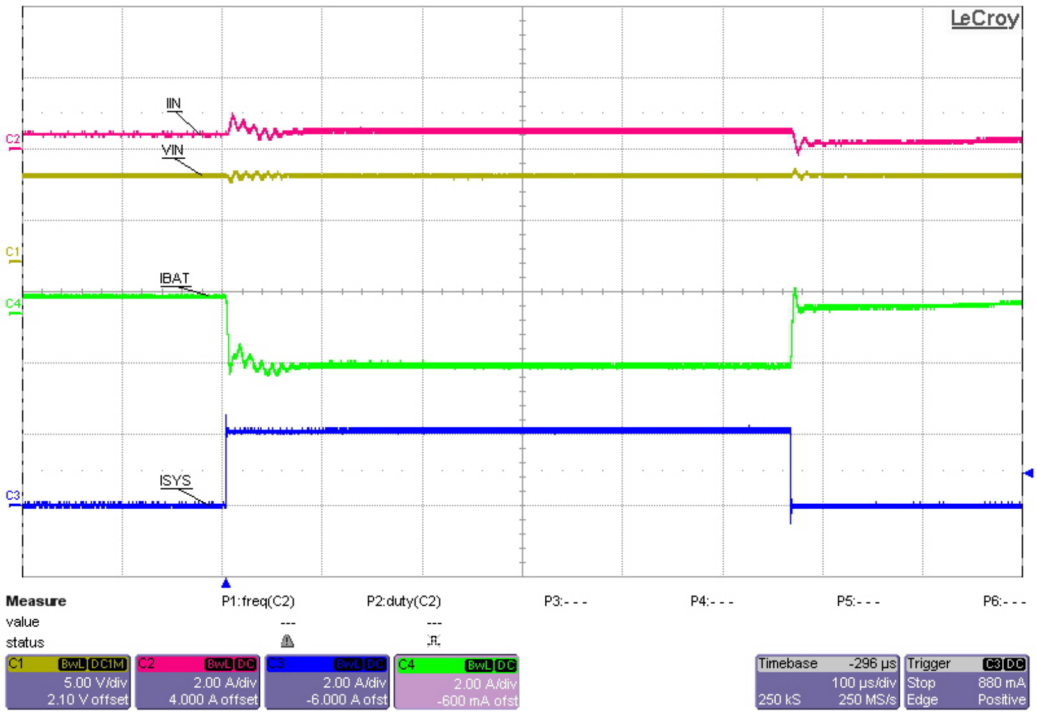


Figure 25. 2A Load Step Transient

AnyBoot Battery Detection

The bq2425x family includes a sophisticated battery detection algorithm used to provide the system with the proper status of the battery connection. The AnyBoot battery algorithm also guarantees the detection of voltage based battery protectors that may have a long closure time (due to the hysteresis of the protection switch and the cell capacity). The AnyBoot battery detection algorithm utilizes a dual-voltage based detection methodology where the system rail switches between two primary voltage levels. The period of the voltage level shift is 64ms and therefore the power supply rejection of the down-system electronics detects this shift as essentially DC.

The AnyBoot algorithm has essentially 3 states. The 1st state is used to determine if the device has terminated with a battery attached. If it has terminated due to the battery not being present, then the algorithm moves to the 2nd and 3rd states. The 2nd and 3rd states shift the system voltage level between 4.2V and 3.72V. In each state there are comparator checks to determine if a battery has been inserted. The two states guarantees the detection of a battery even if the voltage of the cell is at the same level of the comparator thresholds. The algorithm will remain in states 2 and 3 until a battery has been inserted. The flow diagram details for the Anyboot algorithm are shown in Figure 26.

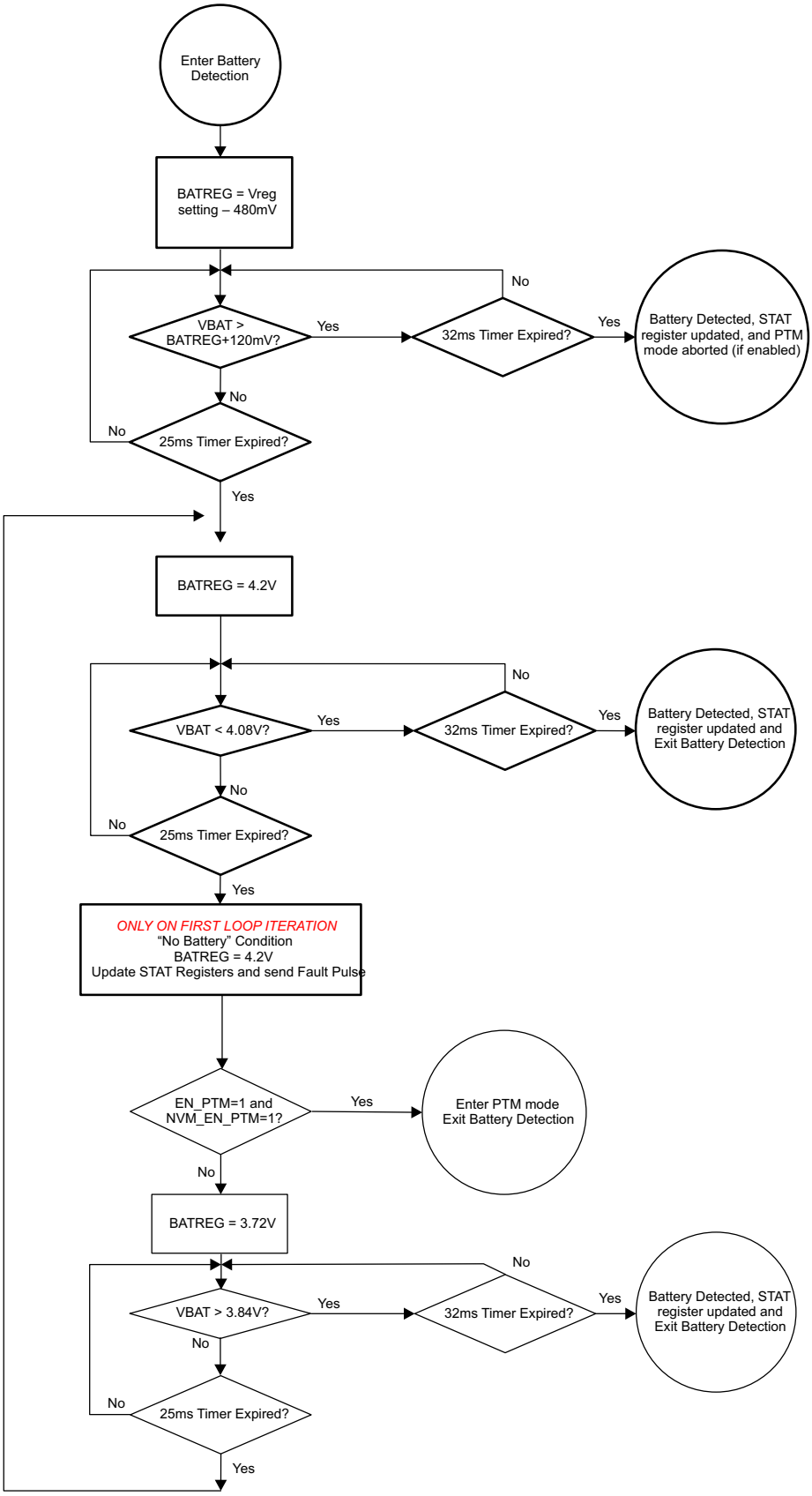


Figure 26. AnyBoot Battery Detection Flow Diagram

Input Voltage Based DPM

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage deceases. Once the supply drops to VIN_DPM, the input current limit is reduced down to prevent the further drop of the supply. When the IC enters this mode, the charge current is lower than the set. This feature ensures IC compatibility with adapters with different current capabilities without a hardware change.

Sleep Mode

The bq2425x enters the low-power sleep mode if the voltage on VIN falls below sleep-mode entry threshold, VBAT+VSLP, and VIN is higher than the under-voltage lockout threshold, VUVLO. This feature prevents draining the battery during the absence of VIN. When VIN < VBAT+VSLP, the bq2425x turns off the PWM converter, turns on the battery FET, sends a single 256µs pulse is sent on the STAT and INT outputs and the FAULT/STAT bits of the status registers are updated in the I^2C. Once VIN > VBAT+VSLP with the hysteresis, the FAULT bits are cleared and the device initiates a new charge cycle.

Input Over-Voltage Protection

The bq2425x provides over-voltage protection on the input that protects downstream circuitry. The built-in input over-voltage protection to protect the device and other components against damage from overvoltage on the input supply (Voltage from VIN to PGND). When VIN > VOVP, the bq2425x turns off the PWM converter, turns the battery FET, sends a single 256µs pulse is sent on the STAT and INT outputs and the FAULT/STAT bits of the status registers and the battery/supply status registers are updated in the I^2C. Once the OVP fault is removed, the FAULT bits are cleared and the device returns to normal operation. The OVP threshold for the bq24250 is programmable from 6.5V to 10.5V using VOVP bits in register #7.

NTC Monitor

The bq24250/1/3 includes the integration of an NTC monitor pin that complies with the JEITA specification (PSE also available upon request). The voltage based NTC monitor allows for the use of any NTC resistor with the use of the circuit shown in Figure 27.

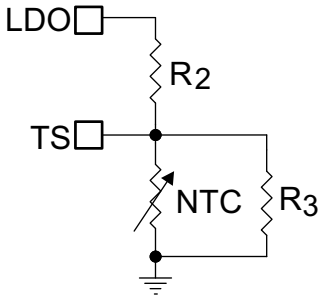


Figure 27. Voltage Based NTC circuit

The use of R3 is only necessary when the NTC does not have a beta near 3500K. When deviating from this beta, error will be introduced in the actual temperature trip thresholds. The trip thresholds are summarized below which are typical values provided in the specification table.

Table 4. Ratiometric TS Trip Thresholds for JEITA Compliant Charging

V_{HOT}	30.0%
V_{WARM}	38.3%
V_{COOL}	56.5%
V_{COLD}	60%

When sizing for R2 and R3, it is best to solve two simultaneous equations that ensure the temperature profile of the NTC network will cross the V_{HOT} and V_{COLD} thresholds. The accuracy of the V_{WARM} and V_{COOL} thresholds will depend on the beta of the chosen NTC resistor. The two simultaneous equations are shown below:

$$\%V_{COLD} = \frac{\left(\frac{R_3 R_{NTC}|_{TCOLD}}{R_3 + R_{NTC}|_{TCOLD}}\right)}{\left(\frac{R_3 R_{NTC}|_{TCOLD}}{R_3 + R_{NTC}|_{TCOLD}}\right) + R2} \times 100$$

$$\%V_{HOT} = \frac{\left(\frac{R_3 R_{NTC}|_{THOT}}{R_3 + R_{NTC}|_{THOT}}\right)}{\left(\frac{R_3 R_{NTC}|_{THOT}}{R_3 + R_{NTC}|_{THOT}}\right) + R2} \times 100 \quad (4)$$

Where the NTC resistance at the V_{HOT} and V_{COLD} temperatures must be resolved as follows:

$$R_{NTC}|_{TCOLD} = R_o e^{\beta\left(1/T_{COLD} - 1/T_o\right)}$$

$$R_{NTC}|_{THOT} = R_o e^{\beta\left(1/T_{HOT} - 1/T_o\right)} \quad (5)$$

To be JEITA compliant, T_{COLD} must be 0°C and T_{HOT} must be 60°C. If an NTC resistor is chosen such that the beta is 4000K and the nominal resistance is 10kΩ, the following R2 and R3 values result from the above equations:

R_2 = 5 kΩ
R_3 = 9.82 kΩ

Figure 28 illustrates the temperature profile of the NTC network with R2 and R3 set to the above values.

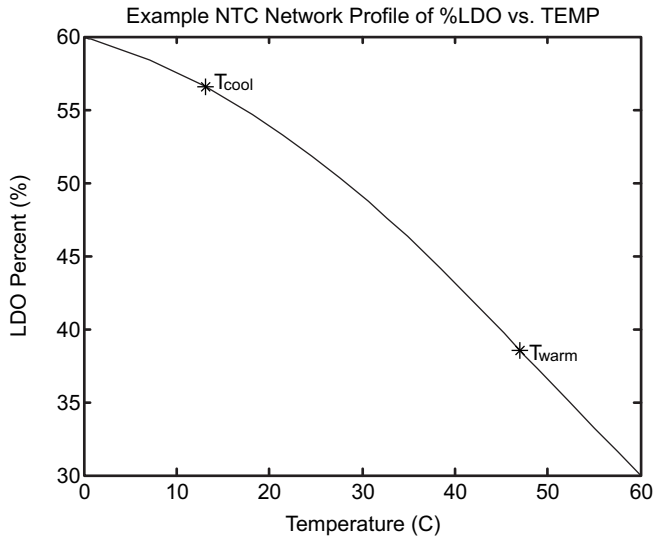


Figure 28. Voltage Based NTC Circuit Temperature Profile

For JEITA compliance, the T_{COOL} and T_{WARM} levels are to be 10°C and 45°C respectively. However, there is some error due to the variation in beta from 3500K. As shown above, the actual temperature points at which the NTC network crosses the V_{COOL} and V_{WARM} are 13°C and 47°C respectively. This error is small but should be considered when choosing the final NTC resistor.

Once the resistors are configured, the internal JEITA algorithm will apply the below profile at each trip point for battery voltage regulation and charge current regulation.

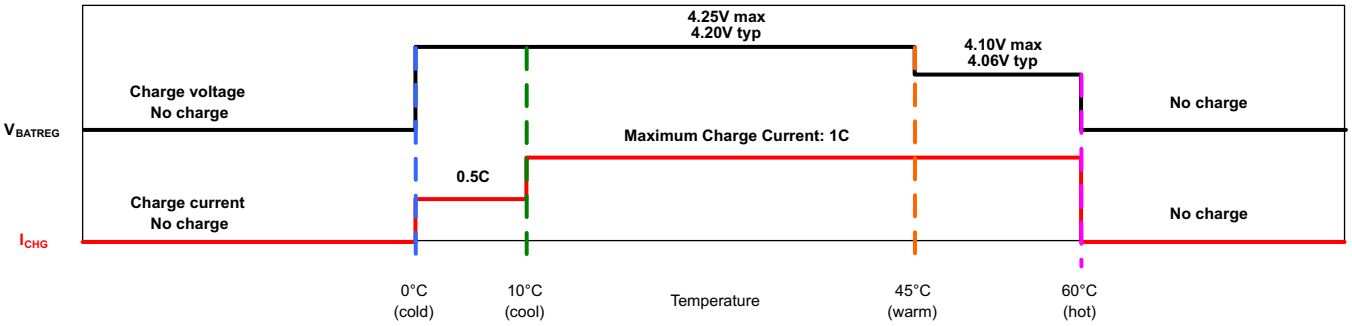


Figure 29. JEITA Profile for Voltage and Current Regulation Loops

Dynamic Power Path Management

The bq24250/1/3 features a SYS output that powers the external system load connected to the battery. This output is active whenever a valid source is connected to IN or BAT. The following discusses the behavior of SYS with a source connected to the supply or a battery source only.

When a valid input source is connected to the input and the charge is enabled, the charge cycle is initiated. In case of VBAT > ~3.5V, the SYS output is connected to VBAT. If the SYS voltage falls to VMINSYS, it is regulated to the VSYSREG threshold to maintain the system output even with a deeply discharged or absent battery. In this mode, the SYS output voltage is regulated by the buck converter and the battery FET is linearly regulated to regulate the charge current into the battery. The current from the supply is shared between charging the battery and powering the system load at SYS.

The dynamic power path management (DPPM) circuitry of the bq24250/1/3 monitors the current limits continuously and if the SYS voltage falls to the VMINSYS voltage, it adjusts charge current to maintain the minimum system voltage and supply the load on SYS. If the charge current is reduced to zero and the load increases further, the bq24250/1/3 enters battery supplement mode. During supplement mode, the battery FET is turned on and the battery supplements the system load.

If the battery is ever 5% above the regulation threshold, the battery OVP circuit shuts the PWM converter off and the battery FET is turned on to discharge the battery to safe operating levels. Battery OVP FAULT is shown in the I2C FAULT registers.

When no input source is available at the input and the battery is connected, the battery FET is turned on similar to supplement mode. The battery must be above VBATUVLO threshold to turn on the SYS output. In this mode, the current is not regulated; however, there is a short circuit current limit. If the short circuit limit is reached, the battery FET is turned off for the deglitch time. After the deglitch time, the battery FET is turned on to test and see if the short has been removed. If it has not, the FET turns off and the process repeats until the short is removed. This process is to protect the internal FET from over current.

Production Test Mode

To aid in end mobile device product manufacturing, the bq2425x includes a Production Test Mode (PTM), where the device is essentially a DC-DC buck converter. In this mode the input current limit to the charger is disabled and the output current limit is limited only by the inductor cycle-by-cycle current (e.g. 3.5A). The PTM mode can be used to test systems with high transient loads such as GSM transmission without the need of a battery being present.

As a means of safety, the Anyboot algorithm will determine if a battery is not present at the output prior to enabling the PTM mode. If a battery is present and the software attempts to enter PTM mode, the device will not enable PTM mode.

Safety Timer

At the beginning of charging process, the bq24250/1/3 starts the safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, the IC enters suspend mode where charging is disabled. The safety timer time is selectable using the I^2C interface. A single 256µs pulse is sent on the STAT and INT outputs and the FAULT/ bits of the status registers are updated in the I^2C. This function prevents continuous charging of a defective battery if the host fails to reset the safety timer. The safety timer runs at 2x the normal rate under the following conditions: Pre-charge or linear mode (minimum system voltage mode), during thermal regulation where the charge current is reduced, during TS fault where the charge current reduced due to temperature rise on the battery, input current limit. The safety timer is suspended during OVP, TS fault where charge is disabled, thermal shut down, and sleep mode.

Watchdog Timer

In addition to the safety timer, the bq24250/1 contains a 50-second watchdog timer that monitors the host through the I2C interface. Once a write is performed on the I2C interface, a watchdog timer is reset and started. The watchdog timer can be disabled by writing “0” on WD_EN bit of register #1. Writing “1” on that bit enables it and reset the timer.

If the watchdog timer expires, the IC enters DEFAULT mode where the default charge parameters are loaded and charging continues. The I2C may be accessed again to re-initialize the desired values and restart the watchdog timer as long as the safety timer has not expired. Once the safety timer expires, charging is disabled.

Thermal Regulation and Thermal Shutdown

During the charging process, to prevent overheat of the chip, bq24250/1/3 monitors the junction temperature, T_J, of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, TREG. The charge current is reduced when the junction temperature increases above TREG. Once the charge current is reduced, the system current is reduced while the battery supplements the load to supply the system. This may cause a thermal shutdown of the IC if the die temperature rises too. At any state, if T_J exceeds TSHTDWN, bq2425x suspends charging and disables the buck converter. During thermal shutdown mode, PWM is turned off, all safety timers are suspended, and a single 256µs pulse is sent on the STAT and INT outputs and the FAULT/STAT bits of the status registers are updated in the I2C. A new charging cycle begins when T_J falls below TSHTDWN by approximately 10°C.

Fault Modes

The bq2425x family includes several hardware fault detections. This allows for specific conditions that could cause a safety concern to be detected. With this feature, the host can be alleviated from monitoring unsafe charging conditions and also allows for a “fail-safe” if the host is not present. The table below summarizes the faults that are detected and the resulting behavior.

FAULT CONDITION	CHARGER BEHAVIOR	SAFETY TIMER BEHAVIOR
Input OVP	VSYS and ICHG Disabled	Suspended
Input UVLO	VSYS and ICHG Disabled	Reset
Sleep (VIN < VBAT)	VSYS and ICHG Disabled	Suspended
TS Fault (Batter Over Temp)	VSYS Active and ICHG Disabled	Suspended
Thermal Shutdown	VSYS and ICHG Disabled	Suspended
Timer Fault	VSYS Active and ICHG Disabled	Reset
No Battery	VSYS Active and ICHG Disabled	Suspended
ISET Short	VSYS Active and ICHG Disabled	Suspended
Input Good	VSYS and ICHG Disabled	Suspended

Register Mapping and Description

Register #1

Memory location: 00, Reset state: x0xx xxxx

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	WD_FAULT	Read only	Read:0 – No fault 1 – WD timeout if WD enabled
B6	WD_EN	Read/Write	0 – Disable 1 – Enable (also resets WC timer)
B5	STAT_1	Read only	00 – Ready 01 – Charge in progress 10 – Charge done 11 – Fault
B4	STAT_0	Read only	
B3	FAULT_3	Read only	0000 – Normal 0001 – Input OVP 0010 – Input UVLO 0011 – Sleep 0100 – Battery Temperature (TS) Fault 0101 – Battery OVP 0110 – Thermal Shutdown 0111 – Timer Fault 1000 – No Battery connected 1001 – ISET short 1010 – Input Fault and LDO low
B2	FAULT_2	Read only	
B1	FAULT_1	Read only	
B0(LSB)	FAULT_0	Read only	

- **WD_FAULT –** '0' indicates no watch dog fault has occurred, where a '1' indicates a fault has previously occurred.
- **WD_EN –** Enables or disables the internal watch dog timer. A '1' enables the watch dog timer and a '0' disables it.
- **STAT –** Indicates the charge controller status.
- **FAULT –** Indicates the faults that have occurred. If multiple faults occurred, they can be read by sequentially addressing this register (e.g. reading the register 2 or more times). Once all faults have been read and the device is in a non-fault state, the fault register will show "Normal". Regarding the "Input Fault & LDO Low" the IC indicates this if LDO is low and at the same time the input is below UVLO or coming out of UVLO with LDO still low.

Register #2

Memory location: 01, Reset state: 1010 1100

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	Reset	Write only	Write: 1 – Reset all registers to default values 0 – No effect
B6	$I_{IN\_ILIMIT\_2}$	Read/Write	000 – USB2.0 host with 100mA current limit 001 – USB3.0 host with 150mA current limit 010 – USB2.0 host with 500mA current limit 011 – USB3.0 host with 900mA current limit 100 – Charger with 1500mA current limit 101 – Charger with 2000mA current limit 110 – External ILIM current limit(5) 111- No input current limit with internal clamp at 3A (PTM MODE)
B5	$I_{IN\_ILIMIT\_1}$	Read/Write	
B4	$I_{IN\_ILIMIT\_0}$	Read/Write	
B3	EN_STAT	Read/Write	0 – Disable STAT function 1 – Enable STAT function
B2	EN_TERM	Read/Write	0 – Disable charge termination 1 – Enable charge termination
B1	$\overline{CE}$	Read/Write	0 – Charging is enabled 1 – Charging is disabled
B0 (LSB)	HZ_MODE	Read/Write	0 – Not high impedance mode 1 – High impedance mode

- **I_{IN_LIMIT} –** Sets the input current limit level. When in host mode this register sets the regulation level. However, when in standalone mode (e.g. no I^2C writes have occurred after power up or the WD timer has expired) the external resistor setting for I_{ILIM} sets the regulation level.
- **EN_STAT –** Enables and disables the STAT pin. When set to a '1' the STAT pin is enabled and function normally. When set to a '0' the STAT pin is disabled and the open drain FET is in HiZ mode.
- **EN_TERM –** Enables and disables the termination function in the charge controller. When set to a '1' the termination function will be enabled. When set to a '0' the termination function will be disabled. When termination is disabled, there are no indications of the charger terminating (i.e. STAT pin or STAT registers).
- **$\overline{CE}$ –** The charge enable bit which enables or disables the charge function. When set to a '0', the charger operates normally. When set to a '1', the charger is disables by turning off the BAT FET between SYS and BAT. The SYS pin continues to stay active via the switch mode controller if an input is present.
- **HZ_MODE –** Sets the charger IC into low power standby mode. When set to a '1', the switch mode controller is disabled but the BAT FET remains ON to keep the system powered. When set to a '0', the charger operates normally.

Register #3

Memory location: 02, Reset state: 1000 1111

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	VBATREG_5(1)	Read/Write	Battery Regulation Voltage: 640mV (default 1)
B6	VBATREG_4(1)	Read/Write	Battery Regulation Voltage: 320mV (default 0)
B5	VBATREG_3(1)	Read/Write	Battery Regulation Voltage: 160mV (default 0)
B4	VBATREG_2(1)	Read/Write	Battery Regulation Voltage: 80mV (default 0)
B3	VBATREG_1(1)	Read/Write	Battery Regulation Voltage: 40mV (default 1)
B2	VBATREG_0(1)	Read/Write	Battery Regulation Voltage: 20mV (default 1)
B1(4)(5)	USB_DET_1/EN1	Read Only	Return USB detection result or pin EN1/EN0 status – 00 – DCP detected / EN1=0, EN0=0 01 – CDP detected / EN1=0, EN0=1 10 – SDP detected / EN1=1, EN0=0 11 – Apple/TT or non-standard adaptor detected / EN1=1, EN0=1
B0(LSB)	USB_DET_0/EN0	Read Only	

(1) Charge voltage range is 3.5V—4.44V with the offset of 3.5V and step of 20mV (default 4.2V)

- **V_{BATREG} –** Sets the battery regulation voltage
- **USB_DET/EN –** Provides status of the D+/D– detection results for spins that include the D+/D– pins or the state of EN1/EN2 for spins that include the EN1/EN2 pins

Register #4

Memory location: 03, Reset state: 0000 0000

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	ICHG_4(1)(2)	Read/Write	Charge current 800mA – (default 0)
B6	ICHG_3(1)(2)	Read/Write	Charge current: 400mA – (default 0)
B5	ICHG_2(1)(2)	Read/Write	Charge current: 200mA – (default 0)
B4	ICHG_1(1)(2)	Read/Write	Charge current: 100mA – (default 0)
B3	ICHG_0(1)(2)	Read/Write	Charge current: 50mA – (default 0)
B2	ITERM_2(3)	Read/Write	Termination current sense threshold: 100mA (default 0)
B1	ITERM_1(3)	Read/Write	Termination current sense threshold: 50mA (default 0)
B0(LSB)	ITERM_0(3)	Read/Write	Termination current sense threshold: 25mA (default 0)

(1) Charge current offset is 500 mA and default charge current is 500mA (maximum is 2.0A)
(2) When all bits are 1's, it is external ISET charging mode
(3) Termination threshold voltage offset is 50mA. The default termination current is 50mA if the charge is selected from I2C. Otherwise, termination is set to 10% of ICHG in external I_set mode with +/-10% accuracy.

- **I_{CHG} –** Sets the charge current regulation
- **I_{TERM} –** Sets the current level at which the charger will terminate

Register #5

Memory location: 04, Reset state: xx00 x010

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	LOOP_STATUS1(1)	Read Only	00 – No loop is active that slows down timer 01 – V_{IN_DPM} regulation loop is active 10 – Input current limit loop is active 11 – Thermal regulation loop is active
B6	LOOP_STATUS0(1)	Read Only	
B5	LOW_CHG	Read/Write	0 – Normal charge current set by 03h 1 – Low charge current setting 330mA (default 0)
B4	DPDM_EN	Read/Write	0 – Bit returns to 0 after D+/D– detection is performed 1 – Force D+/D– detection (default 0)
B3	CE_STATUS	Read Only	0 – CE low 1 – CE high
B2	V_{INDPM_2}(2)	Read/Write	Input $V_{IN\text{-}DPM}$ voltage: 320mV (default 0)
B1	V_{INDPM_1}(2)	Read/Write	Input $V_{IN\text{-}DPM}$ voltage: 160mV (default 1)
B0(LSB)	V_{INDPM_0}(2)	Read/Write	Input $V_{IN\text{-}DPM}$ voltage: 80mV (default 0)

(1) LOOP_STATUS bits show if there are any loop is active that slow down the safety timer. If a status occurs, these bits announce the status and do not clear until read. If more than one occurs, the first one is shown.
(2) VIN-DPM voltage offset is 4.20V and default V_{IN_DPM} threshold is 4.36V.

- **LOOP_STATUS –** Provides the status of the active regulation loop. The charge controller allows for only one loop can regulate at a time.
- **LOW_CHG –** When set to a '1', the charge current is reduced 330mA independent of the charge current setting in register 0x03. When set to '0', the charge current is set by register 0x03.
- **DPDM_EN –** Forces a D+/D- detection routine to be executed once a '1' is written. This is independent of the input being supplied.
- **$\overline{CE}$_STATUS –** Provides the status of the $\overline{CE}$ pin level. If the $\overline{CE}$ pin is forced high, this bit returns a '1'. If the $\overline{CE}$ pin is forced low, this bit returns a '0'.
- **V_{INDPM} –** Sets the input VDPM level.

Register #6

Memory location: 05, Reset state: 101x 1xxx

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	2XTMR_EN	Read/Write	0 – Timer not slowed at any time 1 – Timer slowed by 2x when in thermal regulation, V_{IN_DPM} or DPPM (default 1)
B6	TMR_1	Read/Write	Safety Timer Time Limit 00 – 0.75 hour fast charge 01 – 6 hour fast charge (default 01) 10 – 9 hour fast charge 11 – Disable safety timers
B5	TMR_2	Read/Write	
B4	SYSOFF	Read/Write	0 – SYSOFF disabled 1 – SYSOFF enabled
B3	TS_EN	Read/Write	0 – TS function disabled 1 – TS function enabled (default 1)
B2	TS_STAT2	Read only	TS Fault Mode: 000 – Normal, No TS fault 100 – TS temp < T_{COLD} (Charging suspended for JEITA and Standard TS) 101 – T_{FREEZE} < TS temp < T_{COLD} (Charging at 3.9V and 100mA and only for PSE option only) 110 – TS temp < T_{FREEZE} (Charging suspended for PSE option only) 111 – TS open (TS disabled)
B1	TS_STAT1	Read only	
B0(LSB)	TS_STAT0	Read only	

- **2xTMR_EN –** When set to a '1', the 2x Timer function is enabled and allows for the timer to be extended if a condition occurs where the charge current is reduced (i.e. V_{IN_DPM}, thermal regulation, etc.). When set to a '0', this function is disabled and the normal timer will always be executed independent of the current reduce conditions.
- **SYSOFF –** When set to a '1' and the input is removed, the internal battery FET is turned off in order to reduce the leakage from the BAT pin to less than 1µA. Note that this disconnects the battery from the system. When set to a '0', this function is disabled.
- **TS_EN –** Enables and disables the TS function. When set to a '1' the TS function is disabled otherwise it is enabled. Only applies to spins that have a TS pin.
- **TS_STAT –** Provides status of the TS pin state for spins that have a TS pin.

Register #7

Memory location: 06, Reset state: 1110 0000

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	VOVP_2	Read/Write	OVP voltage: 000 – 6.0V; 001 – 6.5V; 010 – 7.0V; 011 – 8.0V 100 – 9.0V; 101 – 9.5V; 110 – 10.0V; 111 –10.5V
B6	VOVP_1	Read/Write	
B5	VOVP_0	Read/Write	
B4	CLR_VDP	Read/Write	0 – Keep D+ voltage source on during DBP charging 1 – Turn off D+ voltage source to release D+ line
B3	FORCE_BAT DET	Read/Write	0 – Enter the battery detection routine only if TERM is true or EN_PTM is true 1 – Enter the battery detection routine
B2	FORCE_PTM	Read/Write	0 – PTM mode is disabled 1 – PTM mode is enabled if OTP_EN_PTM=1
B1	N/A	Read/Write	Not available. Keep set to 0.
B0(LSB)	N/A	Read/Write	Not available. Keep set to 0.

- **VOVP –** Sets the OVP level
- **CLR_VDP –** When the D+/D– detection has finished, some cases require the D+ pin to force a voltage of 0.6V. This bit allows the system to clear the voltage prior to any communication on the D+/D– pins. A '1' clears the voltage at the D+ pin if present.
- **FORCE_BATDET –** Forces battery detection and provides status of the battery presence. A logic '1' enables this function.
- **FORCE_PTM –** Puts the device in production test mode (PTM) where the input current limit is disabled. Note that a battery must not be present prior to using this function. Otherwise the function will not be allowed to execute. A logic '1' enables the PTM function.

APPLICATION INFORMATION

Inductor Selection

The inductor selection depends on the application requirements. The bq2425x is designed to operate at around 1 µH. The value will have an effect on efficiency, and the ripple requirements, stability of the charger, package size, and DCR of the inductor. The 1µH inductor provides a good tradeoff between size and efficiency and ripple.

Once the inductance has been selected, the peak current is needed in order to choose the saturation current rating of the inductor. Make sure that the saturation current is always greater than or equal to the calculated IPEAK. The following equation can be used to calculate the current ripple:

$$\Delta I_L = \{VBAT\ (VIN - VBAT)\}/(VIN \times fs \times L) \quad (6)$$

Then use current ripple to calculate the peak current as follows:

$$I_{PEAK} = I_{CHARGE} \times (1 + \Delta I_L/2) \quad (7)$$

In this design example, the regulation voltage is set to 4.2V, the input voltage is 5V and the inductance is selected to be 1µH. The maximum charge current that can be used in this application is 1A and can be set by I2C command. The peak current is needed in order to choose the saturation current rating of the inductor. Using equation 6 and 7, ΔI_L is calculated to be 0.224A and the inductor peak current is 1.112A. A 1µF BAT cap is needed and 22µF SYS cap is needed on the system trace.

The default settings for external fast charge current and external setting of current limit are chosen to be IFC=500mA and ILIM=1A. RISET and RILIM need to be calculated using equation 1 and 2 in the data sheet.

The fast charge current resistor (RISET) can be set as follows:

RISET=250/0.5A=500Ω

The input current limit resistor (RILIM) can be set as follows:

RILIM= 270/1A=270Ω

The external settings of VIN_DPM can be designed by calculating R1 and R2 according to equation 3 in this data sheet and the typical application circuit. VIN_DPM should be chosen first along with R1. VIN_DPM is chosen to be 4.6V and R1 is set to 274KΩ in this design example. Using equation 3, the value of R2 is calculated to be 100KΩ.

In this design example, the application needs to be JEITA compliant. Thus, T_{COLD} must be 0°C and T_{HOT} must be 60°C. If an NTC resistor is chosen such that the beta is 4500K and the nominal resistance is 13KΩ, the calculated R2 and R3 values are 5KΩ and 8.8KΩ respectively. These results are obtained from equation 4 and 5 in this data sheet.

Layout Guidelines

1. Place the BOOT, PMID, IN, BAT, and LDO capacitors as close as possible to the IC for optimal performance.
2. Connect the inductor as close as possible to the SW pin, and the SYS/CSIN cap as close as possible to the inductor minimizing noise in the path.
3. Place a 1-µF PMID capacitor as close as possible to the PMID and PGND pins, making the high frequency current loop area as small as possible.
4. The local bypass capacitor from SYS/CSIN to GND must be connected between the SYS/CSIN pin and PGND of the IC. This minimizes the current path loop area from the SW pin through the LC filter and back to the PGND pin.
5. Place all decoupling capacitors close to their respective IC pins and as close as possible to PGND (do not place components such that routing interrupts power-stage currents). All small control signals must be routed away from the high-current paths.
6. To reduce noise coupling, use a ground plane if possible, to isolate the noisy traces from spreading its noise all over the board. Put vias inside the PGND pads for the IC.
7. The high-current charge paths into IN, Micro-USB, BAT, SYS/CSIN, and from the SW pins must be sized appropriately for the maximum charge current to avoid voltage drops in these traces.
8. For high-current applications, the balls for the power paths must be connected to as much copper in the board as possible. This allows better thermal performance because the board conducts heat away from the IC.

Board Layout

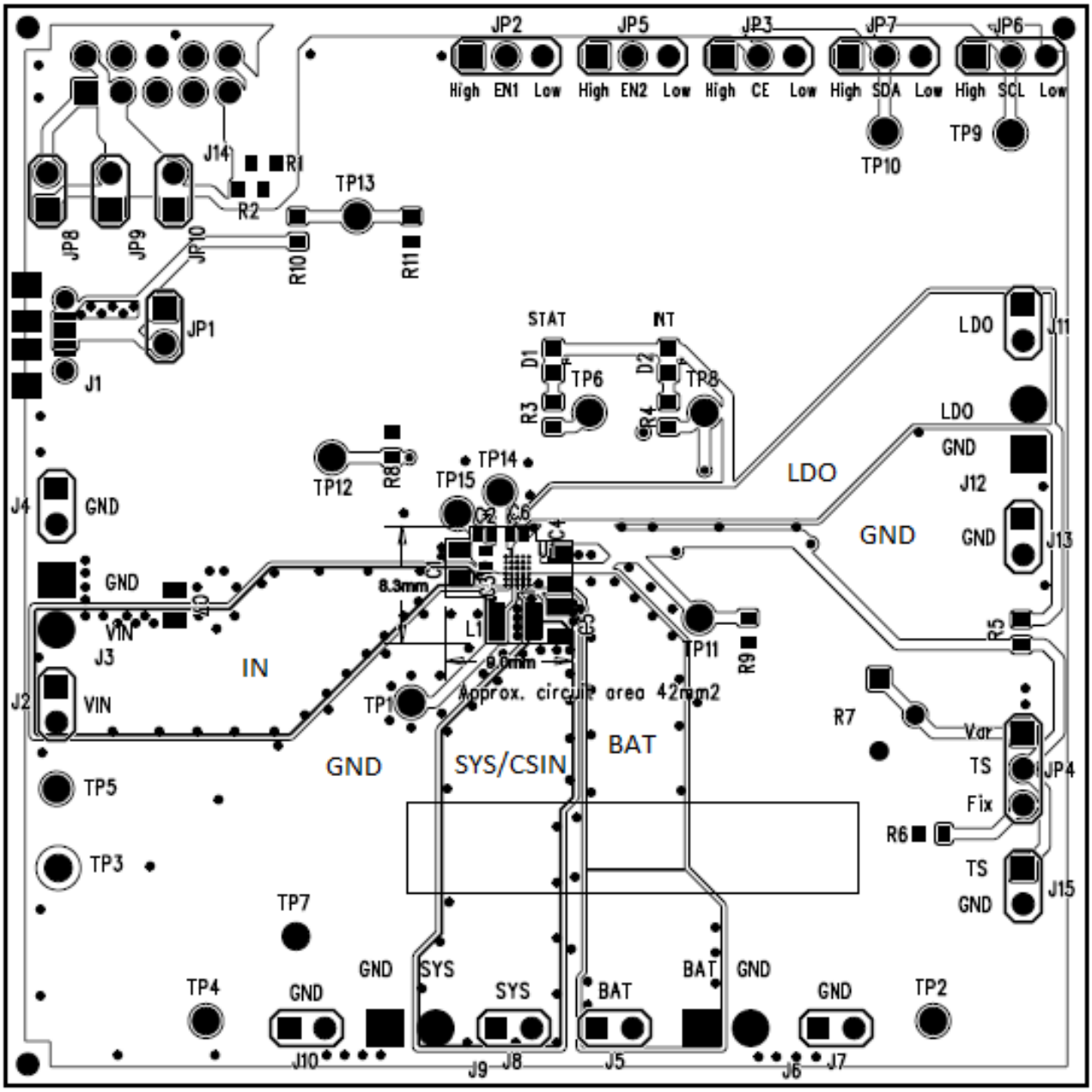
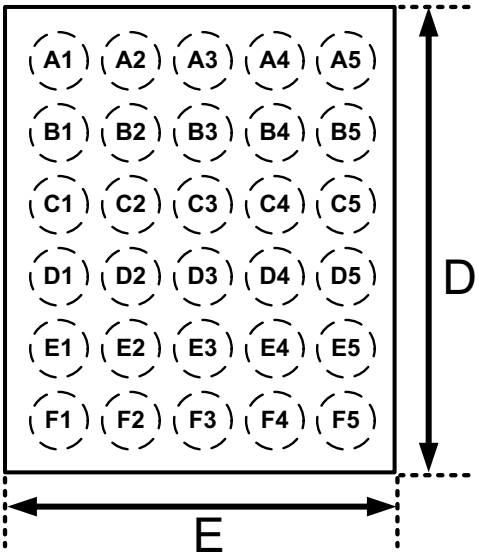


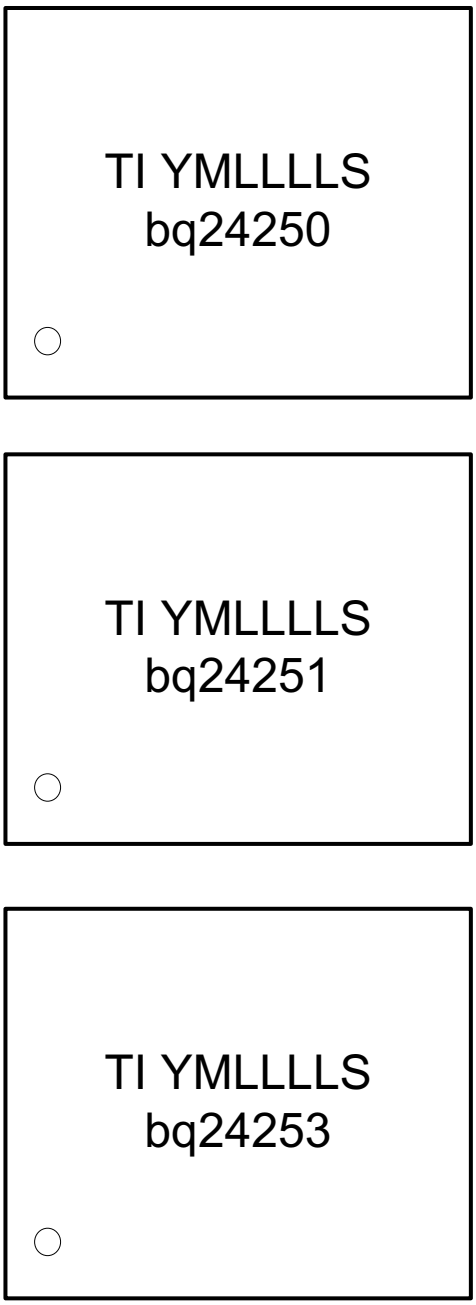
Figure 30. Recommended bq2425x PCB Layout for WCSP Package

PACKAGE SUMMARY

YFF Package
(Top View)



YFF Package Symbol
(Top Side Symbol for bq2425x)



0-Pin A1 Marker, TI-TI Letters, YM- Year Month Date Code, LLLL-Lot Trace Code, S-Assembly Site Code

The bq2425x devices are available in a 30-bump chip scale package (YFF, NanoFree™). The package dimensions are:

D – 2.427mm ±0.035mm

E – 2.027mm ±0.035mm

REVISION HISTORY

Changes from Original (October 2012) to Revision A **Page**

- Changed From: Product Brief To: Full data sheet 1
- Changed Block Diagram 10
- Added Typical Characteristics graphs 16
- Changed Equation (3) 23

Changes from Revision A (March 2013) to Revision B **Page**

- Added PREVIEW status to devices in the Ordering Information table, except the bq24250RGER and bq24250RGET 3

Changes from Revision B (May 2013) to Revision C **Page**

- Deleted PREVIEW status note from devices bq24250YFF, bq24251YFF, bq24251RGE, and bq24253RGE in the Ordering Information table 3

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)
BQ24250RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ24250RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ24250YFFR	ACTIVE	DSBGA	YFF	30	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85
BQ24250YFFT	ACTIVE	DSBGA	YFF	30	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85
BQ24251RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85
BQ24251RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85
BQ24251YFFR	ACTIVE	DSBGA	YFF	30	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85
BQ24251YFFT	ACTIVE	DSBGA	YFF	30	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85
BQ24253RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85
BQ24253RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85
BQ24253YFFR	PREVIEW	DSBGA	YFF	30	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85
BQ24253YFFT	PREVIEW	DSBGA	YFF	30	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/produc
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in speci
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-ba the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or S in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is of the previous line and the two combined represent the entire Device Marking for that device.

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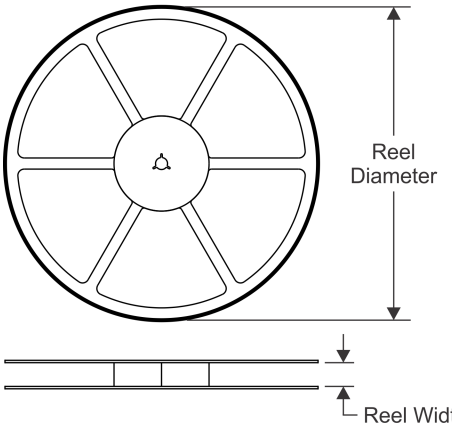
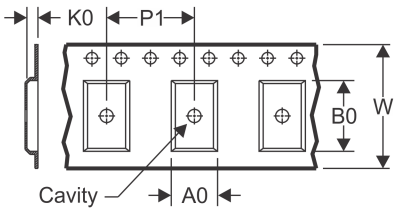
TAPE AND REEL INFORMATION

REEL DIMENSIONS

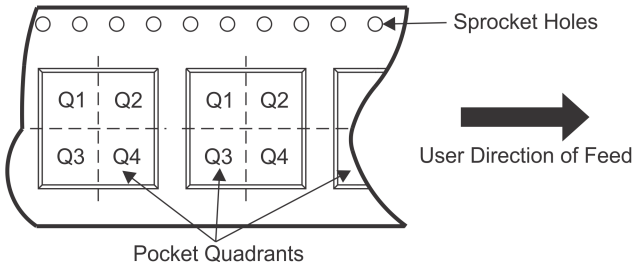


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

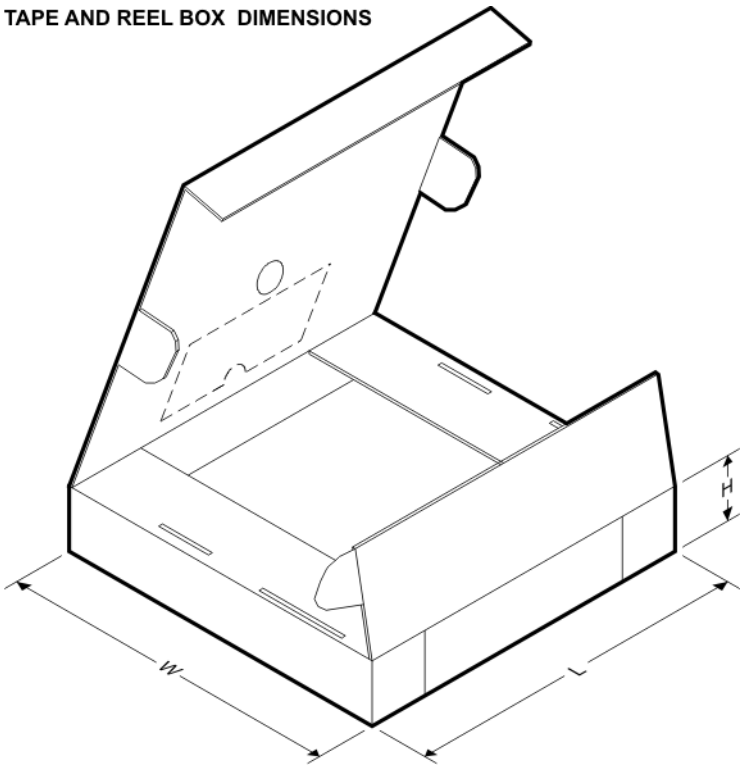
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24250RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24250RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24250YFFR	DSBGA	YFF	30	3000	180.0	8.4	2.09	2.59	0.78	4.0	8.0	Q1
BQ24250YFFT	DSBGA	YFF	30	250	180.0	8.4	2.09	2.59	0.78	4.0	8.0	Q1
BQ24251RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24251RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24251YFFR	DSBGA	YFF	30	3000	180.0	8.4	2.09	2.59	0.78	4.0	8.0	Q1
BQ24251YFFT	DSBGA	YFF	30	250	180.0	8.4	2.09	2.59	0.78	4.0	8.0	Q1
BQ24253RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24253RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

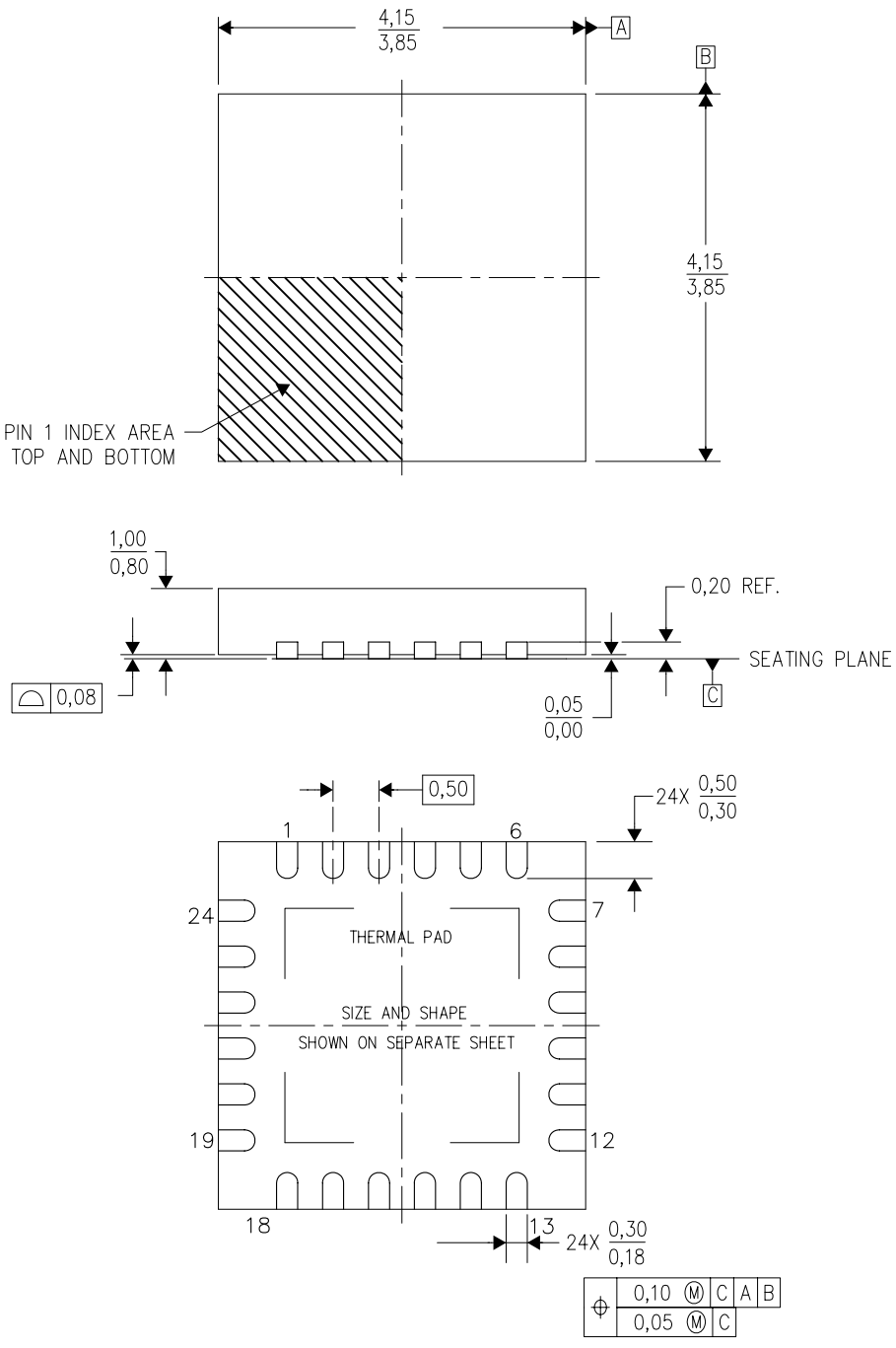
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24250RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24250RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24250YFFR	DSBGA	YFF	30	3000	210.0	185.0	35.0
BQ24250YFFT	DSBGA	YFF	30	250	210.0	185.0	35.0
BQ24251RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24251RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24251YFFR	DSBGA	YFF	30	3000	210.0	185.0	35.0
BQ24251YFFT	DSBGA	YFF	30	250	210.0	185.0	35.0
BQ24253RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24253RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

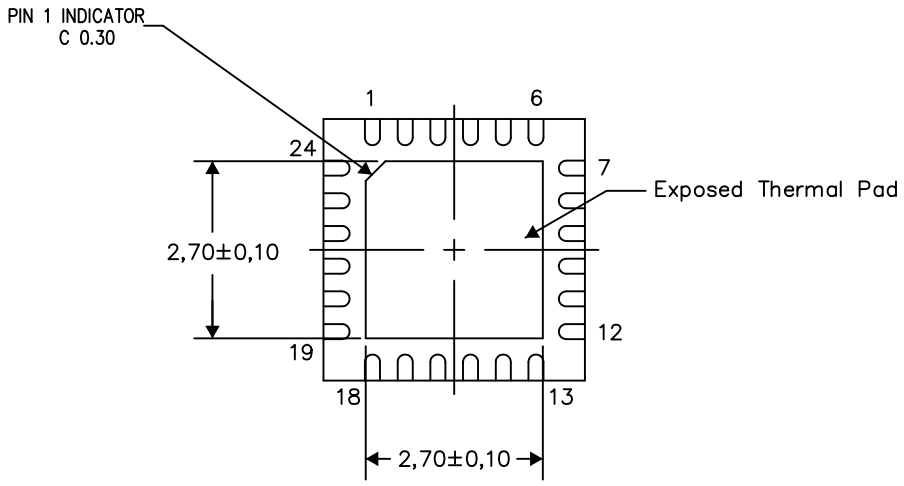
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



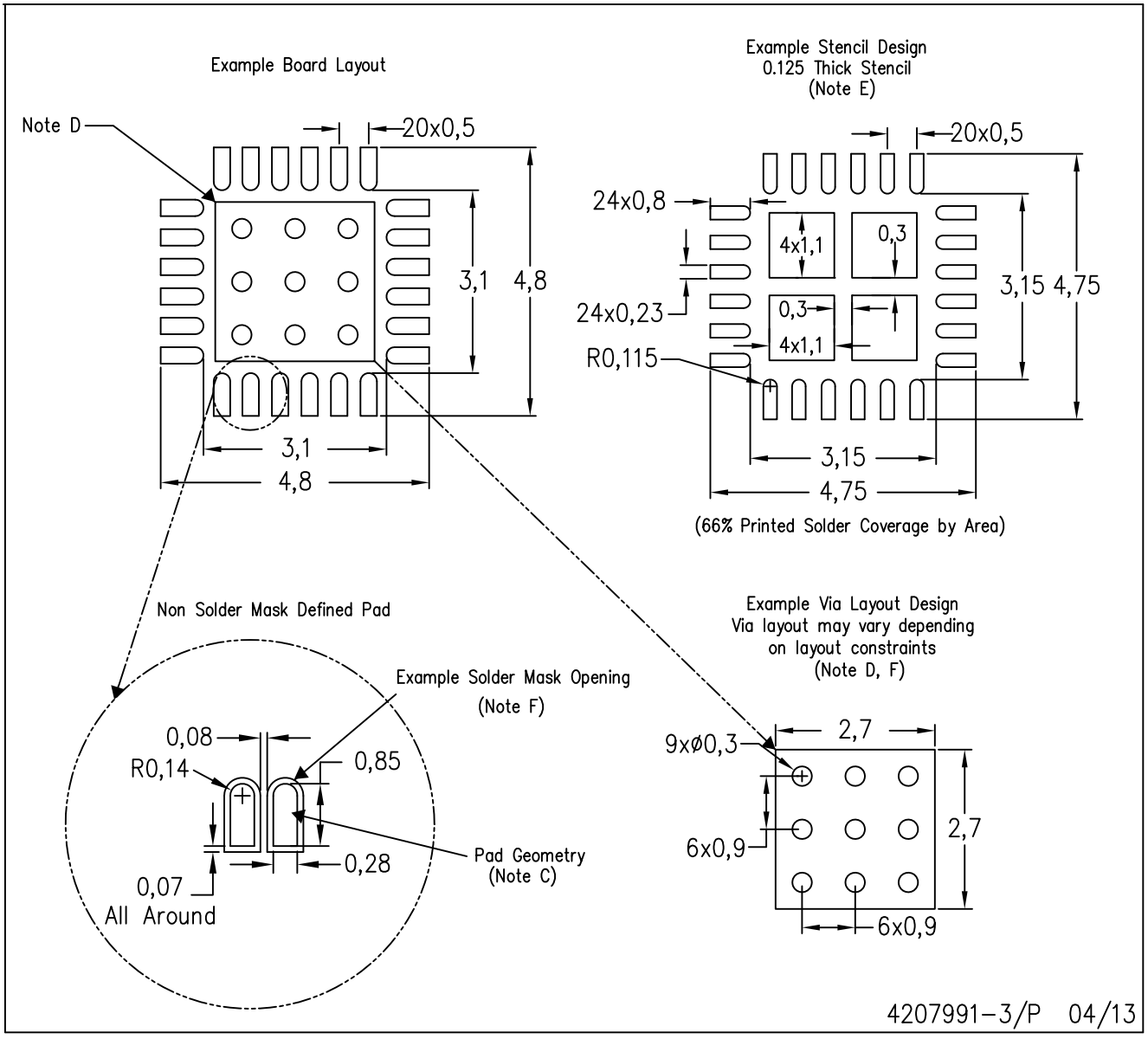
Bottom View

Exposed Thermal Pad Dimensions

4206344–4/AD 04/13

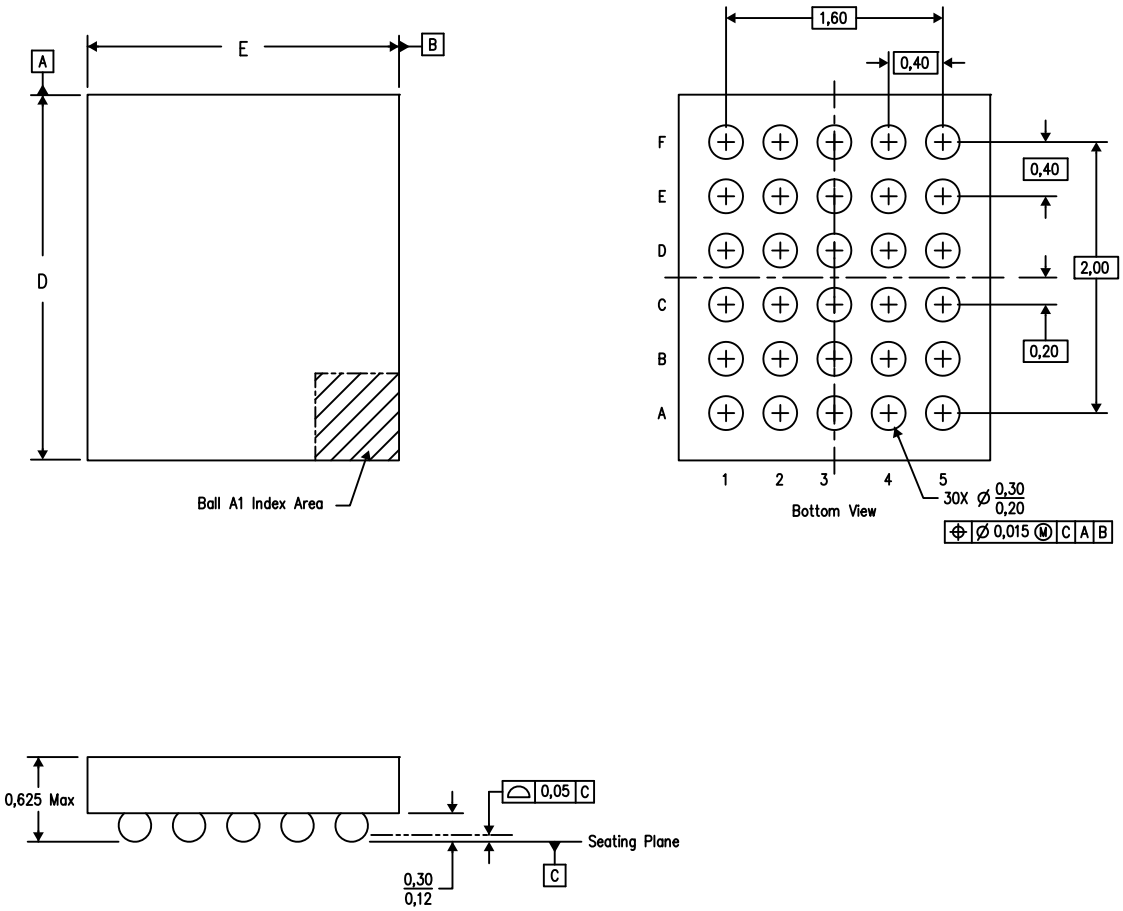
NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

YFF (R–XBGA–N30) DIE–SIZE BALL GRID ARRAY



4207625–13/AM 06/13

NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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