High Performance Narrowband ISM Transceiver IC

Preliminary Technical Data

ADF7021

FEATURES

- Low power, low IF transceiver
- Frequency bands
  - 80 MHz to 650 MHz
  - 862 MHz to 940 MHz
- Modulation schemes
  - 2FSK, 3FSK, 4FSK
- Spectral shaping
  - Gaussian and raised-cosine filtering
- Data rates supported
  - 0.05 kbps to 25 kbps
- 2.3 V to 3.6 V power supply
- Programmable output power
  - −16 dBm to +13 dBm in 63 steps
- Automatic PA ramp control
- Receiver sensitivity
  - −125 dBm at 1 kbps, 2 FSK
- On-chip VCO and fractional-N PLL
- On-chip 7-bit ADC and temperature sensor
- Fully automatic frequency control loop (AFC)
- Digital RSSI
- Integrated Tx/Rx switch
- Leakage current <1 µA in power-down mode

APPLICATIONS

- Narrow-band standards
  - ETSI EN 300-220, FCC Part 90, FCC Part 15, FCC Part 95, ARIB STD-T67
- Low cost, wireless data transfer
- Remote control/security systems
- Wireless metering
- Private mobile radio
- Wireless medical telemetry service (WMTS)
- Keyless entry
- Home automation
- Process and building control
- Pagers

FUNCTIONAL BLOCK DIAGRAM

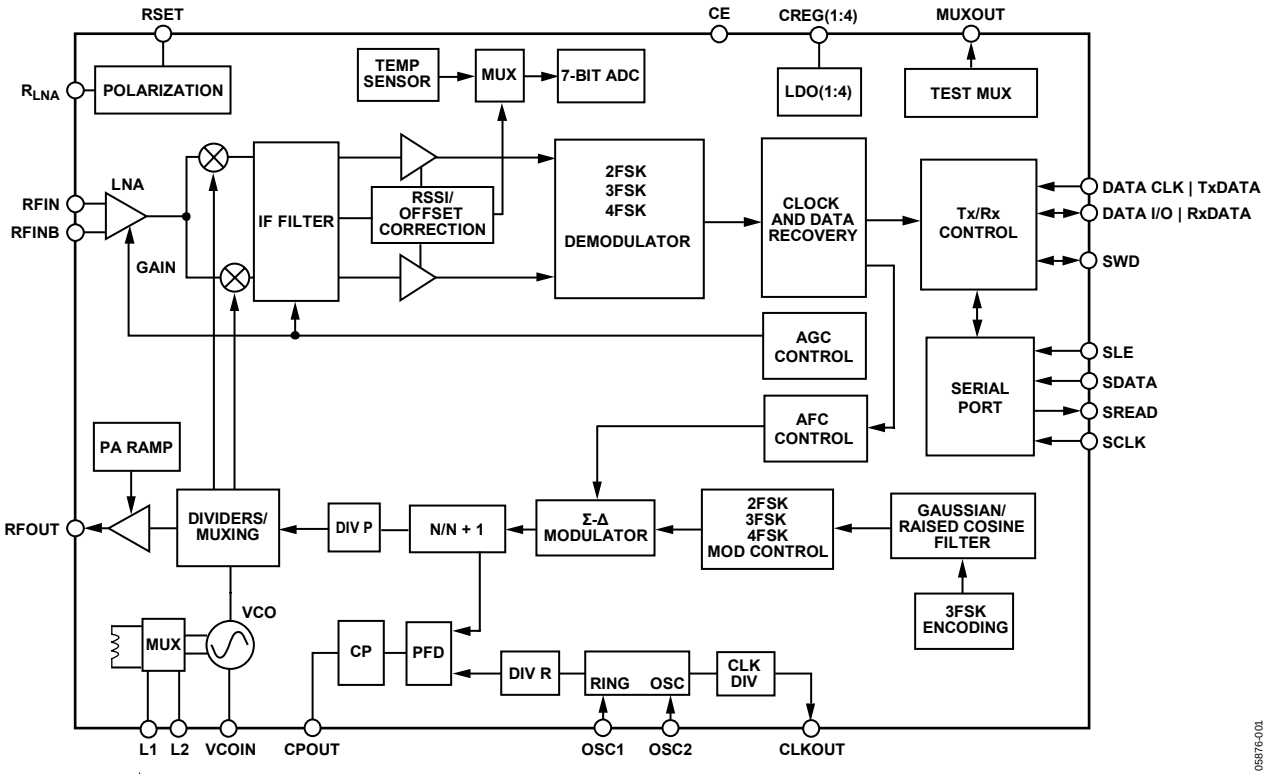

Figure 1.

Rev. PrI

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GENERAL DESCRIPTION

The ADF7021 is a low power, highly integrated 2FSK/3FSK/4FSK transceiver. It is designed to operate in the narrow-band, license-free ISM bands and licensed bands in the 80 MHz to 650 MHz and 862 MHz to 940 MHz frequency ranges. It has both Gaussian and raised cosine data filtering options to improve spectral efficiency for narrow-band applications. It is suitable for circuit applications targeted at European ETSI-EN 300-220, the Japanese ARIB STD-T67, the Chinese Short Range Device regulations, and the North American FCC Part 15, Part 90, and Part 95 regulatory standards. A complete transceiver can be built using a small number of external discrete components, making the ADF7021 very suitable for price-sensitive and area-sensitive applications.

The transmit section contains a voltage controlled oscillator (VCO) and a low noise fractional-N PLL with output resolution of <1 ppm. This frequency-agile PLL allows the ADF7021 to be used in frequency hopping spread spectrum (FHSS) systems. The VCO operates at twice the fundamental frequency to reduce spurious emissions and frequency pulling problems.

The transmitter output power is programmable in 63 steps from −16 dBm to +13 dBm and has an automatic power ramp control to prevent spectral splatter and help meet regulatory standards. The transceiver RF frequency, channel spacing, and modulation are programmable using a simple 3-wire interface. The device operates with a power supply range of 2.3 V to 3.6 V and can be powered down when not in use.

A low IF architecture is used in the receiver (100 kHz), minimizing power consumption and the external component count while avoiding interference problems at low frequencies. The IF filter has programmable bandwidths of 12.5 kHz, 18.75 kHz, and 25 kHz. The ADF7021 supports a wide variety of programmable features including Rx linearity, sensitivity, and IF bandwidth, allowing the user to trade off receiver sensitivity and selectivity against current consumption, depending on the application. The receiver also features a patent-pending automatic frequency control (AFC) loop with programmable pull-in range, allowing the PLL to track out the frequency error in the incoming signal.

An on-chip ADC provides readback of an integrated temperature sensor, an external analog input, the battery voltage, and the RSSI signal, which provides savings on an ADC in some applications. The temperature sensor is accurate to ±10°C over the full operating temperature range of −40°C to +85°C. This accuracy can be improved by doing a 1-point calibration at room temperature and storing the result in memory.

SPECIFICATIONS

V_{DD} = 2.3 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C.
All measurements are performed with the EVAL-ADF7021DBx using PN9 data sequence, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
RF CHARACTERISTICS					
Frequency Ranges (Direct Output)	135		650	MHz	External VCO inductor
Frequency Ranges (Divide-by-2 Mode)	80		325	MHz	External VCO inductor, divide-by-2 enabled
Frequency Ranges (Direct Output)	862		940	MHz	Internal VCO inductor
Frequency Ranges (Divide-by-2 Mode)	431		470	MHz	Internal VCO inductor, divide-by-2 enabled
Phase Frequency Detector (PFD) Frequency	RF/256		TBD	MHz	
TRANSMISSION PARAMETERS					
Data Rate	0.05		25	kbps	
Frequency Shift Keying					
Frequency Deviation[1]	56			Hz	Phase frequency detector (PFD) = 3.625 MHz
	306			Hz	PFD = 20 MHz
Deviation Frequency Resolution	56			Hz	PFD = 3.625 MHz
Gaussian Filter BT		0.5			
Raised Cosine Filter Alpha		0.5			
Transmit Power [2]	−20		+13	dBm	V_{DD} = 3.0 V, T_A = 25°C
Transmit Power Variation vs. Temperature		±1		dB	From −40°C to +85°C
Transmit Power Variation vs. V_{DD}		±1		dB	From 2.3 V to 3.6 V at 915 MHz, T_A = 25°C
Transmit Power Flatness		±1		dB	From 902 MHz to 928 MHz, 3 V, T_A = 25°C
Programmable Step Size					
−20 dBm to +13 dBm		0.3125		dB	
Spurious Emissions					
Integer Boundary		−55		dBc	50 kHz loop bandwidth (BW)
Reference		−65		dBc	
Harmonics					
Second Harmonic		−27		dBc	Unfiltered conductive
Third Harmonic		−21		dBc	Unfiltered conductive
All Other Harmonics		−35		dBc	Unfiltered conductive
Optimum PA Load Impedance[3]		39 + j61		Ω	F_{RF} = 915 MHz
		48 + j54		Ω	F_{RF} = 868 MHz
		54 + j94		Ω	F_{RF} = 433 MHz
RECEIVER PARAMETERS					
2FSK Input Sensitivity					Bit error rate (BER) = 10^{-3}, F_{RF} = 915 MHz, low noise amplifier (LNA) and power amplifier (PA) matched separately[4]
Sensitivity at 1 kbps		−125		dBm	F_{DEV} = 1 kHz, high sensitivity mode[5]
LNA and Mixer, Input IP3					
Enhanced Linearity Mode		6.8		dBm	Pin = −20 dBm, 2 CW interferers
Low Current Mode		−3.2		dBm	F_{RF} = 915 MHz, F1 = F_{RF} + 3 MHz
High Sensitivity Mode		−35		dBm	F2 = F_{RF} + 6 MHz, maximum gain
Rx Spurious Emissions[6]			−57	dBm	<1 GHz at antenna input
			−47	dBm	>1 GHz at antenna input
AFC					
Maximum Pull-In Range		±127.5		kHz	
Response Time		48		Bits	Mod index = 0.875
Accuracy		1		kHz	

Parameter	Min	Typ	Max	Unit	Test Conditions
CHANNEL FILTERING					
Adjacent Channel Rejection (Offset = ±1 × IF Filter BW Setting)		27		dB	IF filter BW setting = 12.5 kHz, 18.75 kHz, 25 kHz
Second Adjacent Channel Rejection (Offset = ±2 × IF Filter BW Setting)		50		dB	Desired signal 3 dB above the input sensitivity level, CW interferer power level
Third Adjacent Channel Rejection (Offset = ±3 × IF Filter BW Setting)		55		dB	Increased until BER = 10^{-3}, image channel excluded
Image Channel Rejection		35		dB	Image at F_{RF} − 200 kHz
Co-Channel Rejection		−3		dB	
Wideband Interference Rejection		70		dB	Swept from 100 MHz to 2 GHz, measured as channel rejection
BLOCKING					
±1 MHz		60		dB	Desired signal 3 dB above the input sensitivity level, CW interferer power level
±5 MHz		68		dB	Increased until BER = 10^{-2}
±10 MHz		65		dB	
±10 MHz (High Linearity Mode)		72		dB	
Saturation (Maximum Input Level)		12		dBm	FSK mode, BER = 10^{-3}
LNA Input Impedance		24 – j60		Ω	F_{RF} = 915 MHz, RFIN to GND
		26 – j63		Ω	F_{RF} = 868 MHz
		71 – j128		Ω	F_{RF} = 433 MHz
RECEIVE SIGNAL STRENGTH INDICATOR (RSSI)					
Range at Input		−110 to −36		dBm	
Linearity		±2		dB	
Absolute Accuracy		±3		dB	
Response Time		150		µs	See the RSSI/AGC section
PHASE-LOCKED LOOP (PLL)					
VCO Gain		65		MHz/V	902 MHz to 928 MHz band, VCO adjust = 0, VCO_BIAS_SETTING = 8
		130		MHz/V	860 MHz to 870 MHz band, VCO adjust = 0
		65		MHz/V	433 MHz, VCO adjust = 0
Phase Noise (In-Band)		−99		dBc/Hz	PA = 10 dBm, V_{DD} = 3.0 V, PFD = 24.57 MHz, F_{RF} = 433 MHz, VCO_BIAS_SETTING = 15
Phase Noise (Out-of-Band)		−113		dBc/Hz	1 MHz offset
Residual FM		128		Hz	From 200 Hz to 20 kHz, F_{RF} = 868 MHz
PLL Settling		40		µs	Measured for a 10 MHz frequency step to within 5 ppm accuracy, PFD = 20 MHz, loop bandwidth (LBW) = 50 kHz
REFERENCE INPUT					
Crystal Reference	3.625		TBD	MHz	
External Oscillator	3.625		TBD	MHz	
Load Capacitance		33		pF	PC board layout and crystal specific
Crystal Start-Up Time		2.1		ms	11.0592 MHz crystal, using 33 pF load capacitors
Input Level				CMOS levels	See the Reference Input section
ADC PARAMETERS					
INL		±1		LSB	From 2.3 V to 3.6 V, T_A = 25°C
DNL		±1		LSB	From 2.3 V to 3.6 V, T_A = 25°C
TIMING INFORMATION					
Chip Enabled to Regulator Ready		10		µs	C_{REG} = 100 nF
Chip Enabled to RSSI Ready		3.0		ms	See Table 14 for more details
Tx to Rx Turnaround Time		150 µs + (5 × T_{BIT})			Time to synchronized data out, includes AGC settling; see AGC Information and Timing section for more details

Parameter	Min	Typ	Max	Unit	Test Conditions
LOGIC INPUTS					
Input High Voltage, V_{INH}	$0.7 \times V_{DD}$			V	
Input Low Voltage, V_{INL}			$0.2 \times V_{DD}$	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
Control Clock Input			50	MHz	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	$DV_{DD} - 0.4$			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
CLK_{OUT} Rise/Fall			5	ns	
CLK_{OUT} Load			10	pF	
TEMPERATURE RANGE (T_A)	−40		+85	°C	
POWER SUPPLIES					
Voltage Supply					
V_{DD}	2.3		3.6	V	All V_{DD} pins must be tied together
Transmit Current Consumption					V_{DD} = 3.0 V, PA is matched into 50 Ω
0 dBm		12.7		mA	F_{RF} = 460 MHz
10 dBm		21		mA	F_{RF} = 460 MHz
0 dBm		19.3		mA	F_{RF} = 868 MHz
10 dBm		28		mA	F_{RF} = 868 MHz
Receive Current Consumption					
Low Current Mode		20		mA	
High Sensitivity Mode		22		mA	
Power-Down Mode					
Low Power Sleep Mode		0.1	1	µA	

[1] For definition of frequency deviation, see the Register 2—Transmit Modulation Register section.
[2] Measured as maximum unmodulated power. Output power varies with both supply and temperature.
[3] For matching details, see the LNA/PA Matching section.
[4] Sensitivity for combined matching network case is typically 2 dB less than separate matching networks.
[5] See Table 8 for a description of different receiver modes.
[6] Follow the matching and layout guidelines to achieve the relevant FCC/ETSI specifications.

TIMING CHARACTERISTICS

V_{DD} = 3 V ± 10%, VGND = 0 V, T_A = 25°C, unless otherwise noted. Guaranteed by design, but not production tested.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	<10	ns	SDATA to SCLK setup time
t_2	<10	ns	SDATA to SCLK hold time
t_3	<25	ns	SCLK high duration
t_4	<25	ns	SCLK low duration
t_5	<10	ns	SCLK to SLE setup time
t_6	<20	ns	SLE pulse width
t_8	<25	ns	SCLK to SREAD data valid, readback
t_9	<25	ns	SREAD hold time after SCLK, readback
t_{10}	<10	ns	SCLK to SLE disable time, readback

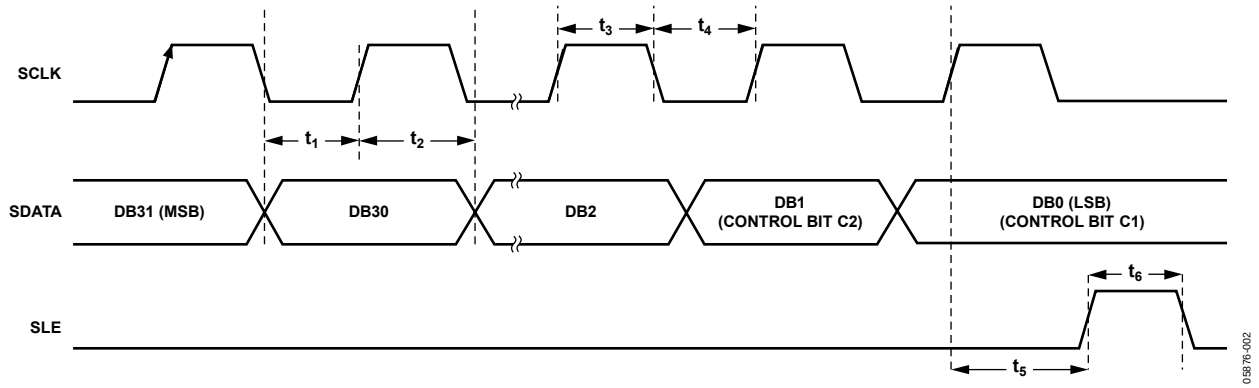


Figure 2. Serial Interface Timing Diagram

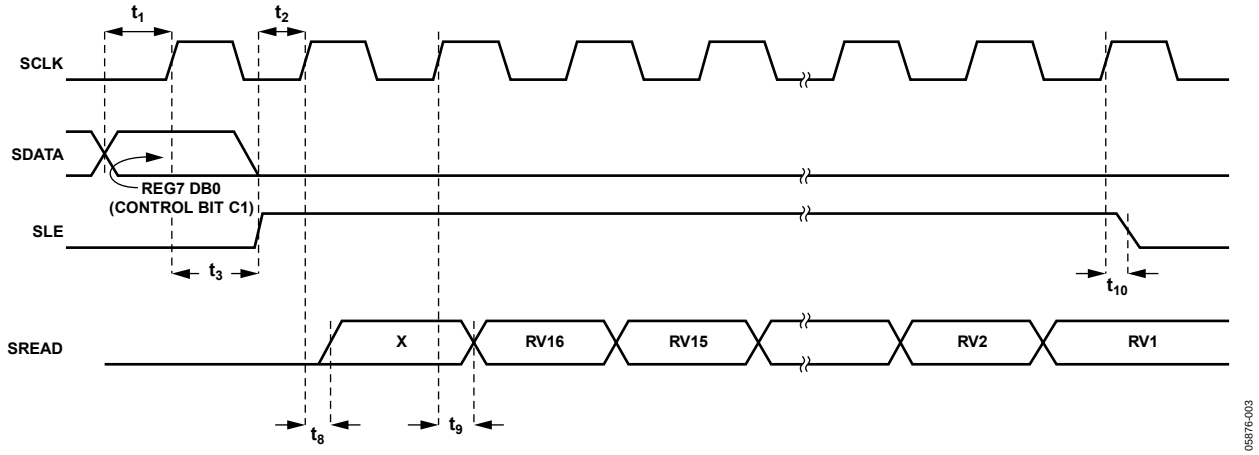


Figure 3. Readback Timing Diagram

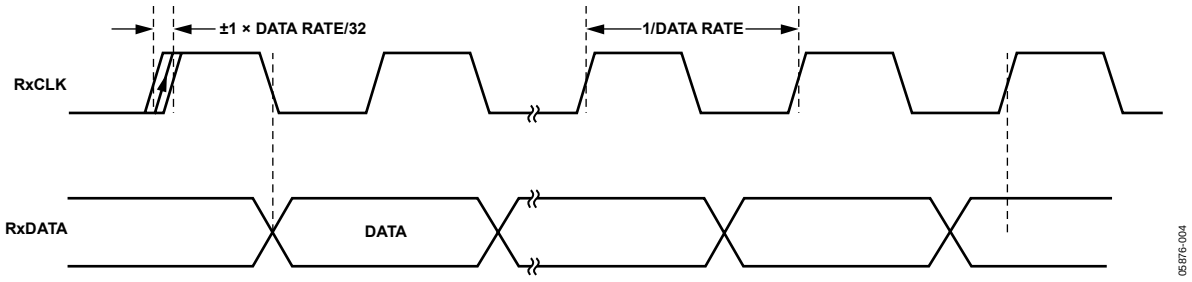


Figure 4. RxData/RxCLK Timing Diagram

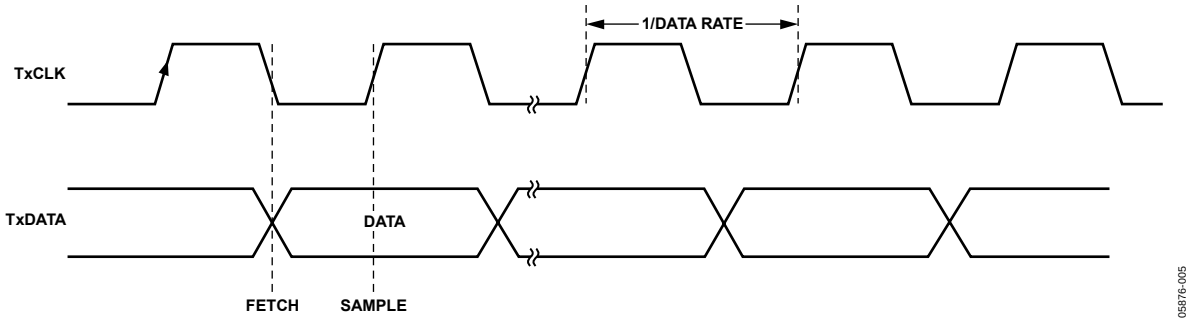


Figure 5. TxData/TxCLK Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND[1]	−0.3 V to +5 V
Analog I/O Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Digital I/O Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
MLF θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time-at-Peak Temperature	40 sec

[1] GND = CPGND = RFGND = DGND = AGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

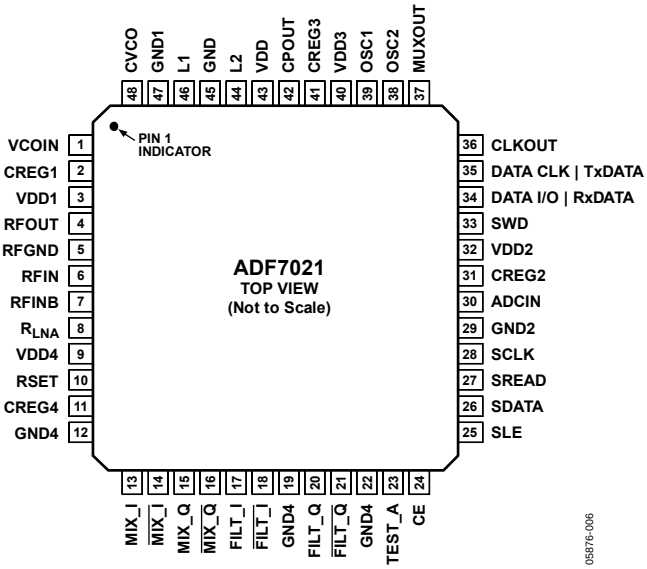


Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	VCOIN	The tuning voltage on this pin determines the output frequency of the voltage controlled oscillator (VCO). The higher the tuning voltage, the higher the output frequency.
2	CREG1	Regulator Voltage for PA Block. A 100 nF in parallel should be placed between this pin and ground for regulator stability and noise rejection.
3	VDD1	Voltage Supply for PA Block. Decoupling capacitors of 0.1 µF and 100 pF should be placed as close as possible to this pin. All VDD pins should be tied together.
4	RFOUT	The modulated signal is available at this pin. Output power levels are from −16 dBm to +13 dBm. The output should be impedance matched to the desired load using suitable components. See the Transmitter section.
5	RFGND	Ground for Output Stage of Transmitter. All GND pins should be tied together.
6	RFIN	LNA Input for Receiver Section. Input matching is required between the antenna and the differential LNA input to ensure maximum power transfer. See the LNA/PA Matching section.
7	RFINB	Complementary LNA Input. See the LNA/PA Matching section.
8	R_{LNA}	External Bias Resistor for LNA. Optimum resistor is 1.1 kΩ with 5% tolerance.
9	VDD4	Voltage Supply for LNA/MIXER Block. This pin should be decoupled to ground with a 10 nF capacitor.
10	RSET	External Resistor. Sets charge pump current and some internal bias currents. Use a 3.6 kΩ with 5% tolerance.
11	CREG4	Regulator Voltage for LNA/MIXER Block. A 100 nF capacitor should be placed between this pin and GND for regulator stability and noise rejection.
12	GND4	Ground for LNA/MIXER Block.
13 to 18	MIX_I, $\overline{\text{MIX\_I}}$, MIX_Q, $\overline{\text{MIX\_Q}}$, FILT_I, $\overline{\text{FILT\_I}}$,	Signal Chain Test Pins. These pins are high impedance under normal conditions and should be left unconnected.
19, 22	GND4	Ground for LNA/MIXER Block.
20, 21, 23	FILT_Q, $\overline{\text{FILT\_Q}}$, TEST_A	Signal Chain Test Pins. These pins are high impedance under normal conditions and should be left unconnected.
24	CE	Chip Enable. Bringing CE low puts the ADF7021 into complete power-down. Register values are lost when CE is low, and the part must be reprogrammed once CE is brought high.
25	SLE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches. A latch is selected using the control bits.
26	SDATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs as the control bits. This pin is a high impedance CMOS input.
27	SREAD	Serial Data Output. This pin is used to feed readback data from the ADF7021 to the microcontroller. The SCLK input is used to clock each readback bit (for example, AFC or ADC) from the SREAD pin.

Pin No.	Mnemonic	Function
28	SCLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This pin is a digital CMOS input.
29	GND2	Ground for Digital Section.
30	ADCIN	Analog-to-Digital Converter Input. The internal 7-bit ADC can be accessed through this pin. Full scale is 0 V to 1.9 V. Readback is made using the SREAD pin.
31	CREG2	Regulator Voltage for Digital Block. A 100 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
32	VDD2	Voltage Supply for Digital Block. A decoupling capacitor of 10 nF should be placed as close as possible to this pin.
33	SWD	Sync Word Detect. The ADF7021 asserts this pin when it has found a match for the sync word sequence (See the Register 11—Sync Word Detect Register section). This provides an interrupt for an external microcontroller indicating valid data is being received.
34	DATA I/O | RxDATA	Transmit Data Input/Received Data Output. This is a digital pin and normal CMOS levels apply. In UART mode, this pin provides an output for the received data in receive mode. In transmit mode, this pin is high impedance (see the Register 0—N Register section).
35	DATA CLK | TxDATA	Outputs the data clock in both receive and transmit modes. This is a digital pin and normal CMOS levels apply. The positive clock edge is matched to the center of the received data. In transmit mode, this pin outputs an accurate clock to latch the data from the microcontroller into the transmit section at the exact required data rate. In UART mode, this pin is used to input the transmit data in transmit mode. In receive mode, this pin is high impedance (see the Register 0—N Register section).
36	CLKOUT	A Divided-Down Version of the Crystal Reference with Output Driver. The digital clock output can be used to drive several other CMOS inputs such as a microcontroller clock. The output has a 50:50 mark-space ratio.
37	MUXOUT	Provides the Lock_Detect Signal. This signal is used to determine if the PLL is locked to the correct frequency. Other signals include Regulator_Ready, which is an indicator of the status of the serial interface regulator (see the Register 0—N Register section).
38	OSC2	The reference crystal should be connected between this pin and OSC1. A TCXO reference can be used by driving this pin with CMOS levels and disabling the crystal oscillator.
39	OSC1	The reference crystal should be connected between this pin and OSC2.
40	VDD3	Voltage Supply for the Charge Pump and PLL Dividers. This pin should be decoupled to ground with a 10 nF capacitor.
41	CREG3	Regulator Voltage for Charge Pump and PLL Dividers. A 100 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
42	CPOUT	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
43	VDD	Voltage Supply for VCO Tank Circuit. This pin should be decoupled to ground with a 10 nF capacitor.
44, 46	L2, L1	External VCO Inductor Pins. If using an external VCO inductor, a chip inductor should be connected across these pins to set the VCO operating frequency. If using the internal VCO inductor, these pins can be left floating. See the Voltage Controlled Oscillator (VCO) section for more information.
45, 47	GND, GND1	Grounds for VCO Block.
48	CVCO	A 22 nF capacitor should be placed between this pin and CREG1 to reduce VCO noise.

FREQUENCY SYNTHESIZER

REFERENCE INPUT

The on-board crystal oscillator circuitry (see Figure 7) can use an inexpensive quartz crystal as the PLL reference. The oscillator circuit is enabled by setting R1_DB12 high. It is enabled by default on power-up and is disabled by bringing CE low. Errors in the crystal can be corrected by using the automatic frequency control feature or by adjusting the fractional-N value (see the N Counter section). A single-ended reference (TCXO, CXO) can also be used. The CMOS levels should be applied to OSC2 with R1_DB12 set low.

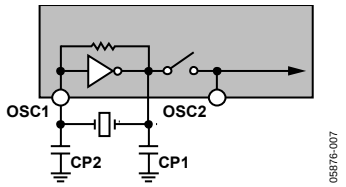


Figure 7. Oscillator Circuit on the ADF7021

Two parallel resonant capacitors are required for oscillation at the correct frequency. Their values are dependent upon the crystal specification. They should be chosen to make sure that the series value of capacitance added to the PCB track capacitance adds up to the load capacitance of the crystal, usually 18 pF to 20 pF. Track capacitance values vary from 2 pF to 5 pF, depending on board layout. When possible, choose capacitors that have a very low temperature coefficient to ensure stable frequency operation over all conditions.

Programmable Crystal Bias Current

Bias current in the oscillator circuit can be configured between 20 µA and 35 µA by writing to Bits R1_DB[13:14].

CLKOUT Divider and Buffer

The CLKOUT circuit takes the reference clock signal from the oscillator section, shown in Figure 7, and supplies a divided-down 50:50 mark-space signal to the CLKOUT pin. An even divide from 2 to 30 is available. This divide number is set in R1_DB[7:10]. On power-up, the CLKOUT defaults to divide-by-8.

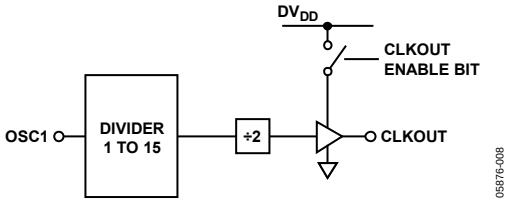


Figure 8. CLKOUT Stage

To disable CLKOUT, set the divide number to 0. The output buffer can drive up to a 20 pF load with a 10% rise time at 4.8 MHz. Faster edges can result in some spurious feedthrough to the output. A small series resistor (50 Ω) can be used to slow the clock edges to reduce these spurs at F_{CLK}.

R Counter

The 3-bit R counter divides the reference input frequency by an integer from 1 to 7. The divided-down signal is presented as the reference clock to the phase frequency detector (PFD). The divide ratio is set in Register 1. Maximizing the PFD frequency reduces the N value. This reduces the noise multiplied at a rate of 20 log(N) to the output and reduces occurrences of spurious components. Register 1 defaults to R = 1 on power-up:

$$PFD\ [\text{Hz}] = XTAL/R$$

Loop Filter

The loop filter integrates the current pulses from the charge pump to form a voltage that tunes the output of the VCO to the desired frequency. It also attenuates spurious levels generated by the PLL. A typical loop filter design is shown in Figure 9.

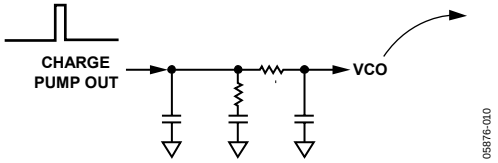


Figure 9. Typical Loop Filter Configuration

The loop should be designed so that the loop bandwidth (LBW) is approximately three times the data rate. Widening the LBW excessively reduces the time spent jumping between frequencies, but can cause insufficient spurious attenuation.

Narrow-loop bandwidths can result in the loop taking long periods of time to attain lock. Careful design of the loop filter is critical to obtain accurate modulation.

When using the Gaussian or raised cosine data filtering options, it is recommended to use a LBW of 2.0 to 2.5 times the data rate to ensure that sufficient samples of the input data are taken while filtering system noise. The free design tool ADIsimPLL can be used to design loop filters for the ADF7021.

N Counter

The feedback divider in the ADF7021 PLL consists of an 8-bit integer counter and a 15-bit Σ-Δ fractional-N divider. The integer counter is the standard pulse-swallow type common in PLLs. This sets the minimum integer divide value to 23. The fractional divide value gives very fine resolution at the output, where the output frequency of the PLL is calculated as

$$F_{OUT} = \frac{XTAL}{R} \times \left(Integer\_N + \frac{Fractional - N}{2^{15}} \right)$$

When VCO divide-by-2 (see the Voltage Controlled Oscillator (VCO) section) is selected, this formula becomes:

$$F_{OUT} = \frac{XTAL}{R} \times 0.5 \times \left(Integer\_N + \frac{Fractional - N}{2^{15}} \right)$$

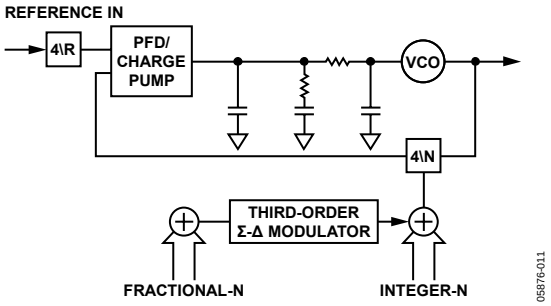


Figure 10. Fractional-N PLL

The combination of the integer-N (maximum = 255) and the fractional-N (maximum = 32768/32768) give a maximum N divider of 255 + 1. Therefore, the minimum usable PFD is

$$PFD_{MIN}[\text{Hz}] = \frac{Maximum\ Required\ Output\ Frequency}{(255+1)}$$

For example, when operating in the European 868 MHz to 870 MHz band, PFD_{MIN} equals 3.4 MHz.

Voltage Regulators

The ADF7021 contains four regulators to supply stable voltages to the part. The nominal regulator voltage is 2.3 V. Each regulator should have a 100 nF capacitor connected between CREG and GND. When CE is high, the regulators and other associated circuitry are powered on, drawing a total supply current of 2 mA. Bringing the CE pin low disables the regulators, reduces the supply current to less than 1 μA, and erases all values held in the registers. The serial interface operates from a regulator supply; therefore, to write to the part, the user must have CE high and the regulator voltage must be stabilized. Regulator status (CREG4) can be monitored using the regulator ready signal from muxout.

MUXOUT

The MUXOUT pin allows the user to access various digital points in the ADF7021. The state of MUXOUT is controlled by Bits R0_DB[29:31].

Regulator Ready

Regulator ready is the default setting on MUXOUT after the transceiver is powered up. The power-up time of the regulator is typically 50 μs. Because the serial interface is powered from the regulator, the regulator must be at its nominal voltage before the ADF7021 can be programmed. The status of the regulator can be monitored at MUXOUT. When the regulator ready signal on MUXOUT is high, programming of the ADF7021 can begin.

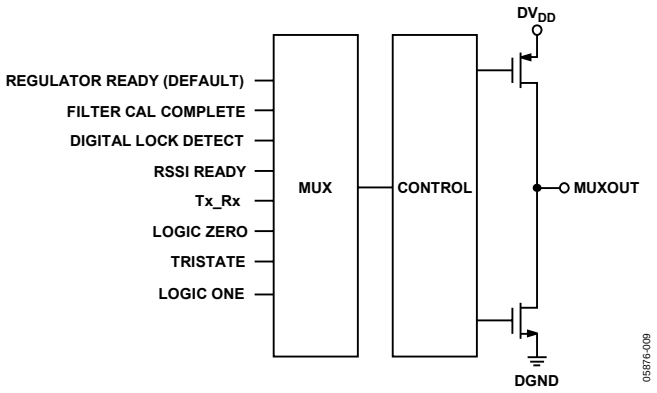


Figure 11. MUXOUT Circuit

Filter Cal Complete

MUXOUT can be set to filter cal complete, which is active high. This indicates when a fine filter calibration has been completed. It can be used as an interrupt to a microcontroller.

Digital Lock Detect

Digital lock detect indicates when the PLL has locked. The lock detect circuit is located at the PFD. When the phase error on five consecutive cycles is less than 15 ns, lock detect is set high. Lock detect remains high until a 25 ns phase error is detected at the PFD.

RSSI Ready

MUXOUT can be set to RSSI ready. This indicates that the internal analog RSSI has settled and a digital RSSI readback can be performed.

TX_RX

TX_RX signifies whether the ADF7021 is in transmit or receive mode. When in transmit ,mode, this signal is low. When in receive mode, this signal is high. It can be used to control an external Tx/Rx switch.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

To minimize spurious emissions, the on-chip VCO operates from 1724 MHz to 1880 MHz. The VCO signal is then divided by 2 to give the required frequency for the transmitter and the required LO frequency for the receiver.

The VCO should be recentered, depending on the required frequency of operation, by programming the VCO adjust bits R1_DB[23:24]. The VCO is enabled by Bit R1_DB17.

A further frequency divide-by-2 is included after the PLL to allow operation from 432 MHz to 470 MHz using the internal VCO inductor and 80 MHz to 325 MHz using the external VCO inductor. This divide-by-2 is enabled by setting R1_DB18 to 1.

The VCO needs an external 22 nF capacitor between the VCO and the regulator to reduce internal noise.

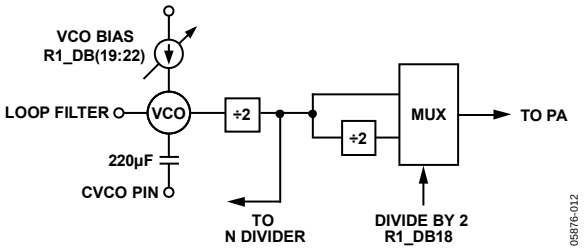


Figure 12. Voltage Controlled Oscillator (VCO)

The ADF7021 on-chip VCO can use either an internal or external tank inductor. The possible frequency ranges are given in Table 5.

Table 5. RF Output Frequency Ranges for Internal/External VCO Inductor and Divide-by-2 Enabled/Disabled

RF Frequency Output (MHz)	Int/Ext VCO Inductor R1_DB25	Divide-by-2 R1_DB18
862 to 940	0	0
431 to 470	0	1
135 to 650	1	0
80 to 325	1	1

Internal VCO Inductor

To select the internal VCO inductor, set R1_DB25 to Logic 0, which is the default setting.

VCO bias current can be adjusted using Bits R1_DB[19:22]. To ensure VCO oscillation, the minimum bias current setting under all conditions when using the internal VCO inductor is 0xA.

The VCO should be recentered, depending on the required frequency of operation, by programming the VCO adjust bits R1_DB[23:24].

Using the External VCO Inductor

When using an external inductor, the center frequency of the VCO is set by the internal varactor capacitance and the combined inductance of the external chip inductor, bond wire, and PCB track. A plot of the VCO operating frequency vs. total external inductance (chip inductor + PCB track) is shown in Figure 13. The inductance for a PCB track using FR4 material is approximately 0.57 nH/mm. This should be subtracted from the total value to determine the correct chip inductor value.

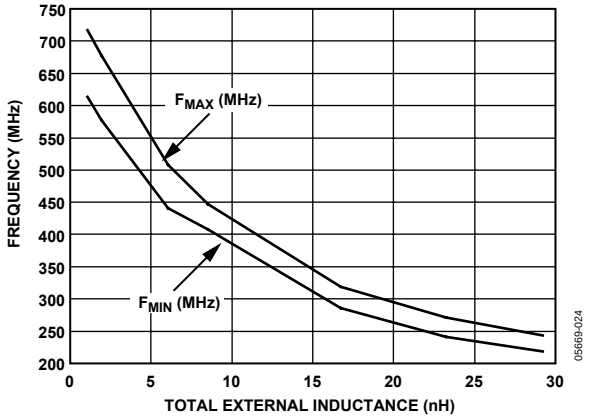


Figure 13. VCO Operating Frequency vs. Total External Inductance

VCO bias current can be adjusted using Bits R1_DB[19:22]. To minimize current consumption and to ensure reliable operation, the bias current setting should be as indicated in Table 6.

Table 6. Recommended VCO Bias Currents for External VCO Inductor

RF Frequency Output (f)	VCO Bias R1_DB[19:22]
f < 200 MHz	0001
200 MHz < f < 450 MHz	0010
f > 450 MHz	0011

CHOOSING CHANNELS FOR BEST SYSTEM PERFORMANCE

The architecture of fractional-N results in some level of the nearest integer channel moving through the loop to the RF output. These beat-note spurs are not attenuated by the loop, if the desired RF channel and the nearest integer channel are separated by a frequency of less than the LBW. The occurrence of beat-note spurs is rare because the integer frequencies are at multiples of the reference, which is typically >10 MHz. Beat-note spurs can be significantly reduced in amplitude by avoiding very small or very large values in the fractional register using the frequency doubler.

TRANSMITTER

RF OUTPUT STAGE

The power amplifier (PA) of the ADF7021 is based on a single-ended, controlled current, open-drain amplifier that has been designed to deliver up to 13 dBm into a 50 Ω load at a maximum frequency of 940 MHz.

The PA output current and, consequently, the output power are programmable over a wide range. The PA configuration is shown in Figure 14. The output power is set using Bits R2_DB[13:18].

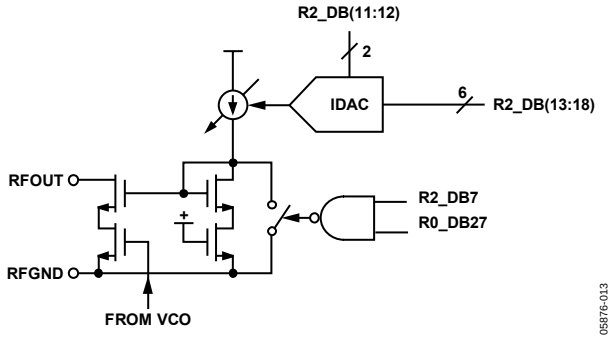


Figure 14. PA Configuration in FSK/GFSK Mode

The PA is equipped with overvoltage protection, which makes it robust in severe mismatch conditions. Depending on the application, users can design a matching network for the PA to exhibit optimum efficiency at the desired radiated output power level for a wide range of different antennas, such as loop or mono-pole antennas. See the LNA/PA Matching section for details.

PA Ramping

When the PA is switched on or off quickly, its changing input impedance momentarily disturbs the VCO output frequency. This process is called VCO pulling, and it manifests as spectral splatter, or spurs in the output spectrum around the desired carrier frequency. Some radio emissions regulations now place limits on these PA transient-induced spurs (for example, ETSI EN 300-220). By gradually ramping the PA on and off, PA transient spurs can be minimized. The ADF7021 has built-in PA ramping configurability. As Figure 15 illustrates, there are eight ramp rate settings, defined as a certain number of PA setting codes per one data-bit period. The PA steps through each of its 64 code levels, but at different speeds for each setting. The ramp rate is set by configuring Bits R2_DB[8:10].

If the PA is enabled/disabled by the PA_ENABLE bit in Register 2 (R2_DB7) it ramps up at the programmed rate but turns hard off. If the PA is enabled/disabled by the TX_RX bit in Register 0 (R0_DB27), it ramps up and down at the programmed rate.

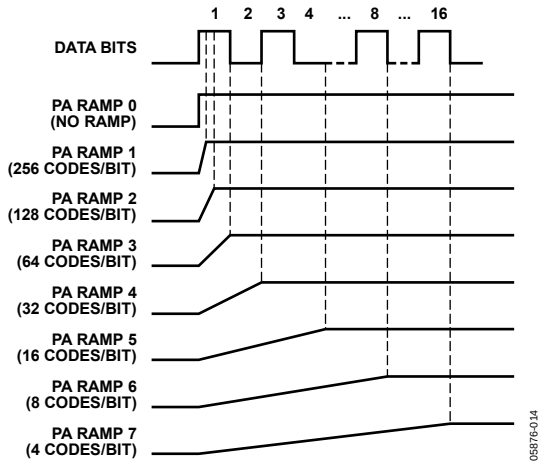


Figure 15. PA Ramping Settings

PA Bias Currents

Control Bits R2_DB[11:12] facilitate an adjustment of the PA bias current to further extend the output power control range, if necessary. If this feature is not required, the default value of 7 μA is recommended. If output power of greater than 10 dBm is required, a PA bias setting of 11 μA is recommended. The output stage is powered down by resetting Bit R2_DB7.

MODULATION SCHEMES

In all modulation schemes, an accurate clock is provided on the DATA_CLK pin to latch the data from the microcontroller into the transmit section at the exact required data rate. The exact frequency of this clock is defined by:

$$DATA\_CLK = \frac{XTAL}{DEMOD\_DIVIDER \times CDR\_DIVIDER \times 32}$$

where:

XTAL is the crystal frequency.

DEMOD_DIVIDER is the divider that sets the demod-clock rate (R3_DB[6:9]).

CDR_DIVIDER is the divider that sets the CDR clock rate (R3_DB[10:17]).

Binary Frequency Shift Keying (2FSK)

Two-level frequency shift keying is implemented by setting the N value for the center frequency and then toggling it with the TxDATA line. The deviation from the center frequency is set using Bits R2_DB[19:27]. The deviation from the center frequency in Hz is:

Direct RF output:

$$FSK_{DEVIATION}[\text{Hz}] = \frac{PFD \times TX\_FREQUENCY\_DEVIATION}{2^{16}}$$

Divide-by-2 enabled:

$$FSK_{DEVIATION}[\text{Hz}] = 0.5 \times \frac{PFD \times TX\_FREQUENCY\_DEVIATION}{2^{16}}$$

where:
TX_FREQUENCY_DEVIATION is a number from 1 to 511 (R2_DB[19:27]).

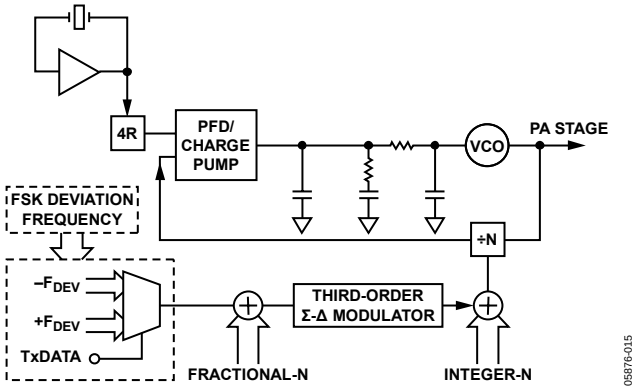


Figure 16. 2FSK Implementation

Three-Level Frequency Shift Keying (3FSK)

In three-level FSK modulation (also known as ternary FSK), the binary data (Logic 0 and Logic 1) is mapped onto three distinct frequencies:

- the carrier frequency (F_C),
- the carrier frequency minus a deviation frequency ($F_C - F_{DEV}$), and
- the carrier frequency plus the deviation frequency ($F_C + F_{DEV}$).

A Logic 0 is mapped to the carrier frequency while a Logic 1 is either mapped onto frequency $F_C - F_{DEV}$ or $F_C + F_{DEV}$.

The bits to frequency mapping result in a reduced transmission bandwidth as energy is removed from the sidebands and transferred to the carrier frequency. This increases the spectral efficiency in comparison to 2FSK.

To ensure there is no loss in SNR at the receiver due to the ternary nature of the modulation, a simple convolutional encoder is used. A block diagram of the transmit hardware used to realize this system is shown in Figure 17. The convolutional encoder polynomial used to implement the transmit spectral shaping is $P(D) = 1 - D^2$. A precoder with transfer function $1/P(D)$ is used to undo the encoding process of the convolutional code P(D) at the transmitter side.

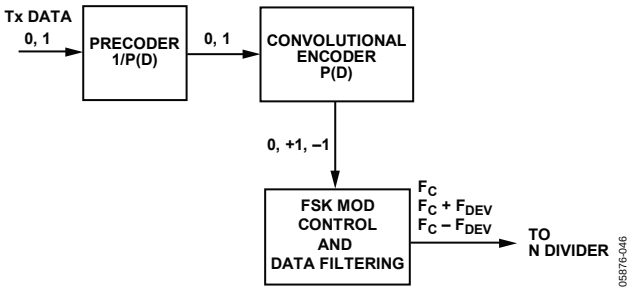


Figure 17. 3FSK Encoding

The signal map of one-zero binary data to the 3-level convolutional output follows. The convolutional encoder restricts the maximum number of sequential +1's or −1's to two and also delivers an equal number of +1's and −1's to the FSK modulator, thus ensuring equal spectral energy in both 3FSK sidebands.

3-Level Signal Mapping of the Convolutional Encoder

Tx DATA	1	0	1	1	0	0	1	0	0	1
Precoder O/P	1	0	0	1	0	1	1	1	1	0
Encoder O/P	+1	0	−1	+1	0	0	+1	0	0	−1

3FSK is selected by setting bits in R2_DB[4:6]. It can also be used with raised cosine filtering to further increase the spectral efficiency of the transmit signal.

Four-Level Frequency Shift Keying (4FSK)

Four-level frequency shift keying differs from binary FSK in that four possible frequencies are used to represent each pair of data bits to be transmitted instead of two possible frequencies for each bit of data. This halves the symbol rate because a frequency change is only required after every second bit. It also doubles the number of symbols because there are four possible arrangements of a pair of consecutive NRZ data bits. By minimizing the separation between symbol frequencies, 4FSK can have high spectral efficiency.

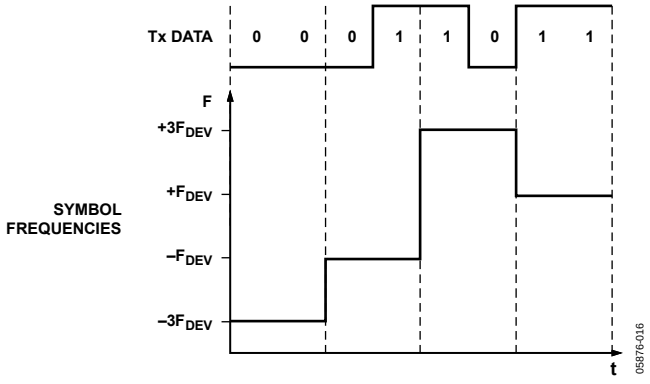


Figure 18. 4FSK Encoding

Oversampled 2FSK

In oversampled 2FSK, the data is sampled at 32 times the programmed rate, allowing odd data rates.

SPECTRAL SHAPING

Gaussian or raised cosine filtering can be used to improve transmit spectral efficiency. The ADF7021 supports Gaussian filtering (BT = 0.5) on 2FSK modulation. Raised cosine filtering (alpha = 0.5) can be used with 2FSK, 3FSK, or 4FSK modulation.

Gaussian Frequency Shift Keying (GFSK)

Gaussian frequency shift keying reduces the bandwidth occupied by the transmitted spectrum by digitally prefiltering the transmit data. The bandwidth time (BT) product of the Gaussian filter used is 0.5.

Gaussian filtering can just be used with 2FSK modulation. This is selected by setting Bits R2_DB[4:6] to 001.

Raised Cosine Filtering

Raised cosine filtering provides digital prefiltering of the transmit data using a rasied cosine filter with a roll-off factor (alpha) of 0.5. Rasied cosine filtering can be used with 2FSK, 3FSK, and 4FSK.

Raised cosine filtering is enabled by setting Bits R2_DB[4:6] as outlined in Table 7.

MODULATION AND FILTERING OPTIONS

The various modulation and data filtering options are described in Table 7.

Table 7. Modulation and Filtering Options on the ADF7021

Modulation	Data Filtering	R2_DB[4:6]
2FSK	None	000
	Gaussian	001
	Raised cosine	101
3FSK	None	010
	Raised cosine	110
4FSK	None	011
	Raised cosine	111
Oversampled 2FSK	None	100

RECEIVER SECTION

RF FRONT END

The ADF7021 is based on a fully integrated, low IF receiver architecture. The low IF architecture facilitates a very low external component count and does not suffer from power-line-induced interference problems.

Figure 19 shows the structure of the receiver front end. The many programming options allow users to trade off sensitivity, linearity, and current consumption against each other in the way best suited for their applications. To achieve a high level of resilience against spurious reception, the low noise amplifier (LNA) features a differential input. Switch SW2 shorts the LNA input when transmit mode is selected (R0_DB27 = 0). This feature facilitates the design of a combined LNA/PA matching network, avoiding the need for an external Rx/Tx switch. See the LNA/PA Matching section for details on the design of the matching network.

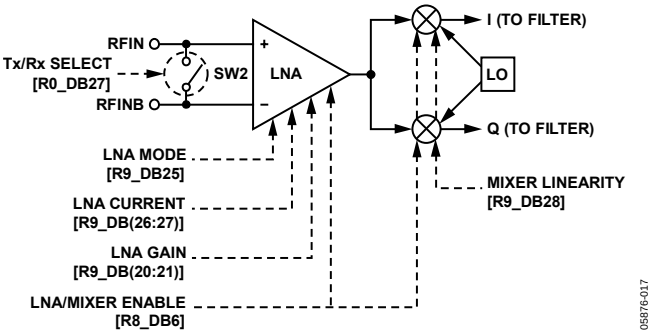


Figure 19. ADF7021 RF Front End

The LNA is followed by a quadrature downconversion mixer, which converts the RF signal to the IF frequency of 100 kHz. An important consideration is that the output frequency of the synthesizer must be programmed to a value 100 kHz below the center frequency of the received channel.

The LNA has two basic operating modes: high gain/low noise mode and low gain/low power mode. To switch between these two modes, use the LNA Mode Bit, R9_DB25. The mixer is also configurable between a low current and an enhanced linearity mode using the Mixer Linearity Bit, R9_DB28.

Based on the specific sensitivity and linearity requirements of the application, it is recommended to adjust control bits LNA mode (R9_DB25) and mixer linearity (R9_DB28) as outlined in Table 8.

The gain of the LNA is configured by the LNA gain field, R9_DB[20:21], and can be set by either the user or the automatic gain control (AGC) logic.

IF Filter Settings

Out-of-band interference is rejected by means of a fifth-order Butterworth polyphase IF filter centered on a frequency of 100 kHz. The bandwidth of the IF filter can be programmed between 12.5 kHz and 25 kHz by Control Bits R4_DB[30:31], and should be chosen as a compromise between interference rejection, attenuation of the desired signal, and the AFC pull-in range.

Coarse/Fine Filter Calibration

To compensate for manufacturing tolerances, the IF filter should be calibrated once after power-up. Coarse and fine calibration schemes are provided in order to offer a choice between fast calibration with the coarse scheme and high filter centering accuracy with fine calibration. Coarse calibration is enabled by setting Bit R5_DB4 high. Fine calibration is enabled by setting Bit R6_DB4 high. It is necessary to do a coarse calibration before doing a fine calibration. If the IF_FINE_CAL bit, R6_DB4, has already been configured high, it is possible to do a fine calibration by writing only to Register 5. Once initiated by writing to the part, the calibration is performed automatically without any user intervention. Calibration time is 200 µs for coarse calibration and a few milliseconds for fine calibration, during which the ADF7021 should not be accessed. The IF filter calibration logic requires that the IF filter divider in Bits R5_DB[5:13] be set depending on the crystal frequency. It is important not to initiate the calibration cycle before the crystal oscillator has fully settled. If the AGC loop is disabled, the gain of IF filter can be set to three levels using the Filter Gain Field, R9_DB[22:23]. The filter gain is adjusted automatically if the AGC loop is enabled.

Table 8. LNA/Mixer Modes

Receiver Mode	LNA Mode (R9_DB25)	LNA Gain Value (R9_DB[20:21])	Mixer Linearity (R9_DB28)	Sensitivity (DR = 9.6 kbps, F_{DEV} = 4.8 kHz)	Rx Current Consumption (mA)	Input IP3 (dBm)
High Sensitivity Mode (default)	0	30	0	−117	22	TBD
Rx Mode2	1	10	0	TBD	20	TBD
Low Current Mode	1	3	0	TBD	19	TBD
Enhanced Linearity Mode	1	3	1	TBD	19	TBD
Rx Mode5	1	10	1	TBD	20	TBD
Rx Mode6	0	30	1	TBD	21	TBD

RSSI/AGC

The RSSI is implemented as a successive compression log amp following the base band channel filtering. The log amp achieves ±3 dB log linearity. It also doubles as a limiter to convert the signal-to-digital levels for the FSK demodulator. Offset correction is achieved using a switched capacitor integrator in feedback around the log amp. This uses the BB offset clock divide. The RSSI level is converted for user readback and digitally controlled AGC by an 80-level (7-bit) flash ADC. This level can be converted to input power in dBm.

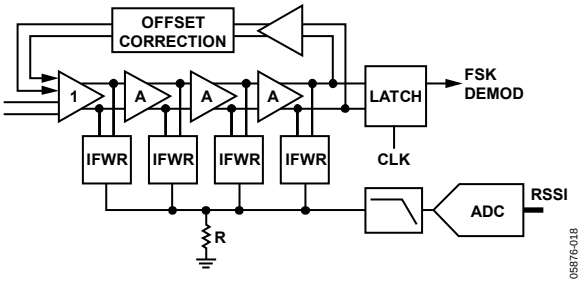


Figure 20. RSSI Block Diagram

RSSI Thresholds

When the RSSI is above AGC_HIGH_THRESHOLD, the gain is reduced. When the RSSI is below AGC_LOW_THRESHOLD, the gain is increased. A delay (AGC_DELAY) is programmed to allow for settling of the loop. All of these parameters are set in Register 9. The user can program the two threshold values (defaults 30 and 70) and the delay value (default 10). The default AGC setup values should be adequate for most applications. The threshold values must be chosen to be more than 30 apart for the AGC to operate correctly.

Offset Correction Clock

In Register 3, the user should set the BB Offset Clock Divide Bits R3_DB[4:5] to give an offset clock between 1 MHz and 2 MHz:

$$BBOS\_CLK\ [\text{Hz}] = XTAL/(BBOS\_CLK\_DIVIDE)$$

where:

BBOS_CLK_DIVIDE can be set to 4, 8, or 16.

AGC Information and Timing

AGC is selected by default and operates by selecting the appropriate LNA and filter gain settings for the measured RSSI level. It is possible to disable AGC by writing to Register 9 if the user wants to enter one of the modes listed in Table 8. The time for the AGC circuit to settle and therefore, the time it takes to measure the RSSI accurately, is typically 150 µs. However, this depends on how many gain settings the AGC circuit has to cycle through. After each gain change, the AGC loop waits for a programmed time to allow transients to settle. This wait time can be altered to speed up the settling by adjusting the appropriate parameters.

$$AGC\_Wait\_Time = \frac{AGC\_Delay \times SEQ\_CLK\_DIVIDE}{XTAL}$$

where:

AGC Settling = *AGC_Wait_Time* × Number of Gain Changes

Thus, in the worst-case scenario, if the AGC loop has to go through all five gain changes,

AGC_Delay =10 cycles
SEQ_CLK = 200 kHz
AGC Settling = 10 × 5 µs × 5 = 250 µs
Minimum *AGC_Wait_Time* must be at least 25 µs.

RSSI Formula (Converting to dBm)

$$Input\_Power\ [\text{dBm}] = -120\ \text{dBm} + (Readback\_Code + Gain\_Mode\_Correction) \times 0.5$$

where:

Readback_Code is given by Bit RV7 to Bit RV1 in the readback register (see the Readback Format section).
Gain_Mode_Correction is given by the values in Table 9.

LNA gain (LG2, LG1) and filter gain (FG2, FG1) are obtained from Register 9.

Table 9. Gain Mode Correction

LNA Gain (LG2, LG1)	Filter Gain (FG2, FG1)	Gain Mode Correction
H (1, 0)	H (1, 0)	TBD
H (1, 0)	M (0, 1)	TBD
M (0, 1)	M (0, 1)	TBD
L (0, 0)	M (0,1)	TBD
L (0, 0)	L (0, 0)	TBD

An additional factor should be introduced to account for losses in the front-end-matching network/antenna.

FSK DEMODULATORS ON THE ADF7021

There are four demodulators on the ADF7021:

- 2FSK correlator/demodulator
- 2FSK linear demodulator
- 3FSK demodulator
- 4FSK demodulator

Select these using the Demod Scheme Bits, R4_DB[4:6].

FSK CORRELATOR/DEMODULATOR

The quadrature outputs of the IF filter are first limited and then fed to a pair of digital frequency correlators that perform band-pass filtering of the binary FSK frequencies at (IF + F_{DEV}) and (IF − F_{DEV}). Data is recovered by comparing the output levels from each of the two correlators. The performance of this frequency discriminator approximates that of a matched filter detector, which is known to provide optimum detection in the presence of AWGN.

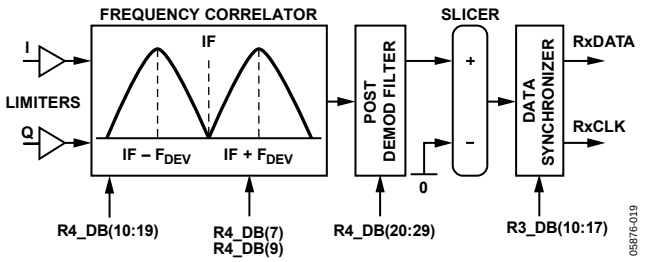


Figure 21. FSK Correlator/Demodulator Block Diagram

Postdemodulator Filter

A second-order, digital low-pass filter removes excess noise from the demodulated bit stream at the output of the discriminator. The bandwidth of this postdemodulator filter is programmable and must be optimized for the user's data rate. If the bandwidth is set too narrow, performance is degraded due to intersymbol interference (ISI). If the bandwidth is set too wide, excess noise degrades the receiver's performance. Typically, the 3 dB bandwidth of this filter is set at approximately 0.75 times the user's data rate, using Bits R4_DB[20:29].

Bit Slicer

The received data is recovered by threshold detecting the output of the postdemodulator low-pass filter. In the correlator/demodulator, the binary output signal levels of the frequency discriminator are always centered on 0. Therefore, the slicer threshold level can be fixed at 0 and the demodulator performance is independent of the run-length constraints of the transmit data bit stream. This results in robust data recovery, which does not suffer from the classic baseline wander problems that exist in the more traditional FSK demodulators.

Frequency errors are removed by an internal AFC loop that measures the average IF frequency at the limiter output and applies a frequency correction value to the fractional-N synthesizer. This loop should be activated when the frequency errors are greater than approximately 40% of the transmit frequency deviation.

Data Synchronizer

An oversampled digital PLL is used to resynchronize the received bit stream to a local clock. The oversampled clock rate of the PLL (CDR_CLK) must be set at 32 times the data rate. See the Register 3—Transmit/Receive Clock Register section for programming notes. The clock recovery PLL can accommodate frequency errors of up to ±2%.

FSK Correlator Register Settings

To enable the FSK correlator/demodulator, Bits R4_DB[4:6] should be set to 001. To achieve best performance, the bandwidth of the 2FSK correlator must be optimized for the specific deviation frequency that is used by the 2FSK transmitter.

The discriminator BW is controlled in Register 4 by DB[10:19] and is defined as

$$Discriminator\_BW = DEMOD\_CLK \times K/(400 \times 10^3)$$

where:

DEMOD_CLK is as defined in the Register 3—Transmit/Receive Clock Register Comments section.
K = Round (100e3/Fdeviation) and Fdeviation is the 2FSK frequency deviation in Hz.

To optimize the coefficients of the 2FSK correlator, Bits R4_DB7 and R4_DB[8:9] must be assigned. The value of these bits depends on whether K is odd or even. These bits are assigned according to Table 10 and Table 11.

Table 10. When K Is Even

K	K/2	R4_DB7	R4_DB[8:9]
Even	Even	0	00
Even	Odd	0	10

Table 11. When K Is Odd

K	(K + 1)/2	R4_DB7	R4_DB[8:9]
Odd	Even	1	00
Odd	Odd	1	10

Postdemodulator Bandwidth Register Settings

The 3 dB bandwidth of the postdemodulator filter is controlled by Bits R4_DB[20:29] and is given by

$$Post\_Demod\_BW\_Setting = \frac{2^{11} \times \pi \times F_{CUTOFF}}{DEMOD\_CLK}$$

where:

F_{CUTOFF} is the target 3 dB bandwidth in Hz of the postdemodulator filter. This should typically be set to 0.75 times the data rate (DR).

Some sample settings for the FSK correlator/demodulator are

DEMOD_CLK = 11.0592 MHz
DR = 9.6 kbps
F_{DEV} = 4.8 kHz

therefore,

$F_{CUTOFF} = 0.75 \times 9.6 \times 10^3$ Hz
Post_Demod_BW = $2^{11} \times \pi \times 7.2 \times 10^3$ Hz/(11.0592×10^6)
Post_Demod_BW = Round(4.188) = 4

and

K = Round(100 kHz)/4.8 kHz) = 21
Discriminator_BW = $(11.0592 \times 10^6 \times 21)/(400 \times 10^3)$ = 580.6 = 581 (rounded to nearest integer)

Table 12. Example Register Settings

Setting Name	Register Address	Value
Post_Demod_BW	R4_DB[20:29]	0x04
Discriminator BW	R4_DB[10:19]	0x245
Dot Product	R4_DB7	1
Rx Data Invert	R4_DB[8:9]	10

LINEAR 2FSK DEMODULATOR

Figure 22 shows a block diagram of the linear 2FSK demodulator.

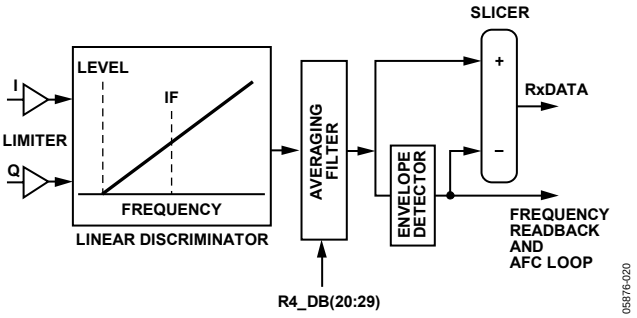


Figure 22. Block Diagram of Frequency Measurement System and Linear FSK Demodulator

This method of frequency demodulation is useful when the system protocol cannot support the overhead of the settling time of the internal feedback AFC loop.

A digital frequency discriminator provides an output signal that is linearly proportional to the frequency of the limiter outputs. The discriminator output is then filtered and averaged using a combined averaging filter and envelope detector. The demodulated 2FSK data is recovered by threshold detecting the output of the averaging filter, as shown in Figure 22. In this mode, the slicer output shown in Figure 22 is routed to the data synchronizer PLL for clock synchronization. To enable the linear FSK demodulator, set Bits R4_DB[4:6] to 000.

The 3 dB bandwidth of the postdemodulation filter is set in the same way as the 2FSK correlator/demodulator, which is set in R4_DB[20:29] and is defined as

$$Post\_Demod\_BW\_Setting = \frac{2^{11} \times \pi \times F_{CUTOFF}}{DEMOD\_CLK}$$

where:

F_{CUTOFF} is the target 3 dB bandwidth in Hz of the postdemodulator filter.
DEMOD_CLK is as defined in the Register 3—Transmit/Receive Clock Register Comments section.

3FSK DEMODULATOR

The 3FSK demodulator uses a pair of digital frequency correlators followed by a Viterbi decoder and clock and data recovery to perform three-level FSK demodulation. To enable 3FSK demodulation, Bits R4_DB[4:6] must be set to 010. The settings for the 3FSK demodulator are set in Register 13. The post demod BW, discriminator BW, dot product, and Rx invert settings of Register 4 also need to be set appropriately as outlined in the FSK Correlator/Demodulator section.

4FSK DEMODULATOR

The 4FSK demodulator uses a pair of digital frequency correlators and clock and data recovery to perform four-level FSK demodulation. To enable 4FSK demodulation, Bits R4_DB[4:6] must be set to 011. The post demod BW, discriminator BW, dot product, and Rx invert settings of Register 4 also need to be set appropriately as outlined in the FSK Correlator/Demodulator section.

AFC SECTION

The ADF7021 supports a real-time AFC loop that is used to remove frequency errors that can arise due to mismatches between the transmit and receive crystals. The AFC loop also uses the frequency discriminator block, as described in the Linear 2FSK Demodulator section and in Figure 22. The discriminator output is filtered and averaged to remove the FSK frequency modulation using a combined averaging filter and envelope detector. In receive mode, the output of the envelope detector provides an estimate of the average IF frequency.

Two methods of AFC, external and internal, are supported on the ADF7021.

External AFC

Here, the user reads back the frequency information through the ADF7021 serial port and applies a frequency correction value to the fractional-N synthesizer N divider.

The frequency information is obtained by reading the 16-bit signed AFC_readback, as described in the Readback Format section, and by applying the following formula:

$$FREQ\_RB\ [\text{Hz}] = (AFC\_READBACK \times DEMOD\_CLK)/2^{18}$$

Note that while the AFC_READBACK value is a signed number, under normal operating conditions it is positive. In the absence of frequency errors, the FREQ_RB value is equal to the IF frequency of 100 kHz.

Internal AFC

The ADF7021 supports a real-time, internal, automatic frequency control loop. In this mode, an internal control loop automatically monitors the frequency error and adjusts the synthesizer-N divider using an internal PI control loop.

The internal AFC control loop parameters are controlled in Register 10. The internal AFC loop is activated by setting R10_DB4 to 1. A scaling coefficient must also be entered, based on the crystal frequency in use. This is set up in R10_DB[5:16] and should be calculated using

$$AFC\_Scaling\_Coefficient = (500 \times 2^{24})/XTAL$$

Maximum AFC Range

The maximum AFC frequency range is ±127.5 kHz. This is set by Bits R10_DB[24:31]. The maximum AFC pull-in range should be less than or equal to half the channel spacing to prevent the AFC pulling in a signal in the adjacent channel. If the maximum AFC pull-in range is larger than the IF filter bandwidth, the attenuation of the IF filter must be considered.

When AFC errors have been removed using either the internal or external AFC, further improvement in the receiver's sensitivity can be obtained by reducing the IF filter bandwidth using Bits R4_DB[30:31].

AUTOMATIC SYNC WORD RECOGNITION

The ADF7021 also supports automatic detection of the sync or ID fields. To activate this mode, the sync (or ID) word must be preprogrammed into the ADF7021. In receive mode, this preprogrammed word is compared to the received bit stream, and when a valid match is identified, the external SWD pin is asserted by the ADF7021 on the next Rx clock pulse.

This feature can be used to alert the microprocessor that a valid channel has been detected. It relaxes the computational requirements of the microprocessor and reduces the overall power consumption.

The SWD signal can also be used to frame a received packet length by staying high for a preprogrammed number of bytes. The data packet length can be set in Bits R12_DB[8:15].

The SWD pin status can be configured by setting Bits R12_DB[6:7]. Bits R11_DB[4:5] are used to set the length of the sync/ID word, which can be 12, 16, 20, or 24 bits long. The transmitter must transmit the MSB of the sync byte first and the LSB last to ensure proper alignment in the receiver sync-byte-detection hardware.

For systems using FEC, an error tolerance parameter can also be programmed that accepts a valid match when up to 3 bits of the word are incorrect. The error tolerance value is assigned in R11_DB[6:7].

APPLICATIONS

LNA/PA MATCHING

The ADF7021 exhibits optimum performance in terms of sensitivity, transmit power, and current consumption, only if its RF input and output ports are properly matched to the antenna impedance. For cost-sensitive applications, the ADF7021 is equipped with an internal Rx/Tx switch that facilitates the use of a simple, combined passive PA/LNA matching network. Alternatively, an external Rx/Tx switch such as the ADG919 can be used, which yields a slightly improved receiver sensitivity and lower transmitter power consumption.

External Rx/Tx Switch

Figure 23 shows a configuration using an external Rx/Tx switch. This configuration allows an independent optimization of the matching and filter network in the transmit and receive path. Therefore, it is more flexible and less difficult to design than the configuration using the internal Rx/Tx switch. The PA is biased through Inductor L1, while C1 blocks dc current. Both elements, L1 and C1, also form the matching network that transforms the source impedance into the optimum PA load impedance, Z_{OPT}_PA.

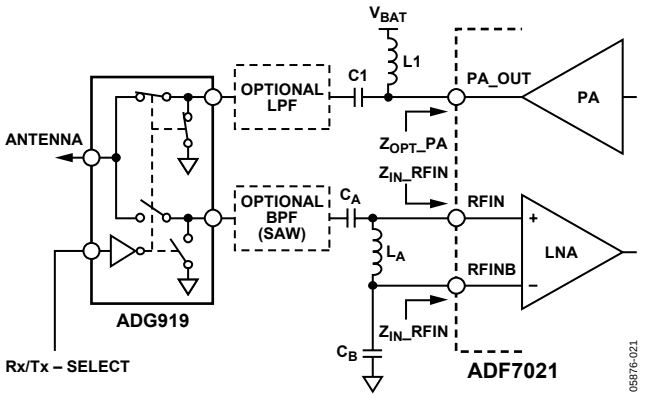


Figure 23. ADF7021 with External Rx/Tx Switch

Z_{OPT}_PA depends on various factors, such as the required output power, the frequency range, the supply voltage range, and the temperature range. Selecting an appropriate Z_{OPT}_PA helps to minimize the Tx current consumption in the application. Application Note AN-764 contains a number of Z_{OPT}_PA values for representative conditions. Under certain conditions however, it is recommended to obtain a suitable Z_{OPT}_PA value by means of a load-pull measurement.

Due to the differential LNA input, the LNA matching network must be designed to provide both a single-ended to differential conversion, and a complex conjugate impedance match. The network with the lowest component count that can satisfy these requirements is the configuration shown in Figure 23, consisting of two capacitors and one inductor. A first-order implementation of the matching network can be obtained by understanding the arrangement as two L-type matching networks in a back-to-back configuration. Due to the asymmetry of the network with respect to ground, a compromise between the input reflection coefficient and the maximum differential signal swing at the LNA input must be established. The use of appropriate CAD software is strongly recommended for this optimization.

Depending on the antenna configuration, the user might need a harmonic filter at the PA output to satisfy the spurious emission requirement of the applicable government regulations. The harmonic filter can be implemented in various ways, such as a discrete LC pi or T-stage filter. Dielectric low-pass filter components, such as the LFL18924MTC1A052 (for operation in the 915 MHz and 868 MHz band) by Murata Manufacturing Co. Ltd., represent an attractive alternative to discrete designs. The immunity of the ADF7021 to strong out-of-band interference can be improved by adding a band-pass filter in the Rx path. Apart from discrete designs, SAW or dielectric filter components such as the SAFCH869MAM0T00B0S, SAFCH915MAL0N00B0S, DCFB2869MLEJAA-TT1, or DCFB3915MLDJAA-TT1, all by Murata Manufacturing Co. Ltd., are well suited for this purpose. Alternatively, the ADF7021 blocking performance can be improved by selecting the high linearity mode, as described in Table 8.

Internal Rx/Tx Switch

Figure 24 shows the ADF7021 in a configuration where the internal Rx/Tx switch is used with a combined LNA/PA matching network. For most applications, the slight performance degradation of 1 dB to 2 dB caused by the internal Rx/Tx switch is acceptable, allowing the user to take advantage of the cost-saving potential of this solution. The design of the combined matching network must compensate for the reactance presented by the networks in the Tx and the Rx paths, taking the state of the Rx/Tx switch into consideration.

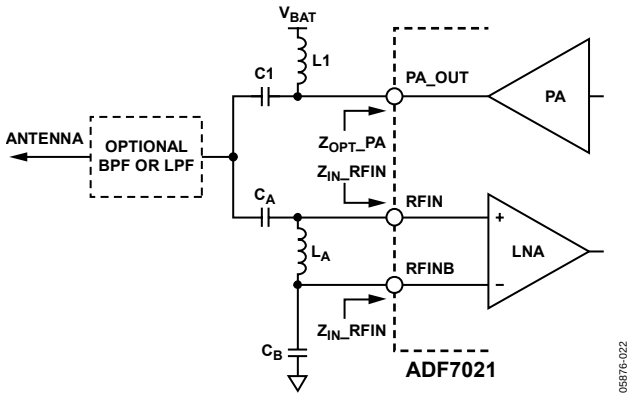


Figure 24. ADF7021 with Internal Rx/Tx Switch

The procedure typically requires several iterations until an acceptable compromise has been reached. The successful implementation of a combined LNA/PA matching network for the ADF7021 is critically dependent upon the availability of an accurate electrical model for the PC board. In this context, the use of a suitable CAD package is strongly recommended. To avoid this effort, the reference design provided for the ADF7021 RF module can be used. Gerber files are available on request.

As with the external Rx/Tx switch, an additional LPF or BPF could be required to suppress harmonics in the transmit spectrum or to improve the resilience of the receiver against out-of-band interferers.

TRANSMIT PROTOCOL AND CODING CONSIDERATIONS

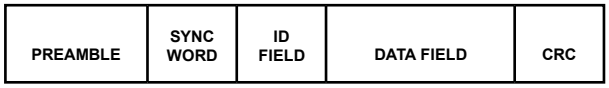


Figure 25. Typical Format of a Transmit Protocol

A dc-free preamble pattern is recommended for FSK demodulation. The recommended preamble pattern is a dc-free pattern such as a 10101010 … pattern. Preamble patterns with longer run-length constraints such as 11001100… can also be used. However, this results in a longer synchronization time of the received bit stream in the receiver.

Manchester coding can be used for the entire transmit protocol. However, the remaining fields that follow the preamble header do not have to use dc-free coding. For these fields, the ADF7021 can accommodate coding schemes with a run length of up to 6 bits without any performance degradation.

If longer run-length coding must be supported, the ADF7021 has several other features that can be activated. These involve a range of programmable options that allow the envelope detector output to be frozen after preamble acquisition.

DEVICE PROGRAMMING AFTER INITIAL POWER-UP

Table 13 lists the minimum number of writes needed to set up the ADF7021 in either Tx or Rx mode after CE is brought high. Additional registers can also be written to tailor the part to a particular application, such as setting up sync byte detection or enabling AFC. When going from Tx to Rx or vice versa, the user needs to write only to Register 1 to alter the LO by 100 kHz and to toggle the Tx/Rx bit.

Table 13. Minimum Register Writes Required for Tx/Rx Setup

Mode	Registers				
Tx	Reg 0	Reg 1	Reg 2	Reg 3	
Rx	Reg 0	Reg 1	Reg 3	Reg 4	Reg 5
Tx <-> Rx	Reg 0				

Figure 26 and Figure 27 show the recommended programming sequence and associated timing for power-up from standby mode.

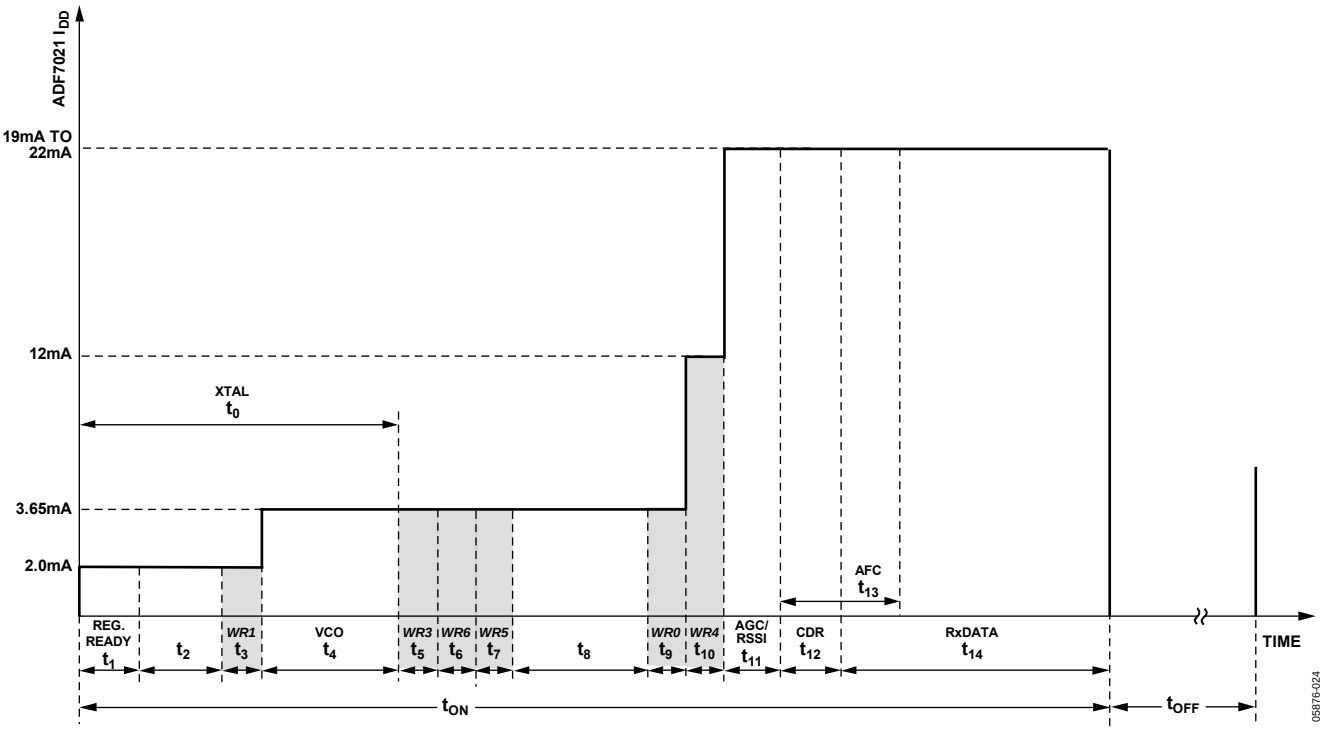


Figure 26. Rx Programming Sequence and Timing Diagram

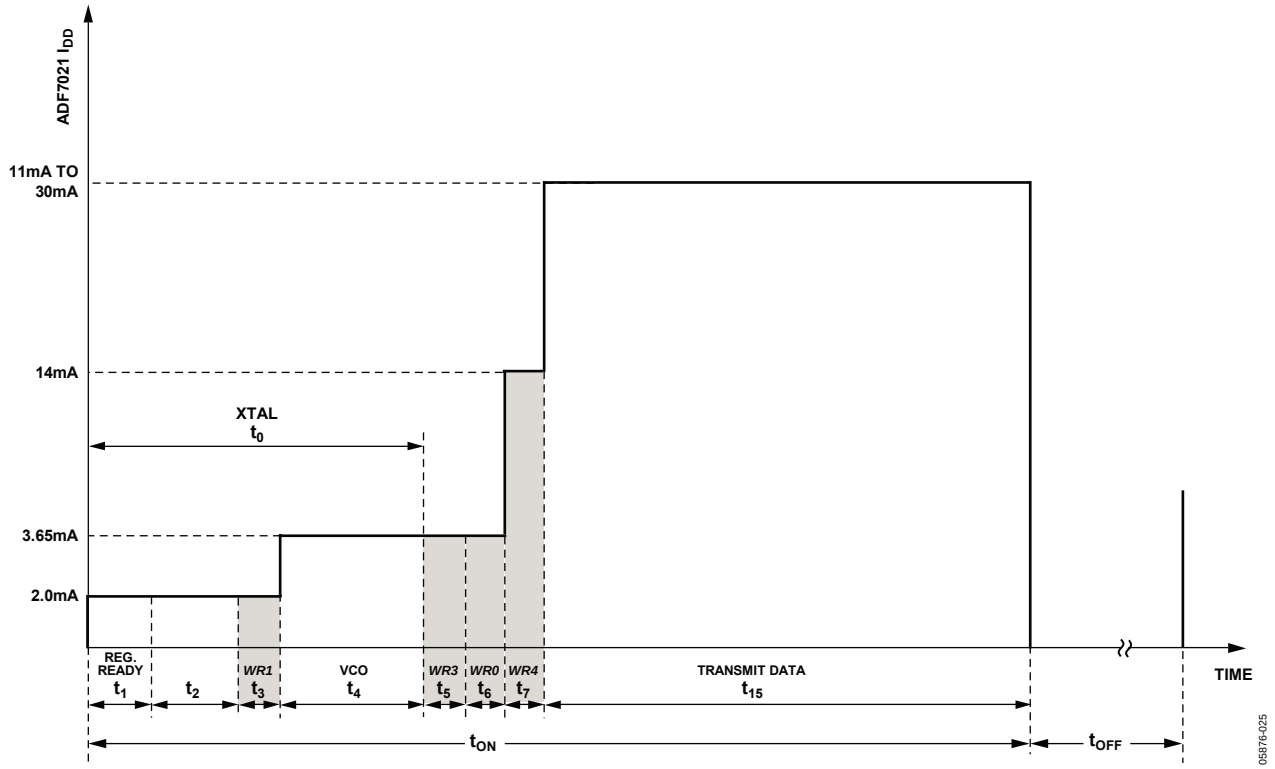


Figure 27. Tx Programming Sequence and Timing Diagram

Table 14. Power-Up Sequence Description

Parameter	Value	Description/Notes	Signal to Monitor
T_0	2 ms typ	Crystal starts power-up after CE is brought high. This typically depends on the specified crystal type and load capacitance.	CLKOUT
T_1	10 µs	Time for regulator to power up. The serial interface can be written to after this time.	MUXOUT
T_2	1ms typ	Variable delay that depends on XTAL settling and VCO settling. Should be set so that VCO and XTAL finish settling at the same time, thus minimizing current consumption.	
T_3, T_5,T_6, T_7, T_9, T_{10}	32 × 1/SPI_CLK	Time to write to a single register. Maximum SPI_CLK is 25 MHz.	
T_4	1 ms	The VCO can power up in parallel with the crystal. This depends on the CVCO capacitance value used. A value of 22 nF is recommended as a trade-off between phase noise performance and power-up time.	CVCO pin
T_8	3.2 ms	IF filter coarse and fine calibration times. A coarse calibration typically takes 200 µs, while a fine calibration typically takes 3 ms (see the settings in the Register 7—Readback Setup Register section).	
T_{11}	150 µs	This depends on the number of gain changes the AGC loop needs to cycle through and AGC settings programmed. This is described in more detail in the AGC Information and Timing section.	Analog RSSI on TEST_A pin (available by writing 0x0B00 000F)
T_{12}	5 × Bit_Period	This is the time for the clock and data recovery circuit to settle. This typically requires 5-bit transitions to acquire sync and is usually covered by the preamble.	
T_{13}	20 × Bit_Period	This is the time for the automatic frequency control circuit to settle. This typically requires 16-bit transitions to acquire lock and is usually covered by an appropriate length preamble.	
T_{14}, T_{15}	Packet length	Number of bits in payload by the bit period.	

INTERFACING TO MICROCONTROLLER/DSP

Low level device drivers are available for interfacing to the ADF7021, such as the ADuC84x microcontroller parts, or the Blackfin® ADSP-BF53x DSPs. Use the hardware connections shown in Figure 28 and Figure 29.

UART Mode

If a data synchronization clock is not required, the DATA_CLK|TxDATA pin can be configured to input transmit data in transmit mode. In receive mode, the receive data is available on the DATA_I/O|RxDATA pin. This allows a UART to be easily interfaced to the part, with dedicated pins for transmitted and received data, as shown in Figure 30. To enable this UART interface mode, set Bit R0_DB28 high.

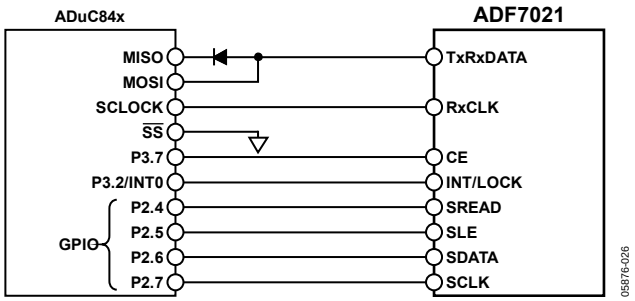


Figure 28. ADuC84x to ADF7021 Connection Diagram

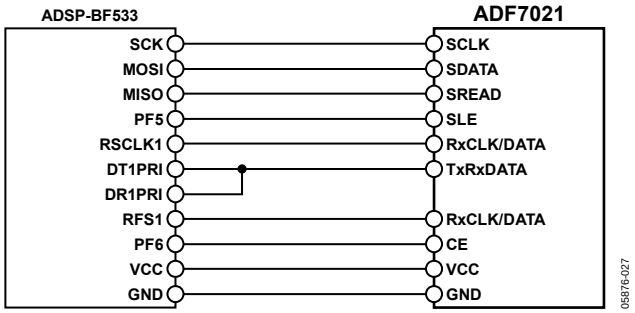


Figure 29. ADSP-BF533 to ADF7021 Connection Diagram

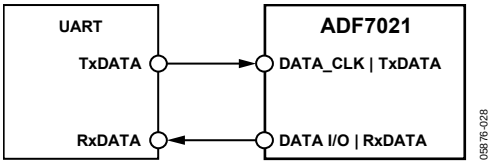


Figure 30. UART to ADF7021 Connection Diagram

SERIAL INTERFACE

The serial interface allows the user to program the 16, 32-bit registers using a 3-wire interface (SCLK, SDATA, and SLE). It consists of a level shifter, 32-bit shift register, and 16 latches. Signals should be CMOS-compatible. The serial interface is powered by the regulator, and, therefore, is inactive when CE is low.

Data is clocked into the register, MSB first, on the rising edge of each clock (SCLK). Data is transferred to one of 16 latches on the rising edge of SLE. The destination latch is determined by the value of the four control bits (C4 to C1). These are the bottom 4 LSBs, DB3 to DB0, as shown in Figure 2. Data can also be read back on the SREAD pin.

READBACK FORMAT

The readback operation is initiated by writing a valid control word to the readback register and setting the readback-enable bit (R7_DB8 = 1). The readback can begin after the control word has been latched with the SLE signal. SLE must be kept high while the data is being read out. Each active edge at the SCLK pin clocks the readback word out successively at the SREAD pin, as shown in Figure 31, starting with the MSB first. The data appearing at the first clock cycle following the latch operation must be ignored.

AFC Readback

The AFC readback is valid only during the reception of FSK signals with either the linear or correlator demodulator active. The AFC readback value is formatted as a signed 16-bit integer comprised of Bit RV1 to Bit RV16, and is scaled according to the following formula:

$$FREQ\_RB\ [\text{Hz}] = (AFC\_READBACK \times DEMOD\_CLK)/2^{18}$$

In the absence of frequency errors, the FREQ_RB value is equal to the IF frequency of 100 kHz. Note that for the AFC readback to yield a valid result, the down converted input signal must not fall outside the bandwidth of the analog IF filter. At low-input signal levels, the variation in the readback value can be improved by averaging.

RSSI Readback

The RSSI readback operation yields valid results in Rx mode with ASK or FSK signals. The format of the readback word is shown in Figure 31. It is comprised of the RSSI level information (Bit RV1 to Bit RV7), the current filter gain (FG1, FG2), and the current LNA gain (LG1, LG2) setting. The filter and LNA gain are coded in accordance with the definitions in Register 9. With the reception of ASK modulated signals, averaging of the measured RSSI values improves accuracy. The input power can be calculated from the RSSI readback value as outlined in the RSSI/AGC.

Battery Voltage ADCIN/Temperature Sensor Readback

The battery voltage is measured at Pin VDD4. The readback information is contained in Bit RV1 to Bit RV7. This also applies for the readback of the voltage at the ADCIN pin and the temperature sensor. From the readback information, the battery or ADCIN voltage can be determined using

$$V_{BATTERY} = (Battery\_Voltage\_Readback)/21.1$$

$$V_{ADCIN} = (ADCIN\_Voltage\_Readback)/42.1$$

Silicon Revision Readback

The silicon revision readback word is valid without setting any other registers, especially directly after power-up. The silicon revision word is coded with four quartets in BCD format. The product code (PC) is coded with three quartets extending from Bit RV5 to Bit RV16. The revision code (RV) is coded with one quartet extending from Bit RV1 to Bit RV4. The product code for the ADF7021 should read back as PC = 0x210. The current revision code should read as RC = 0x2.

Filter Calibration Readback

The filter calibration readback word is contained in Bit RV1 to Bit RV8, and is for diagnostic purposes only. Using the automatic filter calibration function (accessible through Register 5 and Register 6) is recommended. Before filter calibration is initiated, decimal 32 should be read back.

READBACK MODE	READBACK VALUE															
	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
AFC READBACK	RV16	RV15	RV14	RV13	RV12	RV11	RV10	RV9	RV8	RV7	RV6	RV5	RV4	RV3	RV2	RV1
RSSI READBACK	X	X	X	X	X	LG2	LG1	FG2	FG1	RV7	RV6	RV5	RV4	RV3	RV2	RV1
BATTERY VOLTAGE/ADCIN/ TEMP. SENSOR READBACK	X	X	X	X	X	X	X	X	X	RV7	RV6	RV5	RV4	RV3	RV2	RV1
SILICON REVISION	RV16	RV15	RV14	RV13	RV12	RV11	RV10	RV9	RV8	RV7	RV6	RV5	RV4	RV3	RV2	RV1
FILTER CAL READBACK	0	0	0	0	0	0	0	0	RV8	RV7	RV6	RV5	RV4	RV3	RV2	RV1

05876-029

Figure 31. Readback Value Table

REGISTER 0—N REGISTER

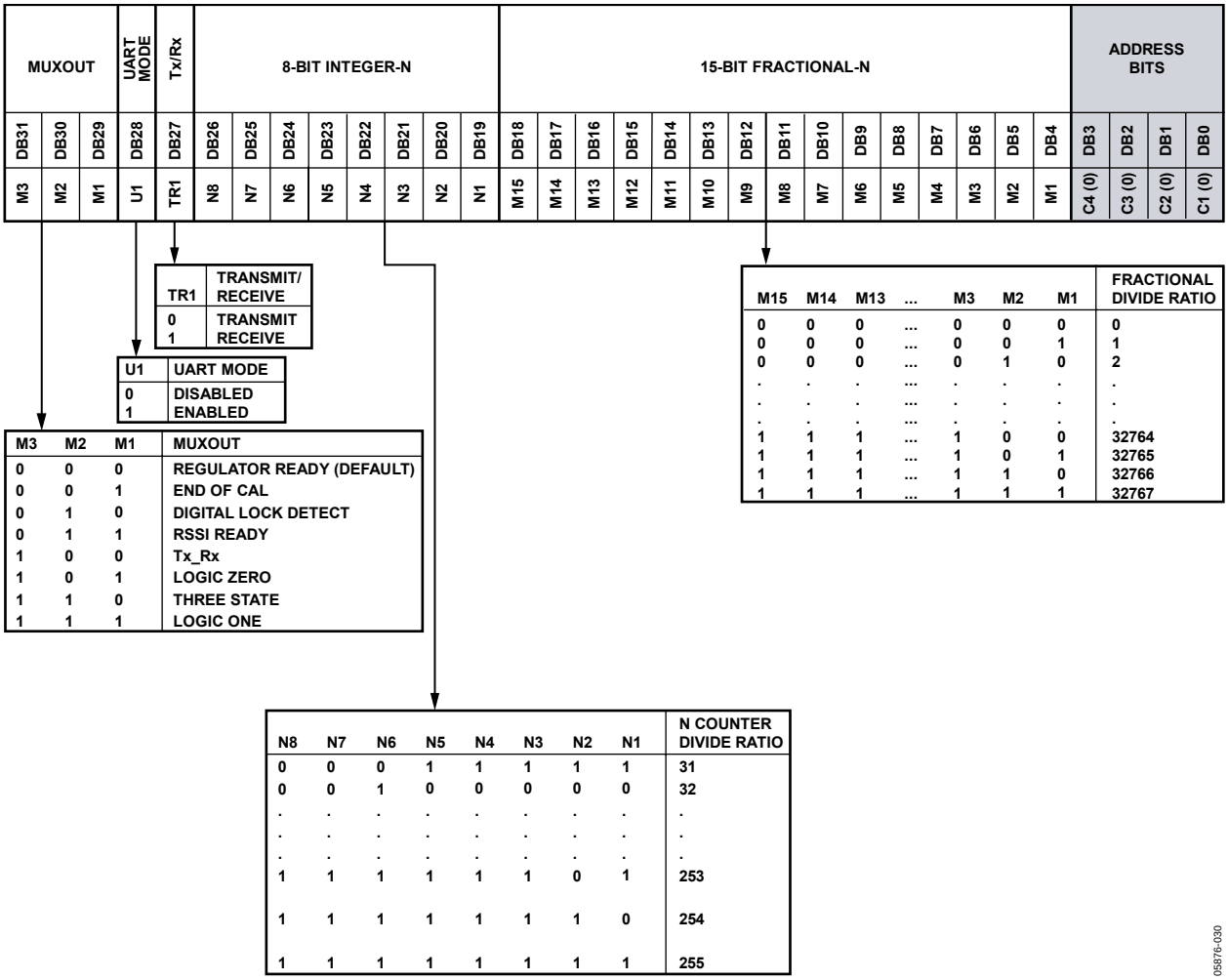


Figure 32.

Register 0—N Register Comments

- RF Output Frequency

  Direct output: $RF_{OUT} = PFD \times \left(Integer\_N + \frac{Fractional\_N}{2^{15}} \right)$

  Divide-by-2 selected: $RF_{OUT} = PFD \times 0.5 \times \left(Integer\_N + \frac{Fractional\_N}{2^{15}} \right)$

- In UART mode, the DATA CLK | TxDATA pin is used to input the Tx data. The Rx Data is available on the DATA I/O | RxDATA pin.
- MUXOUT

  END OF CAL (Active High): Indicates when a fine IF filter calibration has finished.

  DIGITAL LOCK DETECT (Active High): Indicates when the PLL has locked.

  RSSI READY (Active High): Indicates RSSI signal has settled and RSSI readback can be performed.

  Tx_Rx: Gives the status of Bit DB27 in this register. Can be used to control an external Tx/Rx switch.

REGISTER 1—VCO/OSCILLATOR REGISTER

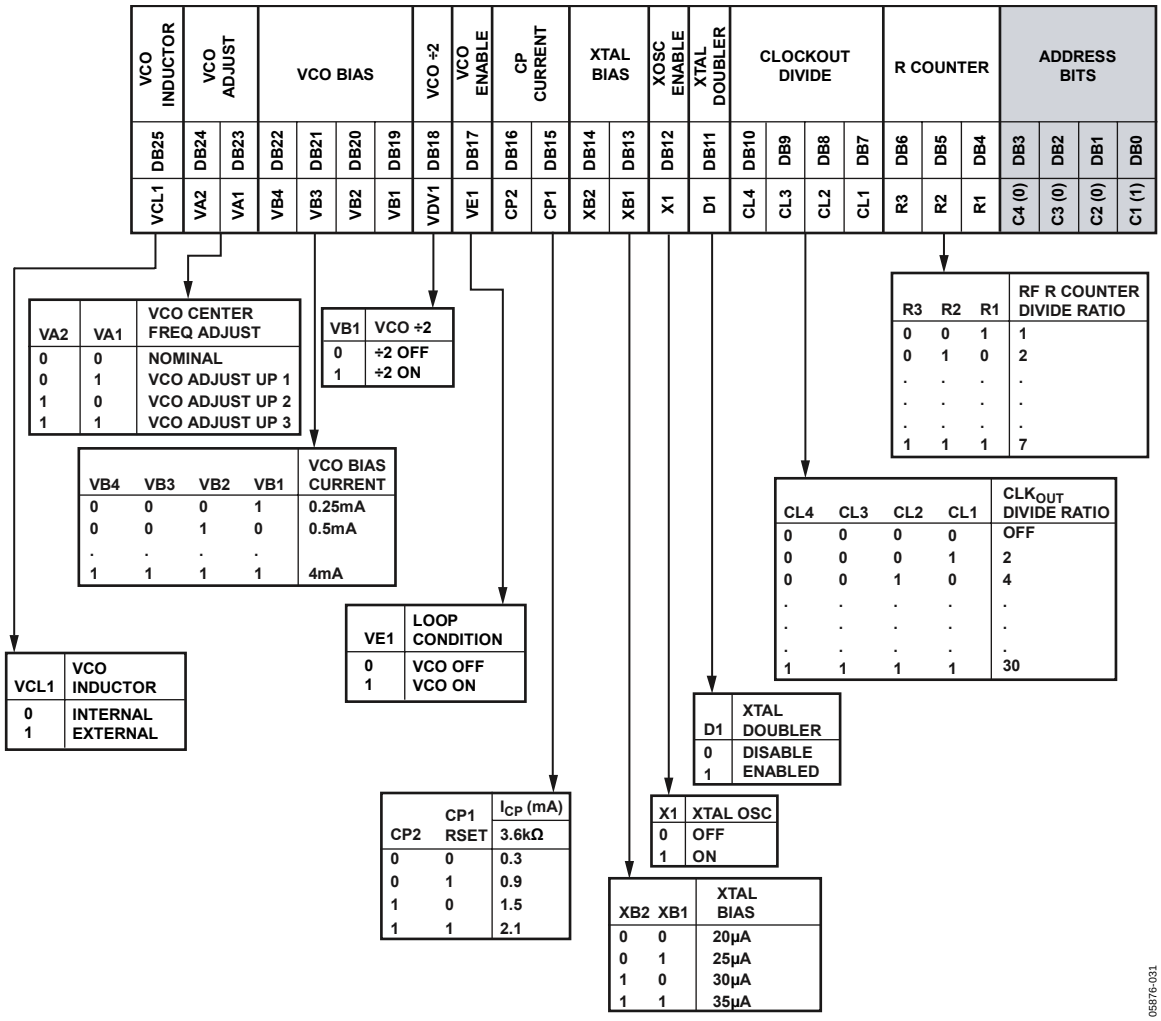


Figure 33.

Register 1—VCO/Oscillator Register N Comments

- R_DIVIDE and XTAL DOUBLER

  If XTAL DOUBLER = 0, $PFD = \frac{XTAL}{R\_DIVIDE}$

  If XTAL DOUBLER =1, $PFD = \frac{XTAL \times 2}{R\_DIVIDE}$

- CLOCKOUT is a divided-down version of the XTAL and is available on Pin 36 (CLKOUT).
- XOSC_ENABLE should be set high when using an external crystal. If using an external oscillator (such as TCXO, OCXO) with CMOS-level outputs into Pin OSC2, the XOSC enable should be set low.
- The VCO_ADJUST bits adjust the center of the VCO operating band. Each bit typically adjusts the VCO band up by 1% of the RF operating frequency (0.5% if divide-by-2 is enabled).
- Setting VCO_INDUCTOR to external allows the use of an external VCO tank inductor, which gives RF operating frequencies of 80 Hz to 650 MHz. If the internal inductor is being used for operation, this bit should be set low.

REGISTER 2—TRANSMIT MODULATION REGISTER

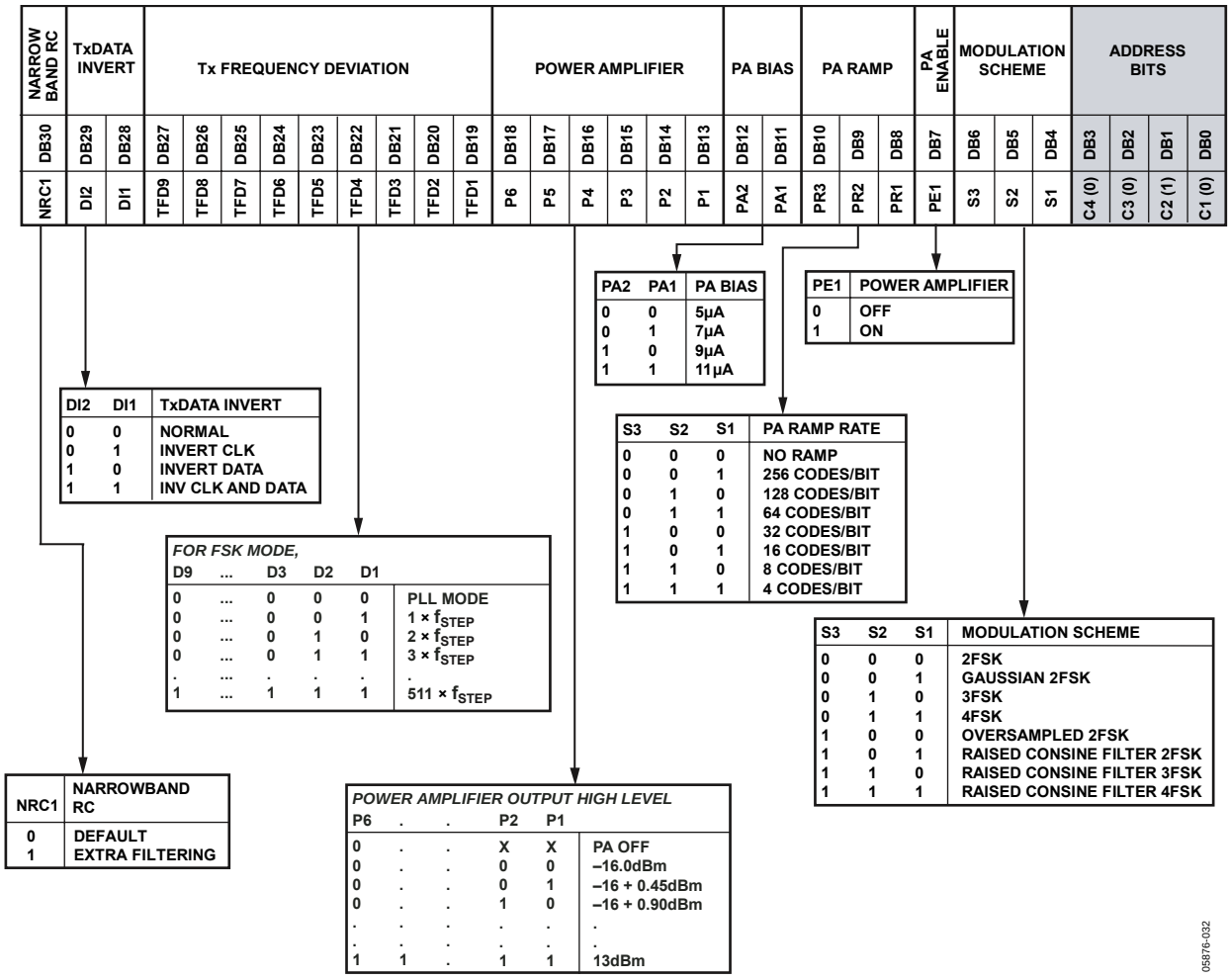


Figure 34.

Register 2—Transmit Modulation Register Comments

- 2FSK/3FSK/4FSK frequency deviation

  Direct output:

$$Frequency\ Deviation[\text{Hz}] = \frac{TX\_FREQUENCY\_DEVIATION \times PFD}{2^{16}}$$

  Divide-by-2 enabled:

$$Frequency\ Deviation[\text{Hz}] = 0.5 \times \frac{TX\_FREQUENCY\_DEVIATION \times PFD}{2^{16}}$$

  where: *TX_FREQUENCY_DEVIATION* is set by R2_DB[19:27] and *PFD* is the PFD frequency.

- In the case of 4FSK, there are tones at ±3 times the frequency deviation and at ±1 times the deviation.
- Oversampled 2FSK is sampled at 32 times the programmed data rate.
- The PA ramps at the programmed rate (R2_DB[8:10]) until it reaches its programmed level (R2_DB[13:18]).
- If the PA is enabled/disabled by the PA_Enable Bit (R2_DB7), it ramps up and down. If it is enabled/disabled by the Tx_Rx bit (R0_DB27), it ramps up and turns hard off.

REGISTER 3—TRANSMIT/RECEIVE CLOCK REGISTER

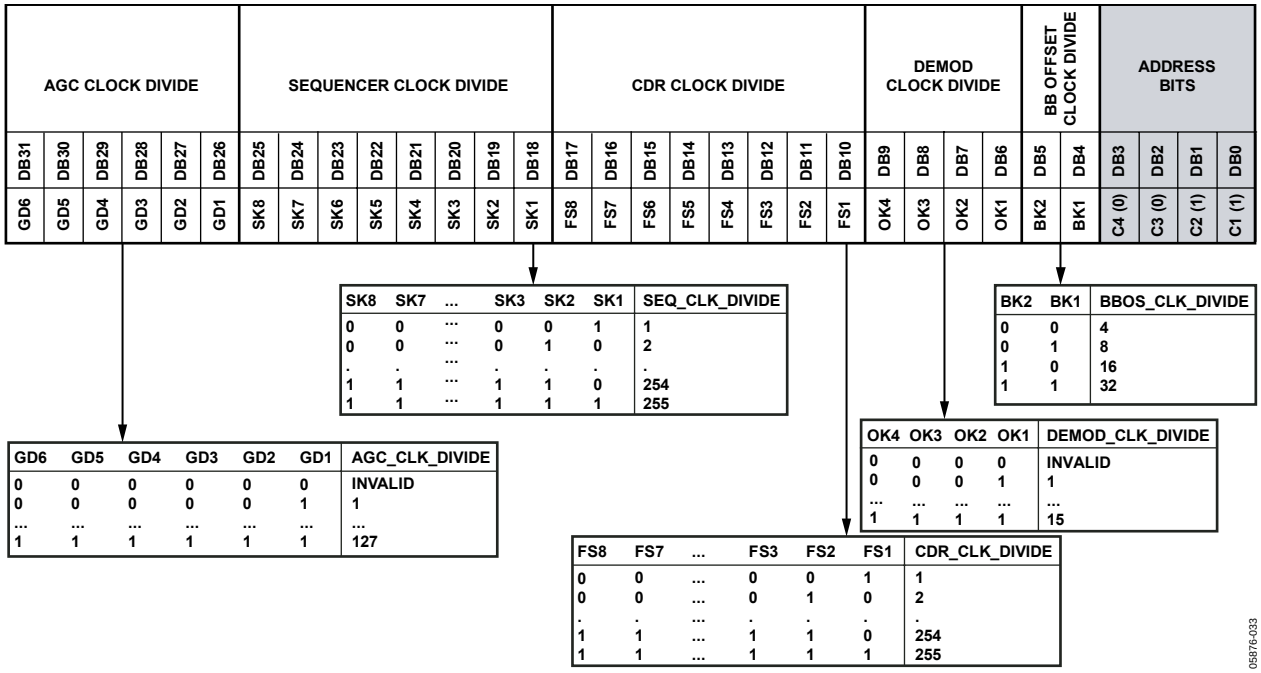


Figure 35.

Register 3—Transmit/Receive Clock Register Comments

- Baseband offset clock frequency (BBOS_CLK) must be greater than 1 MHz and less than 2 MHz, where:

$$BBOS\_CLK = \frac{XTAL}{BBOS\_CLK\_DIVIDE}$$

- Set the demodulator clock (DEMOD_CLK) such that 2 MHz ≤ *DEMOD_CLK* ≤ 15 MHz, where:

$$DEMOD\_CLK = \frac{XTAL}{DEMOD\_CLK\_DIVIDE}$$

- Data/clock recovery frequency (CDR _CLK) needs to be within 2% of (32 × data rate). The user should choose CDR_CLK frequency to be as high as possible without breaking this 2% constraint or breaking the DEMOD_CLK condition. This 2% constraint can also affect the choice of XTAL frequency, depending on the desired data rate.

$$CDR\_CLK = \frac{DEMOD\_CLK}{CDR\_CLOCK\_DIVIDE}$$

The sequencer clock (SEQ_CLK) supplies the clock to the digital receive block. It should be as close to 100 kHz as possible.

$$SEQ\_CLK = \frac{XTAL}{SEQUENCER\_CLOCK\_DIVIDE}$$

- The time allowed for each AGC step to settle is determined by the AGC update rate. It should be set close to 20 kHz.

$$AGC\,Update\,Rate\,[\mathrm{Hz}] = \frac{SEQ\_CLK}{AGC\_DIVIDE}$$

REGISTER 4—DEMODULATOR SETUP REGISTER

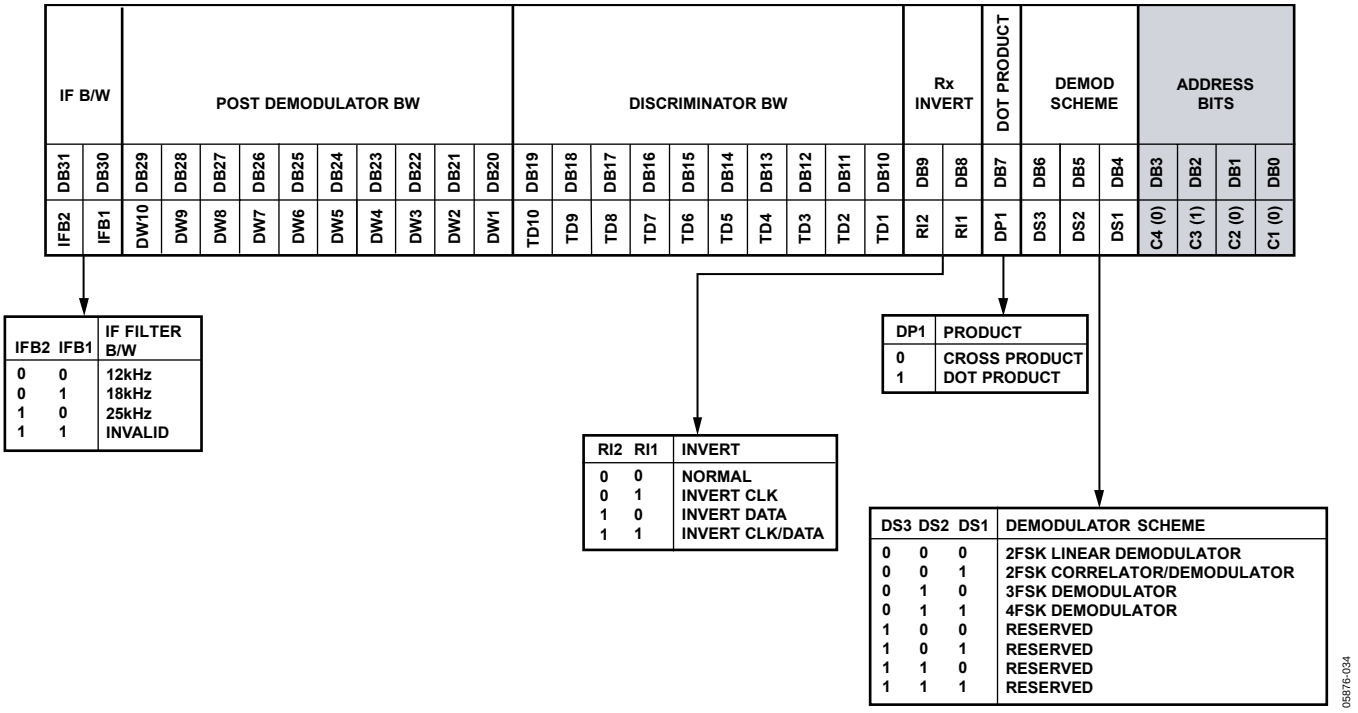


Figure 36.

Register 4—Demodulator Setup Register Comments

- $Discriminator\_BW = \frac{DEMOD\_CLK \times K}{400 \times 10^3}$

  where:

  $K = \frac{100 \times 10^3}{Frequency\ Deviation[\text{Hz}]}$

  Maximum value = 660.

- RX_INVERT(R4_DB[8:9]) and DOT_PRODUCT (R4_DB7) need to be set as outlined below in order to optimize the correlator demodulator. K is calculated using the previous formula and then rounded to the nearest integer.

K	K/2	Dot Product (R4_DB7)	Rx Invert (R4_DB[8:9])
Even	Even	0	00
Even	Odd	0	10

K	(K + 1)/2	Dot Product (R4_DB7)	Rx Invert (R4_DB[8:9])
Odd	Even	1	00
Odd	Odd	1	10

- $Post\_Demod\_BW = \frac{2^{11} \times \pi \times F_{CUTOFF}}{DEMOD\_CLK}$

where the cutoff frequency (F_{CUTOFF}) of the postdemodulator filter should typically be 0.75 times the data rate.

REGISTER 5—IF FILTER SETUP REGISTER

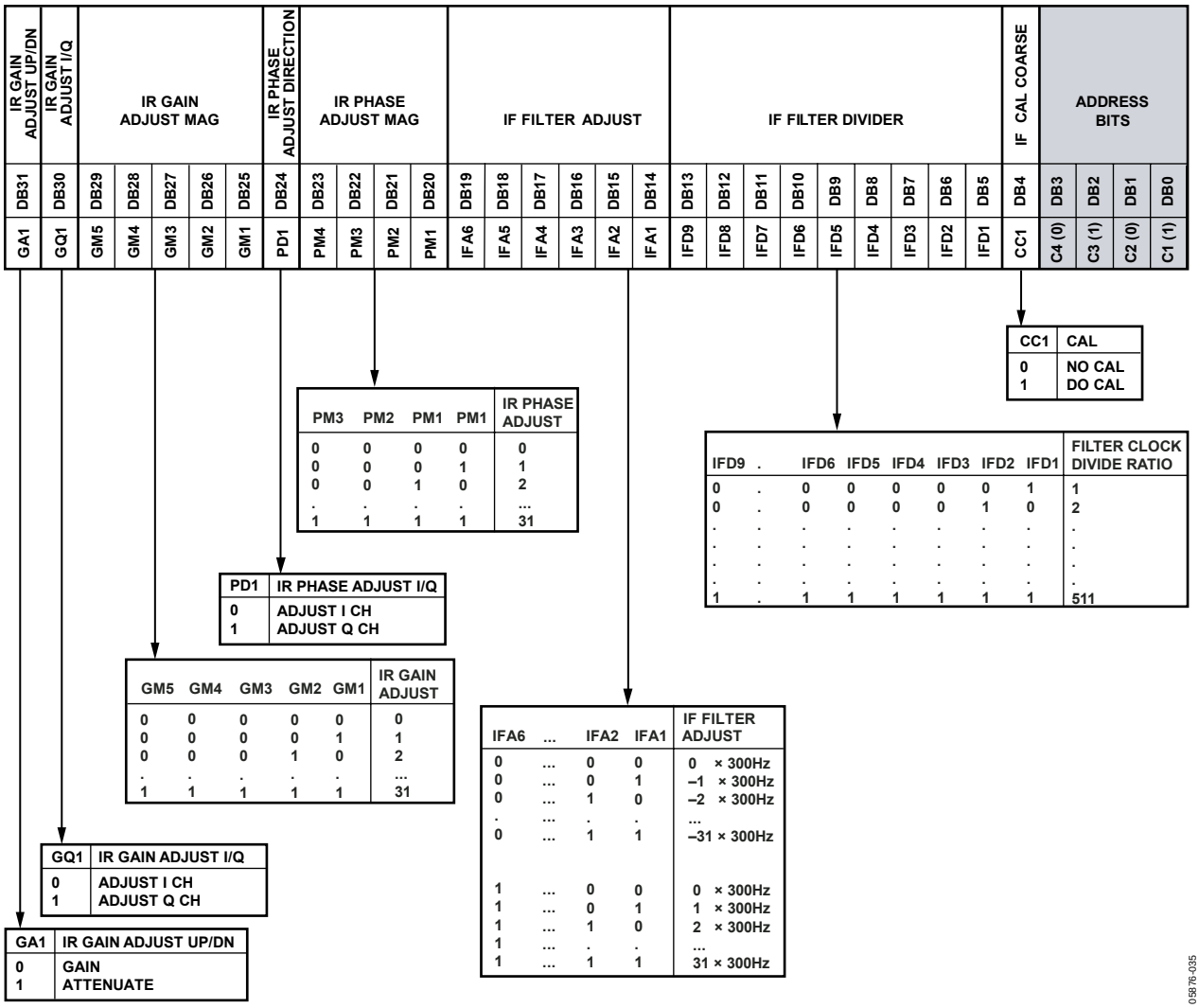


Figure 37.

Register 5—IF Filter Setup Register Comments

- A coarse IF filter calibration is performed when the Coarse Cal Bit (R5_DB4) is set. If the Fine Cal Bit (R6_DB4) in is set, a fine IF filter calibration is performed after the coarse calibration.
- Set IF_Filter_DIVIDE such that

$$\frac{XTAL}{IF\_FILTER\_DIVIDE} = 50\,\text{kHz}$$

- IF_FILTER_ADJUST allows the IF filter response to be manually adjusted in 300 Hz steps.

REGISTER 6—IF FINE CAL SETUP REGISTER

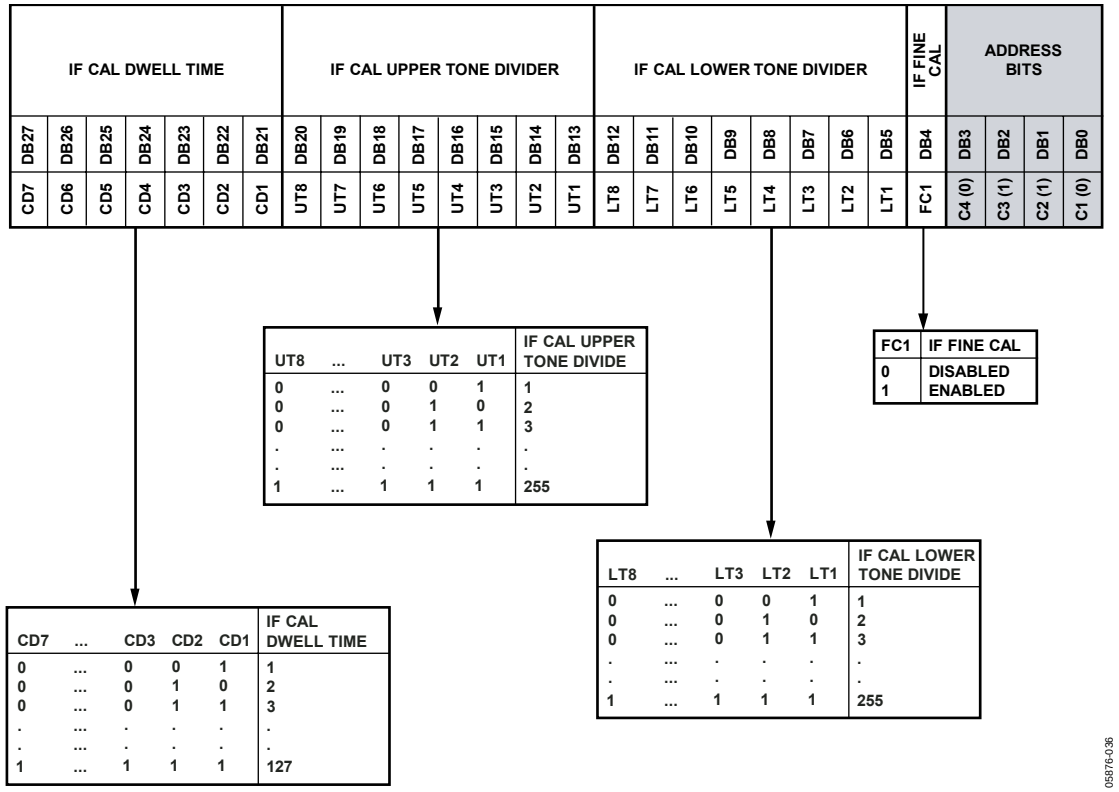


Figure 38.

Register 6—IF Fine Cal Setup Register Comments

- A fine IF filter calibration is set by enabling the IF_FINE_CAL Bit (DB4). A fine calibration is then carried out only when Register 5 is written to and Bit R5_DB4 is set.
- The IF upper and lower tones used during fine filter calibration should be set as follows:

$$\frac{XTAL}{IF\_CAL\_LOWER\_TONE\_DIVIDE} = 160\,\text{kHz}$$

$$\frac{XTAL}{IF\_CAL\_UPPER\_TONE\_DIVIDE} = 220\,\text{kHz}$$

- The IF tone calibration time is the amount of time that is spent at an IF calibration tone. It is dependent upon the sequencer clock. It is recommended to have the IF_CAL_DWELL_TIME be at least 300 µs.

$$IF\ Tone\ Calibration\ Time = \frac{IF\_CAL\_DWELL}{SEQ\_CLK}$$

The total time for a fine IF filter calibration is = *IF Tone Calibration Time* × 10.

REGISTER 7—READBACK SETUP REGISTER

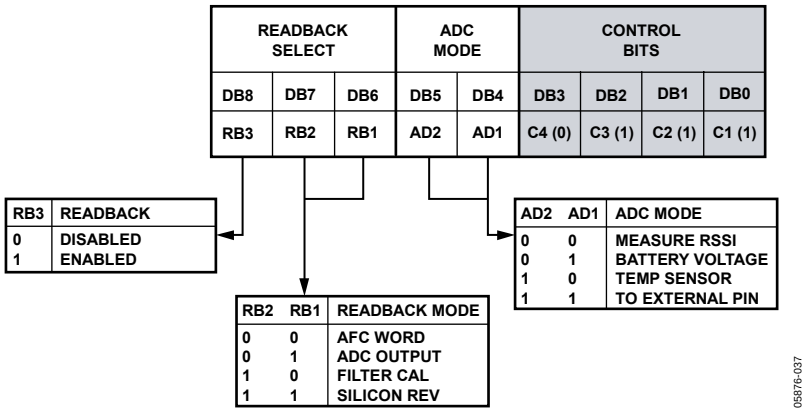


Figure 39.

Register 7—Readback Setup Register Comments

- Readback of the measured RSSI value is valid only in Rx mode. To enable readback of the battery voltage, the temperature sensor, or the voltage at the external pin in Rx mode, users need to disable AGC function in Register 9. To read back these parameters in Tx mode, first power up the ADC using Register 8, as this is off by default in Tx mode to save power. This is the recommended method of using the battery readback function, as most configurations typically require AGC.
- AFC readback:

  $FREQ\_RB$ [Hz] = ($AFC\_READBACK \times DEMOD\_CLK$)/$2^{18}$
- $V_{BATTERY}$ = *Battery_Voltage_Readback*/21.1
- V_{ADCIN} = *ADCIN_Voltage_Readback*/42.1
- See the Readback Format section for more information.

REGISTER 8—POWER DOWN TEST REGISTER

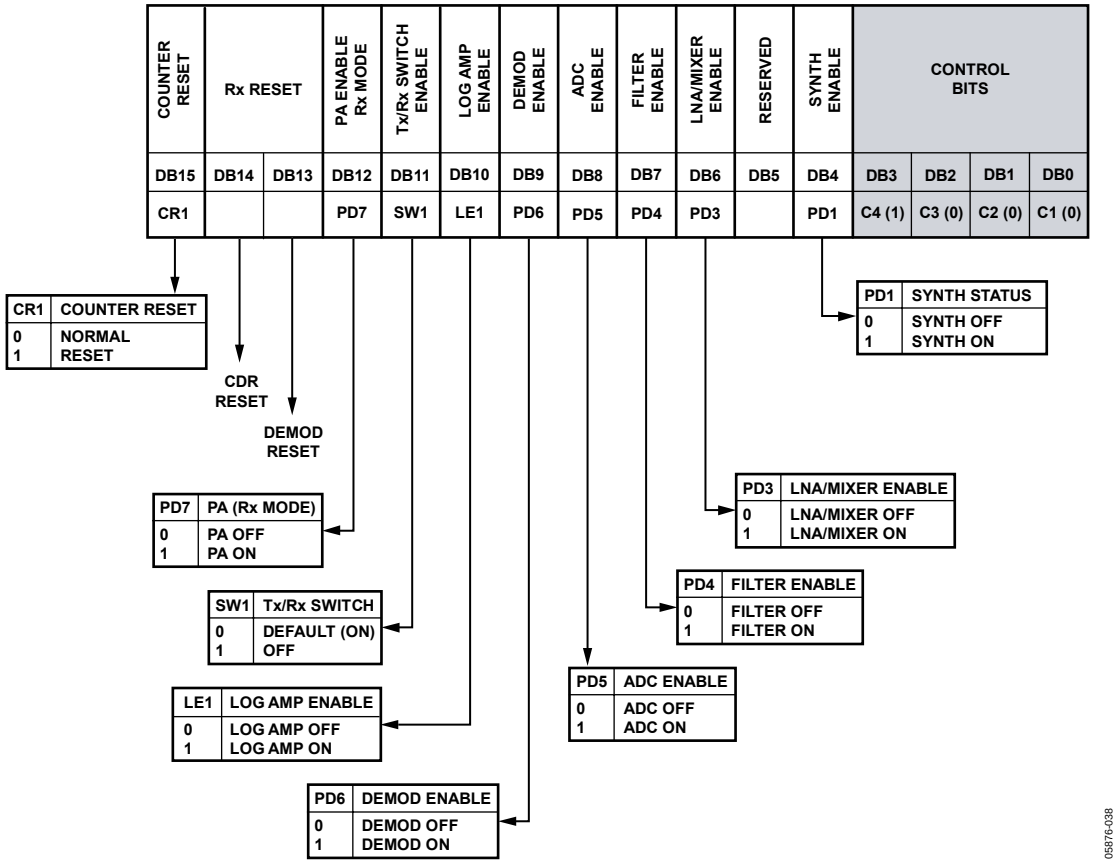


Figure 40.

Register 8—Power Down Test Register Comments

- It is not necessary to write to this register under normal operating conditions.
- For a combined LNA/PA matching network, Bit R8_DB11 should always be set to 0, which enables the internal Tx_Rx switch. This is the power-up default condition.

REGISTER 9—AGC REGISTER

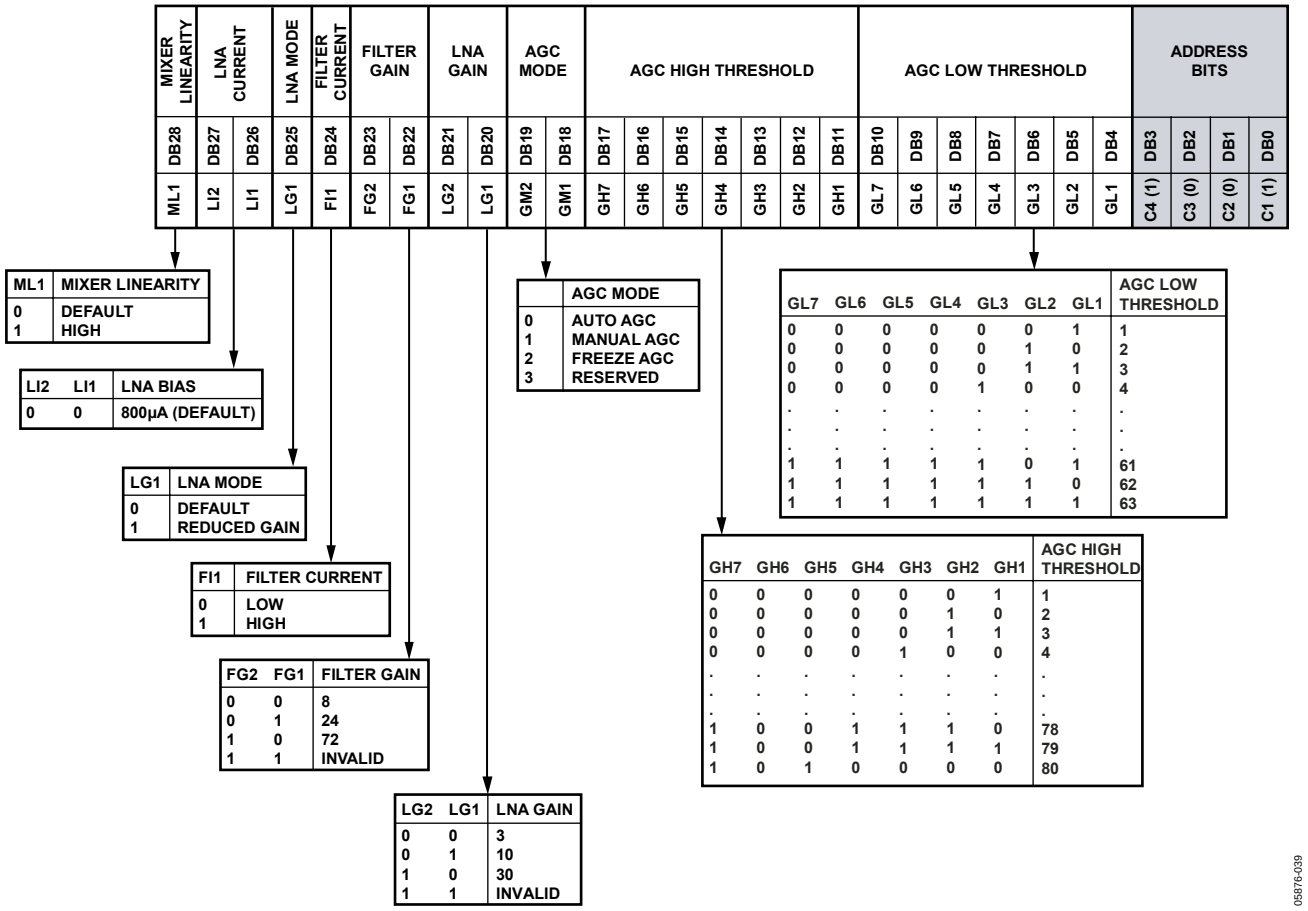
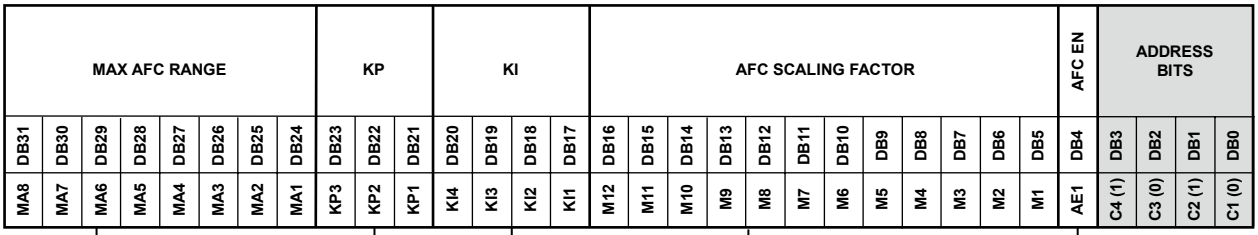


Figure 41.

Register 9—AGC Register Comments

- Default AGC_LOW_THRESHOLD = 30, default AGC_HIGH_THRESHOLD = 70. See the RSSI/AGC section for details.
- AGC high and low settings must be more than 30 apart to ensure correct operation.
- LNA gain of 30 is available only if LNA mode, R9_DB25, is set to zero.

REGISTER 10—AFC REGISTER



KP3	KP2	KP1	KP
0	0	0	2^0
0	0	1	2^1
.	.	.	...
1	1	1	2^7

KI4	KI3	KI2	KI1	KI
0	0	0	0	2^0
0	0	0	1	2^1
.	.	.	.	...
1	1	1	1	2^15

AE1	AFC ENABLE
0	OFF
1	AFC ON

MA8	...	MA3	MA2	MA1	MAX AFC RANGE
0	...	0	0	1	1
0	...	0	1	0	2
0	...	0	1	1	3
0	...	1	0	0	4
.	...	.	.	.	.
.	...	.	.	.	.
.	...	.	.	.	.
1	...	1	0	1	253
1	...	1	1	0	254
1	...	1	1	1	255

M12	...	M3	M2	M1	AFC SCALING FACTOR
0	...	0	0	1	1
0	...	0	1	0	2
0	...	0	1	1	3
0	...	1	0	0	4
.	...	.	.	.	.
.	...	.	.	.	.
.	...	.	.	.	.
1	...	1	0	1	4093
1	...	1	1	0	4094
1	...	1	1	1	4095

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Figure 42.

Register 10—AFC Register Comments

- AFC scaling factor:

$$AFC\_SCALING\_FACTOR = ROUND\left(\frac{2^{24} \times 500}{XTAL}\right)$$

- The recommended settings for KI and KP are given below. Note that these settings affect the AFC settling time and AFC accuracy.

  $KI > 6$ and $KP < 7$

- Maximum AFC pull-in range:

  $AFC\ Pull-in\ Range = MAX\_AFC\_RANGE \times 500\ \text{Hz}$

- Signals that are within the AFC pull-in range but outside the IF filter bandwidth are attenuated by the IF filter. As a result, the signals may be below the sensitivity point of the receiver, and therefore, not detectable by the AFC. In this case, it is best to scan bandwidths that are equal to the IF filter bandwidth.

REGISTER 11—SYNC WORD DETECT REGISTER

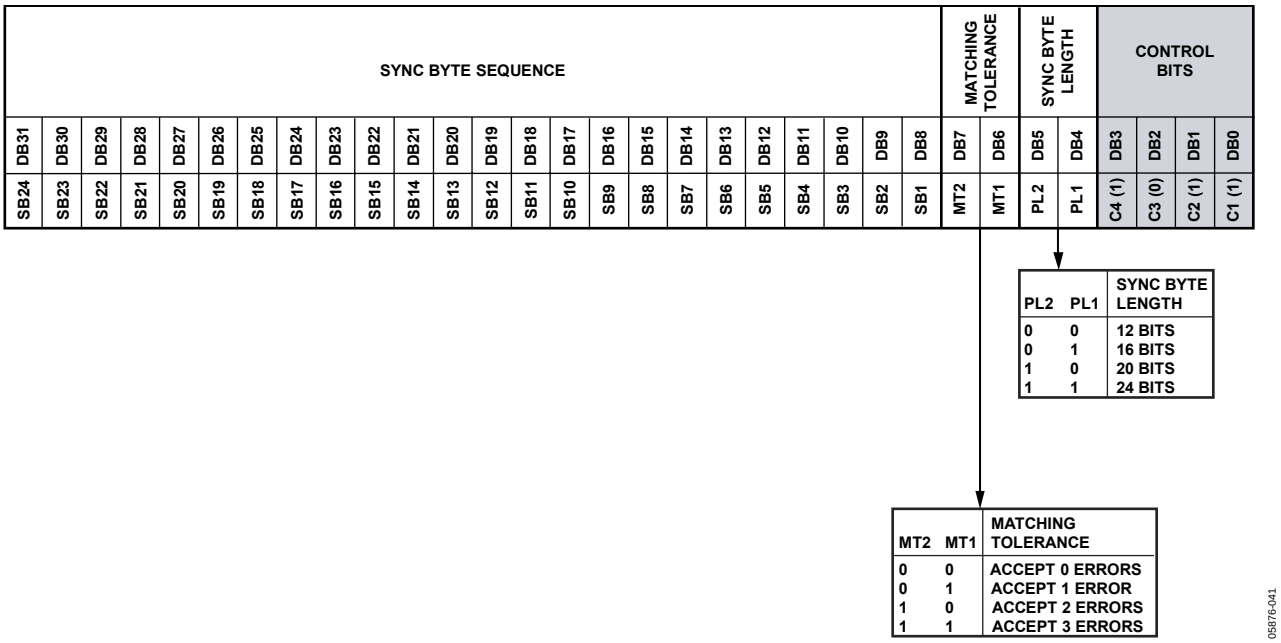

Figure 43.

REGISTER 12—SWD/THRESHOLD SETUP REGISTER

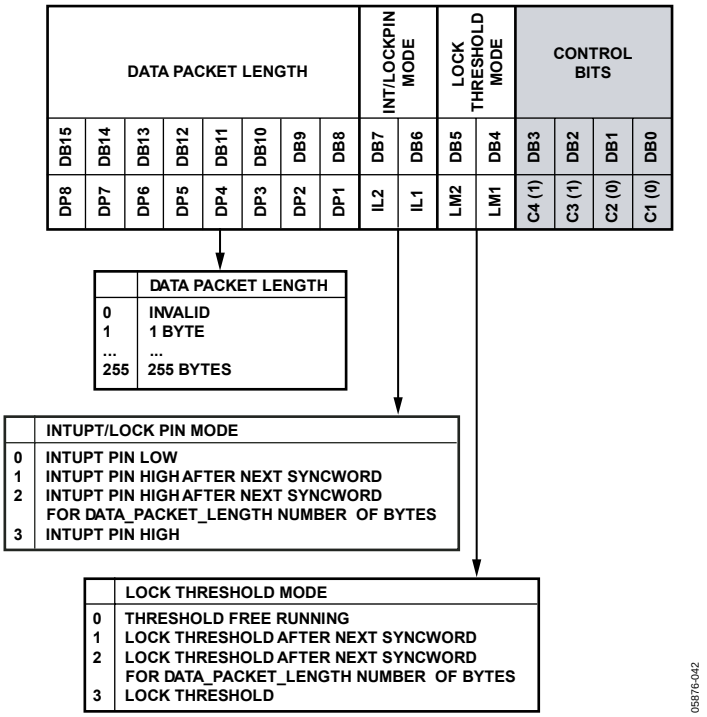

Figure 44.

Register 12—SWD/Threshold Setup Register Notes

- Lock threshold locks the threshold of the envelope detector. This has the effect of locking the slicer in linear demod and also locking the AFC and AGC loops.

REGISTER 13—3FSK DEMOD REGISTER

3FSK PREAMBLE TIME VALIDATE				3FSK CDR THRESHOLD							VITERBI PATH MEMORY		HANGUP RECOVERY	VITERBI ENABLE	3FSK/4FSK SLICER THRESHOLD							CONTROL BITS			
DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
PTV4	PTV3	PTV2	PTV1	VT7	VT6	VT5	VT4	VT3	VT2	VT1	VM2	VM1	HR1	VE1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	C4 (1)	C3 (1)	C2 (0)	C1 (1)

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Figure 45.

REGISTER 14—TEST-DAC REGISTER

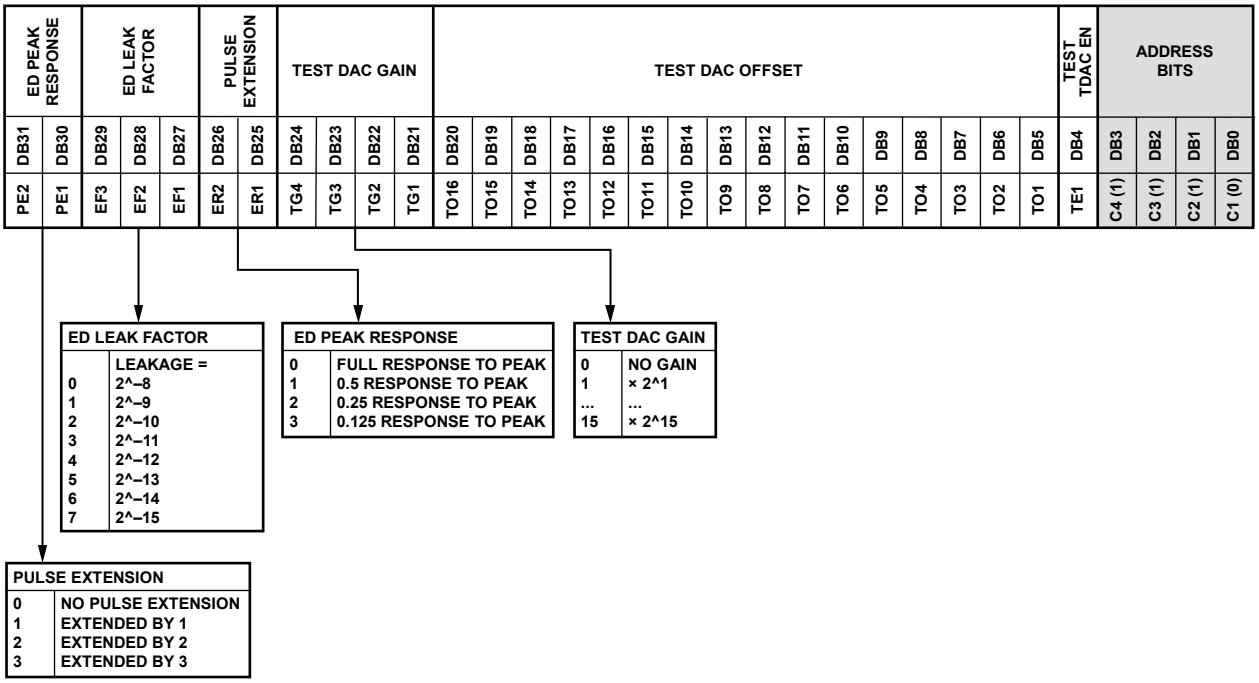

Figure 46.

Register 14—Test-DAC Register Comments

- The demod tuning parameters PULSE_EXTENSION, ED_LEAK_FACTOR, and ED_PEAK_RESPONSE can only be enabled by setting Bits R15_DB[4:7] to 0x9.

REGISTER 15—TEST MODE REGISTER

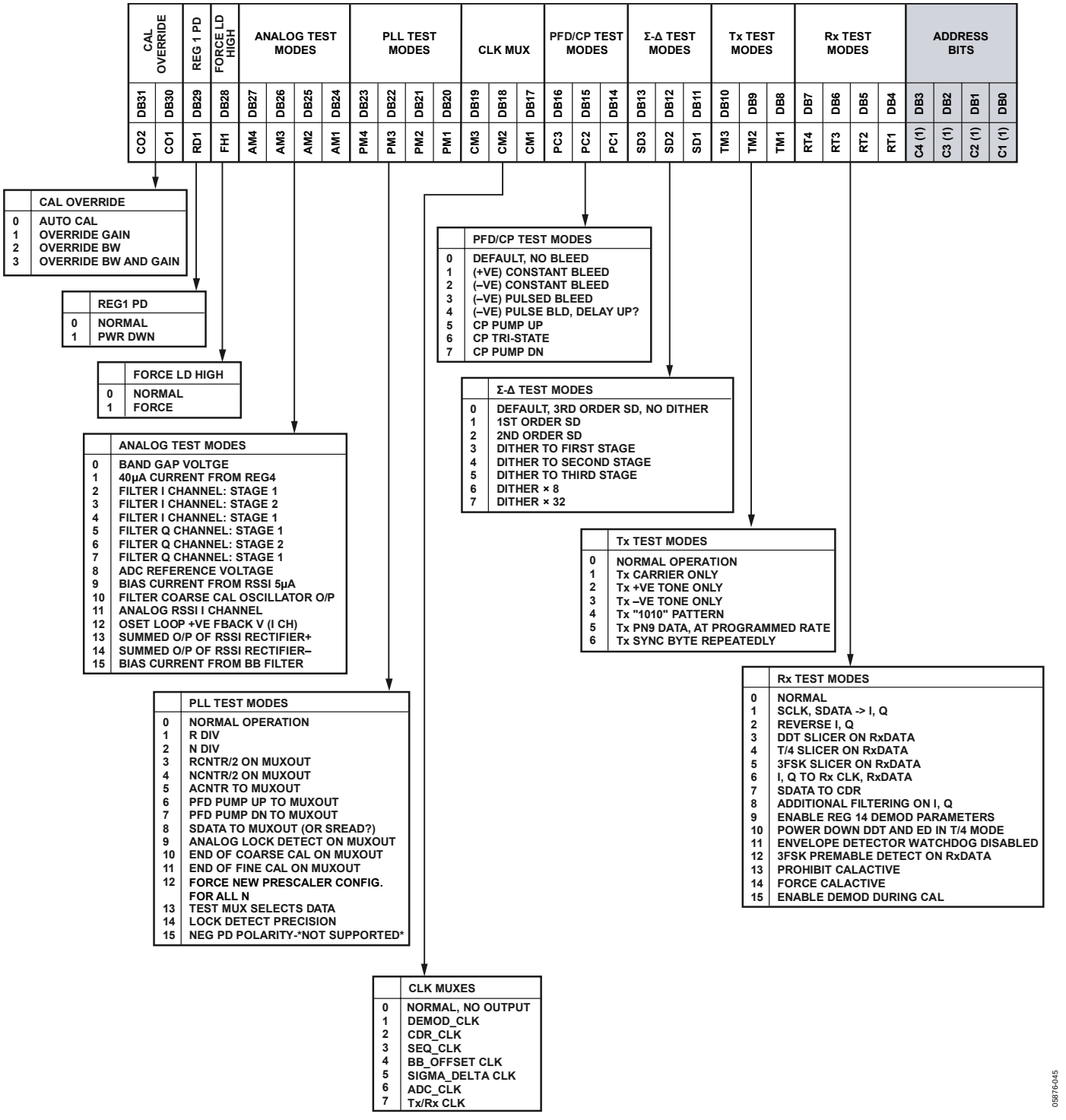

Figure 47.

Using the Test DAC on the ADF7021 to Implement Analog FM DEMOD and Measuring SNR

The test DAC allows the output of the postdemodulator filter for both the linear and correlator/demodulators (Figure 21 and Figure 22) to be viewed externally. It takes the 16-bit filter output and converts it to a high frequency, single-bit output using a second-order error feedback Σ-Δ converter. The output can be viewed on the $XCLK_{OUT}$ pin. This signal, when IF filtered appropriately, can then be used to

- Monitor the signals at the FSK postdemodulator filter output. This allows the demodulator output SNR to be measured. Eye diagrams can also be constructed of the received bit stream to measure the received signal quality.
- Provide analog FM demodulation.

While the correlators and filters are clocked by DEMOD_CLK, CDR_CLK clocks the test DAC. Note that although the test DAC functions in regular user mode, the best performance is achieved when the CDR_CLK is increased up to or above the frequency of DEMOD_CLK. The CDR block does not function when this condition exists.

Programming Register 14 enables the test DAC. Both the linear and correlator/demodulator outputs can be multiplexed into the DAC.

Register 14 allows a fixed offset term to be removed from the signal (to remove the IF component in the ddt case). It also has a signal gain term to allow the usage of the maximum dynamic range of the DAC.

OUTLINE DIMENSIONS

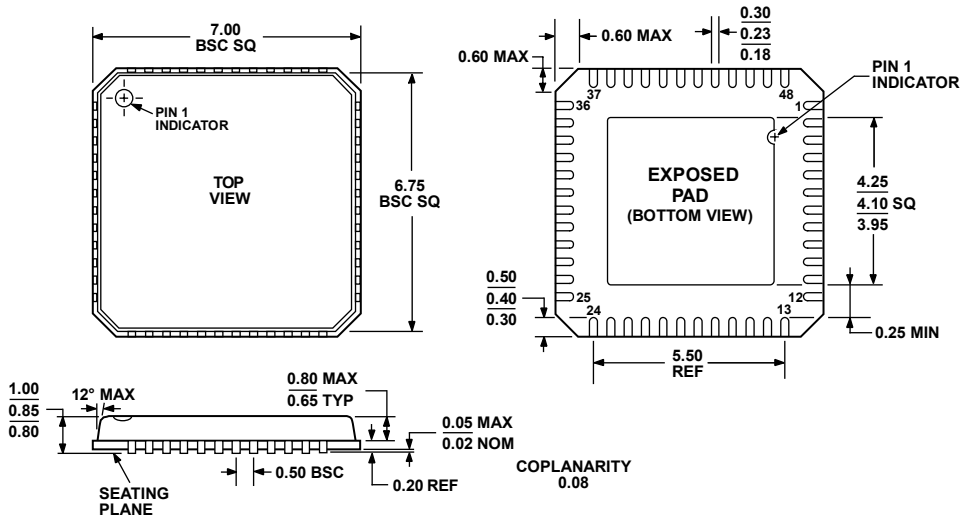

Figure 48. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 × 7 mm Body, Very Thin Quad
(CP-48-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF7021BCPZ[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-3
EVAL-ADF70XXMB		Control Mother Board	
EVAL-ADF70XXMB2		Evaluation Platform	
EVAL-ADF7021DB2		860 MHz to 870 MHz Daughter Board	
EVAL-ADF7021DB3		431 MHz to 470 MHz Daughter Board	

[1] Z = Pb-free part.