Low Power, Unity Gain, Fully Differential Amplifier and ADC Driver

Data Sheet **AD8476**

FEATURES

- Very low power
  - 330 µA supply current
- Extremely low harmonic distortion
  - −126 HD2 at 10 kHz
  - −128 HD3 at 10 kHz
- Fully differential or single-ended inputs/outputs
- Differential output designed to drive precision ADCs
  - Drives switched capacitor and Σ-Δ ADCs
  - Rail-to-rail outputs
- VOCM pin adjusts output common mode
- Robust overvoltage up to 18 V beyond supplies
- High performance
  - Suitable for driving 16-bit converter up to 250 kSPS
  - 39 nV/√Hz output noise
  - 1 ppm/°C gain drift maximum
  - 200 µV maximum output offset
  - 10 V/µs slew rate
  - 6 MHz bandwidth
- Single supply: 3 V to 18 V
- Dual supplies: ±1.5 V to ±9 V

APPLICATIONS

- ADC driver
- Differential instrumentation amplifier building block
- Single-ended-to-differential converter
- Battery-powered instruments

FUNCTIONAL BLOCK DIAGRAM

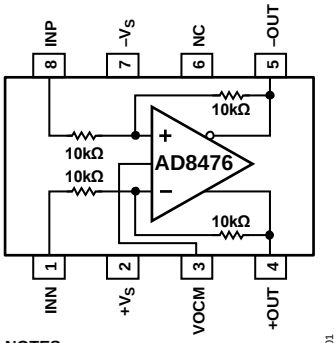

Figure 1. 8-Lead MSOP

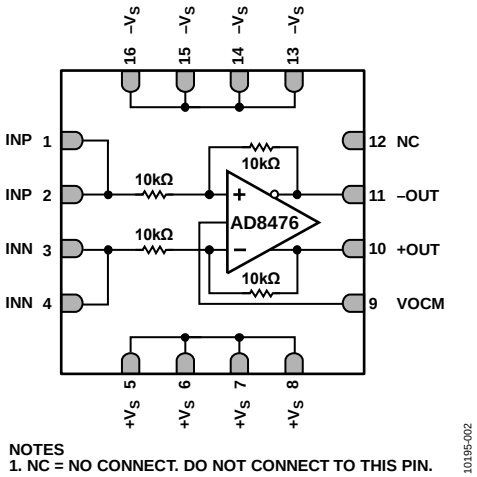

Figure 2. 16-Lead LFCSP

GENERAL DESCRIPTION

The AD8476 is a very low power, fully differential precision amplifier with integrated gain resistors for unity gain. It is an ideal choice for driving low power, high performance ADCs as a single-ended-to-differential or differential-to-differential amplifier. It provides a precision gain of 1, common-mode level shifting, low temperature drift, and rail-to-rail outputs for maximum dynamic range.

The AD8476 also provides overvoltage protection from large industrial input voltages up to ±23 V while operating on a dual 5 V supply. Power dissipation on a single 5 V supply is only 1.5 mW.

The AD8476 works well with SAR, Σ-Δ, and pipeline converters. The high current output stage of the part allows it to drive the switched capacitor front-end circuits of many ADCs with minimal error.

Unlike many differential drivers on the market, the AD8476 is a high precision amplifier. With 200 µV maximum output offset, 39 nV/√Hz noise, and −102 dB THD + N at 10 kHz, the AD8476 pairs well with low power, high accuracy converters.

Considering its low power consumption and high precision, the slew-enhanced AD8476 has excellent speed, settling to 16-bit precision for 250 kSPS acquisition times.

The AD8476 is available in space-saving 16-lead, 3 mm × 3 mm LFCSP and 8-lead MSOP packages. It is fully specified over the −40°C to +125°C temperature range.

Rev. B

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REVISION HISTORY

5/12—Rev. A to Rev. B

Added LFCSP Throughout ... 1
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Changed −3 dB Small Signal Bandwidth from 5 MHz to 6 MHz, Changed HD2 from −120 dB to −126 dB, and Changed HD3 from −122 dB to −128 dB, Table 1 ... 3
Changes to Figure 17 and Figure 19 ... 10
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Added Low Power ADC Driving Section ... 20
Updated Outline Dimensions ... 21
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11/11—Rev. 0 to Rev. A

Changes to Table 1 ... 3
Changes to Typical Performance Characteristics ... 7
Added Figure 39; Renumbered Sequentially ... 13
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10/11—Revision 0: Initial Version

SPECIFICATIONS

V_S = +5 to ±5 V, VOCM = midsupply, $V_{OUT} = V_{+OUT} - V_{-OUT}$, R_L = 2 kΩ differential, referred to output (RTO), T_A = 25°C, unless otherwise noted.

Table 1.

		B Grade			A Grade			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE								
−3 dB Small Signal Bandwidth	V_{OUT} = 200 mV p-p		6			6		MHz
−3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p		1			1		MHz
Slew Rate	V_{OUT} = 2 V step		10			10		V/µs
Settling Time to 0.01%	V_{OUT} = 2 V step		1.0			1.0		µs
Settling Time to 0.001%	V_{OUT} = 2 V step		1.6			1.6		µs
NOISE/DISTORTION[1]								
THD + N	f = 10 kHz, V_{OUT} = 2 V p-p, 22 kHz filter		−102			−102		dB
HD2	f = 10 kHz, V_{OUT} = 2 V p-p		−126			−126		dB
HD3	f = 10 kHz, V_{OUT} = 2 V p-p		−128			−128		dB
IMD3	f_1 = 95 kHz, f_2 = 105 kHz, V_{OUT} = 2 V p-p		−82			−82		dBc
Output Voltage Noise	f = 0.1 Hz to 10 Hz		6			6		µV p-p
Spectral Noise Density	f = 10 kHz		39			39		nV/√Hz
GAIN			1			1		V/V
Gain Error	$R_L = \infty$			0.02			0.04	%
Gain Drift	−40°C ≤ T_A ≤ +125°C			1			1	ppm/°C
Gain Nonlinearity	V_{OUT} = 4 V p-p		5			5		ppm
OFFSET AND CMRR								
Differential Offset[2]			50	200		50	500	µV
vs. Temperature	−40°C ≤ T_A ≤ +125°C			900			900	µV
Average TC	−40°C ≤ T_A ≤ +125°C		1	4		1	4	µV/°C
vs. Power Supply (PSRR)	V_S = ±2.5 V to ±9 V	90			90			dB
Common-Mode Offset[2]			50			50		µV
Common-Mode Rejection Ratio	$V_{IN,cm}$ = ±5 V	90			80			dB
INPUT CHARACTERISTICS								
Input Voltage Range[3]	Differential input	$-V_S + 0.05$		$+V_S - 0.05$	$-V_S + 0.05$		$+V_S - 0.05$	V
	Single-ended input	$2(-V_S + 0.05)$		$2(+V - 0.05)$	$2(-V_S + 0.05)$		$2(+V_S - 0.05)$	V
Impedance[4]	$V_{cm} = V_S/2$							
Single-Ended Input			13.3			13.3		kΩ
Differential Input			20			20		kΩ
Common-Mode Input			10			10		kΩ
OUTPUT CHARACTERISTICS								
Output Swing	V_S = +5 V	$-V_S + 0.125$		$+V_S - 0.14$	$-V_S + 0.125$		$+V_S - 0.14$	
	V_S = ±5 V	$-V_S + 0.155$		$+V_S - 0.18$	$-V_S + 0.155$		$+V_S - 0.18$	
Output Balance Error	$\Delta V_{OUT,cm}/\Delta V_{OUT,dm}$	90			80			dB
Output Impedance			0.1			0.1		Ω
Capacitive Load	Per output		20			20		pF
Short-Circuit Current Limit			35			35		mA
VOCM CHARACTERISTICS								
VOCM Input Voltage Range		$-V_S + 1$		$+V_S - 1$	$-V_S + 1$		$+V_S - 1$	V
VOCM Input Impedance			500			500		kΩ
VOCM Gain Error				0.05			0.05	%

Parameter	Test Conditions/Comments	B Grade			A Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY								
Specified Supply Voltage			±5			±5		V
Operating Supply Voltage Range		3		18	3		18	V
Supply Current	V_S = +5 V, T_A = 25°C		300	330		300	330	µA
	V_S = ±5 V, T_A = 25°C		330	380		330	380	µA
Over Temperature	−40°C ≤ T_A ≤ +125°C		400	500		400	500	µA
TEMPERATURE RANGE								
Specified Performance Range		−40		+125	−40		+125	°C

[1] Includes amplifier voltage and current noise, as well as noise of internal resistors.
[2] Includes input bias and offset current errors.
[3] The input voltage range is a function of the voltage supplies and ESD diodes.
[4] Internal resistors are trimmed to be ratio matched but have ±20% absolute accuracy.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±10 V
Maximum Voltage at Any Input Pin	$+V_S$ + 18 V
Minimum Voltage at Any Input Pin	$-V_S$ – 18 V
Storage Temperature Range	−65°C to +150°C
Specified Temperature Range	−40°C to +125°C
Package Glass Transition Temperature (T_G)	150°C
ESD (Human Body Model)	2500 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The θ_{JA} values in Table 3 assume a 4-layer JEDEC standard board with zero airflow.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead MSOP	209.0	°C/W
16-Lead LFCSP, 3 mm × 3 mm	78.5	°C/W

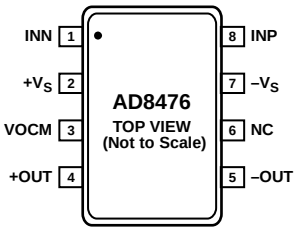
MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8476 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 150°C for an extended period may result in a loss of functionality.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



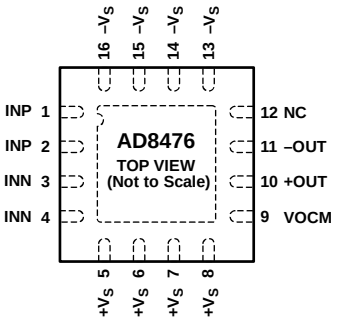
NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.

10195-004

Figure 3. 8-Lead MSOP Pin Configuration

Table 4. 8-Lead MSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INN	Negative Input .
2	$+V_S$	Positive Supply.
3	VOCM	Output Common-Mode Adjust.
4	+OUT	Noninverting Output.
5	–OUT	Inverting Output.
6	NC	This pin is not connected internally (see Figure 3).
7	$–V_S$	Negative Supply.
8	INP	Positive Input.



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.
2. SOLDER THE EXPOSED PADDLE ON THE BACK OF THE PACKAGE TO A GROUND PLANE.

10195-003

Figure 4. 16-Lead LFCSP Pin Configuration

Table 5. 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INP	Positive Input.
2	INP	Positive Input.
3	INN	Negative Input.
4	INN	Negative Input .
5	$+V_S$	Positive Supply.
6	$+V_S$	Positive Supply.
7	$+V_S$	Positive Supply.
8	$+V_S$	Positive Supply.
9	VOCM	Output Common-Mode Adjust.
10	+OUT	Noninverting Output.
11	−OUT	Inverting Output.
12	NC	This pin is not connected internally (see Figure 4).
13	$-V_S$	Negative Supply.
14	$-V_S$	Negative Supply.
15	$-V_S$	Negative Supply.
16	$-V_S$	Negative Supply.
	EPAD	Solder the exposed paddle on the back of the package to a ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = +5 V, G = 1, VOCM connected to 2.5 V, R_L = 2 kΩ differentially, T_A = 25°C, referred to output (RTO), unless otherwise noted.

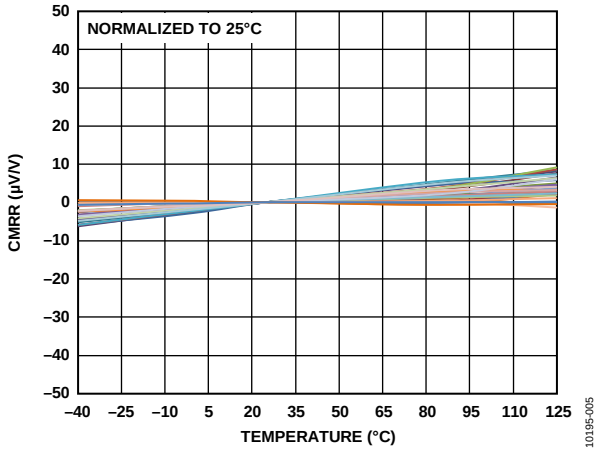


Figure 5. CMRR vs. Temperature

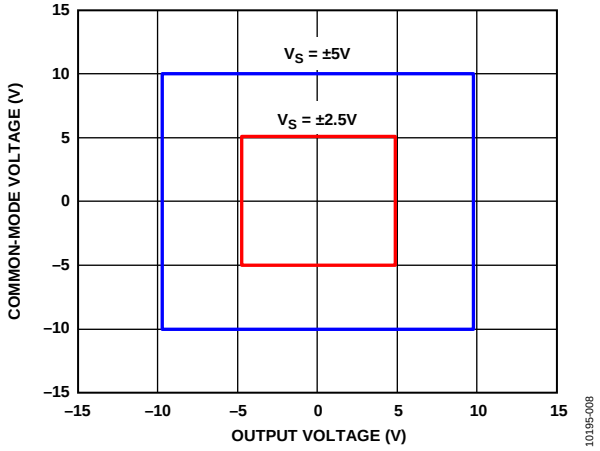


Figure 8. Input Common-Mode Voltage vs. Output Voltage, V_S = ±5 V and ±2.5 V

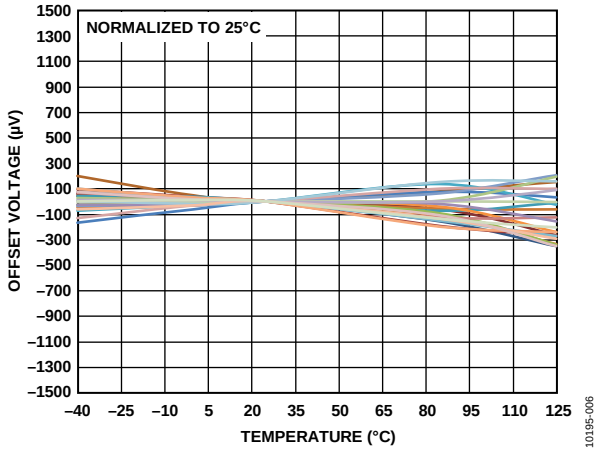


Figure 6. System Offset Temperature Drift

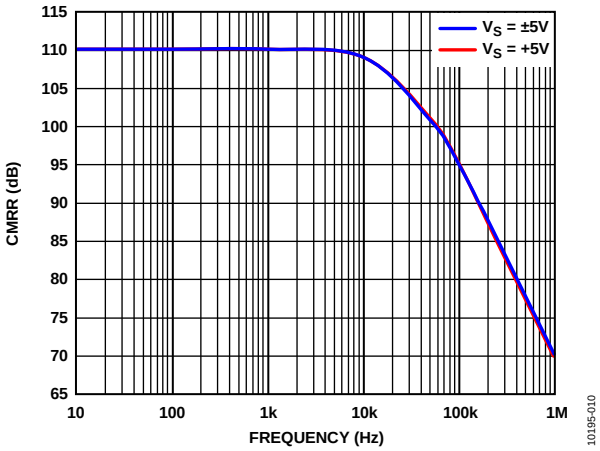


Figure 9. Common-Mode Rejection vs. Frequency

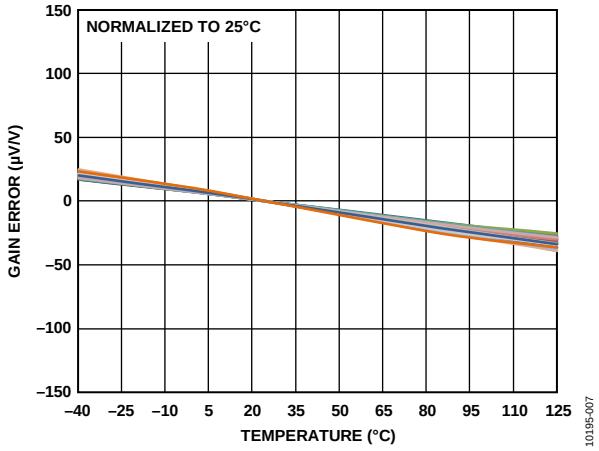


Figure 7. Gain Error vs. Temperature

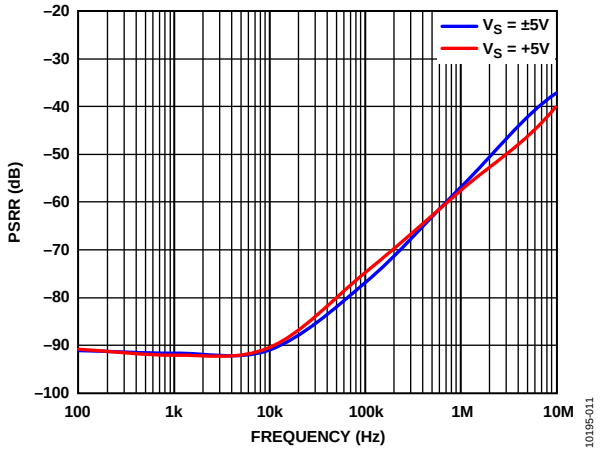


Figure 10. Power Supply Rejection vs. Frequency

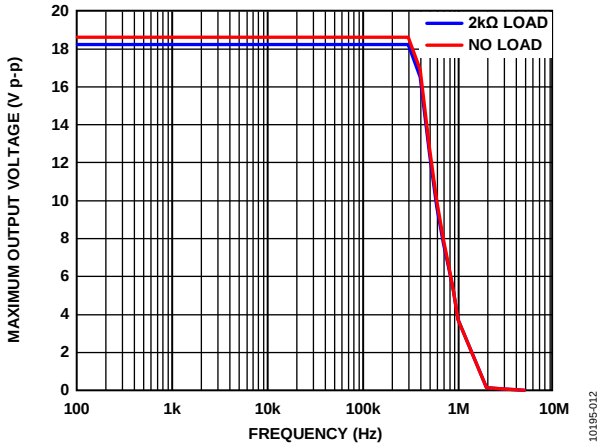


Figure 11. Maximum Output Voltage vs. Frequency

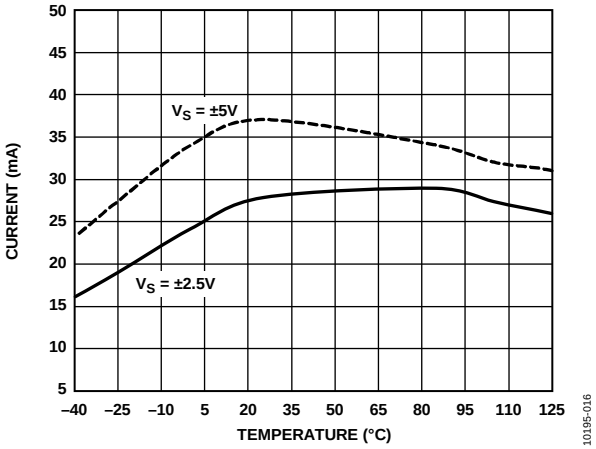


Figure 14. Short-Circuit Current vs. Temperature

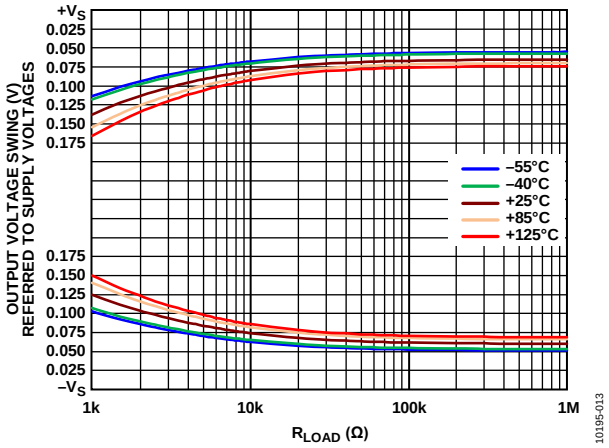


Figure 12. Output Voltage Swing vs. R_{LOAD} vs. Temperature, $V_S = \pm 5$ V

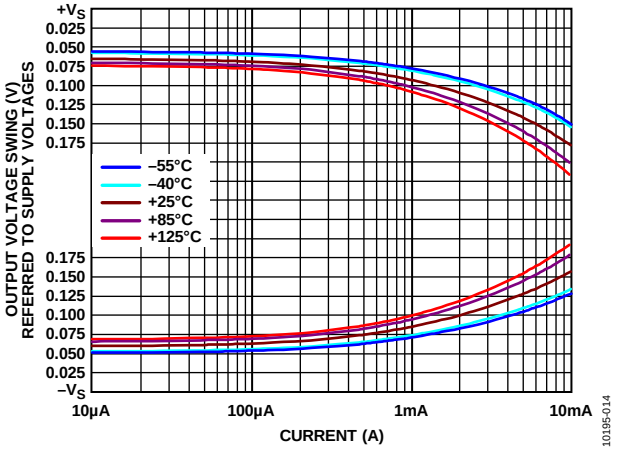


Figure 15. Output Voltage Swing vs. Load Current vs. Temperature, $V_S = \pm 5$ V

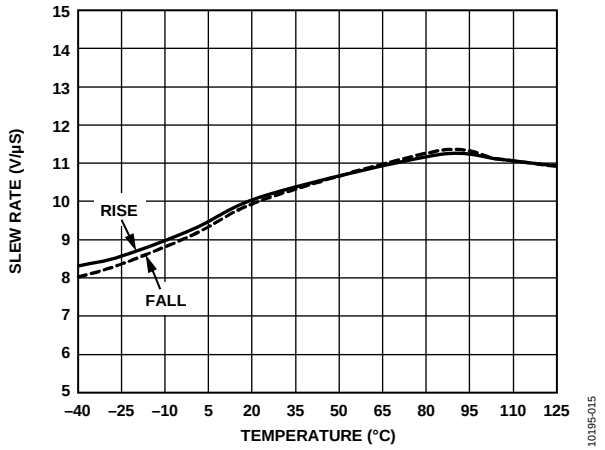


Figure 13. Slew Rate vs. Temperature

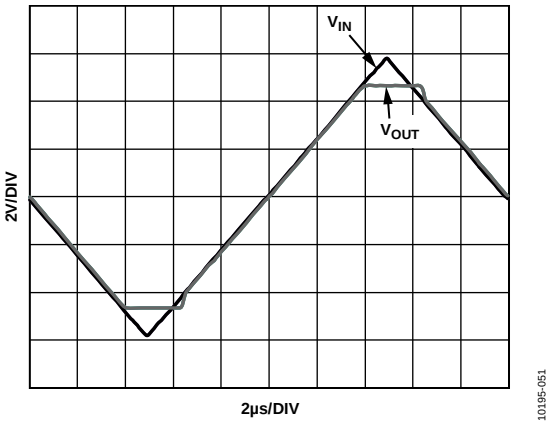


Figure 16. Overdrive Recovery, $V_S = +5$ V

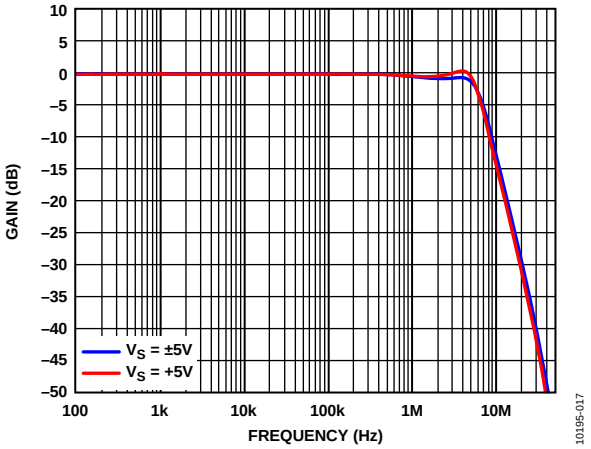


Figure 17. Small Signal Frequency Response for Various Supplies

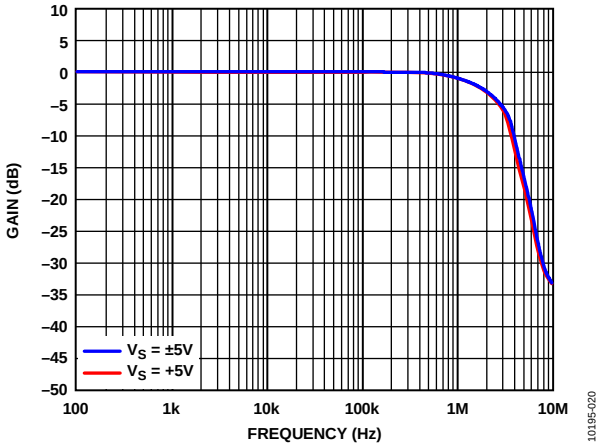


Figure 20. Large Signal Frequency Response for Various Supplies

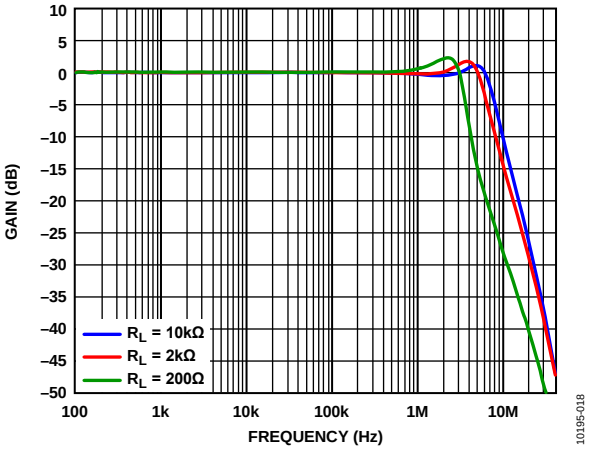


Figure 18. Small Signal Frequency Response for Various Loads

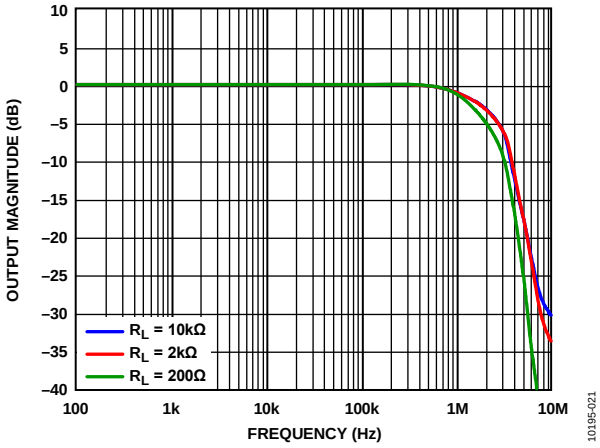


Figure 21. Large Signal Frequency Response for Various Loads

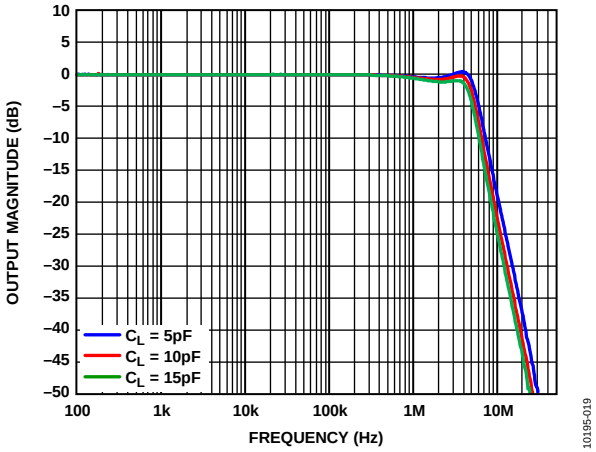


Figure 19. Small Signal Frequency Response for Various Capacitive Loads

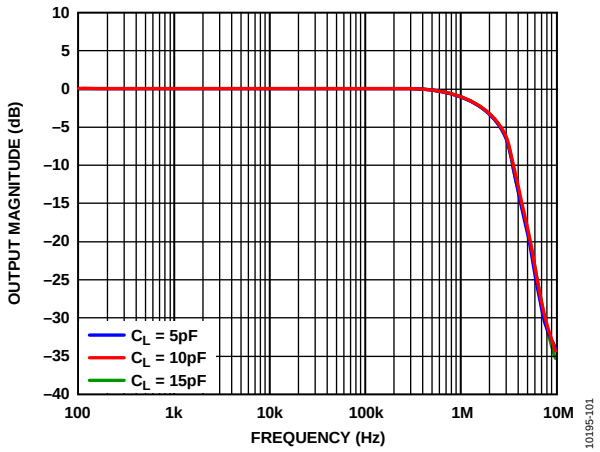


Figure 22. Large Signal Frequency Response for Various Capacitive Loads

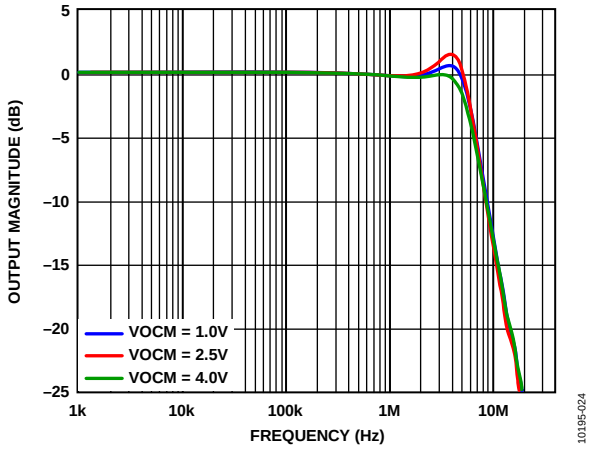


Figure 23. Small Signal Frequency Response for Various VOCM Levels

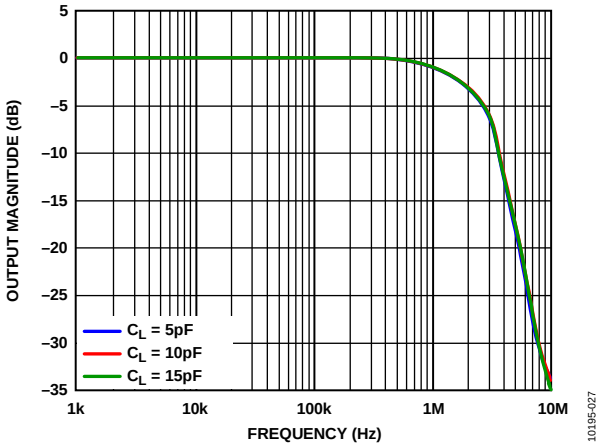


Figure 26. Large Signal Frequency Response for Various VOCM Level

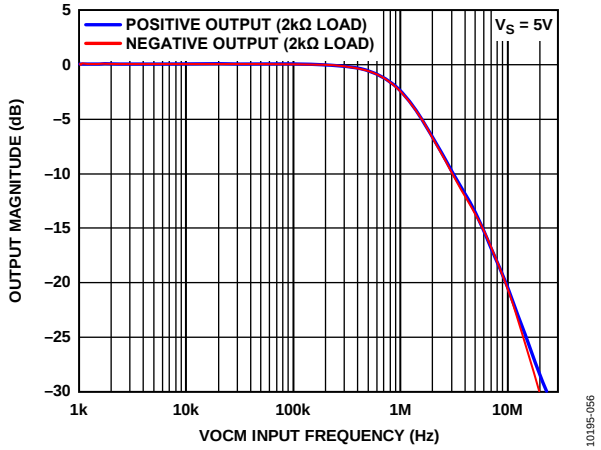


Figure 24. VOCM Small Signal Frequency Response

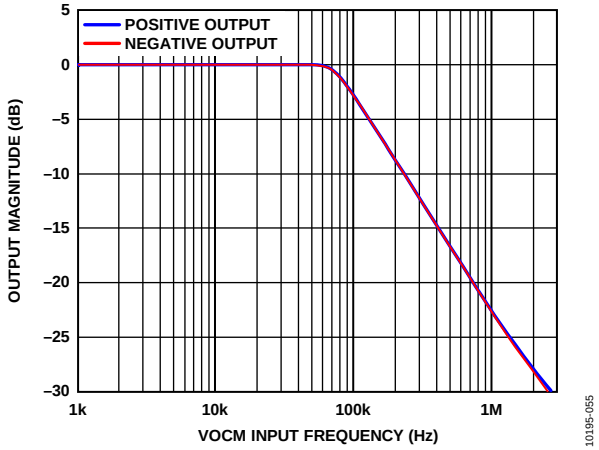


Figure 27. VOCM Large Signal Frequency Response

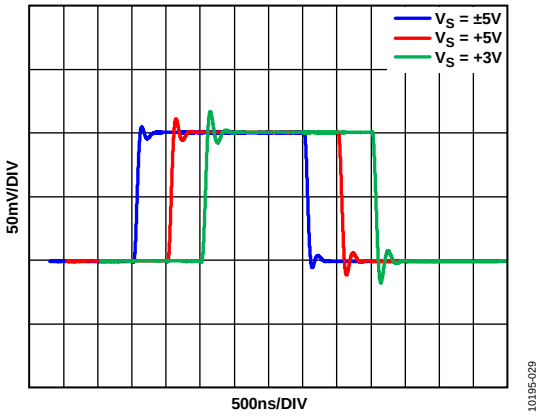


Figure 25. Small Signal Pulse Response for Various Supplies

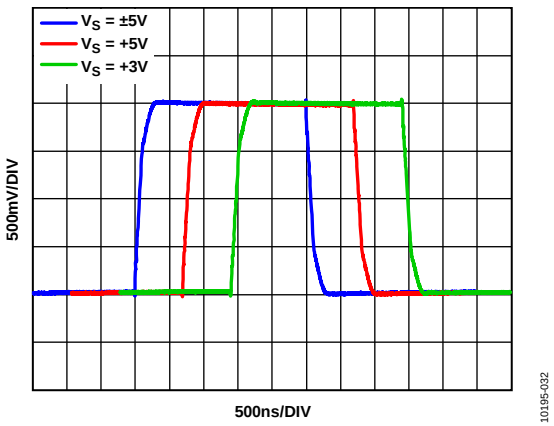


Figure 28. Large Signal Pulse Response for Various Supplies

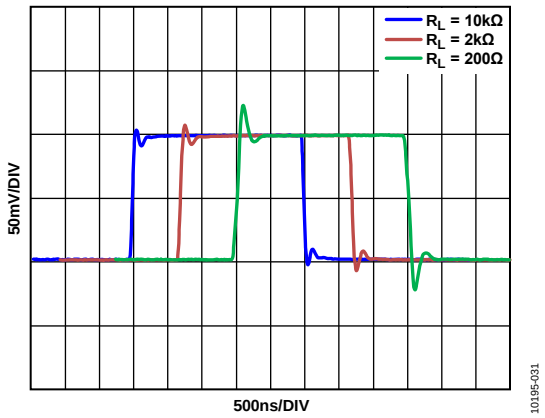


Figure 29. Small Signal Step Response for Various Resistive Loads, V_S = ±5 V

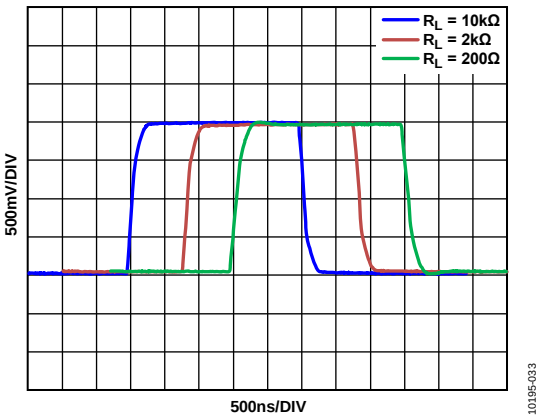


Figure 32. Large Signal Step Response for Various Resistive Loads, V_S = ±5 V

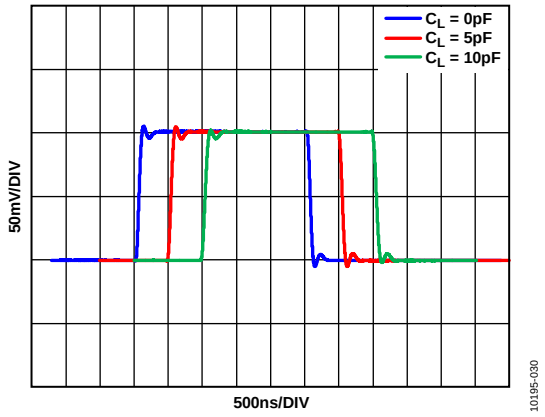


Figure 30. Small Signal Step Response for Various Capacitive Loads, V_S = ±5 V

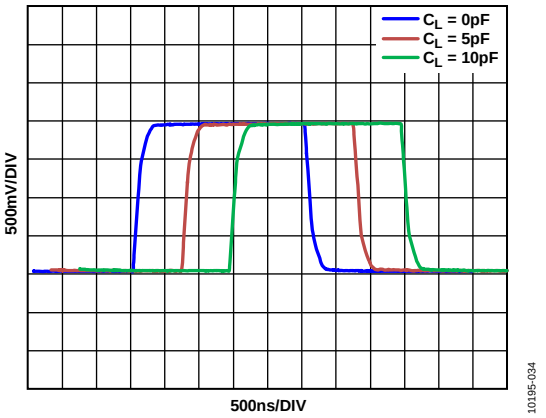


Figure 33. Large Signal Step Response for Various Capacitive Loads, V_S = ±5 V

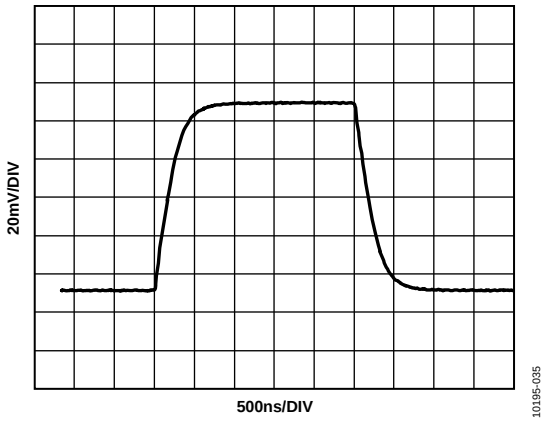


Figure 31. VOCM Small Signal Step Response

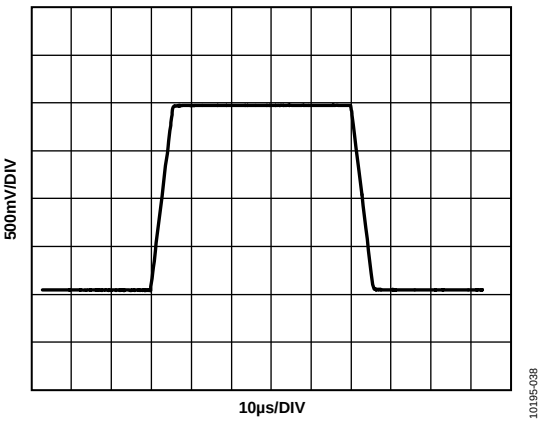


Figure 34. VOCM Large Signal Step Response

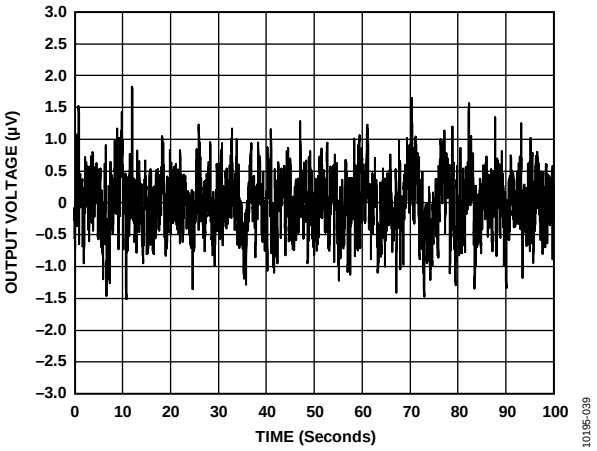


Figure 35. 0.1 Hz to 10 Hz Voltage Noise

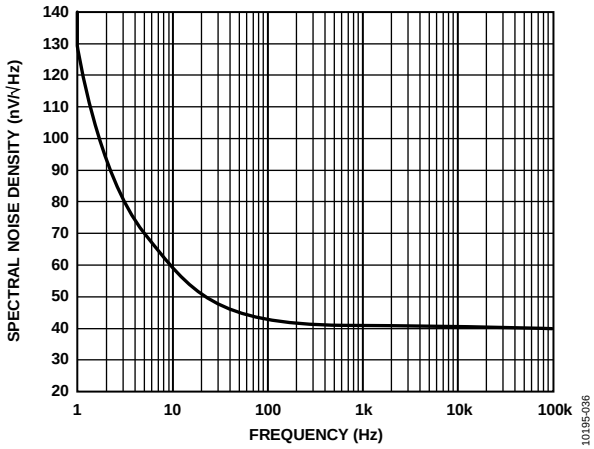


Figure 38. Voltage Noise Density vs. Frequency

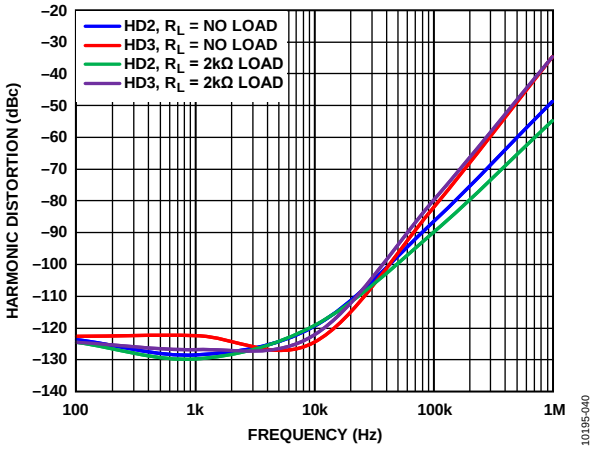


Figure 36. Harmonic Distortion vs. Frequency at Various Loads

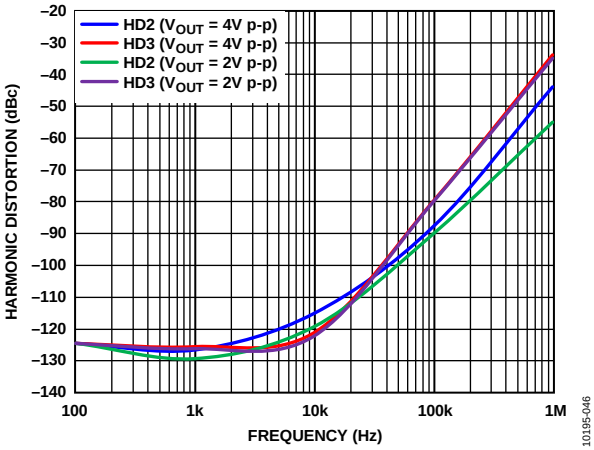


Figure 39. Harmonic Distortion vs. Frequency at Various $V_{OUT,dm}$

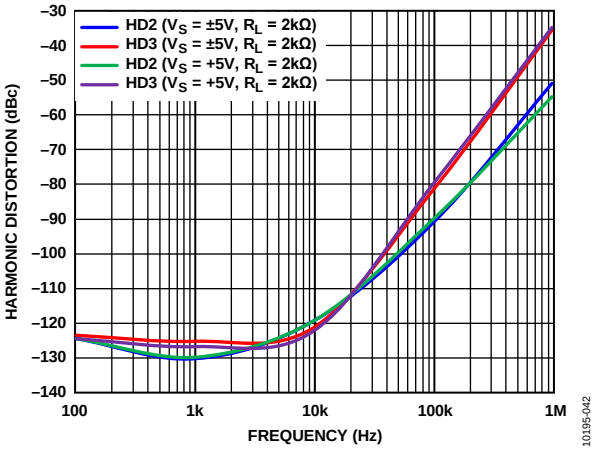


Figure 37. Harmonic Distortion vs. Frequency at Various Supplies

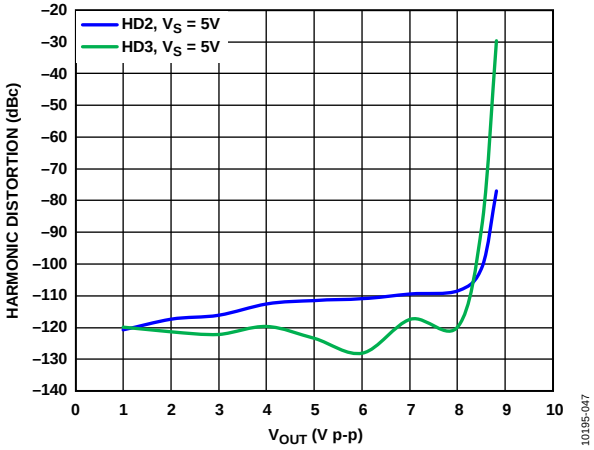


Figure 40. Harmonic Distortion vs. $V_{OUT,dm}$, f = 10 kHz

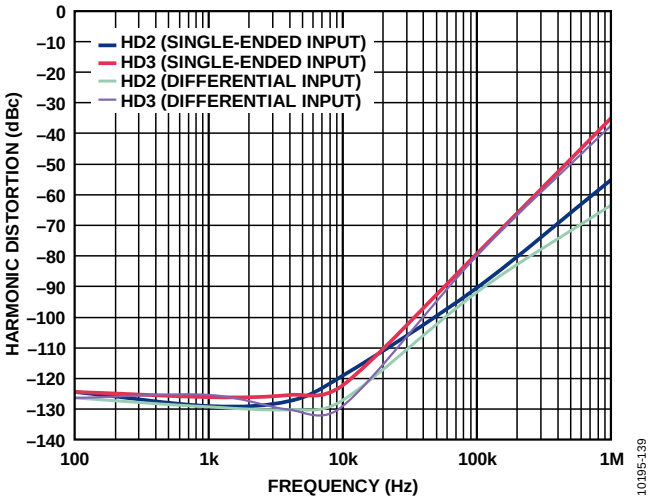


Figure 41. Harmonic Distortion vs. Input Drive

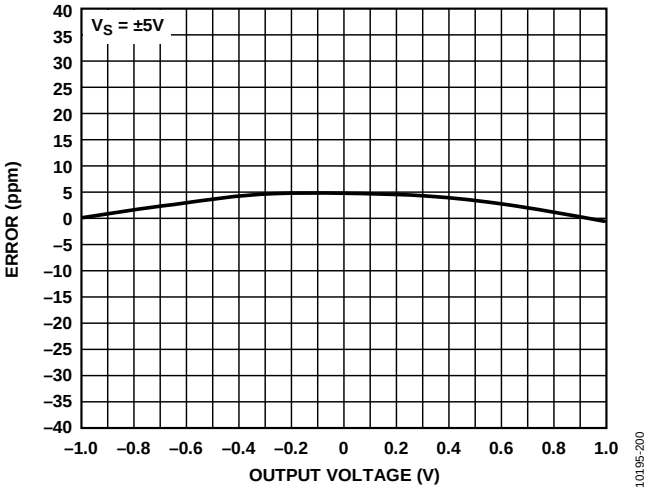


Figure 44. Gain Nonlinearity

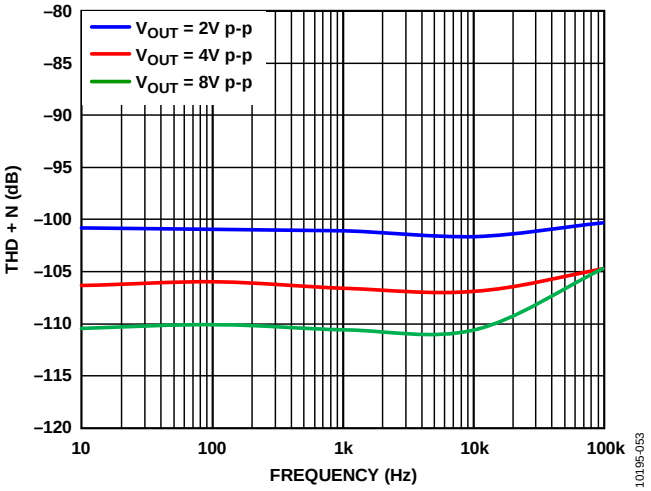


Figure 42. Total Harmonic Distortion + Noise vs. Frequency

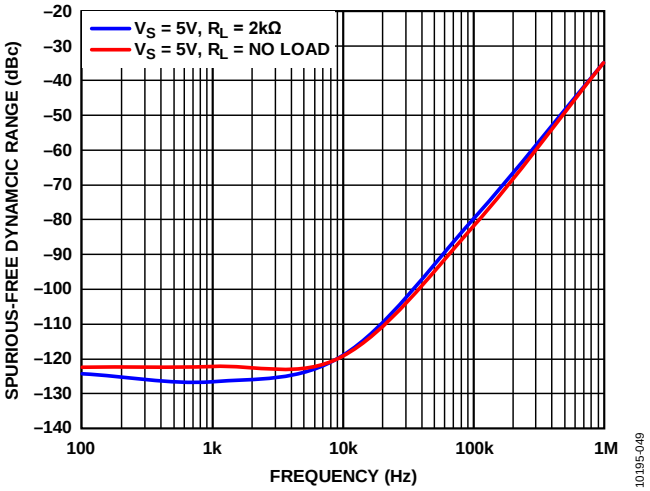


Figure 45. Spurious-Free Dynamic Range vs. Frequency at Various Loads

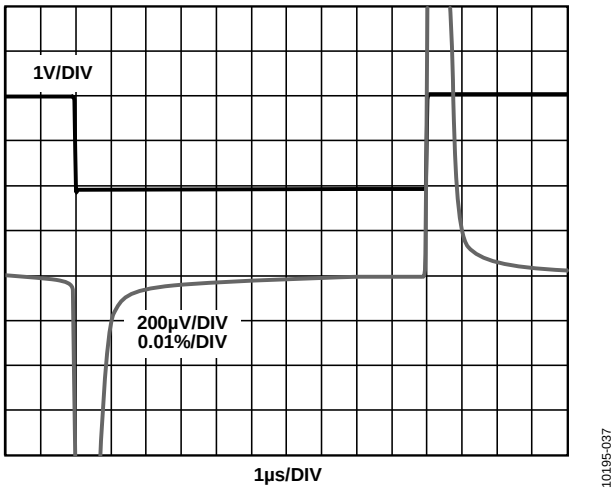


Figure 43. Settling Time to 0.01% of 2 V Step

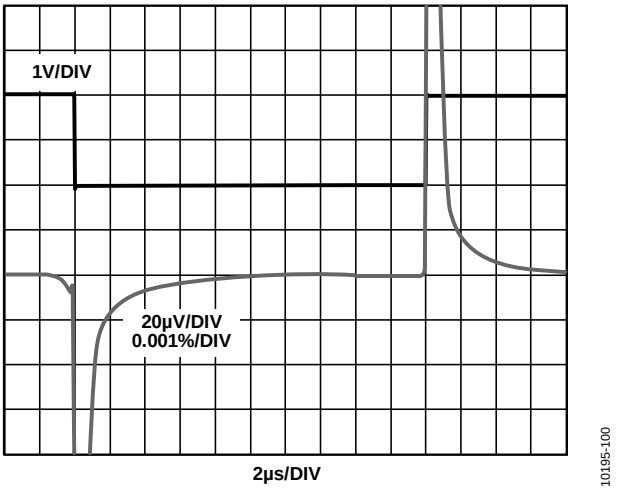


Figure 46. Settling Time to 0.001% of 2 V Step

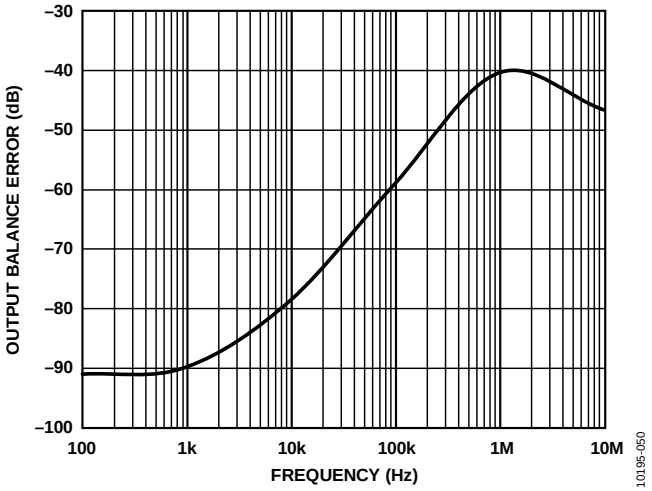


Figure 47. Output Balance Error vs. Frequency

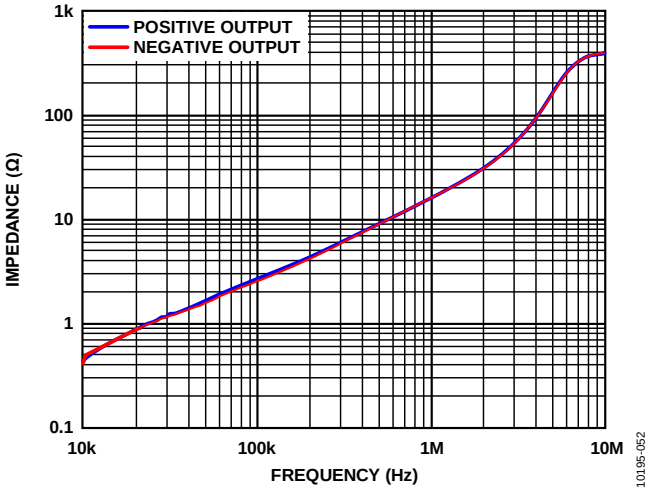


Figure 49. Output Impedance vs. Frequency

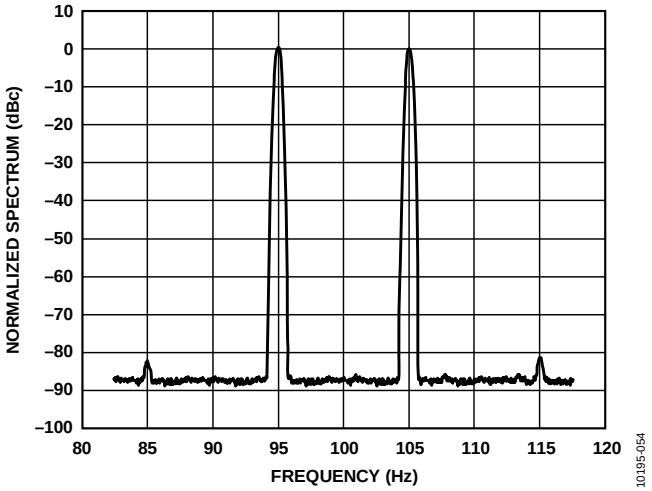


Figure 48. 100 kHz Intermodulation Distortion

TERMINOLOGY

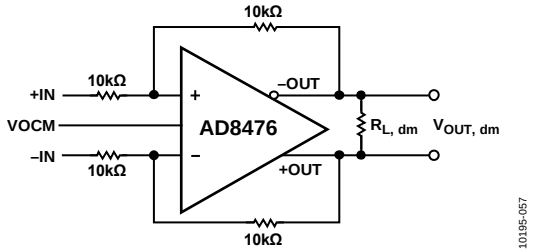


Figure 50. Signal and Circuit Definitions

Differential Voltage

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently, output differential mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT terminals with respect to a common ground reference. Similarly, the differential input voltage is defined as

$$V_{IN,\,dm} = (V_{+IN} - V_{-IN})$$

Common-Mode Voltage

Common-mode voltage refers to the average of two node voltages with respect to the local ground reference. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

Balance

Output balance is a measure of how close the output differential signals are to being equal in amplitude and opposite in phase. Output balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the divider midpoint with the magnitude of the differential signal. By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{\Delta V_{OUT,\,cm}}{\Delta V_{OUT,\,dm}} \right|$$

THEORY OF OPERATION

OVERVIEW

The AD8476 is a fully differential amplifier, with integrated laser-trimmed resistors, that provides a precision gain of 1. The internal differential amplifier of the AD8476 differs from conventional operational amplifiers in that it has two outputs whose voltages are equal in magnitude, but move in opposite directions (180° out of phase).

The AD8476 is designed to greatly simplify single-ended-to-differential conversion, common-mode level shifting and precision driving of differential signals into low power, differential input ADCs. The VOCM input allows the user to set the output common-mode voltage to match with the input range of the ADC. Like an operational amplifier, the VOCM function relies on high open-loop gain and negative feedback to force the output nodes to the desired voltages.

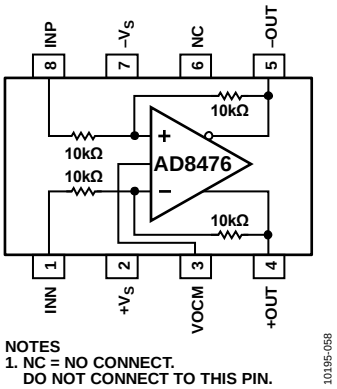


Figure 51. Block Diagram

CIRCUIT INFORMATION

The AD8476 amplifier uses a voltage feedback topology; therefore, the amplifier exhibits a nominally constant gain bandwidth product. Like a voltage feedback operational amplifier, the AD8476 also has high input impedance at its internal input terminals (the summing nodes of the internal amplifier) and low output impedance.

The AD8476 employs two feedback loops, one each to control the differential and common-mode output voltages. The differential feedback loop, which is fixed with precision laser-trimmed on-chip resistors, controls the differential output voltage.

Output Common-Mode Voltage (VOCM)

The internal common-mode feedback controls the common-mode output voltage. This architecture makes it easy for the user to set the output common-mode level to any arbitrary value independent of the input voltage. The output common-mode voltage is forced by the internal common-mode feedback loop to be equal to the voltage applied to the VOCM input. The VOCM pin can be left unconnected, and the output common-mode voltage self-biases to midsupply by the internal feedback control.

Due to the internal common-mode feedback loop and the fully differential topology of the amplifier, the AD8476 outputs are precisely balanced over a wide frequency range. This means that the amplifier's differential outputs are very close to the ideal of being identical in amplitude and exactly 180° out of phase.

DC PRECISION

The dc precision of the AD8476 is highly dependent on the accuracy of its integrated gain resistors. Using superposition to analyze the circuit shown in Figure 52, the following equation shows the relationship between the input and output voltages of the amplifier:

$$V_{IN,cm}\left(R_P - R_N\right) + V_{IN,dm}\frac{1}{2}\left(2R_PR_N + R_P + R_N\right)$$

$$= V_{OUT,cm}\left(R_P - R_N\right) + V_{OUT,dm}\frac{1}{2}\left(2 + R_P + R_N\right)$$

where:

$$R_P = \frac{RFP}{RGP},\ R_N = \frac{RFN}{RGN}$$

$$V_{IN,dm} = V_P - V_N$$

$$V_{IN,cm} = \frac{1}{2}(V_P + V_N)$$

The differential closed-loop gain of the amplifier is

$$\frac{V_{OUT,dm}}{V_{IN,dm}} = \frac{2R_PR_N + R_P + R_N}{2 + R_P + R_N}$$

and the common rejection of the amplifier is

$$\frac{V_{OUT,dm}}{V_{IN,cm}} = \frac{2\left(R_P - R_N\right)}{2 + R_P + R_N}$$

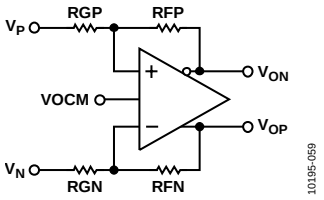


Figure 52. Functional Circuit Diagram of the AD8476 at a Given Gain

The preceding equations show that the gain accuracy and the common-mode rejection (CMRR) of the AD8476 are determined primarily by the matching of the feedback networks (resistor ratios). If the two networks are perfectly matched, that is, if R_P and R_N equal RF/RG, then the resistor network does not generate any CMRR errors and the differential closed loop gain of the amplifier reduces to

$$\frac{v_{OUT,dm}}{v_{IN,dm}} = \frac{RF}{RG}$$

The AD8476 integrated resistors are precision wafer-laser-trimmed to guarantee a minimum CMRR of 90 dB (32 µV/V), and gain error of less that 0.02%. To achieve equivalent precision and performance using a discrete solution, resistors must be matched to 0.01% or better.

INPUT VOLTAGE RANGE

The AD8476 can measure input voltages as large as the supply rails. The internal gain and feedback resistors form a divider, which reduces the input voltage seen by the internal input nodes of the amplifier. The largest voltage that can be measured properly is constrained by the output range of the amplifier and the capability of the amplifier's internal summing nodes. This voltage is defined by the input voltage, and the ratio between the feedback and the gain resistors.

Figure 53 shows the voltage at the internal summing nodes of the amplifier, defined by the input voltage and internal resistor network. If V_N is grounded, the expression shown reduces to

$$V_{PLUS} = V_{MINUS} = \frac{RG}{RF + RG}\left(VOCM + \frac{1}{2}\frac{RF}{RG}V_P\right)$$

The internal amplifier of the AD8476 has rail-to-rail inputs. To obtain accurate measurements with minimal distortion, the voltage at the internal inputs of the amplifier must stay below $+V_S - 1$ V and above $-V_S$.

The AD8476 provides overvoltage protection for excessive input voltages beyond the supply rails. Integrated ESD protection diodes at the inputs prevent damage to the AD8476 up to $+V_S + 18$ V and $-V_S - 18$ V.

DRIVING THE AD8476

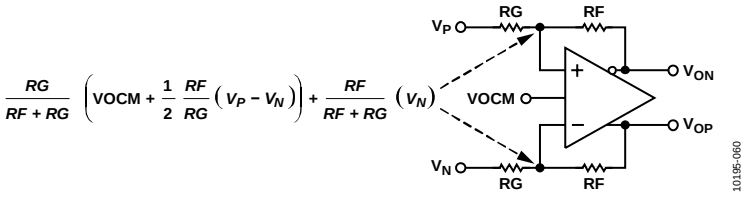
Care should be taken to drive the AD8476 with a low impedance source: for example, another amplifier. Source resistance can unbalance the resistor ratios and, therefore, significantly degrade the gain accuracy and common-mode rejection of the AD8476. For the best performance, source impedance to the AD8476 input terminals should be kept below 0.1 Ω. Refer to the DC Precision section for details on the critical role of resistor ratios in the precision of the AD8476.

POWER SUPPLIES

The AD8476 operates over a wide range of supply voltages. It can be powered on a single supply as low as 3 V and as high as 18 V. The AD8476 can also operate on dual supplies from ±1.5 V to ±9 V

A stable dc voltage should be used to power the AD8476. Note that noise on the supply pins can adversely affect performance. For more information, see the PSRR performance curve in Figure 10.

Place a bypass capacitor of 0.1 µF between each supply pin and ground, as close as possible to each supply pin. Use a tantalum capacitor of 10 µF between each supply and ground. It can be farther away from the supply pins and, typically, it can be shared by other precision integrated circuits.



$$\frac{RG}{RF + RG}\left(VOCM + \frac{1}{2}\frac{RF}{RG}(V_P - V_N)\right) + \frac{RF}{RF + RG}(V_N)$$

Figure 53. Voltages at the Internal Op Amp Inputs of the AD8476

APPLICATIONS INFORMATION

TYPICAL CONFIGURATION

The AD8476 is designed to facilitate single-ended-to-differential conversion, common-mode level shifting, and precision processing of signals so that they are compatible with low voltage ADCs.

Figure 54 shows a typical connection diagram of the AD8476.

SINGLE-ENDED-TO-DIFFERENTIAL CONVERSION

Many industrial systems have single-ended inputs from input sensors; however, the signals are frequently processed by high performance differential input ADCs for higher precision. The AD8476 performs the critical function of precisely converting single-ended signals to the differential inputs of precision ADCs, and it does so with no need for external components.

To convert a single-ended signal to a differential signal, connect one input to the signal source and the other input to ground (see Figure 54). Note that either input can be driven by the source with the only effect being that the outputs have reversed polarity. The AD8476 also accepts truly differential input signals in precision systems with differential signal paths.

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The VOCM pin of the AD8476 is internally biased by a precision voltage divider comprising of two 1 MΩ resistors between the supplies. This divider level shifts the output to midsupply. Relying on the internal bias results in an output common-mode voltage that is within 0.05% of the expected value.

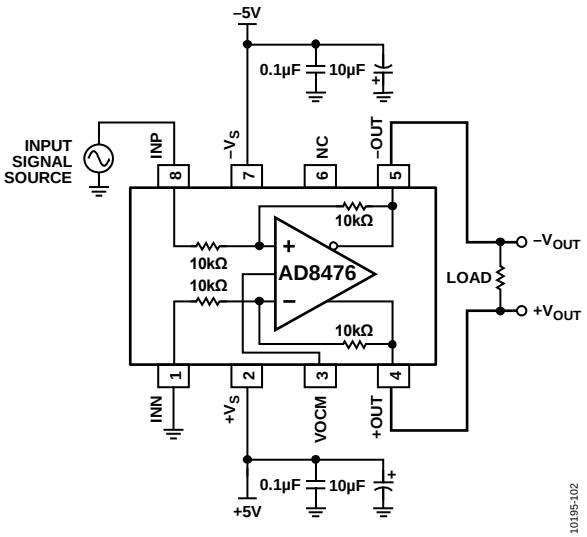


Figure 54. Typical Configuration—8-Lead MSOP

In cases where control of the output common-mode level is desired, an external source or resistor divider can be used to drive the VOCM pin. If driven directly from a source, or with a resistor divider of unequal resistor values, the resistance seen by the VOCM pin should be less than 1 kΩ. If an external voltage divider consisting of equal resistor values is used to set VOCM to midsupply, higher values can be used because the external resistors are placed in parallel with the internal resistors. The output common-mode offset listed in the Specifications section assumes that the VOCM input is driven by a low impedance voltage source.

Because of the internal divider, the VOCM pin sources and sinks current, depending on the externally applied voltage and its associated source resistance.

It is also possible to connect the VOCM input to the common-mode level output of an ADC; however, care must be taken to ensure that the output has sufficient drive capability. The input impedance of the VOCM pin is 500 kΩ. If multiple AD8476 devices share one ADC reference output, a buffer may be necessary to drive the parallel inputs.

Table 6. Differential Input ADCs[1]

ADC	Resolution	Throughput Rate	Power Dissipation
AD7674	16 Bits	100 kSPS	25 mW
AD7684	16 Bits	100 kSPS	6 mW
AD7687	16 Bits	250 kSPS	12.5 mW
AD7688	16 Bits	500 kSPS*	21.5 mW

[1] Depending on measurement/application type, check that the AD8476 meets settling time requirements.

LOW POWER ADC DRIVING

The AD8476 is designed to be a low power driver for ADCs with up to 16-bit precision and sampling rates of up to 250 kSPS. The circuit in Figure 56 shows the AD8476 driving the AD7687, a 16-bit, 250 kSPS fully differential SAR ADC. The filter between the AD8476 and the ADC reduces high frequency noise and reduces switching transients from the sampling of the ADC.

Choose the values of this filter with care. Optimal values for the filter may need to be determined empirically, but the guidelines discussed herein are provided to help the user. For optimum performance, this filter should be fast enough to settle full-scale to 0.5 LSB of the ADC within the acquisition time specified in the ADC data sheet, in this case, the AD7687. If the filter is slower than the acquisition time, distortion can result that looks like harmonics. If the filter is too fast, the noise bandwidth of the amplifier increases, thereby reducing the SNR of your system.

Additional considerations help determine the values of the individual components. THD of the ADC is likely to increase with source resistance. This is stated in the ADC data sheet. To reduce this effect, try to use smaller resistance and larger capacitance. Large capacitance values much greater than 2 nF are hard for the amplifier to drive. Higher capacitance also increases the effect of changes in output impedance.

It is also important to consider the signal frequency range of interest. The AD8476 THD decreases with higher frequency (see Figure 42) and output impedance increases with higher frequency (see Figure 49). This higher output impedance yields slower settling, thus be certain to choose your capacitance so that the filter still meets the settling requirement at the maximum frequency of interest.

In the application shown, a 100 Ω resistors and 2.2 nF capacitors at each output were chosen. For driving the AD7687, this combination yields an SNR loss of 2.5 dB and good THD performance for a 20 kHz fundamental frequency, with an ADC throughput rate of 250kSPS. The filter bandwidth can be determined by the following equation:

$$Filter\ Frequency = \frac{1}{2\pi RC}$$

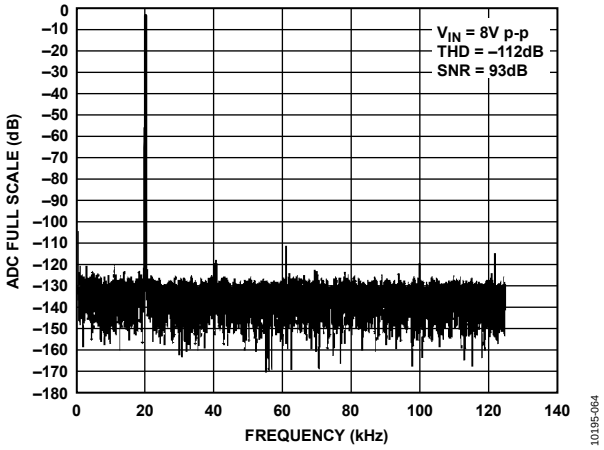


Figure 55. FFT of AD8476 Driving the AD7687

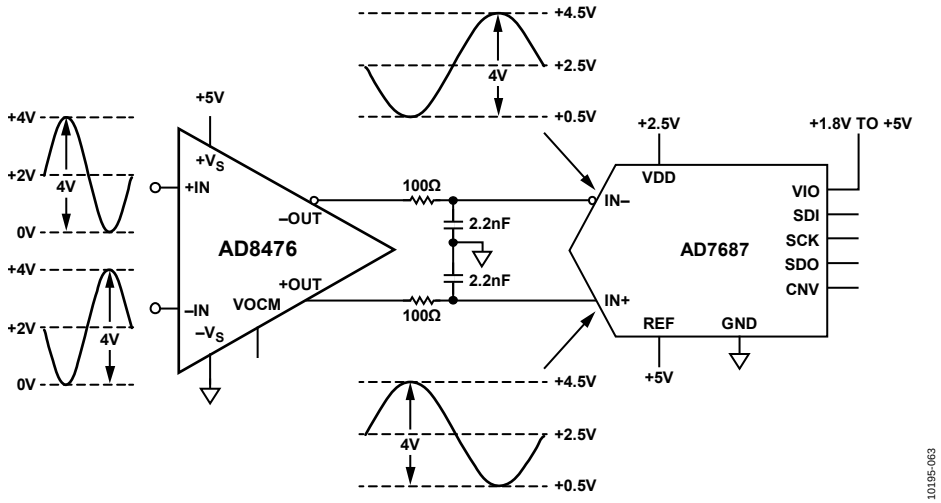


Figure 56. AD8476 Conditioning and Level Shifting a Differential Voltage to Drive Single-Supply ADC

OUTLINE DIMENSIONS

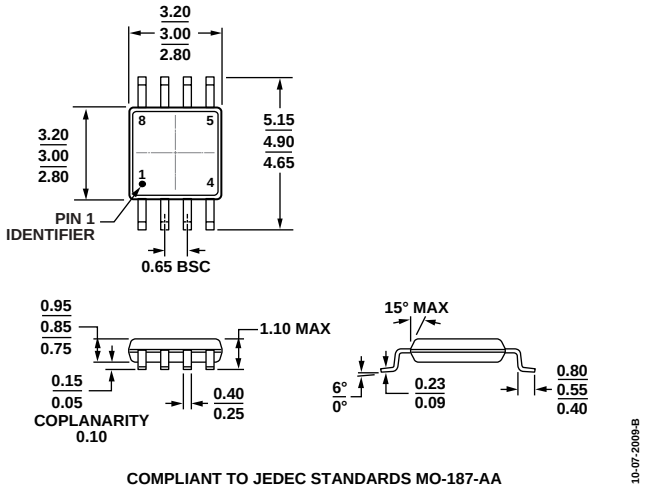


Figure 57. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

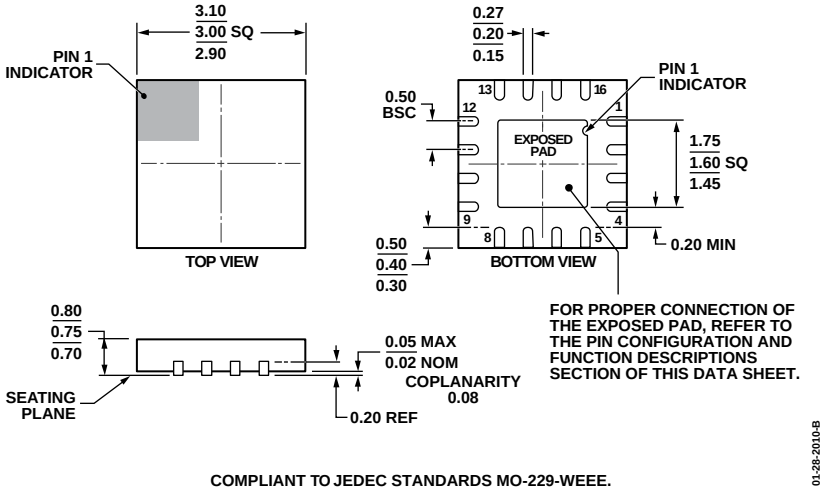


Figure 58. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-25)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8476BCPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-25	Y45
AD8476BCPZ-RL	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-25	Y45
AD8476BCPZ-WP	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-25	Y45
AD8476ACPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-25	Y44
AD8476ACPZ-RL	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-25	Y44
AD8476ACPZ-WP	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-25	Y44
AD8476BRMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y47
AD8476BRMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y47
AD8476BRMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y47
AD8476ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y46
AD8476ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y46
AD8476ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y46
AD8476-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D10195-0-5/12(B)