



N-CHANNEL ENHANCEMENT MODE MOSFET

Features

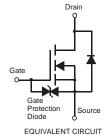
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **ESD Protected Up To 2KV**
- Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

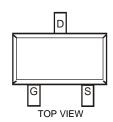
Mechanical Data

- Case: SOT-323
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminals: Finish Matte Tin annealed over Alloy 42 leadframe. Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.006 grams (approximate)









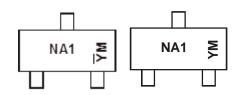
Ordering Information (Note 4)

Part Number	Case	Packaging
DMG1012UW-7	SOT-323	3000 / Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html

Marking Information



Chengdu A/T Site Shanghai A/T Site NA1 = Product Type Marking Code

YM = Date Code Marking for SAT (Shanghai Assembly/ Test site) YM = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Y or \overline{Y} = Year (ex: A = 2013) M = Month (ex: 9 = September)

Date Code Key

Year	200	9	2010		2011	20	12	2013		2014	2	2015
Code	W		Χ		Υ		Z	Α		В		С
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



Cha	Symbol	Value	Unit		
Drain-Source Voltage	V _{DSS}	20	V		
Gate-Source Voltage	V _{GSS}	±6	V		
Continuous Drain Current (Note 5)	Steady State	$T_A = +25$ °C $T_A = +85$ °C	I _D	1.0 0.64	А
Pulsed Drain Current (Note 6)	I _{DM}	6	Α		

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Power Dissipation (Note 3)	P _D	0.29	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 3)	$R_{\theta JA}$	425	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Notes:

- 5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
- 6. Repetitive rating, pulse width limited by junction temperature.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)	•			,	ı	
Drain-Source Breakdown Voltage	BV _{DSS}	20	-	-	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current T _J = 25°C	I _{DSS}	-	-	100	nA	$V_{DS} = 20V, V_{GS} = 0V$
Gate-Source Leakage	I _{GSS}	-	-	±1.0	μΑ	$V_{GS} = \pm 4.5V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	0.5	-	1.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
			0.3	0.45		$V_{GS} = 4.5V, I_D = 600mA$
Static Drain-Source On-Resistance	R _{DS (ON)}	-	0.4	0.6	Ω	$V_{GS} = 2.5V, I_D = 500mA$
	, ,		0.5	0.75		$V_{GS} = 1.8V, I_D = 350mA$
Forward Transfer Admittance	Y _{fs}	-	1.4	-	S	$V_{DS} = 10V, I_D = 400mA$
Diode Forward Voltage	V _{SD}	-	0.7	1.2	V	$V_{GS} = 0V, I_S = 150mA$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	ı	60.67	-	pF	10)/)/
Output Capacitance	Coss	-	9.68	-	pF	$V_{DS} = 16V, V_{GS} = 0V,$ - f = 1.0MHz
Reverse Transfer Capacitance	C _{rss}	-	5.37	-	pF	1 = 1.0WH 12
Total Gate Charge	Qq	-	736.6	-	рС	15/1/
Gate-Source Charge	Q _{gs}	-	93.6	-	рС	$V_{GS} = 4.5V, V_{DS} = 10V,$
Gate-Drain Charge	Q _{qd}	-	116.6	-	рС	$I_D = 250 \text{mA}$
Turn-On Delay Time	t _{D(on)}	-	5.1	-	ns	
Turn-On Rise Time	t _r	-	7.4	-	ns	$V_{DD} = 10V, V_{GS} = 4.5V,$
Turn-Off Delay Time	t _{D(off)}	-	26.7	-	ns	$R_L = 47\Omega$, $R_G = 10\Omega$,
Turn-Off Fall Time	t _f	-	12.3	-	ns	$I_D = 200 \text{mA}$

Notes:

- 7. Short duration pulse test used to minimize self-heating effect.
- 8. Guaranteed by design. Not subject to production testing.

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 $T_A = 150$ °C

T_A = 125°C

T_A = 85°C

T_A = 25°C

T_A = -55°C

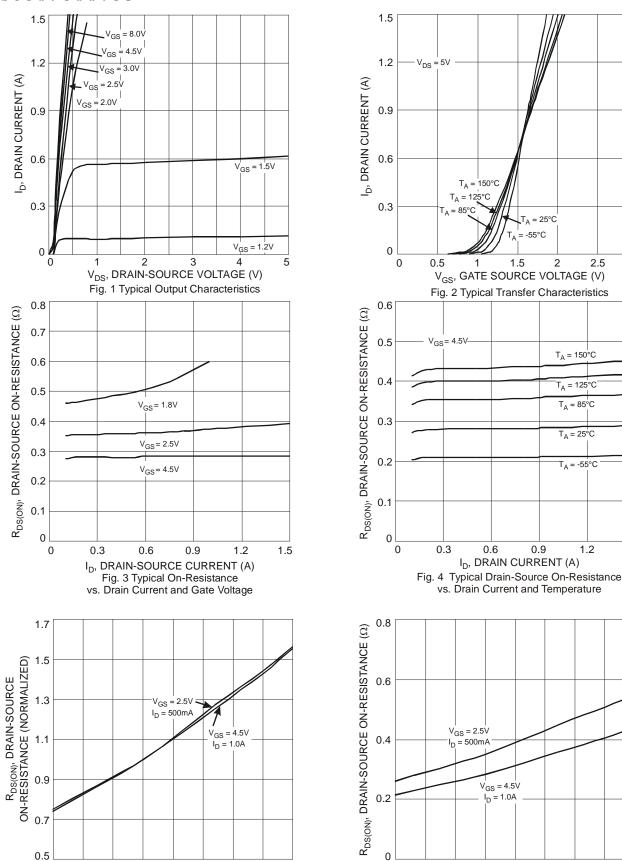
1.2

1.5

2.5

3





25

50

T_J, JUNCTION TEMPERATURE (°C)

Fig. 5 On-Resistance Variation with Temperature

75

100

125

-50

25

50

T_J, JUNCTION TEMPERATURE (°C)

Fig. 6 On-Resistance Variation with Temperature

75

100

125



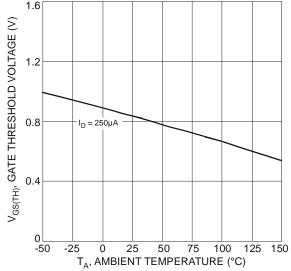
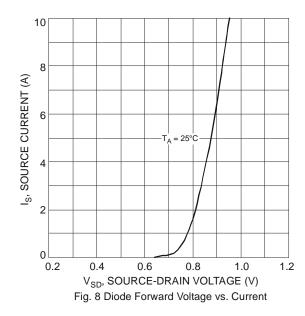
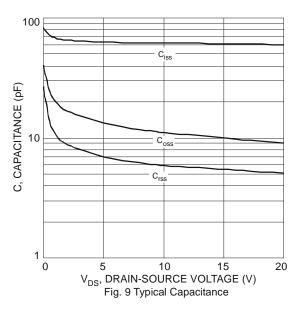
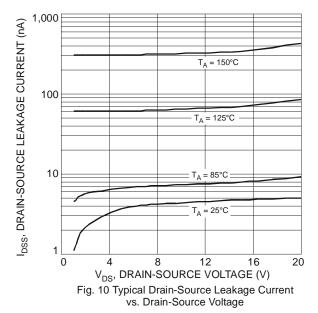


Fig. 7 Gate Threshold Variation vs. Ambient Temperature







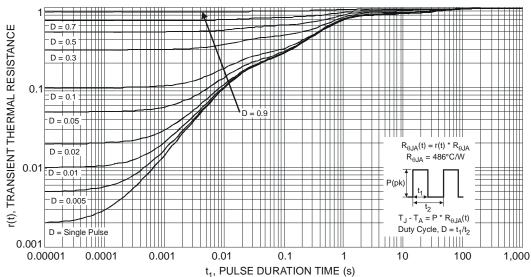
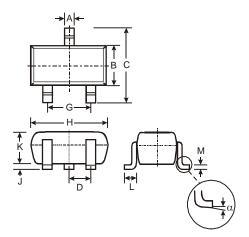


Fig. 11 Transient Thermal Response

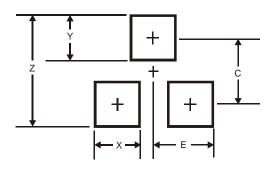


Package Outline Dimensions



	SOT-323						
Dim	Min	Max	Тур				
Α	0.25	0.40	0.30				
В	1.15	1.35	1.30				
С	2.00	2.20	2.10				
D	-	-	0.65				
G	1.20	1.40	1.30				
Н	1.80	2.20	2.15				
J	0.0	0.10	0.05				
K	0.90	1.00	0.95				
L	0.25	0.40	0.30				
M	0.10	0.18	0.11				
α	0°	8°	-				
All Dimensions in mm							

Suggested Pad Layout



Dimensions	Value (in mm)
Z	2.8
Х	0.7
Y	0.9
С	1.9
E	1.0



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