Allegro布线规则的设置说明

PCB布线经常会要求对重要的信号线进行规则的设置。*布线规则*的设置通常包括线宽和线距两大部分。下面就以一主板Layout guide为例部分说明之。

1. 首先是对整板未定义线规则的设置,如下表所示:

Net Name	Width	Spacing	Net Group
Non-special Signal	Inner layer: 4 Outer layer: 5	Inner layer: 4 Outer layer: 5	

选择 並打开set standard values



🙀 Default Values F	'ora 🔳 🗖 🔀
Subclass:	INT1 💌
Line to line:	
Line to pad:	XX
Pad to pad:	5 MIL
Line width:	4 MIL
Etch on subclass:	Allowed
Same net DRC:	On 💌
OK Cancel	Reset Help
🛱 Default Yalues F	使子產品世界 .com.cn □□×
Subclass:	ТОР
Line to line:	xx
Line to pad:	××
Pad to pad:	5 MIL
Line width:	5 MIL
Etch on subclass:	Allowed
Same net DRC:	On 😽
OK Cancel	Reset Help

这里规定了Default line 在outer layer(TOP)和inner layer(INT1)中的line width 和pad to pad 的间距。

2. 接下来设置HOST 部分,见下表要求:

Net Name	Width	Spacing	Space with other signal	Net Group
FSB Signals	Inner layer: 4 Outer layer: 5	8/10	20	HOST

首先将属于此网络的所有net 定义为同一组,即BUS NAME=HOST 选择Edit-Properties 并在右侧的当前命令栏中点击More 打开Find by name or property 窗口,ok

∫ Options ∖∫	Find Visibility		
- Design Object	Find Filter		
All On A	JI Off		
Groups	Shapes		
Comps	🔲 Voids		
Symbols	Cline Segs		
Functions	Other Segs		
🗹 Nets	Tind der A		
🗌 Pins	DRC errors		
Vias	Text		
🔲 Clines	Ratsnests		
🔲 Lines	🗌 Rat Ts		
Find By Name			
Net	💌 Name 💌		
>	More		

Find by Wame or Property		
Dbject type: Net		
Available objects	Selected objects	
Name filter: h* Value filter:		
H_A#3 H_A#4 H_A#5 H_A#6 H_A#7 H_A#8 H_A#9 H_A#10	了 考產品 ★祭 .com.cn	
Use 'selected objects' for a deselection operation	(Apply) H	telp
洋就可以得到下面的窗口:		
Edit Property		
Table of Contents	Delete Property	Value
Available Properties	Bus_Name	HOST DATA0
Min_Neck_Width Min_Noise_Margin Min_Setup	Net_Physical_Type Net_Spacing_Type	HOST 4/5 HOST 8:10/20
Net_Physical_lype Net_Schedule Net_Spacing_Type		Level D
No_Pin_Escape	2 7/2	AR TO AT
No_Hat	.con	n.cn
<		
News		
OK Cancel Help	Reset Apply Sh	now ->
		Concerning and the second s



至此一组HOST 线设置完毕,用同样的方法我们可以继续将DDR 等部分的线设置完

3. 重新打开 **一**,选择 spacing rule set-set value,点击ADD 添加HOST 8:10

🙀 Spacing Rule Set	Etch Spacing	Values	
Constraint Set Name:	HOST 8:10	~	
Subclass:	ALL ETCH	V	
Add Copy	Delete		
Global fields are used to set mu	ltiple constraints only.		
Global 😽	Spacing:		
Pin To Pin:	5 MIL		
Line To Pin:	5 MIL		
Line To Line:	XX		
Via To Pin:	5 MIL		
Via To Via:	5ML 電子撞	品世界	
Via To Line:	5 MIL .CO	n.cn	
Shape To Pin:	8 MIL		
Shape To Via:	8 MIL		
Shape To Line:	8 MIL		
Shape To Shape:	8 MIL		
Non Paired			
Same Net DRC:	On 🖌		
Min BB Via Gap:	5 MIL		
	ar (1)		
** Constraint set values not the se	ame for all subclasses.		
OK Cancel	Reset		Help
然后在Subclass 中,顶底	层Line To Line 的间距	5为 10 ,内月	尽为8.

4. 选择physical rule set-set value,点击ADD 添加HOST 4/5 Physical (Lines/Vias) Rule Set Etch Values 📮 🗆 🔀

Constraint Set Name:	HOST 4/5
Subclass:	ALL ETCH
Add Copy	Delete
Physical property	Value
Min line width:	XX
Max line width:	100 MIL
Min neck width:	XX
Max neck length:	10000 MIL
DiffPair primary gap:	Exercise and support
DiffPair neck gap:	0 MIL
Allow on etch subclass:	Allowed
'T' junctions:	Anywhere
Min BBvia stagger:	5 MIL
Max BBvia stagger:	0 MIL
Pad/pad direct connect:	Not Allowed
Via list property	
- Available database padsta	cks Current via list

然后在Subclass 中,顶底层的线宽为5,内层为4.

5. 无论是线宽还是线距都需要在assignment table 中进行和其他NET 的匹配。