

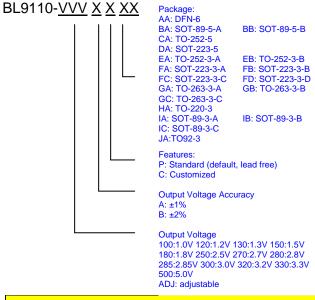
### FEATURES

- Up to 1A Output Current
- 70uA Operating Supply Current
- Excellent Line Regulation: 0.05%/V
- Low Dropout: 350mV@1A(VOUT=3.3V)
- High Power Supply Rejection Ratio
- Wide Operating Voltage Range: 2.5V to 6.0V
- 1V to 5V Factory-Preset Output
- High Accuracy: ±1% or ±2%
- Built-in Auto Discharge Function
- 500mA in-rush Current Limit
- Fold-back Current Limit Protection
- Thermal Shutdown Protection
- DFN-6, SOT-89-5, SOT-89-3, SOT-223-5, SOT-223-3, TO-263-3, TO-220-3, TO-252-3 and TO-252-5 Package
- RoHS Compliant and 100% Lead (Pb)-Free

#### **APPLICATIONS**

- Portable Communication Equipment
- Battery-Powered Equipment
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments

#### **ORDERING INFORMATION**



#### PPMIC BU BL9110 Rev 2.0 04/2016

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- PCMCIA Cards and Wireless LAN
- Electrical appliances such as cameras, VCRS

High PSRR CMOS Linear Regulator

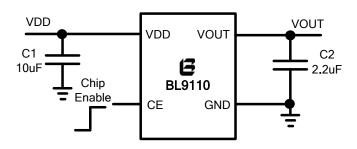
1A Low Dropout, Low Quiescent Current

#### DESCRIPTION

The BL9110 is a low-dropout regulator that operates the input voltage from 2.5V to 6V and delivers 1A load current. The BL9110 is available in two types, either fixed or adjustable output voltage. The output voltage of the fixed types is preset at an internally trimmed voltage 1V, 1.2V, 1.3V, 1.5V, 1.8V, 2.5V, 2.7V, 2.8V, 2.85V, 3.0V, 3.2V, 3.3V, 5V or can be made with options of the output range from 1V to 5V in 50mV increments. The output range of adjustable types is from 1V to 5V. The BL9110 consists of a voltage reference, an error amplifier, resistor net for setting output voltage, a current limit circuit for over-current and a thermal-shutdown circuit.

A standby mode with ultra low supply current can be realized with the chip enable function. Since the packages for BL9110 are DFN-6, SOT-89-5, SOT-223-5, SOT-223-3, TO-263-3, TO-220-3, SOT-89-3, TO-252-3, TO92-3 and TO-252-5 with high power dissipation, high density mounting of the IC on board is possible.

### **TYPICAL APPLICATION**





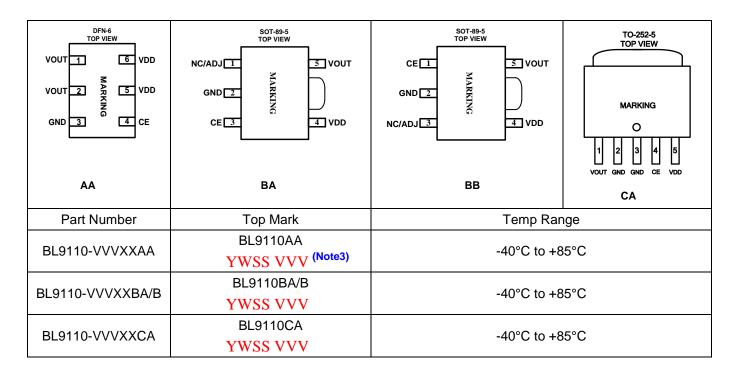
1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

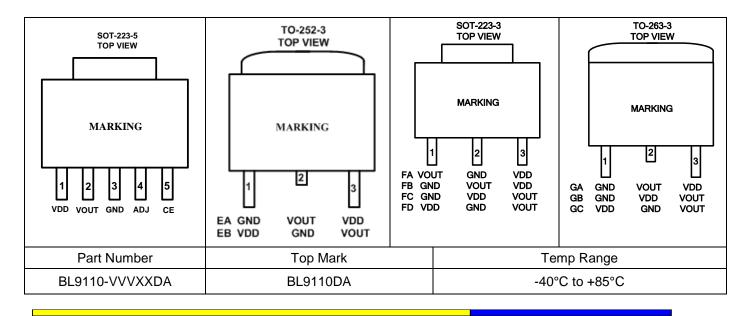
### Absolute Maximum Rating (Note 1)

Input Supply Voltage (V<sub>DD</sub>) CE Input Voltage Output Voltage Output Current -0.3V to +7V -0.3V to +7V -0.3V to V<sub>IN</sub>+0.3V 1.4A

Maximum Junction Temperature125°COperating Temperature Range-40°C to 85°CStorage Temperature Range-65°C to 125°CLead Temperature (Soldering, 10s)300°C

### **Package Information**



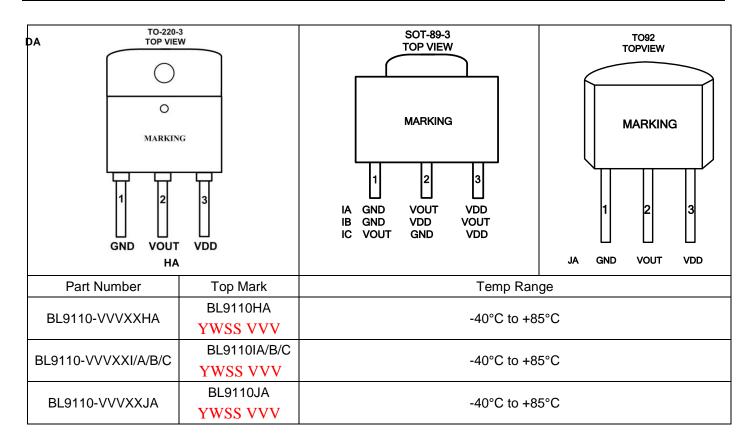


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1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

	YWSS VVV	
BL9110-VVVXXEA/B	BL9110EA/B	10°C to 195°C
DL9110-VVVAAEA/D	YWSS VVV	-40°C to +85°C
BL9110-VVVXXFA/B/C/D	BL9110FA/B/C/D	-40°C to +85°C
DL9110-VVVXXFA/D/C/D	YWSS VVV	-40 0 10 +85 0
	BL9110GA/B/C	-40°C to +85°C
BL9110-VVVXXGA/B/C	YWSS VVV	-40 C 10 +85 C





1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

#### **Pin Descriptions**

Symbol	Description
VOUT	Output Pin
GND	Ground Pin
CE	Chip Enable Pin (High active)
VDD	Input Pin
ADJ/NC	Adjustable/No Connection

VVV	100	120	130	 285	 495	500	ADJ
Voltage (V	) 1.0	1.2	1.3	 2.85	 4.95	5.0	Adjustable

Y	0	1	2	3	4	
Year	2010	2011	2012	2013	2014	

W	01	2	 26	27	28	 52
Week	Α	В	 Ζ	Ā	B	 Z

#### Thermal Resistance (Note 4):

Package	$\Theta_{JA}$	$\Theta_{JC}$
DFN-6	95°C/W	10°C/W
SOT-89-5	160°C/W	45°C/W
TO-252-5	90°C/W	10°C/W
SOT-223-5	160°C/W	20°C/W
TO-252-3	90°C/W	10°C/W
SOT-223-3	160°C/W	20°C/W
TO-263-3	65°C/W	7°C/W
TO-220-3	50°C/W	7°C/W
SOT89-3	180°C/W	50°C/W

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The BL9110 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the -40°C to

85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Y: Year of assembly manufacturing

W: Week of assembly manufacturing

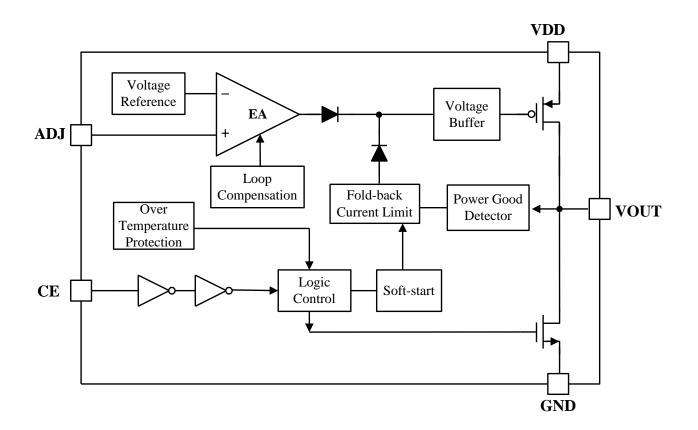
SS: Lot ID (the 7<sup>th</sup> and 8<sup>th</sup> number of Lot numbers)

VVV: Voltage code (for example 100 stands for 1.0V)

Note 4: Thermal Resistance is specified with approximately 1 square of 1 oz copper.



### **Block Diagram**



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1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

#### **Electrical Characteristics** (Note 5)

#### **BL9110-1.2V Electrical Characteristics**

(V<sub>DD</sub>=2.5V, V<sub>OUT</sub>=1.2V, CE=V<sub>DD</sub>, C<sub>IN</sub>=2.2µF, C<sub>OUT</sub>=2.2µF, T<sub>A</sub>=25°C, unless otherwise noted.)

Param		Symbol	Conditions	MIN	TYP	MAX	unit
Input Vo	oltage	V <sub>DD</sub>		2.5		6	V
Output Voltage A	ccuracy <sup>(Note 6)</sup>	$\Delta V_{OUT}$	I <sub>OUT</sub> =1mA	-1 -2		+1 +2	%
Current	Limit	I <sub>LIM</sub>		1.0	1.3		А
Short Circui	t Current	I <sub>SCC</sub>	V <sub>OUT</sub> =0		250		mA
Quiescent	Current	l <sub>Q</sub>	I <sub>OUT</sub> =0mA		70	120	uA
Standby (	Current	I <sub>STBY</sub>	V <sub>CE</sub> =GND, Shutdown		0.01	1	uA
Dropout Volta	note 7)	M	I <sub>OUT</sub> =300mA		420	715	m\/
		V <sub>DROP</sub>	I <sub>OUT</sub> =1A		870	1310	mV
Line Regulat	ion <sup>(Note 8)</sup>	$\Delta V_{\text{LINE}}$	2.5V≤V <sub>DD</sub> ≤ 6V, I <sub>OUT</sub> =100mA		0.05	0.5	%/V
Load Regulat	tion (Note 9)	$\Delta V_{LOAD}$	1mA≤I <sub>OUT</sub> ≤1A		20		mV
Output Voltag	ge (Note 10)	TC <sub>VOUT</sub>	I <sub>OUT</sub> =100mA -40°C≤T≤85°C		±100		ppm/°C
CE	Logic Low	VIL	Shutdown			0.4	V
Input Threshold	Logic High	V <sub>IH</sub>	Start up	1.0			V
CE Pull-down	Resistance	R <sub>CE</sub>			5		MΩ
Output Nois	e Voltage	e <sub>NO</sub>	10Hz to100KHz, I <sub>OUT</sub> =1mA		45		uV <sub>RMS</sub>
Power Supply	f=1kHz (VOUT≤3.3V)	PSRR	0.2V <sub>P-P</sub> Ripple		70		dD
Rejection Ratio f=1kHz (VOUT>3.3V)		FORK	I <sub>OUT</sub> =100mA		60		dB
Thermal Shutdow	n Temperature	T <sub>SD</sub>	Shutdown, Temp increasing		165		С°
Thermal Shutdov	wn Hysteresis	T <sub>SDHY</sub>			30		С°
Output Discharg	e Resistance	R <sub>DSC</sub>			50		Ω

**Note 5:** 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note 6: This IC includes two kinds of output voltage accuracy versions. A: ±1%, B: ±2%.

Note 7: The required minimum input operating voltage is equal to  $V_{OUT}+V_{DROP}$ , and if  $V_{OUT}+V_{DROP} < 2.5V$ , the required minimum input operating voltage must be set to 2.5V.  $V_{OUT}$  is the normal output voltage, e.g.  $V_{OUT}=2.8V$  for 2.8V fixed output version.

**Note 8:** Line regulation is calculated by 
$$\Delta V_{LINE} = \left(\frac{V_{OUT1} - V_{OUT2}}{\Delta V_{DD} \times V_{OUT}}\right) \times 100$$

Where  $V_{OUT1}$  is the output voltage when  $V_{DD1}$ =6.0V,  $V_{OUT2}$  is the output voltage when  $V_{DD2}$ = max ( $V_{OUT}$ +0.5V, 2.5V).  $\triangle V_{DD}$ = $V_{DD1}$ - $V_{DD2}$ .

**Note 9:** Load regulation is calculated by  $\Delta V_{LOAD} = V_{OUT1} - V_{OUT2}$ Where V<sub>OUT1</sub> is the output voltage when I<sub>OUT1</sub>=1mA, and V<sub>OUT2</sub> is the output voltage when I<sub>OUT2</sub>=1A. **Note 10:** The temperature coefficient is calculated by  $TC_{V_{OUT}} = \frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$ 



1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

#### **BL9110-1.5V Electrical Characteristics**

(V <sub>DD</sub> =2.5V, V <sub>0</sub>	<sub>DUT</sub> =1.5V, CE=V <sub>D</sub>	<sub>D</sub> , C <sub>IN</sub> =2.2μ	F, C <sub>OUT</sub> =2.2µF, T <sub>A</sub> =25°C, unles	s otherv	vise not	ed.)	
Param		Symbol	Conditions	MIN	TYP	MAX	unit
Input Vo	oltage	V <sub>DD</sub>		2.5		6	V
Output Voltage A	ccuracy <sup>(Note 6)</sup>	$\Delta V_{OUT}$	I <sub>OUT</sub> =1mA	-1 -2		+1 +2	%
Current	Limit	I <sub>LIM</sub>		1.0	1.3		А
Short Circui	t Current	I <sub>SCC</sub>	V <sub>OUT</sub> =0		250		mA
Quiescent	Current	Ι <sub>Q</sub>	I <sub>OUT</sub> =0mA		70	120	uA
Standby (	Current	I <sub>STBY</sub>	V <sub>CE</sub> =GND, Shutdown		0.01	1	uA
Dropout Volta	(note 7)	V	I <sub>OUT</sub> =300mA		260	445	mV
		V <sub>DROP</sub>	I <sub>OUT</sub> =1A		700	1050	IIIV
Line Regulat	Line Regulation (Note 8)		2.5V≤V <sub>DD</sub> ≤ 6V, I <sub>OUT</sub> =100mA		0.05	0.5	%/V
Load Regulat	tion (Note 9)	$\Delta V_{LINE}$ $\Delta V_{LOAD}$	1mA≤I <sub>o∪T</sub> ≤1A		20		mV
Output Voltag	ge <sup>(Note 10)</sup>	TC <sub>VOUT</sub>	I <sub>OUT</sub> =100mA -40°C≤T≤85°C		±100		ppm/°C
CE	Logic Low	VIL	Shutdown			0.4	V
Input Threshold	Logic High	VIH	Start up	1.0			V
CE Pull-down	Resistance	R <sub>CE</sub>			5		MΩ
Output Nois	e Voltage	e <sub>NO</sub>	10Hz to100KHz, I <sub>OUT</sub> =1mA		45		$\mathrm{uV}_{\mathrm{RMS}}$
Power Supply	f=1kHz (VOUT≤3.3V)		0.2V <sub>P-P</sub> Ripple		70		
Rejection Ratio	f=1kHz (VOUT>3.3V)	PSRR	I <sub>OUT</sub> =100mA		60		dB
Thermal Shutdow	Thermal Shutdown Temperature		Shutdown, Temp increasing		165		°C
Thermal Shutdov		T <sub>SD</sub> T <sub>SDHY</sub>			30		°C
Output Discharg		R <sub>DSC</sub>			50		Ω

**Note 5:** 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note 6: This IC includes two kinds of output voltage accuracy versions. A: ±1%, B: ±2%.

Note 7: The required minimum input operating voltage is equal to  $V_{OUT}+V_{DROP}$ , and if  $V_{OUT}+V_{DROP}$  <2.5V, the required minimum input operating voltage must be set to 2.5V.  $V_{OUT}$  is the normal output voltage, e.g.  $V_{OUT}$ =2.8V for 2.8V fixed output version.

**Note 8:** Line regulation is calculated by  $\Delta V_{LINE} = \left(\frac{V_{OUT1} - V_{OUT2}}{\Delta V_{DD} \times V_{OUT}}\right) \times 100$ 

Where  $V_{\text{OUT1}}$  is the output voltage when  $V_{\text{DD1}}$ =6.0V,  $V_{\text{OUT2}}$  is the output voltage when  $V_{\text{DD2}}$ = max ( $V_{\text{OUT}}$ +0.5V, 2.5V).  $\triangle V_{\text{DD}}$ = $V_{\text{DD1}}$ - $V_{\text{DD2}}$ .

**Note 9:** Load regulation is calculated by  $\Delta V_{LOAD} = V_{OUT1} - V_{OUT2}$ Where V<sub>OUT1</sub> is the output voltage when I<sub>OUT1</sub>=1mA, and V<sub>OUT2</sub> is the output voltage when I<sub>OUT2</sub>=1.0A. **Note 10:** The temperature coefficient is calculated by  $TC_{V_{OUT}} = \frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$ 



1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

#### **BL9110-1.8V Electrical Characteristics**

(V <sub>DD</sub> =2.8V, V <sub>0</sub>	<sub>DUT</sub> =1.8V, CE=V <sub>D</sub>	<sub>D</sub> , C <sub>IN</sub> =2.2μ	F, C <sub>OUT</sub> =2.2µF, T <sub>A</sub> =25°C, unles	s otherv	vise not	ed.)	
Param	eter	Symbol	Conditions	MIN	TYP	MAX	unit
Input Vo	oltage	V <sub>DD</sub>		2.5		6	V
Output Voltage A	ccuracy <sup>(Note 6)</sup>	$\Delta V_{OUT}$	I <sub>OUT</sub> =1mA	-1 -2		+1 +2	%
Current	Limit	I <sub>LIM</sub>		1.0	1.3		А
Short Circui	t Current	I <sub>SCC</sub>	V <sub>OUT</sub> =0		250		mA
Quiescent	Current	l <sub>Q</sub>	I <sub>OUT</sub> =0mA		70	120	uA
Standby (	Current	I <sub>STBY</sub>	V <sub>CE</sub> =GND, Shutdown		0.01	1	uA
Dropout Volta	(note 7)	V	I <sub>OUT</sub> =300mA		180	308	mV
		V <sub>DROP</sub>	I <sub>OUT</sub> =1A		570	855	111V
Line Regulat	Line Regulation (Note 8)		2.5V≤V <sub>DD</sub> ≤ 6V, I <sub>OUT</sub> =100mA		0.05	0.5	%/V
Load Regulat	tion <sup>(Note 9)</sup>	$\Delta V_{LINE}$ $\Delta V_{LOAD}$	1mA≤I <sub>OUT</sub> ≤1A		20		mV
Output Voltag	ge <sup>(Note 10)</sup>	TC <sub>VOUT</sub>	I <sub>OUT</sub> =100mA -40°C≤T≤85°C		±100		ppm/°C
CE	Logic Low	VIL	Shutdown			0.4	V
Input Threshold	Logic High	VIH	Start up	1.0			V
CE Pull-down	Resistance	R <sub>CE</sub>			5		MΩ
Output Nois	e Voltage	e <sub>NO</sub>	10Hz to100KHz, I <sub>OUT</sub> =1mA		45		$\mathrm{uV}_{\mathrm{RMS}}$
Power Supply	f=1kHz (VOUT≤3.3V)	חספח	0.2V <sub>P-P</sub> Ripple		70		
Rejection Ratio	f=1kHz (VOUT>3.3V)	PSRR	I <sub>OUT</sub> =100mA		60		dB
Thermal Shutdow	Thermal Shutdown Temperature		Shutdown, Temp increasing		165		°C
Thermal Shutdov	wn Hysteresis	T <sub>SD</sub> T <sub>SDHY</sub>			30		°C
Output Discharg	e Resistance	R <sub>DSC</sub>			50		Ω

**Note 5:** 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note 6: This IC includes two kinds of output voltage accuracy versions. A: ±1%, B: ±2%.

Note 7: The required minimum input operating voltage is equal to  $V_{OUT}+V_{DROP}$ , and if  $V_{OUT}+V_{DROP}$  <2.5V, the required minimum input operating voltage must be set to 2.5V.  $V_{OUT}$  is the normal output voltage, e.g.  $V_{OUT}$ =2.8V for 2.8V fixed output version.

**Note 8:** Line regulation is calculated by  $\Delta V_{LINE} = \left(\frac{V_{OUT1} - V_{OUT2}}{\Delta V_{DD} \times V_{OUT}}\right) \times 100$ 

Where  $V_{OUT1}$  is the output voltage when  $V_{DD1}$ =6.0V,  $V_{OUT2}$  is the output voltage when  $V_{DD2}$ = max ( $V_{OUT}$ +0.5V, 2.5V).  $\triangle V_{DD}$ = $V_{DD1}$ - $V_{DD2}$ .

**Note 9:** Load regulation is calculated by  $\Delta V_{LOAD} = V_{OUT1} - V_{OUT2}$ Where V<sub>OUT1</sub> is the output voltage when I<sub>OUT1</sub>=1mA, and V<sub>OUT2</sub> is the output voltage when I<sub>OUT2</sub>=1.0A. **Note 10:** The temperature coefficient is calculated by  $TC_{V_{OUT}} = \frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$ 



1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

#### **BL9110-2.5V Electrical Characteristics**

(V <sub>DD</sub> =3.5V, V <sub>0</sub>	DUT=2.5V, CE=VD	<sub>D</sub> , C <sub>IN</sub> =2.2μ	F, C <sub>OUT</sub> =2.2µF, T <sub>A</sub> =25°C, unles	s otherv	vise not	ed.)	
Param		Symbol	Conditions	MIN	TYP	MAX	unit
Input Vo	oltage	$V_{DD}$		2.5		6	V
Output Voltage A	ccuracy <sup>(Note 6)</sup>	$\Delta V_{OUT}$	I <sub>OUT</sub> =1mA	-1 -2		+1 +2	%
Current	Limit	I <sub>LIM</sub>		1.0	1.3		А
Short Circui	t Current	I <sub>SCC</sub>	V <sub>OUT</sub> =0		250		mA
Quiescent	Current	l <sub>Q</sub>	I <sub>OUT</sub> =0mA		70	120	uA
Standby (	Current	I <sub>STBY</sub>	V <sub>CE</sub> =GND, Shutdown		0.01	1	uA
Dropout Volta	(note 7)	V	I <sub>OUT</sub> =300mA		140	240	mV
		V <sub>DROP</sub>	I <sub>OUT</sub> =1A		440	660	mv
Line Regulat	ion <sup>(Note 8)</sup>	$\Delta V_{\text{LINE}}$	3.0V≤V <sub>DD</sub> ≤ 6V, I <sub>OUT</sub> =100mA		0.05	0.5	%/V
Load Regulat	tion (Note 9)	$\Delta V_{LOAD}$	1mA≤I <sub>OUT</sub> ≤1A		20		mV
Output Voltag	ge <sup>(Note 10)</sup>	TC <sub>VOUT</sub>	I <sub>OUT</sub> =100mA -40°C≤T≤85°C		±100		ppm/°C
CE	Logic Low	VIL	Shutdown			0.4	V
Input Threshold	Logic High	VIH	Start up	1.0			V
CE Pull-down	Resistance	R <sub>CE</sub>			5		MΩ
Output Nois	e Voltage	e <sub>NO</sub>	10Hz to100KHz, I <sub>OUT</sub> =1mA		45		$uV_RMS$
Power Supply	f=1kHz (VOUT≤3.3V)		0.2V <sub>P-P</sub> Ripple		70		
Rejection Ratio	f=1kHz (VOUT>3.3V)	PSRR	I <sub>OUT</sub> =100mA		60		dB
Thermal Shutdow	Thermal Shutdown Temperature		Shutdown, Temp increasing		165		°C
Thermal Shutdov		T <sub>SD</sub> T <sub>SDHY</sub>			30		°C
Output Discharg		R <sub>DSC</sub>			50		Ω

**Note 5:** 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note 6: This IC includes two kinds of output voltage accuracy versions. A: ±1%, B: ±2%.

Note 7: The required minimum input operating voltage is equal to  $V_{OUT}+V_{DROP}$ , and if  $V_{OUT}+V_{DROP}$  <2.5V, the required minimum input operating voltage must be set to 2.5V.  $V_{OUT}$  is the normal output voltage, e.g.  $V_{OUT}$ =2.8V for 2.8V fixed output version.

**Note 8:** Line regulation is calculated by  $\Delta V_{LINE} = \left(\frac{V_{OUT1} - V_{OUT2}}{\Delta V_{DD} \times V_{OUT}}\right) \times 100$ 

Where  $V_{\text{OUT1}}$  is the output voltage when  $V_{\text{DD1}}$ =6.0V,  $V_{\text{OUT2}}$  is the output voltage when  $V_{\text{DD2}}$ = max ( $V_{\text{OUT}}$ +0.5V, 2.5V).  $\triangle V_{\text{DD}}$ = $V_{\text{DD1}}$ - $V_{\text{DD2}}$ .

**Note 9:** Load regulation is calculated by  $\Delta V_{LOAD} = V_{OUT1} - V_{OUT2}$ Where V<sub>OUT1</sub> is the output voltage when I<sub>OUT1</sub>=1mA, and V<sub>OUT2</sub> is the output voltage when I<sub>OUT2</sub>=1.0A. **Note 10:** The temperature coefficient is calculated by  $TC_{V_{OUT}} = \frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$ 



1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

#### **BL9110-3.3V Electrical Characteristics**

(V <sub>DD</sub> =4.3V, V	<sub>OUT</sub> =3.3V, CE=V <sub>D</sub>	<sub>D</sub> , C <sub>IN</sub> =2.2µ	F, C <sub>OUT</sub> =2.2µF, T <sub>A</sub> =25°C, unles	s otherv	vise not	ed.)	
Param		Symbol	Conditions	MIN	TYP	MAX	unit
Input Vo	oltage	V <sub>DD</sub>		2.5		6	V
Output Voltage A	ccuracy <sup>(Note 6)</sup>	$\Delta V_{OUT}$	I <sub>OUT</sub> =1mA	-1 -2		+1 +2	%
Current	Limit	I <sub>LIM</sub>		1.0	1.3		А
Short Circu	it Current	I <sub>SCC</sub>	V <sub>OUT</sub> =0		250		mA
Quiescent	Current	lq	I <sub>OUT</sub> =0mA		70	120	uA
Standby (	Current	I <sub>STBY</sub>	V <sub>CE</sub> =GND, Shutdown		0.01	1	uA
Dropout Volt	(note 7)		I <sub>OUT</sub> =300mA		110	188	mV
		V <sub>DROP</sub>	I <sub>OUT</sub> =1A		350	525	IIIV
Line Regulat	Line Regulation (Note 8)		3.8V≤V <sub>DD</sub> ≤ 6V, I <sub>OUT</sub> =100mA		0.05	0.5	%/V
Load Regula	tion (Note 9)	$\Delta V_{LINE}$ $\Delta V_{LOAD}$	1mA≤I <sub>OUT</sub> ≤1A		20		mV
Output Volta Temperature Co	ge <sup>(Note 10)</sup>	TC <sub>VOUT</sub>	I <sub>OUT</sub> =100mA -40°C≤T≤85°C		±100		ppm/°C
CE	Logic Low	VIL	Shutdown			0.4	V
Input Threshold	Logic High	VIH	Start up	1.0			V
CE Pull-down	Resistance	R <sub>CE</sub>			5		MΩ
Output Nois	e Voltage	e <sub>NO</sub>	10Hz to100KHz, I <sub>OUT</sub> =1mA		45		$uV_{RMS}$
Power Supply	f=1kHz (VOUT≤3.3V)		0.2V <sub>P-P</sub> Ripple		70		
Rejection Ratio	f=1kHz (VOUT>3.3V)	PSRR	I <sub>OUT</sub> =100mA		60		dB
Thermal Shutdow	Thermal Shutdown Temperature		Shutdown, Temp increasing		165		°C
Thermal Shutdor	wn Hysteresis	T <sub>SD</sub> T <sub>SDHY</sub>			30		°C
Output Discharg		R <sub>DSC</sub>			50		Ω

**Note 5:** 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note 6: This IC includes two kinds of output voltage accuracy versions. A: ±1%, B: ±2%.

Note 7: The required minimum input operating voltage is equal to  $V_{OUT}+V_{DROP}$ , and if  $V_{OUT}+V_{DROP}$  <2.5V, the required minimum input operating voltage must be set to 2.5V.  $V_{OUT}$  is the normal output voltage, e.g.  $V_{OUT}$ =2.8V for 2.8V fixed output version.

**Note 8:** Line regulation is calculated by  $\Delta V_{LINE} = \left(\frac{V_{OUT1} - V_{OUT2}}{\Delta V_{DD} \times V_{OUT}}\right) \times 100$ 

Where  $V_{OUT1}$  is the output voltage when  $V_{DD1}$ =6.0V,  $V_{OUT2}$  is the output voltage when  $V_{DD2}$ = max ( $V_{OUT}$ +0.5V, 2.5V).  $\triangle V_{DD}$ = $V_{DD1}$ - $V_{DD2}$ .

**Note 9:** Load regulation is calculated by  $\Delta V_{LOAD} = V_{OUT1} - V_{OUT2}$ Where V<sub>OUT1</sub> is the output voltage when I<sub>OUT1</sub>=1mA, and V<sub>OUT2</sub> is the output voltage when I<sub>OUT2</sub>=1.0A. **Note 10:** The temperature coefficient is calculated by  $TC_{V_{OUT}} = \frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$ .



1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

#### **BL9110-5.0V Electrical Characteristics**

(V <sub>DD</sub> =6.0V, V	<sub>OUT</sub> =5.0V, CE=V <sub>D</sub>	<sub>D</sub> , C <sub>IN</sub> =2.2μ	F, C <sub>OUT</sub> =2.2µF, T <sub>A</sub> =25°C, unles	s otherv	vise not	ed.)	
Param		Symbol	Conditions	MIN	TYP	MAX	unit
Input Vo	oltage	V <sub>DD</sub>		2.5		6	V
Output Voltage A	ccuracy <sup>(Note 6)</sup>	$\Delta V_{OUT}$	I <sub>OUT</sub> =1mA	-1 -2		+1 +2	%
Current	Limit	I <sub>LIM</sub>		1.0	1.3		А
Short Circu	it Current	I <sub>SCC</sub>	V <sub>OUT</sub> =0		250		mA
Quiescent	Current	l <sub>Q</sub>	I <sub>OUT</sub> =0mA		70	120	uA
Standby (	Current	I <sub>STBY</sub>	V <sub>CE</sub> =GND, Shutdown		0.01	1	uA
Dropout Volt	(note 7)	V	I <sub>OUT</sub> =300mA		100	170	mV
		V <sub>DROP</sub>	I <sub>OUT</sub> =1A		340	510	111V
Line Regulat	Line Regulation (Note 8)		5.5V≤V <sub>DD</sub> ≤ 6V, I <sub>OUT</sub> =100mA		0.05	0.5	%/V
Load Regula	tion (Note 9)	$\Delta V_{LINE}$ $\Delta V_{LOAD}$	1mA≤I <sub>OUT</sub> ≤1A		20		mV
Output Volta Temperature Co	ge <sup>(Note 10)</sup>	TC <sub>VOUT</sub>	I <sub>OUT</sub> =100mA -40°C≤T≤85°C		±100		ppm/°C
CE	Logic Low	VIL	Shutdown			0.4	V
Input Threshold	Logic High	VIH	Start up	1.0			V
CE Pull-down	Resistance	R <sub>CE</sub>			5		MΩ
Output Nois	e Voltage	e <sub>NO</sub>	10Hz to100KHz, I <sub>OUT</sub> =1mA		45		$\mathrm{uV}_{\mathrm{RMS}}$
Power Supply	f=1kHz (VOUT≤3.3V)		0.2V <sub>P-P</sub> Ripple		70		
Rejection Ratio	f=1kHz (VOUT>3.3V)	PSRR	I <sub>OUT</sub> =100mA		60		dB
Thermal Shutdow	Thermal Shutdown Temperature		Shutdown, Temp increasing		165		°C
Thermal Shutdor	wn Hysteresis	T <sub>SD</sub> T <sub>SDHY</sub>			30		°C
Output Discharg		R <sub>DSC</sub>			50		Ω

**Note 5:** 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note 6: This IC includes two kinds of output voltage accuracy versions. A: ±1%, B: ±2%.

Note 7: The required minimum input operating voltage is equal to  $V_{OUT}+V_{DROP}$ , and if  $V_{OUT}+V_{DROP}$  <2.5V, the required minimum input operating voltage must be set to 2.5V.  $V_{OUT}$  is the normal output voltage, e.g.  $V_{OUT}$ =2.8V for 2.8V fixed output version.

**Note 8:** Line regulation is calculated by  $\Delta V_{LINE} = \left(\frac{V_{OUT1} - V_{OUT2}}{\Delta V_{DD} \times V_{OUT}}\right) \times 100$ 

Where  $V_{OUT1}$  is the output voltage when  $V_{DD1}$ =6.0V,  $V_{OUT2}$  is the output voltage when  $V_{DD2}$ = max ( $V_{OUT}$ +0.5V, 2.5V).  $\triangle V_{DD}$ = $V_{DD1}$ - $V_{DD2}$ .

**Note 9:** Load regulation is calculated by  $\Delta V_{LOAD} = V_{OUT1} - V_{OUT2}$ Where V<sub>OUT1</sub> is the output voltage when I<sub>OUT1</sub>=1mA, and V<sub>OUT2</sub> is the output voltage when I<sub>OUT2</sub>=1.0A. **Note 10:** The temperature coefficient is calculated by  $TC_{V_{OUT}} = \frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$ .



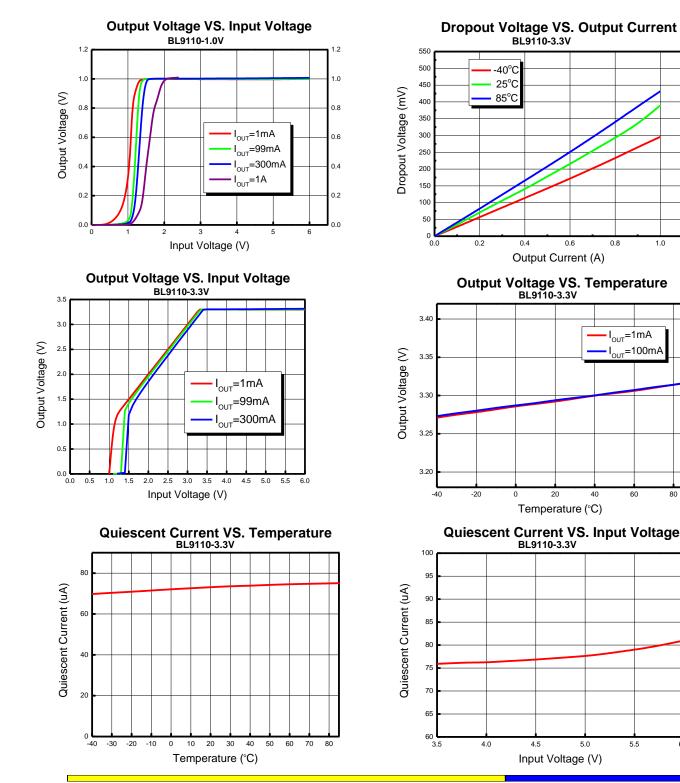
1.0

80

1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

### **Typical Performance Characteristic**

 $(V_{DD}=V_{OUT}+1V)$ , and if  $V_{OUT}<1.5V$ ,  $V_{DD}=2.5V$  CE= $V_{DD}$ ,  $C_{IN}=2.2\mu$ F,  $C_{OUT}=2.2\mu$ F,  $T_A=25^{\circ}$ C, unless otherwise noted.)



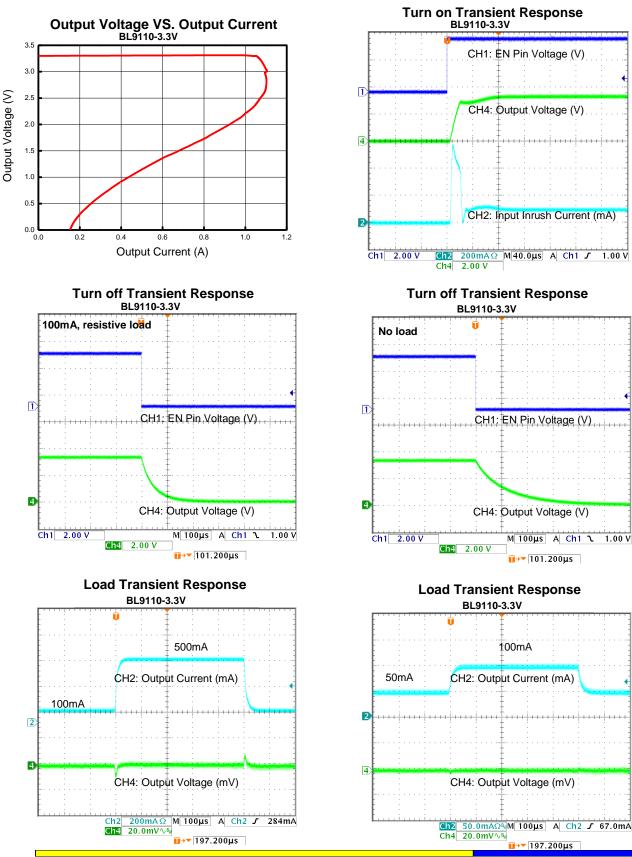
PPMIC BU BL9110 Rev 2.0 04/2016

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6.0



1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

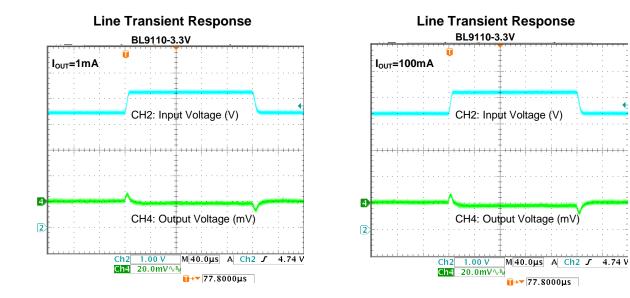


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1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator





### **Applications Information**

The BL9110 is a low dropout CMOS-based positive voltage regulator that operates the input voltage from +2.5V to 6.0V. Output voltages are optional ranging from 1.0V to 5.0V, and can supply current up to 1.0 A.

#### **Enable Function**

The BL9110 is shutdown by pulling the CE input low, and turn on by driving the input high. If this feature is not be used, the CE input should be floating or tied to VDD to keep the regulator on at all times.

## Programming the BL9110 Adjustable LDO regulator

The BL9110 is available in two types, either fixed or adjustable output voltage. The output range of the adjustable types is from 1V to 5V. The output voltage of the BL9110 adjustable regulator is programmed using an external resistor divider as show in Figure as below. The output voltage is calculated using equation as below:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

Where  $V_{REF}=1V$  is the internal reference voltage.

Resistors R1 and R2 should be chosen for approximately 50uA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current at ADJ increases the output voltage error. The recommended design procedure is to choose R2=20k $\Omega$  to set the divider current at 50uA, and then calculate R1 using Equation as below:

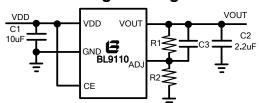
$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2$$

A small compensation capacitor C3 placed between VOUT and ADJ may improve the stability of the adjustable. The suggested value of this capacitor is about 10pF to 22pF.

OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGTE	R1	R2
1.8V	16 kΩ	20 kΩ
2.5V	30 kΩ	20 kΩ
3.3V	51 kΩ	22 kΩ
3.6V	62 kΩ	24 kΩ

#### BL9110 Adjustable LDO regulator Programming



#### **Thermal Protection**

Thermal overload protection limits total power dissipation in the BL9110. When the junction temperature exceeds  $T_J=165^{\circ}C$ , the OTP circuit starts the thermal shutdown function and turns the pass element off allowing the IC to cool. The OTP circuit turns on the pass element again after IC's junction temperature cool by 30°C, result in a pulsed output during continuous thermal





overload conditions. Thermal-overloaded protection is designed to protect the BL9110 in the event of fault conditions. Do not exceed the absolute maximum junction temperature rating of T<sub>J</sub>=125°C for continuous operation. The build-in fold-back current limit protection circuit will reduce current value as output voltage drops. When output is shorted to ground, current limit is reduced to 250mA, avoiding damaging the device.

## Operating Region and Power Dissipation

The maximum power dissipation of BL9110 depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipation across the device is

 $P_{D} = (V_{DD} - V_{OUT}) \times I_{OUT} + V_{DD} \times I_{Q}$ 

The maximum power dissipation is:

 $P_{D}(MAX) = (T_{J}(MAX) - T_{A}) / \theta_{JA}$ 

Where  $T_J$  (MAX) is the maximum operation junction temperature 125°C,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance. The GND pin of the BL9110 performs the dual function of providing an electrical connection to ground and channeling heat away. Connect the GND pin to ground using a large pad or ground plane.

## Capacitor Selection and Regulator Stability

Like any low-dropout regulator, the external

1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

capacitors used with the BL9110 must be carefully selected for regulator stability and performance. The BL9110 requires an output capacitor between the VOUT and GND pins for phase compensation. Using a capacitor whose value is ≥1µF on the BL9110 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance ESR and in all LDO applications. The BL9110 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. In the BL9110, phase compensation is made with the output capacitor for securing stable operation even if the load current is varied. For this purpose, use a 2.2uF capacitor between VOUT pin and GND pin as close as possible.

#### **Load-Transient Considerations**

The BL9110 load-transient response graphs show two components of the output response: a DC shift from the output impedance due to the load current change, and the transient response. The DC shift is quite small due to the excellent load regulation of the IC. Typical output voltage transient spike for a step change in the load current from 0mA to 50mA is tens of mV,



depending on the ESR of the output capacitor. Increasing the output capacitor's value and decreasing the ESR attenuates the overshoot.

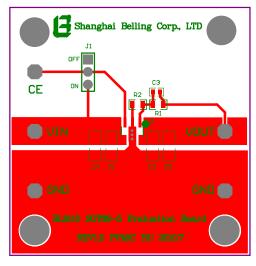
#### Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems. this will determine the useful end-of-life battery voltage. Because the BL9110 uses a P-Channel MOSFET pass transistor, the function dropout voltage is а of drain-to-source on resistance [R<sub>DS(ON)</sub>] multiplied by the load current.

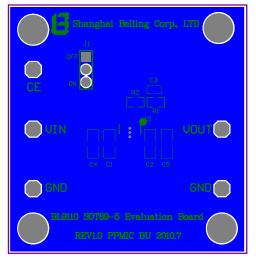
**BL9110 SOT89-5 PCB Layout for Reference** 

#### Layout Considerations

To improve AC performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for VDD and VOUT, with each ground plane connected only at the GND pin of the device. Make VDD and GND lines sufficiently wide. If their impedance is high, noise pickup or unstable operation may result. Connect a capacitor C1 between VDD and GND pin, as close as possible to the pins. Set external components, especially the output capacitor C2, as close as possible to the IC, and make wiring as short as possible.



Top Layer

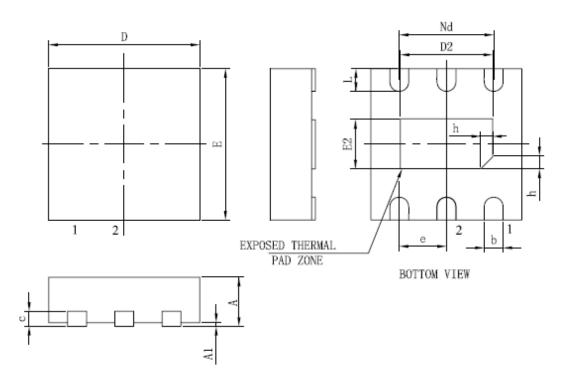


Bottom Layer



### **Package Description**

DFN-6

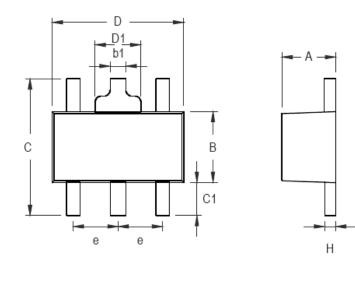


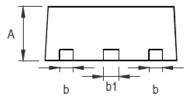
	Dimensions In Millimeters				
Symbol					
	Min NOM		Max		
А	0.7	0.75	0.8		
A1		0.02	0.05		
b	0.25	0.3	0.35		
С	0.18	0.2	0.25		
D	1.95	2	2.05		
D2	1		1.45		
е		0.65BSC			
Nd		1.30BSC			
E	1.95	2	2.05		
E2	0.50		0.85		
L	0.25	0.30	0.40		
h	0.1	0.15	0.2		

**DFN-6 Surface Mount Package** 



SOT89-5





Symbol	Dimensions I	n Millimeters	<b>Dimensions In Inches</b>		
	Min	Max	Min	Max	
А	1.397	1.600	0.055	0.063	
b	0.356	0.508	0.014	0.020	
b1	0.406	0.533	0.016	0.021	
В	2.388	2.591	0.094	0.102	
С	3.937	4.242	0.155	0.167	
C1	0.787	1.194	0.031	0.047	
D	4.394	4.597	0.173	0.181	
D1	1.397	1.702	0.055	0.067	
е	1.500 TYP.		0.060 TYP.		
Н	0.356	0.432	0.014	0.017	

SOT89-5 Surface Mount Package



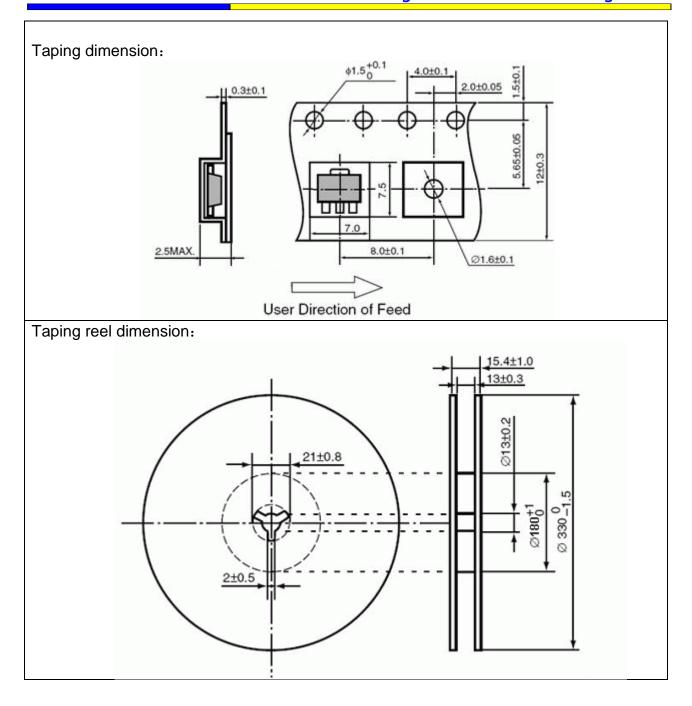
1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

SOT-223-3

Package	SOT-223	Devices pe	er reel	2500	Un	it	mm	า
Package specifi	ication:						1	
Ç	Ç		J	Ţ)		MIN	NOM	MAX
	· · · ·	Ī		°.	А	1.50	1.65	1.80
				171	A1	0.02	0.06	0.10
					A2	1.45	1.60	1.75
			_	E1(BTM)	A3	0.80	0.90	1.00
				E1(E	b	0.67	-	0.80
					b1	0.66	0.71	0.75
					b2	2.96	-	3.09
			J)	θ	b3	2.95	3.00	3.05
					С	0.30	-	0.35
5 L I			L2		c1	0.29	0.30	0.31
e	e1 e	<b>⊕</b> 0.10		Ĺ.	D	6.35	-	7.05
	2				D1	6.30	6.50	6.70
	— D ———	-A3			E	6.80	7.00	7.20
0,			<b>⊦</b> ∎—h		E1	3.40	3.50	3.60
			<mark>⊢</mark> b1		е		2.30BSC	
					e1	2	1.60BSC	
	0.08	A1			L	0.80	1.00	1.20
4	-D1(BTM)	◄	SECTIC	N D-D	L1		I.75REF	
٥ <b>-</b>	b3	- C			L2		).25BSC	
					θ	0°	-	8°
S	SECTION C-C				θ1	10°	12°	14°



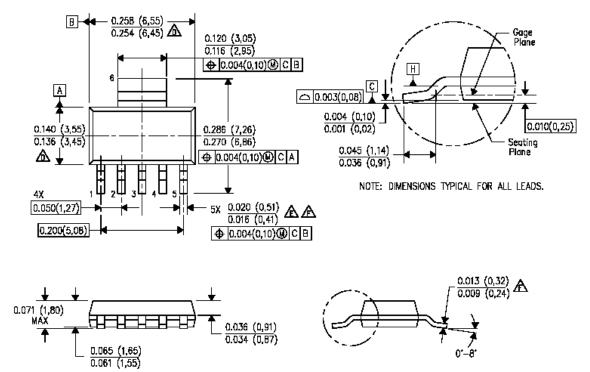
1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator





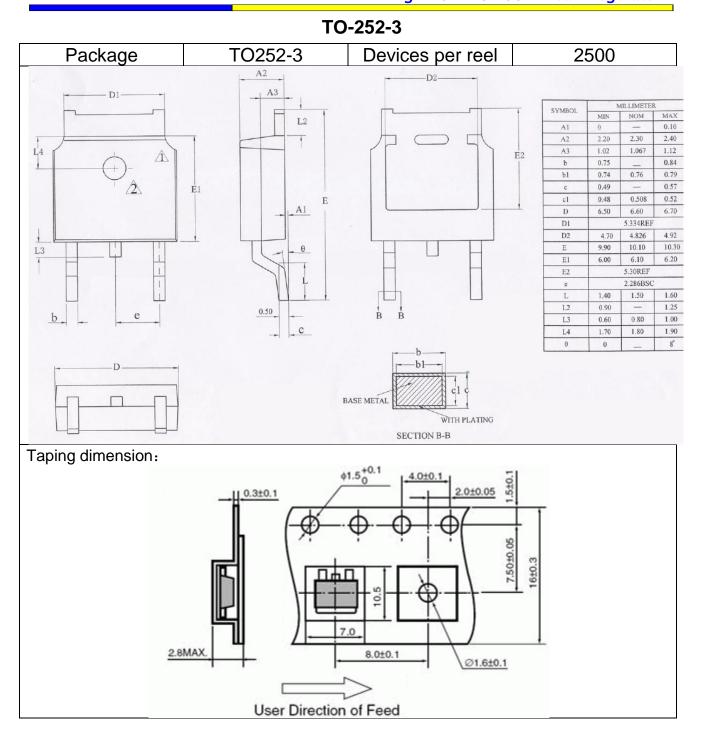
1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

SOT-223-5



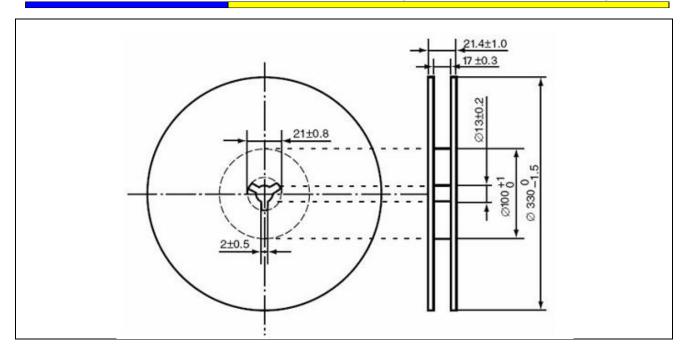


1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator





1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

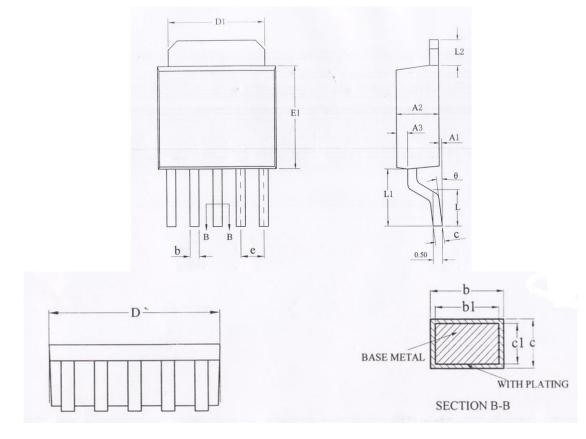


#### TO-252-5

PPMIC BU BL9110 Rev 2.0 04/2016



1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator

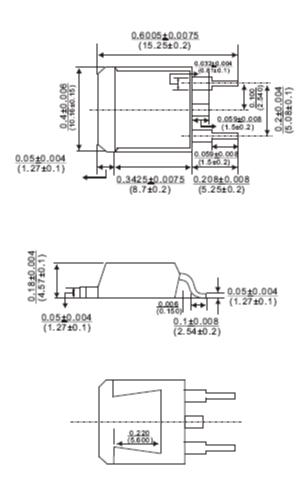


Symbol	Dimensions In Millimeters				
Symbol	MIN	NOM	MAX		
A1	0.05	0.15	0.25		
A2	2.1	2.3	2.5		
A3	0.5	0.6	0.7		
b	0.46		0.6		
b1	0.45	0.5	0.55		
С	0.49		0.56		
c1	0.48	0.5	0.52		
D	6.3	6.5	6.7		
D1	5.30 REF				
E1	5.30	5.50	5.70		
е		1.27BSC			
L	1.40	1.50	1.60		
L1	3.0	3.1	3.2		
L2	1.40BSC				
Θ	0		8°		

### TO-263-3

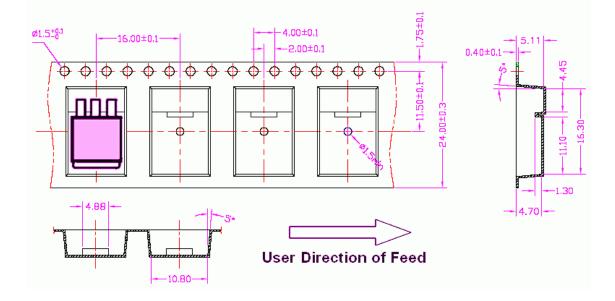


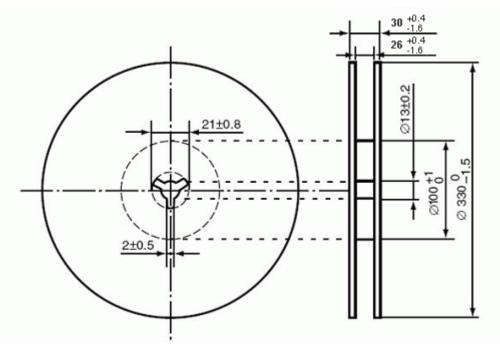
TO-263





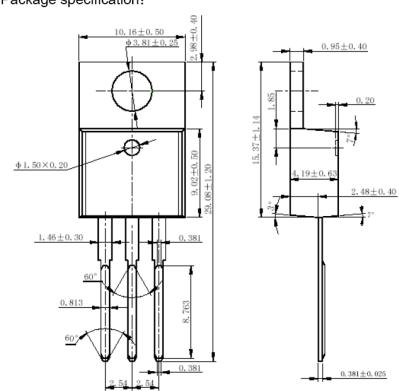
1A Low Dropout, Low Quiescent Current High PSRR CMOS Linear Regulator







TO-220-3

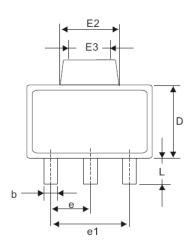


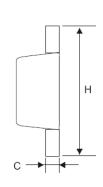
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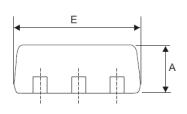


### SOT-89-3

SOT-89-3L



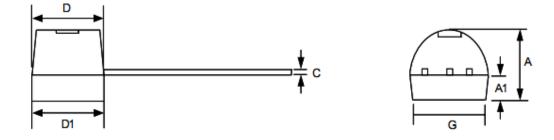




SYMBOL	MILLIM	ETERS	INCHES		
	MIN	MAX	MIN	MAX	
А	1.450	1.500	0.057	0.061	
b	0.440	0.480	0.017	0.019	
С	0.360	0.400	0.014	0.016	
E	4.450	4.550	0.175	0.179	
E2	1.500	1.700	0.059	0.067	
E3	1.400 Ref		0.055 Ref		
е	1.500 BS C		0.059 BS C		
e1	3.000 BS C		0.118 BSC		
D	2.450	2.550	0.096	0.100	
Н	4.150	4.250	0.163	0.167	
L	0.900	1.100	0.035	0.043	



TO92-3



#### TO-92 (TD) Package

SYMBOL	MILLIMETER		INCH		
STMBOL	MIN	MAX	MIN	MAX	
А	3.35	3.86	0.132	0.152	
A1	1.0414	1.55	0.041	0.061	
b	0.254	0.508	0.010	0.020	
E	4.34	4.85	0.171	0.191	
С	0.254	0.508	0.010	0.020	
L	14.53	15.04	0.572	0.592	
е	1.143	1.397	0.045	0.055	
G	3.683	4.191	0.145	0.165	
D	4.29	4.80	0.169	0.189	
D1	4.34	4.85	0.171	0.191	