

General Description

The WSP4409 is the highest performance trench P-Ch MOSFET with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The WSP4409 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Product Summery

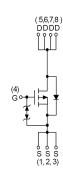
BVDSS	RDSON	ID
-30V	5.0mΩ	-17.6A

Applications

Power Management in Notebook Computer,
Portable Equipment and Battery Powered Systems.

SOP-8 Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±20	V
I _D @T _c =25℃	Continuous Drain Current, V _{GS} @ -10V ¹	-17.6	Α
I _D @T _c =70°C	Continuous Drain Current, V _{GS} @ -10V ¹	-14	А
I _{DM}	300uS Pulsed Drain Current ²	-70	А
EAS	Single Pulse Avalanche Energy ³	72	mJ
I _{AS}	Avalanche Current	-38	Α
P _D @T _A =25°C	Total Power Dissipation⁴	4.2	W
T _{STG}	Storage Temperature Range	-55 to 150	$^{\circ}$
T_J	Operating Junction Temperature Range -55 to 150		$^{\circ}$

Thermal Data

Symbol	Parameter	Тур.	Max.	Unit
R _{0JA}	Thermal Resistance Junction-Ambient ¹		75	°C/W
$R_{ heta JC}$	Thermal Resistance Junction-Case ¹		24	°C/W



Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =-250uA	-30			V
$\triangle BV_{DSS}/\triangle T_{J}$	BV _{DSS} Temperature Coefficient	Reference to 25℃ , I _D =-1mA		-0.018		V/℃
D	Static Drain-Source On-Resistance ²	V _{GS} =-10V , I _D =-17.6A		5	7.2	0
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-4.5V , I _D =-10A		9	12	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} . I _D =-250uA	-1.3	-1.8	-2.3	V
$\triangle V_{GS(th)}$	V _{GS(th)} Temperature Coefficient	V _{GS} =V _{DS} , I _D =-2500A		5.04		mV/℃
,	Drain Source Leakage Current	V _{DS} =-24V , V _{GS} =0V , T _J =25℃			-1	
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V , V _{GS} =0V , T _J =55℃			-5	– uA
I _{GSS}	Gate-Source Leakage Current	V_{GS} = $\pm 20V$, V_{DS} = $0V$			±100	nA
gfs	Forward Transconductance	V _{DS} =-5V , I _D =-10A		18		S
Qg	Total Gate Charge (-4.5V)			45		
Q_{gs}	Gate-Source Charge	V _{DS} =-15V,V _{GS} =-4.5V,I _D =-17.6A		5		nC
Q_{gd}	Gate-Drain Charge			12.7		
T _{d(on)}	Turn-On Delay Time			12		
Tr	Rise Time	V_{DD} =-15V, V_{GS} =-10V, R_{G} =6 Ω ,		14		20
T _{d(off)}	Turn-Off Delay Time	I _D =-1A ,RL=15Ω		98		- ns -
T _f	Fall Time			60		
C _{iss}	Input Capacitance			2110		
Coss	Output Capacitance	V _{DS} =-15V , V _{GS} =0V , f=1MHz		450		pF
C _{rss}	Reverse Transfer Capacitance			330		

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	V _{DD} =-25V , L=0.5mH , I _{AS} =-38A	60			mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
I _S	Continuous Source Current ^{1,6}	V _G =V _D =0V , Force Current			-4.0	Α
I _{SM}	Pulsed Source Current ^{2,6}				-70	Α
V_{SD}	Diode Forward Voltage ²	V _{GS} =0V , I _S =-1A , T _J =25℃			-1.1	V
t _{rr}	Reverse Recovery Time	-IF=-17.6A,dI/dt=100A/μs,T _J =25℃		24		nS
Qrr	Reverse Recovery Charge			16		nC

Note:

- 1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, t<10sec.
- 2.The data tested by pulsed , pulse width $\,\leq\,300\text{us}$, duty cycle $\,\leq\,2\%$
- 3.The EAS data shows Max. rating . The test condition is VDD=-25V,VGS=-10V,L=0.5mH,IAS=-38A
- 4.The power dissipation is limited by 150 $^{\circ}\mathrm{C}$ junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.



Typical Characteristics

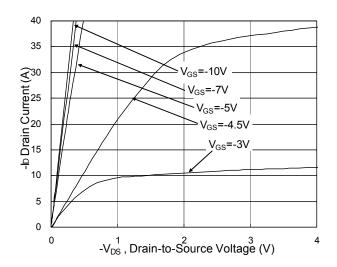


Fig.1 Typical Output Characteristics

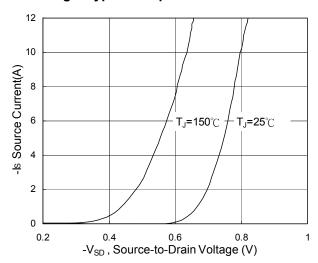


Fig.3 Forward Characteristics Of Reverse

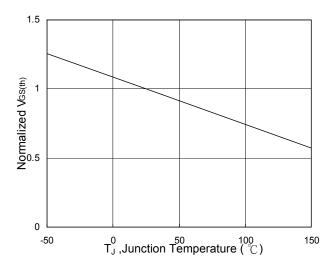


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

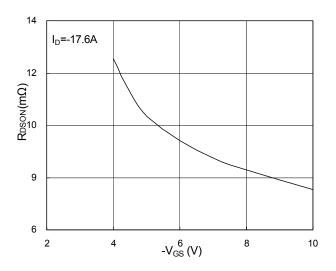


Fig.2 On-Resistance v.s Gate-Source

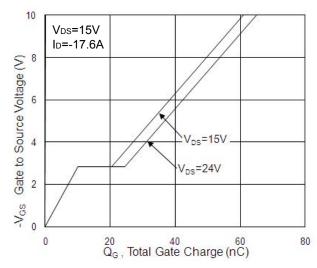


Fig.4 Gate-Charge Characteristics

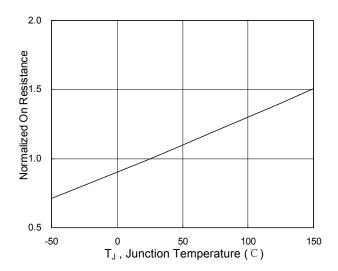
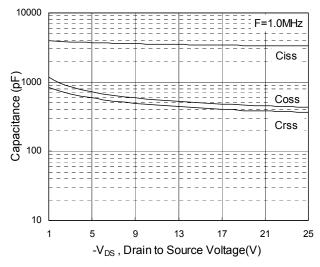


Fig.6 Normalized R_{DSON} vs. T_J





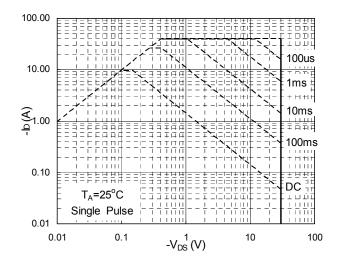


Fig.7 Capacitance

Fig.8 Safe Operating Area

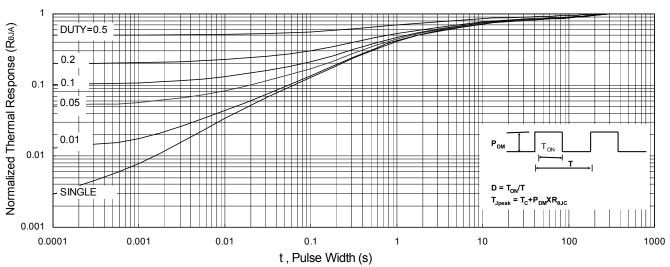


Fig.9 Normalized Maximum Transient Thermal Impedance

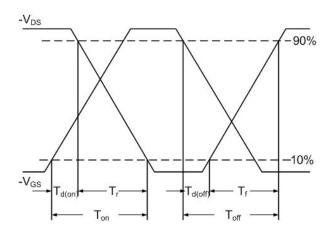


Fig.10 Switching Time Waveform

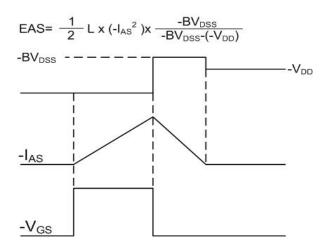


Fig.11 Unclamped Inductive Switching Waveform



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