

General Description

The WST2033 is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide excellent R_{DS(on)} and gate charge for most of the small power switching and load switch applications.

The WST2033 meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available

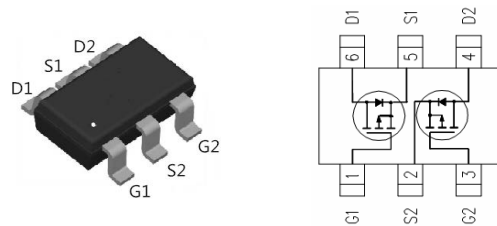
Product Summary

BVDSS	R _{DS(on)}	I _D
-20V	37mΩ	-4.5A

Applications

- High Frequency Point-of-Load Synchronous Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOT-23-6L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		10s	Steady State	
V _{DS}	Drain-Source Voltage	-20		V
V _{GS}	Gate-Source Voltage	± 12		V
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ -4.5V ¹	-5.6	-4.5	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ -4.5V ¹	-4.6	-3.5	A
I _{DM}	Pulsed Drain Current ²	-14		A
P _D @T _A =25°C	Total Power Dissipation ³	1.5	1.1	W
P _D @T _A =70°C	Total Power Dissipation ³	1.0	0.6	W
T _{STG}	Storage Temperature Range	-55 to 150		°C
T _J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	125	°C/W
R _{θJA}	Thermal Resistance Junction-Ambient ¹ (t ≤ 10s)	---	95	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	80	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.011	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-4.5V, I_D=-2A$	---	37	51	$\text{m}\Omega$
		$V_{GS}=-2.5V, I_D=-1A$	---	54	74	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.5	-0.7	-1.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	3.95	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-16V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{DS}=-16V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-2A$	---	8.5	---	S
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-2A$	---	28	31.3	nC
Q_{gs}	Gate-Source Charge		---	2.5	3.7	
Q_{gd}	Gate-Drain Charge		---	4	5.9	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V,$ $V_{GS}=-4.5V, R_G=3.3\Omega,$ $I_D=-1A$	---	7	---	ns
T_r	Rise Time		---	6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	95	---	
T_f	Fall Time		---	60	---	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	1355	---	pF
C_{oss}	Output Capacitance		---	225	---	
C_{rss}	Reverse Transfer Capacitance		---	150	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	-1.7	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	-14	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F=-2A, dI/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	22	---	nS
Q_{rr}	Reverse Recovery Charge		---	16	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper, $t < 10\text{sec}$.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

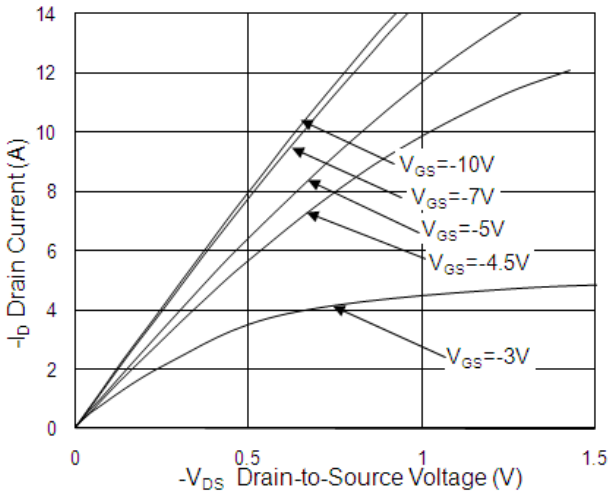


Fig.1 Typical Output Characteristics

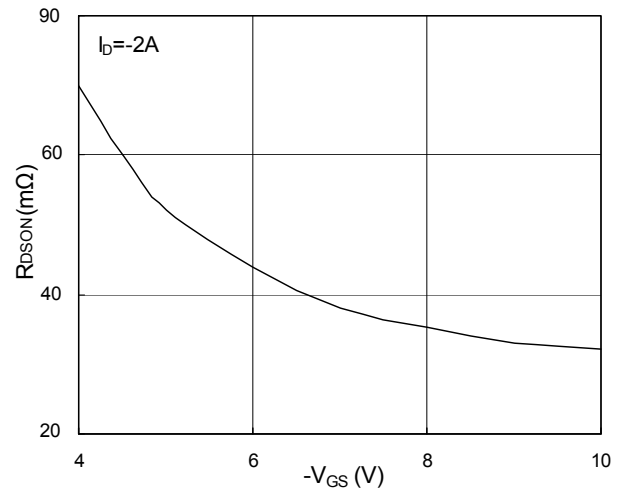


Fig.2 On-Resistance vs. G-S Voltage

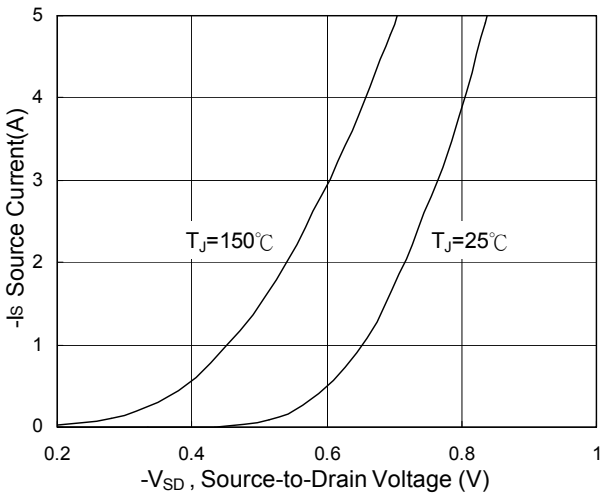


Fig.3 Forward Characteristics Of Reverse

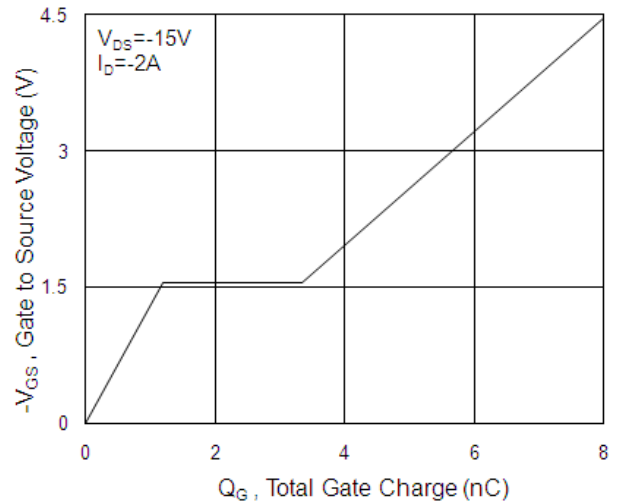


Fig.4 Gate-Charge Characteristics

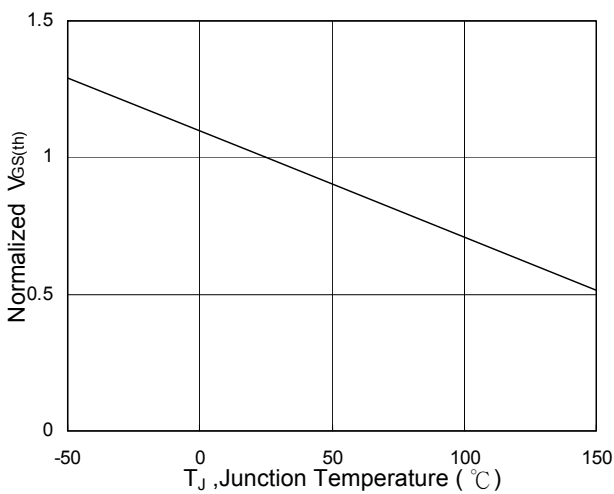


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

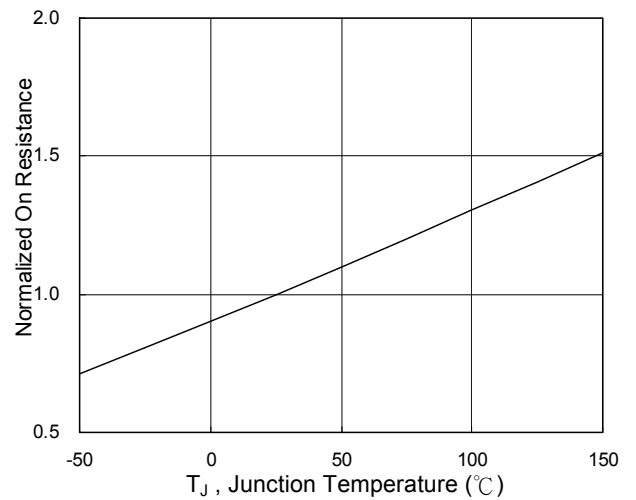


Fig.6 Normalized $R_{DS(ON)}$ vs. T_J

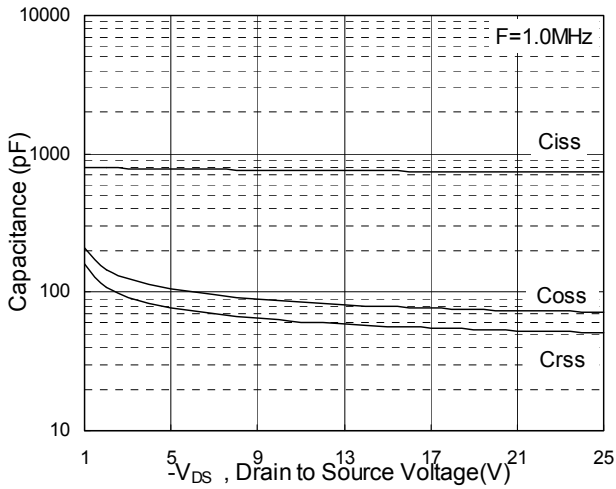


Fig.7 Capacitance

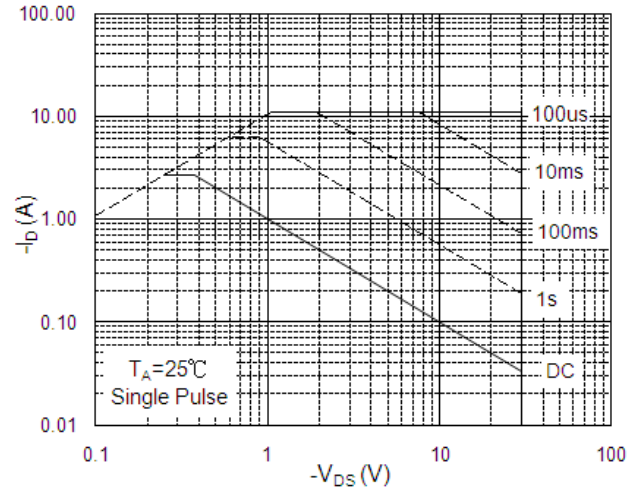


Fig.8 Safe Operating Area

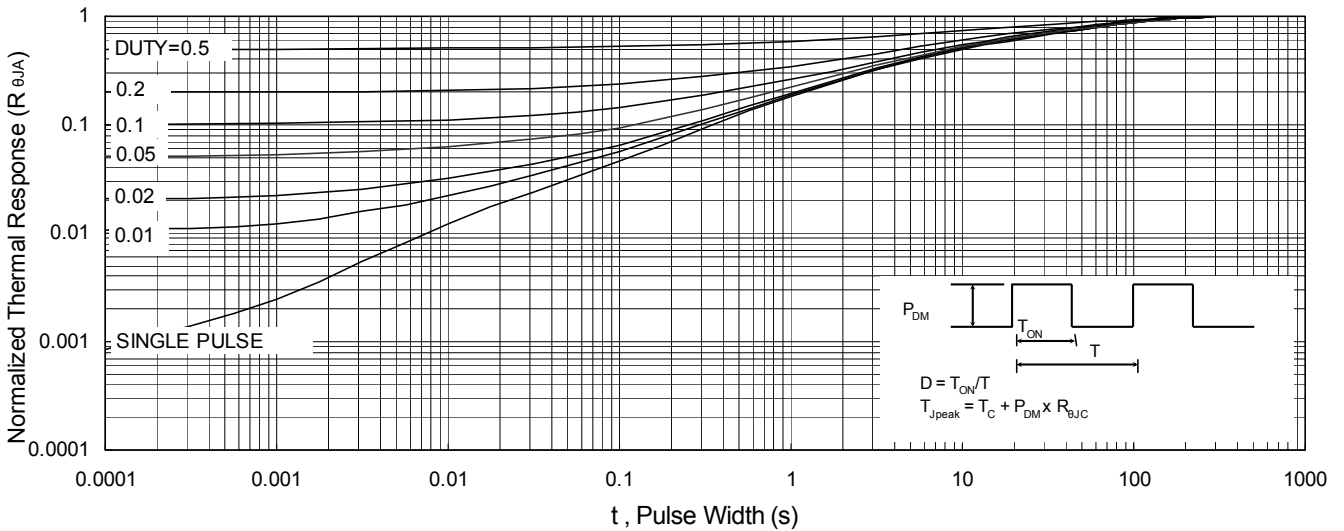


Fig.9 Normalized Maximum Transient Thermal Impedance

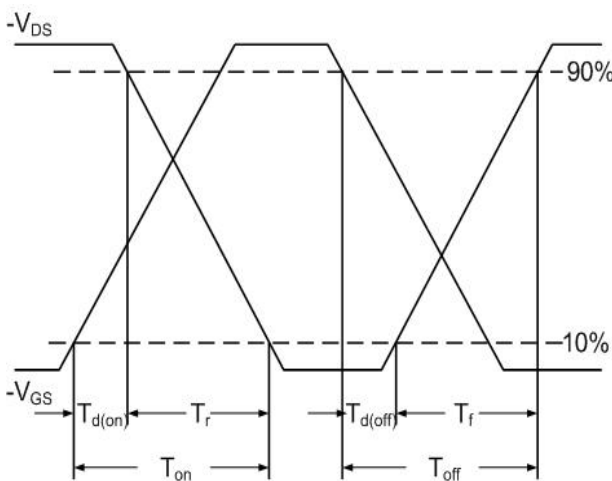


Fig.10 Switching Time Waveform

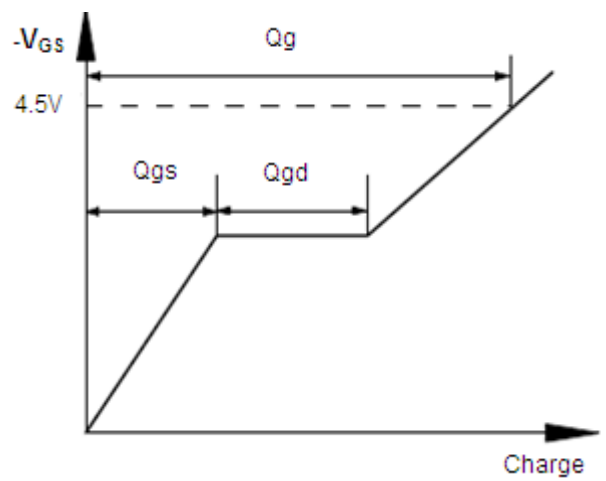


Fig.11 Gate Charge Waveform



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