TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LCX05F, TC74LCX05FK

Low-Voltage HEX Inverter with 5-V Tolerant Inputs and Outputs (open-drain)

The TC74LCX05 is a high-performance CMOS inverter.

Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

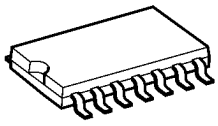
Pin configuration and function are the same as the TC74LCX04, but the TC74LCX05F/FK has high performance MOS N-channel transistor. (open-drain outputs)

The device is designed for low-voltage (3.3 V) V_{CC} applications, but it could be used to interface to 5-V supply* environment for inputs.

All inputs are equipped with protection circuits against static discharge.

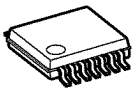
*I_{OUT} absolute maximum rating must be observed.

TC74LCX05F



SOP14-P-300-1.27A

TC74LCX05FK



VSSOP14-P-0030-0.50

Weight

SOP14-P-300-1.27A : 0.18 g (typ.)

VSSOP14-P-0030-0.50 : 0.02 g (typ.)

Features

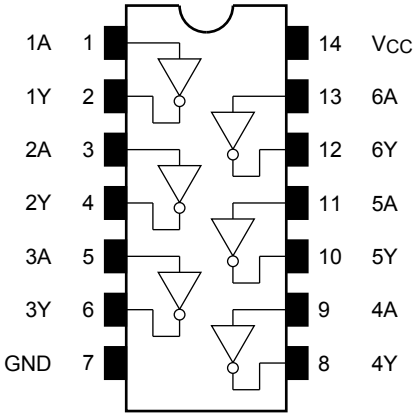
- Low-voltage operation: V_{CC} = 1.65 to 5.5 V
- High-speed operation: t_{pz} = 5.0 ns (max) (V_{CC} = 3.0 to 3.6 V)
- Output current: I_{OL} = 24 mA (min) (V_{CC} = 3.0 V)
- Latch-up performance: >−500 mA
- Available in JEITA SOP, VSSOP (US)
- Open-drain outputs
- Power-down protection is provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 05 type

Note: The Electrical Characteristics of V_{CC} = 1.8 ± 0.15 V and that of V_{CC} = 5.0 ± 0.5 V are only applicable for products which manufactured from January 2009 onward.

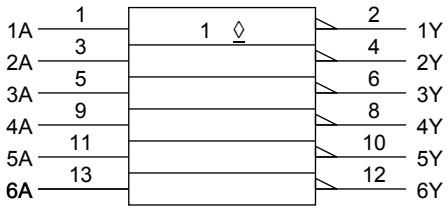
Start of commercial production

1999-10

Pin Assignment (top view)



IEC Logic Symbol

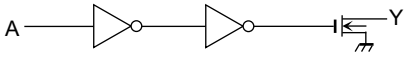


Truth Table

Inputs	Outputs
A	Y
L	Z
H	L

Z: High impedance

System Diagram (per gate)



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to 7.0 (Note 2)	V
Input diode current	I_{IK}	−50	mA
Output diode current	I_{OK}	−50 (Note 3)	mA
DC output current	I_{OUT}	50	mA
Power dissipation	P_D	180	mW
DC V_{CC}/ground current	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in OFF state. I_{OUT} absolute maximum rating must be observed (Output in low state)

Note 3: $V_{OUT} < GND$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.65 to 5.5	V
		1.5 to 5.5 (Note 2)	
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to 5.5	V
Output current	I_{OL}	32 (Note 3)	mA
		24 (Note 4)	
		12 (Note 5)	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 6)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 2: Data retention only

Note 3: V_{CC} = 4.5 to 5.5 V

Note 4: V_{CC} = 3.0 to 3.6 V

Note 5: V_{CC} = 2.7 to 3.0 V

Note 6: V_{CC} = 1.65 to 5.5 V

Electrical Characteristics

DC Characteristics (Ta = –40 to 85°C)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		1.65 to 2.3	V_{CC} × 0.9	—	V
					2.3 to 2.7	1.7	—	
					2.7 to 3.6	2.0	—	
					4.5 to 5.5	V_{CC} × 0.7	—	
	L-level	V_{IL}	—		1.65 to 2.3	—	V_{CC} × 0.1	
					2.3 to 2.7	—	0.7	
					2.7 to 3.6	—	0.8	
					4.5 to 5.5	—	V_{CC} × 0.3	
Output voltage	L-level	V_{OL}	V_{IN} = V_{IH}	I_{OL} = 100 μA	1.65 to 5.5	—	0.2	V
				I_{OL} = 4 mA	1.65	—	0.45	
				I_{OL} = 8 mA	2.3	—	0.7	
				I_{OL} = 12 mA	2.7	—	0.4	
				I_{OL} = 16 mA	3.0	—	0.4	
				I_{OL} = 24 mA	3.0	—	0.55	
				I_{OL} = 32 mA	4.5	—	0.55	
Input leakage current		I_{IN}	V_{IN} = 0 to 5.5 V		1.65 to 5.5	—	±5.0	μA
Output OFF state current		I_{OZ}	V_{IN} = V_{IH}, V_{OUT} = 0 to 5.5 V		1.65 to 5.5	—	±5.0	μA
Power-off leakage current		I_{OFF}	V_{IN}/V_{OUT} = 5.5 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		1.65 to 5.5	—	10.0	μA
Increase in Icc per input		ΔI_{CC}	V_{IH} = V_{CC} – 0.6 V (per 1 input)		2.7 to 3.6	—	500	
					4.5 to 5.5	—	1	mA

AC Characteristics (Ta = –40 to 85°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Output enable time	t_{pZL}	Figure 1, Figure 2	1.8 ± 0.15	1.5	26.0	ns
			2.5 ± 0.2	1.2	13.0	
			2.7	1.0	6.0	
			3.3 ± 0.3	0.8	5.0	
			5.0 ± 0.5	0.5	4.0	
Output disable time	t_{pLZ}	Figure 1, Figure 2	1.8 ± 0.15	1.5	26.0	ns
			2.5 ± 0.2	1.2	13.0	
			2.7	1.0	6.0	
			3.3 ± 0.3	0.8	5.0	
			5.0 ± 0.5	0.5	4.0	
Output to output skew	t_{osZL}	(Note)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

Note: Parameter guaranteed by design.
($t_{osZL} = |t_{pZLm} - t_{pZLn}|$)

Dynamic Switching Characteristics (Ta = 25°C, input: $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500\ \Omega$)

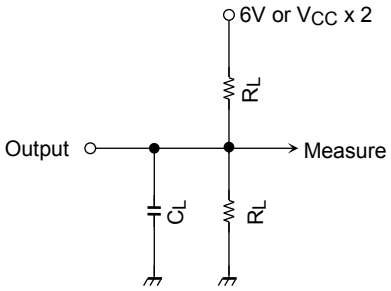
Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V
Quiet output minimum dynamic V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	3.3	7	pF
Output capacitance	C_{OUT}		3.3	8	pF
Power dissipation capacitance	C_{PD}	f_{IN} = 10 MHz (Note)	3.3	5	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
I_{CC} (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per gate)

AC Test Circuit



Parameter	Switch	
t_{pLZ}, t_{pZL}	6.0 V	@ V_{CC} = 3.3 ± 0.3 V @ V_{CC} = 2.7 V
	V_{CC} × 2	@ V_{CC} = 5.0 ± 0.5 V @ V_{CC} = 2.5 ± 0.2 V @ V_{CC} = 1.8 ± 0.15 V

Figure 1

AC Waveform

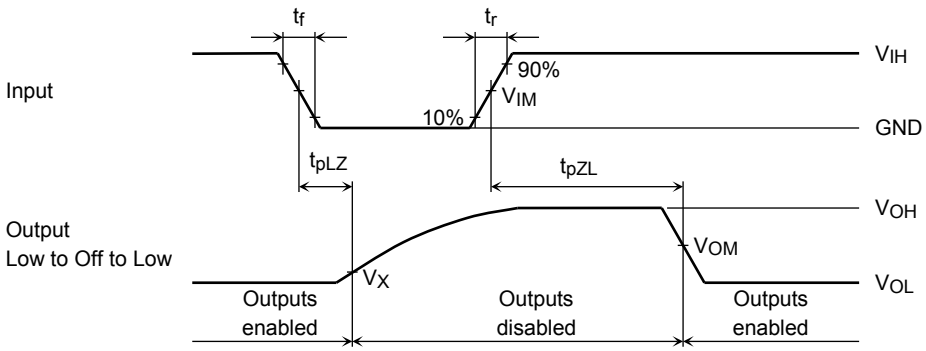
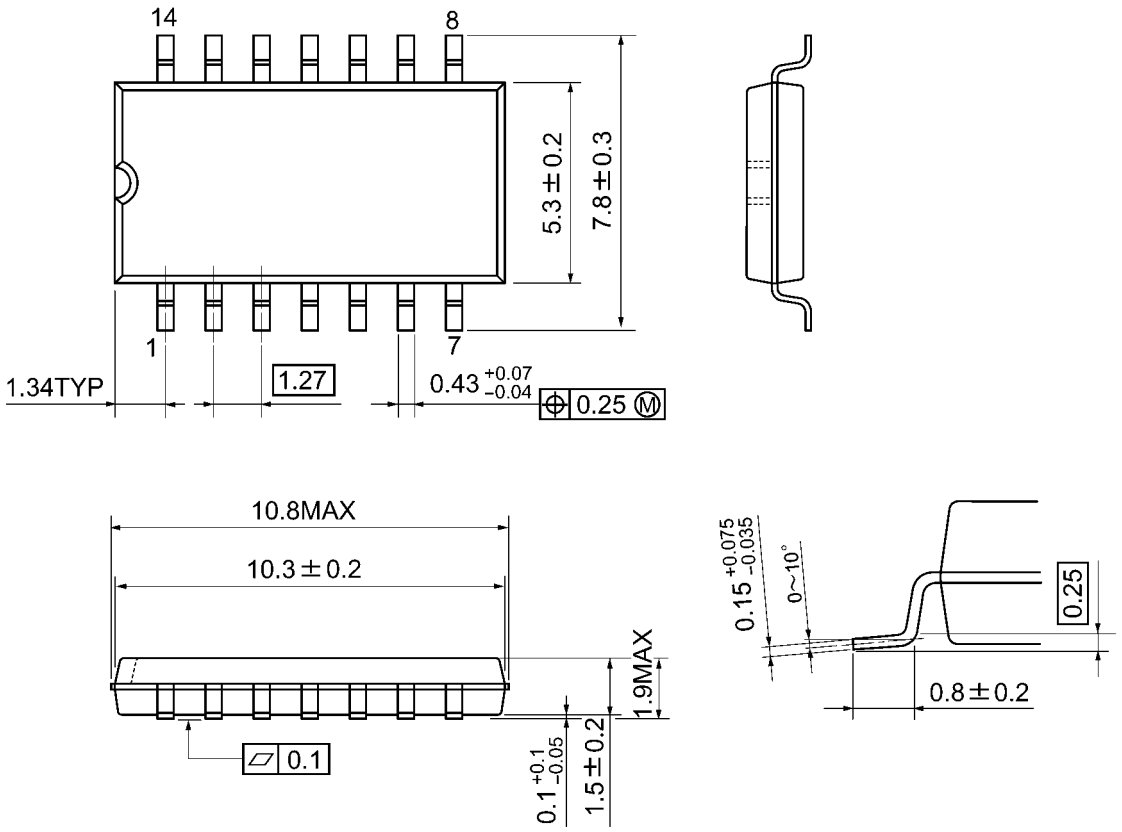


Figure 2 t_{pLZ}, t_{pZL}

	Symbol	V_{CC}			
		5.0 ± 0.5 V	3.3 ± 0.3 V 2.7V	2.5 ± 0.2 V	1.8 ± 0.15 V
Input	V_{IH}	V_{CC}	2.7 V	V_{CC}	V_{CC}
	V_{IM}	V_{CC}/2	1.5 V	V_{CC}/2	V_{CC}/2
	t_r, t_f	2.5 ns	2.5 ns	2.0 ns	2.0 ns
Output	V_{OM}	V_{CC}/2	1.5V	V_{OH}/2	V_{OH}/2
	V_X	V_{OL} +0.3 V	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
Load	C_L	50 pF	50 pF	30 pF	30 pF
	R_L	500 Ω	500 Ω	500 Ω	1 kΩ

Package Dimensions

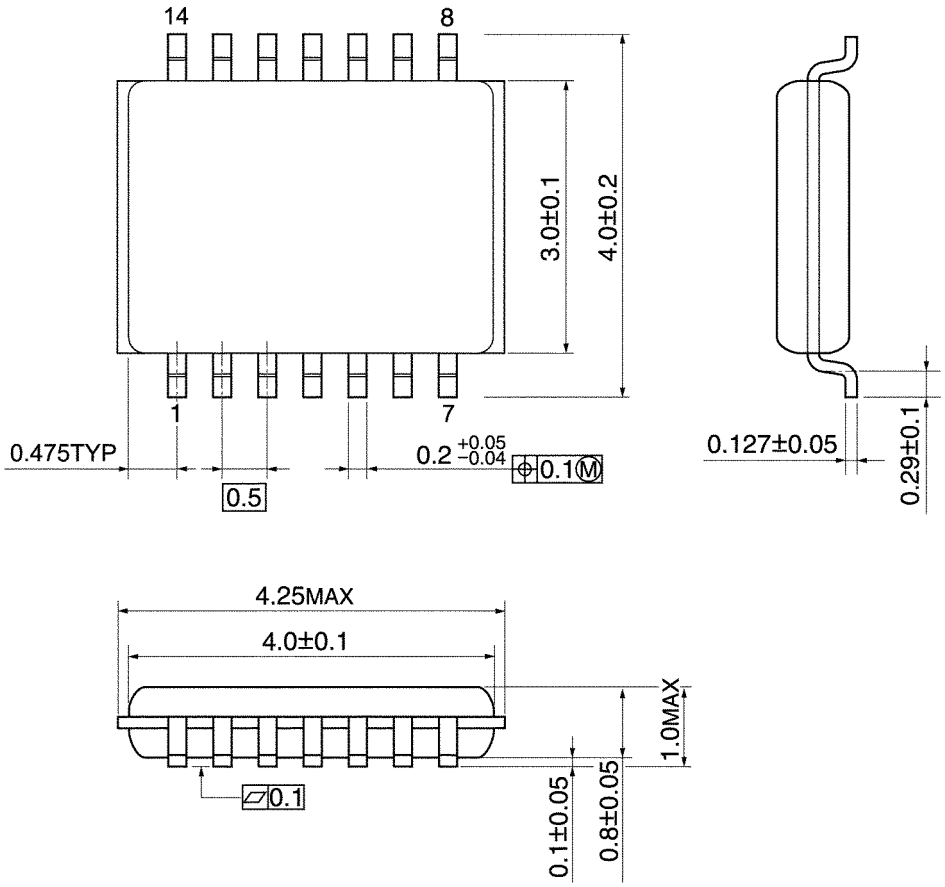
SOP14-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

Package Dimensions

VSSOP14-P-0030-0.50 Unit: mm



Weight: 0.02 g (typ.)

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