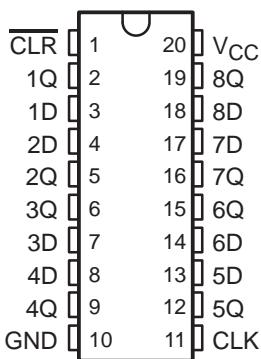


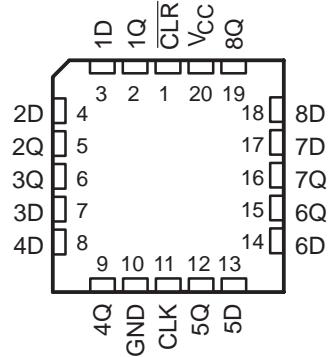
- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max

- Inputs Are TTL-Voltage Compatible
- Contain Eight D-Type Flip-Flops
- Direct Clear Input
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

SN54HCT273 . . . J OR W PACKAGE  
SN74HCT273 . . . DB, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HCT273 . . . FK PACKAGE  
(TOP VIEW)



### description/ordering information

These devices are positive-edge-triggered D-type flip-flops with a common enable input. The 'HCT273 devices are similar to the 'HCT377 devices, but feature a common clear enable (CLR) input instead of a latched clock.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. The circuits are designed to prevent false clocking by transitions at CLR.

### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 20	SN74HCT273N	SN74HCT273N
	SOIC – DW	Tube of 25	SN74HCT273DW	HCT273
		Reel of 2000	SN74HCT273DWR	
	SOP – NS	Reel of 2000	SN74HCT273NSR	HCT273
	SSOP – DB	Reel of 2000	SN74HCT273DBR	HT273
	TSSOP – PW	Tube of 70	SN74HCT273PW	HT273
		Reel of 2000	SN74HCT273PWR	
		Reel of 250	SN74HCT273PWT	
–55°C to 125°C	CDIP – J	Tube of 20	SNJ54HCT273J	SNJ54HCT273J
	CFP – W	Tube of 85	SNJ54HCT273W	SNJ54HCT273W
	LCCC – FK	Tube of 55	SNJ54HCT273FK	SNJ54HCT273FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

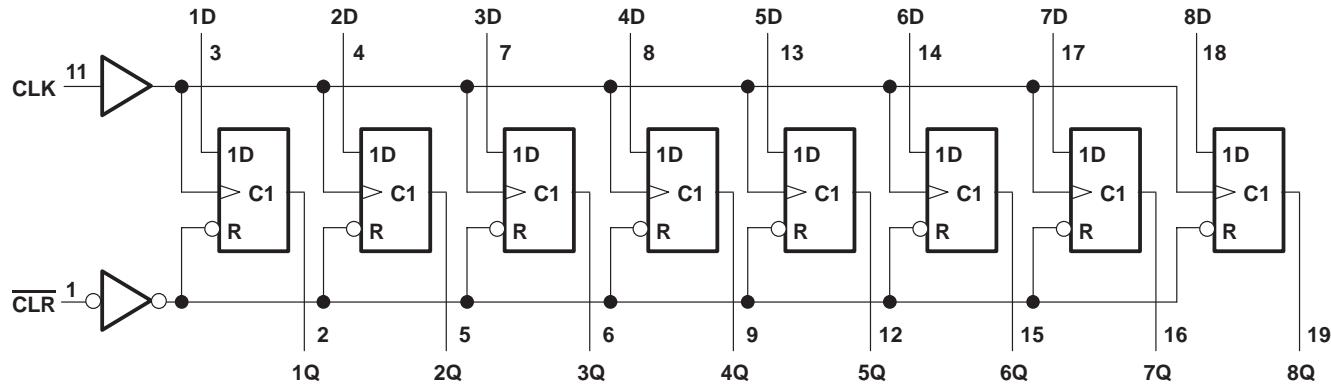
# SN54HCT273, SN74HCT273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCLS068E – NOVEMBER 1988 – REVISED AUGUST 2003

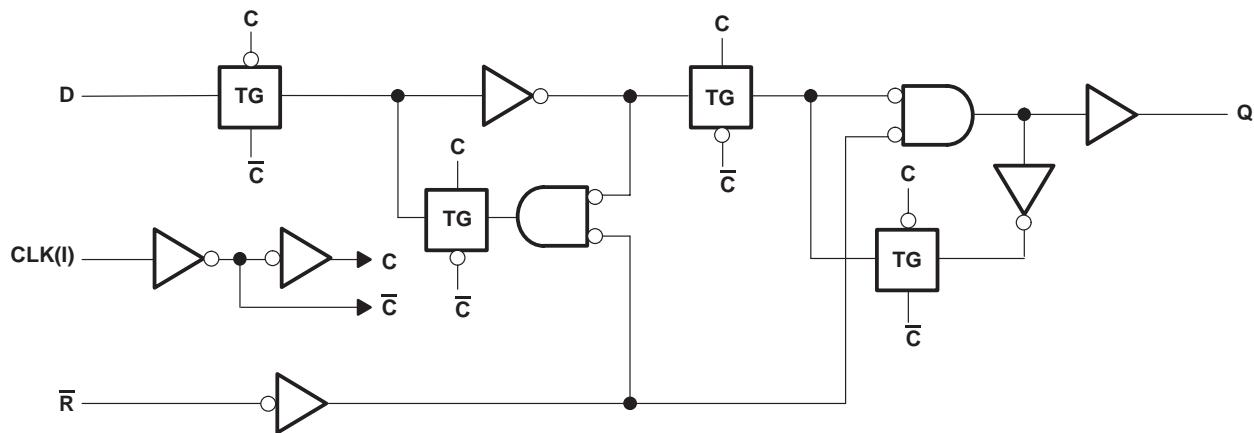
## FUNCTION TABLE (each flip-flop)

INPUTS			OUTPUT Q
CLR	CLK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

## logic diagram (positive logic)



logic diagram, each flip-flop (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DB package .....	70°C/W
DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
PW package .....	83°C/W
Storage temperature range, $T_{Stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HCT273			SN74HCT273			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$			2	2		V
$V_{IL}$	Low-level input voltage		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$			0.8	0.8		V
$V_I$	Input voltage		0	$V_{CC}$	0	$V_{CC}$	0		V
$V_O$	Output voltage		0	$V_{CC}$	0	$V_{CC}$	0		V
$\Delta t/\Delta v$	Input transition rise/fall time			500			500		ns
$T_A$	Operating free-air temperature			-55	125	-40	85		°C

NOTE 3: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT273		SN74HCT273		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 µA	4.5 V	4.4	4.499	4.4	4.4	4.4	4.4	V
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.30	3.7	3.84			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA	4.5 V	0.001	0.1	0.1	0.1	0.1	0.1	V
		I <sub>OL</sub> = 4 mA	4.5 V	0.17	0.26	0.4	0.4	0.33	0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		5.5 V	±0.1	±100	±1000	±1000	±1000	±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		5.5 V		8	160	160	80	80	µA
ΔI <sub>CC</sub> ‡	One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>		5.5 V	1.4	2.4	3	3	2.9	2.9	mA
C <sub>i</sub>			4.5 V to 5.5 V	3	10	10	10	10	10	pF

<sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or  $V_{CC}$ .

**SN54HCT273, SN74HCT273  
OCTAL D-TYPE FLIP-FLOPS  
WITH CLEAR**

SCLS068E – NOVEMBER 1988 – REVISED AUGUST 2003

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

			V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HCT273		SN74HCT273		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency			4.5 V	25	16	20			MHz	
				5.5 V	28	19	23				
t <sub>w</sub>	Pulse duration	CLK high or low	4.5 V	20	30	25				ns	
			5.5 V	18	25	22					
		CLR low	4.5 V	16	24	20					
			5.5 V	14	20	17					
t <sub>su</sub>	Setup time before CLK↑	Data	4.5 V	20	30	25				ns	
			5.5 V	17	25	21					
		CLR inactive	4.5 V	20	30	25					
			5.5 V	17	25	21					
t <sub>h</sub>	Hold time data after CLK↑			4.5 V	0	0	0			ns	
				5.5 V	0	0	0				

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN54HCT273			UNIT	
				T <sub>A</sub> = 25°C				
				MIN	TYP	MAX		
f <sub>max</sub>			4.5 V	25	31	16	MHz	
			5.5 V	28	37	19		
t <sub>pd</sub>	CLR	Any	4.5 V	15	34	50	ns	
			5.5 V	12	29	42		
t <sub>PHL</sub>	CLR	Any	4.5 V	17	15	50	ns	
			5.5 V	15	34	42		
t <sub>t</sub>		Any	4.5 V	8	18	22	ns	
			5.5 V	7	19	21		

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN74HCT273			UNIT	
				T <sub>A</sub> = 25°C				
				MIN	TYP	MAX		
f <sub>max</sub>			4.5 V	25	31	20	MHz	
			5.5 V	28	37	23		
t <sub>pd</sub>	CLR	Any	4.5 V	15	34	42	ns	
			5.5 V	12	29	36		
t <sub>PHL</sub>	CLR	Any	4.5 V	17	34	42	ns	
			5.5 V	15	29	36		
t <sub>t</sub>		Any	4.5 V	8	15	19	ns	
			5.5 V	7	14	17		

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

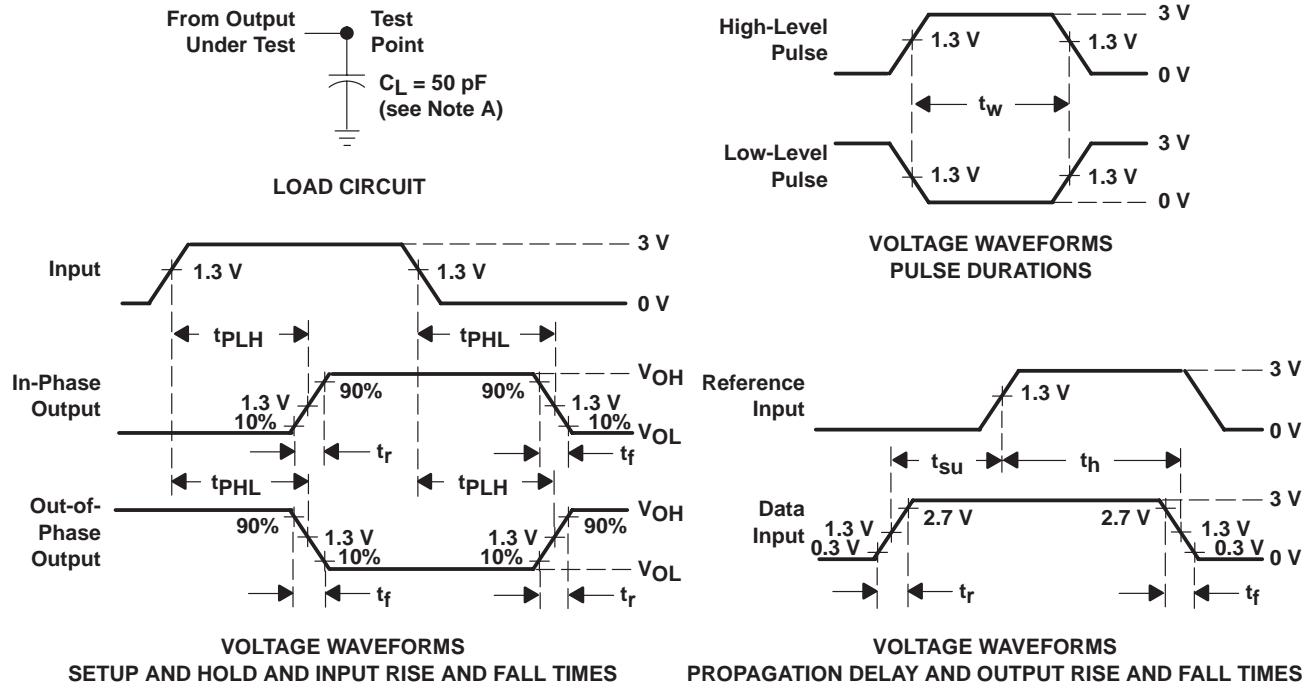


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operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load	30	pF

### PARAMETER MEASUREMENT INFORMATION



NOTES:

- $C_L$  includes probe and test-fixture capacitance.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
- The outputs are measured one at a time with one input transition per measurement.
- For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT273DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT273	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT273DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT273	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT273DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT273	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT273DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT273	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT273DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT273	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT273DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT273	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT273N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT273N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT273NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT273	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT273PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT273	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT273PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT273	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT273PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT273	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74HCT273PWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT273	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

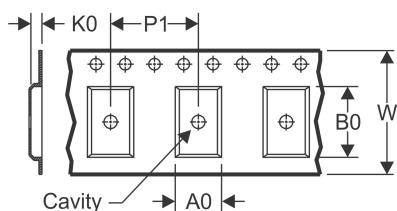
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT273DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HCT273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HCT273NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HCT273PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

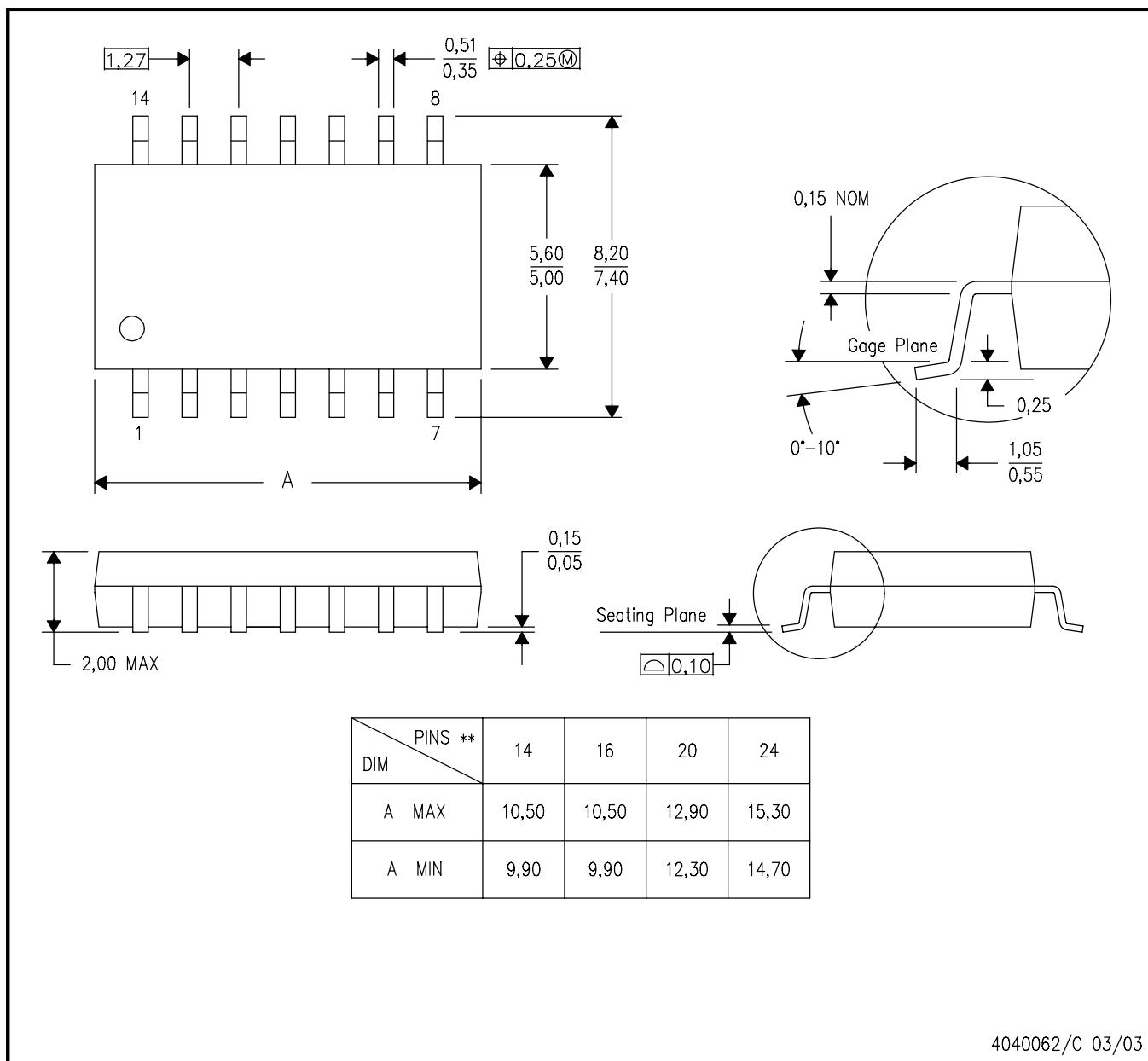
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT273DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74HCT273DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HCT273NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HCT273PWT	TSSOP	PW	20	250	367.0	367.0	38.0

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

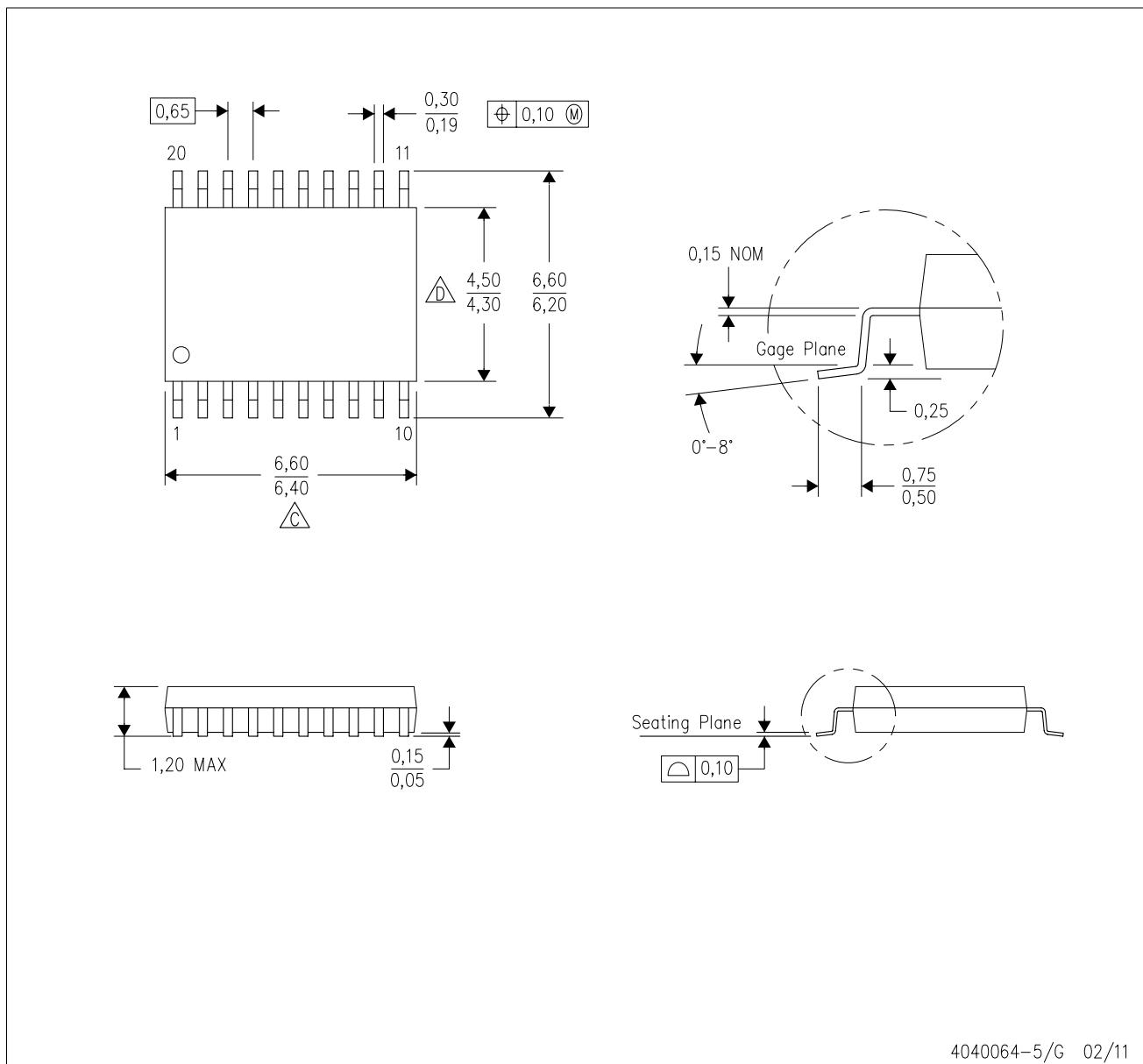


4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

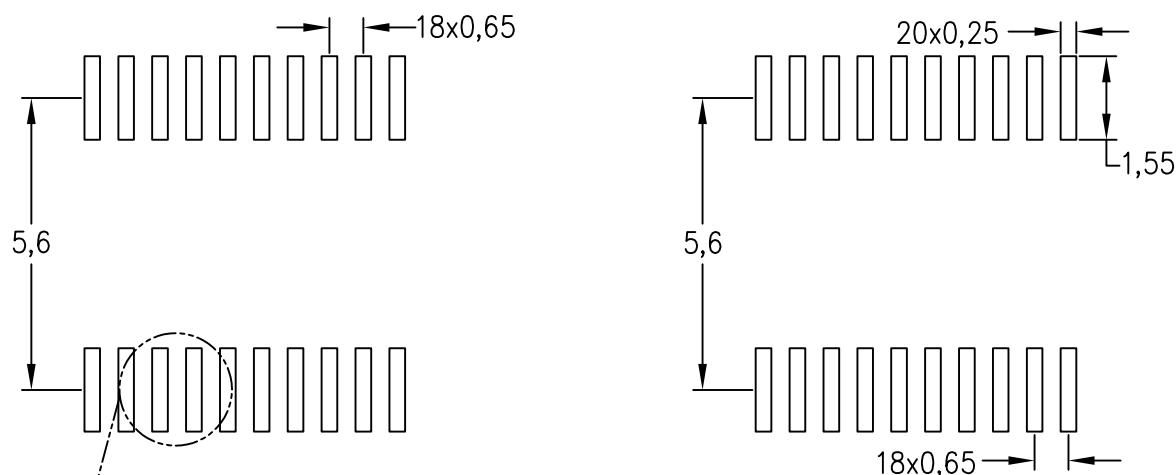
E. Falls within JEDEC MO-153

4040064-5/G 02/11

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

## Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).Example  
Non Soldermask Defined PadExample  
Solder Mask Opening  
(See Note E)

Pad Geometry

0,3  
1,6  
0,07

All Around

4211284-5/G 08/15

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

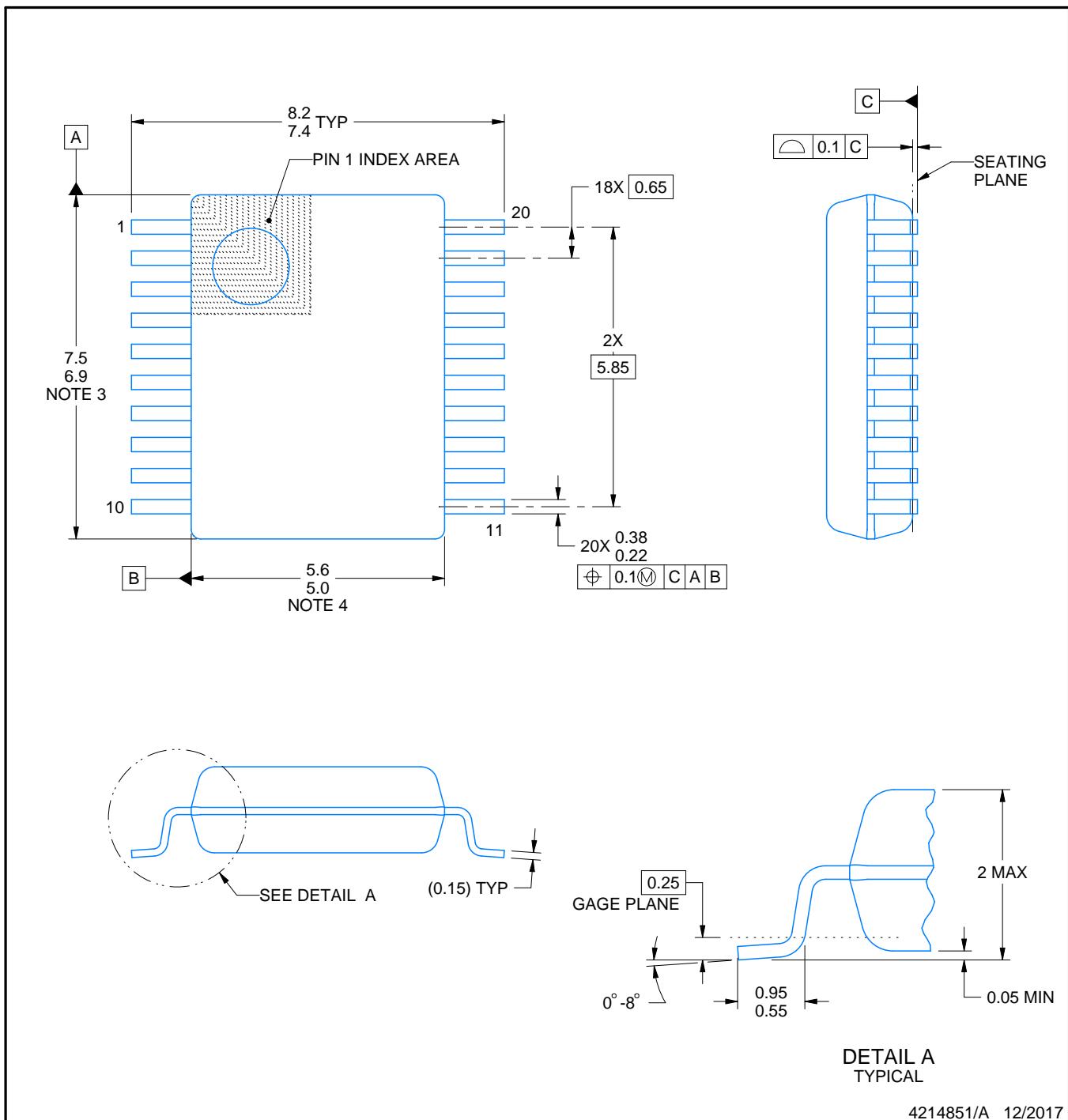
## PACKAGE OUTLINE

DB0020A



## TSSOP - 2 mm max height

## SMALL OUTLINE PACKAGE



## NOTES:

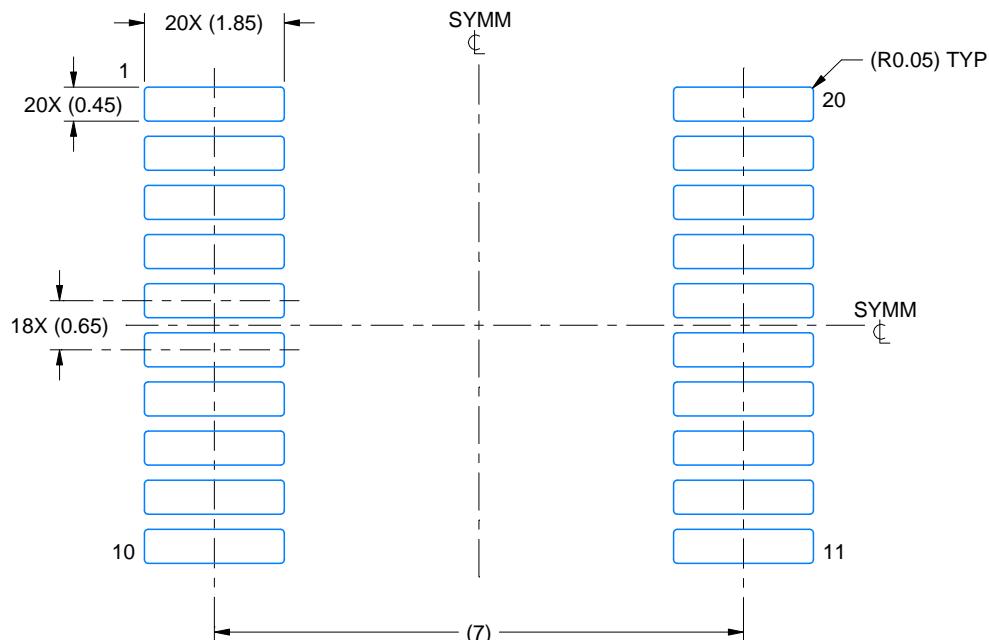
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

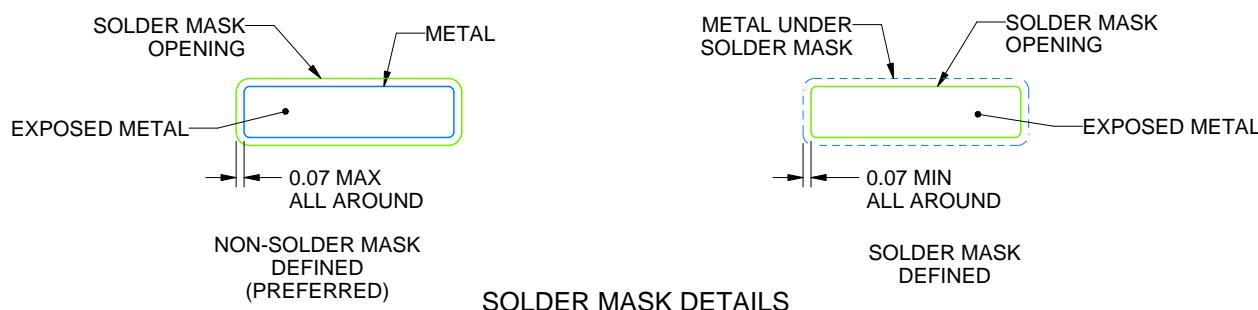
DB0020A

TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/A 12/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

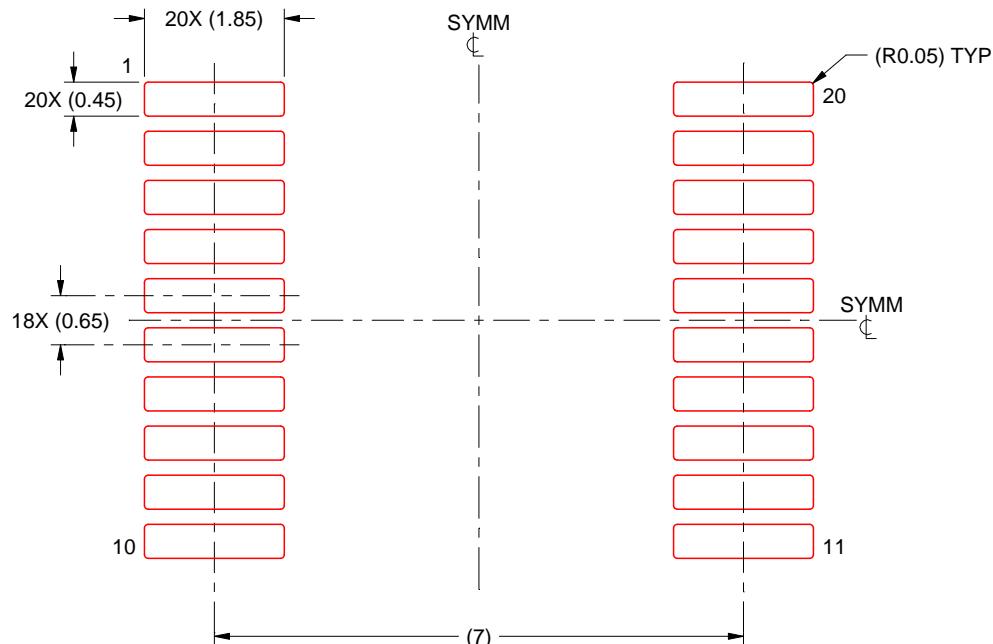
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/A 12/2017

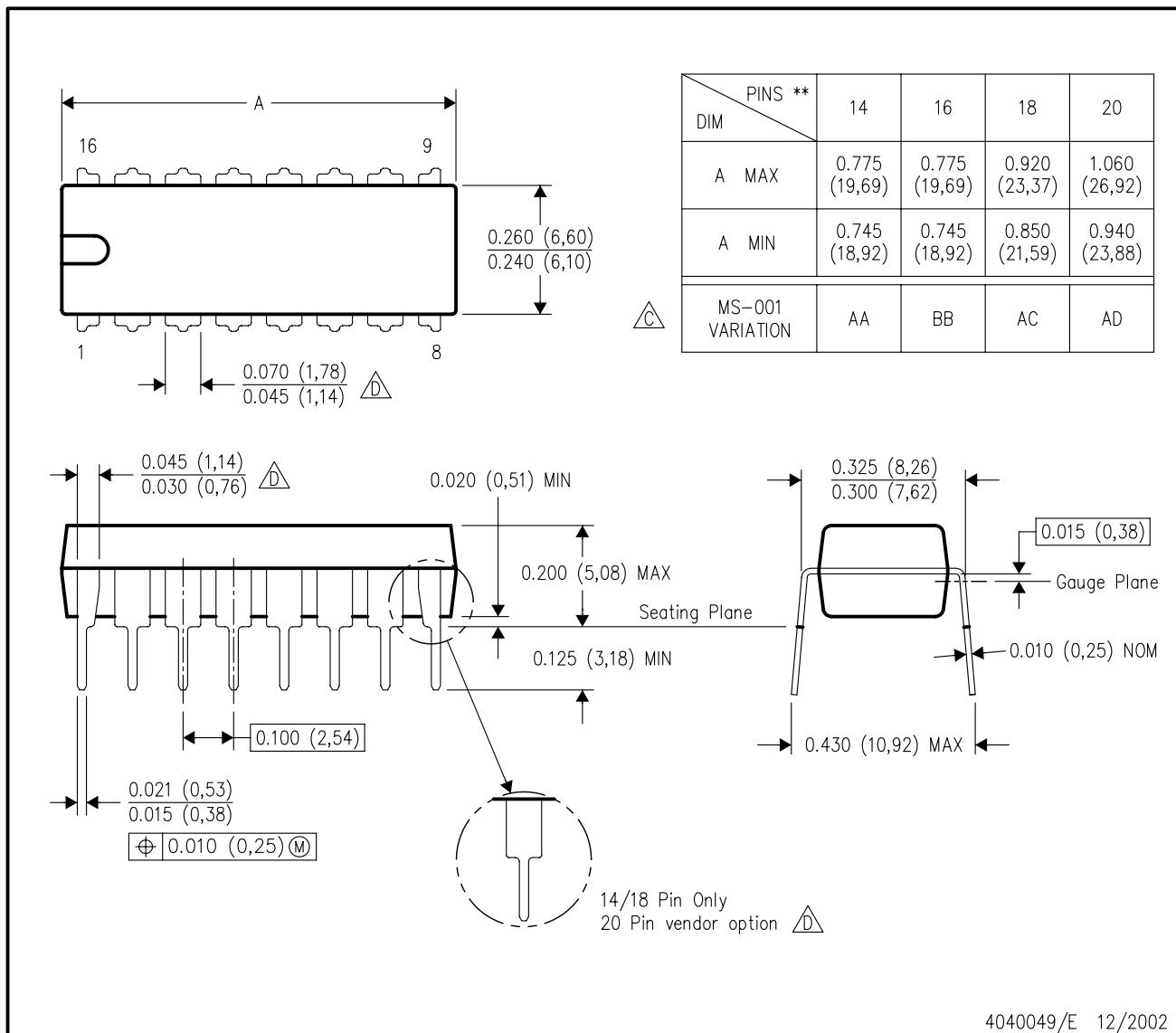
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

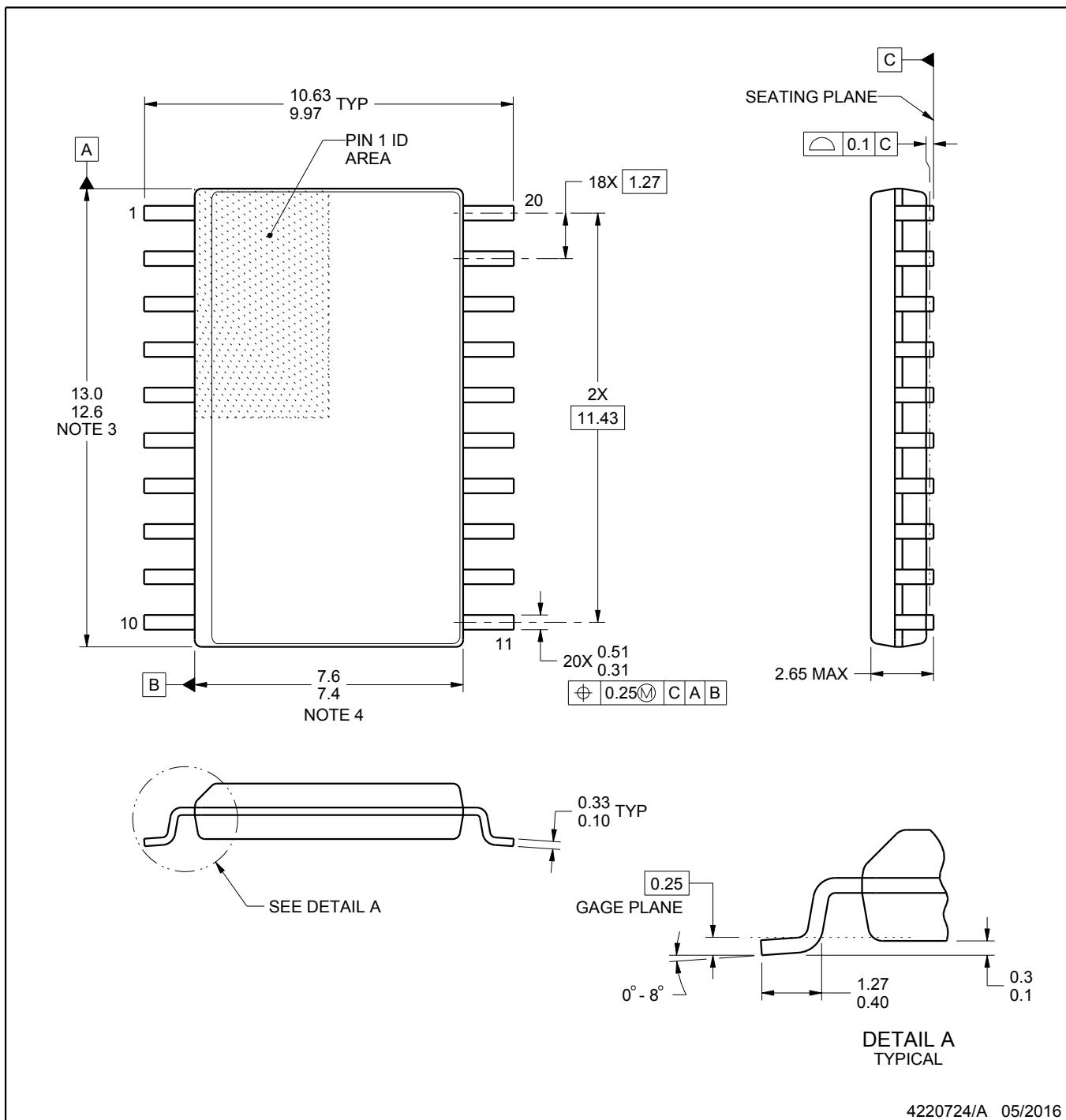
# PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

## NOTES:

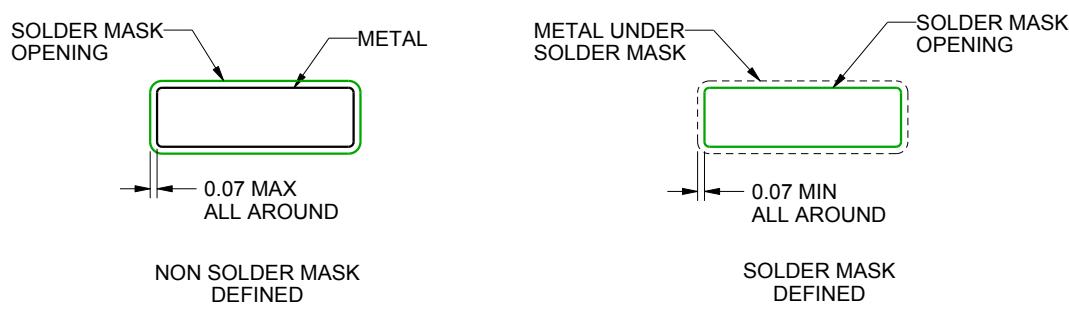
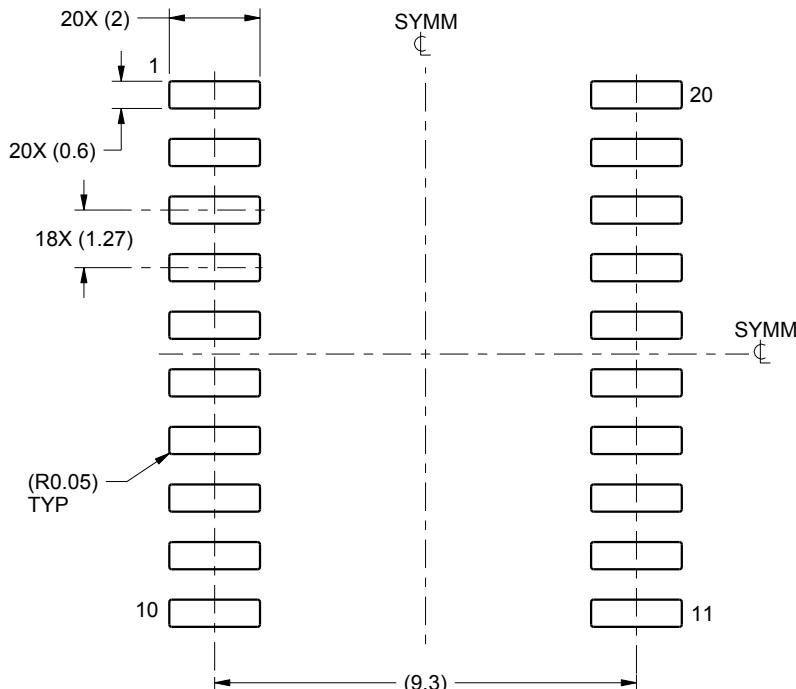
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

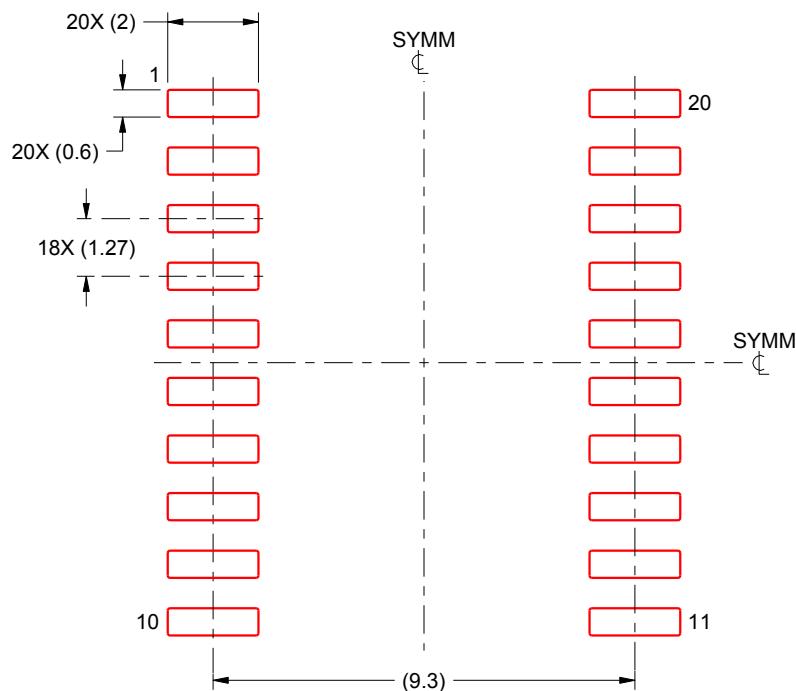
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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