NOVATEK 聯詠科技

Data Sheet

NT96660

Imaging Processor

Version 0.1

Preliminary

Table of Contents

Revision History

Rev.	Date	Author	Contents
0.1	2014/10/01	Kevin Hung	First draft version.

Features

■ High Performance 32-bit CPU

- □ Dual MIPS32 24Kec with ASE DSP extension
- □ MMU embedded
- □ Main: 16KB instruction and 16KB data cache and operation frequency up to 420 MHz
- □ Secondary: 16KB instruction and 16KB data cache and operation frequency up to 420 MHz
- □ Embedded ICE makes firmware debugging easier
- □ CPU operating frequency on the fly programmable

■ High Performance Image/Video Dedicated DSP

- □ Program cache 32 KB and dedicated SRAM size 96 KB
- □ Max. operation frequency 270 MHz (Estimated)

■ Power Management features

- □ Firmware configurable operating frequency of each functional block to meet best power budget
- □ Internal power domain partition

■ Integrated Clock Generator

- □ Internal PLL with spread spectrum capability
- □ 12MHz system/USB oscillator
- □ 32768Hz RTC oscillator

■ Scalable Memory Bus Architecture

- □ 16-bit DDR3 SDRAM bus, supporting up to 4Gb DDR/DDR3L SDRAM
- □ DRAM operating frequency up to 480MHz
- □ Tunable DDR frequency on the fly for power saving

■ Sensor Interface Engine

- □ Support up to 50M pixel CMOS image sensor
- □ Support high speed serial interface like sub-LVDS/MIPI(1.5G)/HiSPi up to 10 channels and 2 clocks for most commercial CMOS sensors including Sony, Panasonic, Aptina, Samsung, Sharp and Omnivision, etc.
- □ Support parallel sensor interface for most commercial CMOS sensors including Aptina and Omnivision
- □ Support max. 4 video input
- □ Support 12-bit (serial) sensor data input
- □ Support burst shot up to 12 fps for 20MP sensor
- □ Support parallel interface sensor pixel clock up to 120MHz

- Support HDR sensor composition such as SONY DOL mode and Omnivision staggered mode
- Support BT.601/656-video input
- Built-in color pattern generation
- Sensor black level clamping
- Efficient defect concealment algorithm
- Raw image scale down for video & high ISO image
- Flexible image analysis flow for AE, AWB and AF purpose
- Programmable histogram analysis
- R/G/B Gamma LUT for sensor linearization correction
- In-pipeline lens shading compensation technology
- In-pipeline color shading compensation technology
- In-pipeline geometric distortion correction technology
- In-pipeline color aberration correction technology
- Support perspective distortion correction for image stitching pre-processing
- Support CMOS sensor spatial crosstalk cancellation
- Support in-frame dark frame subtraction with smart defect detection algorithm
- Support EIS with gyro-sensor input
- Support rolling shutter correction for CMOS sensor
- Mechanical shutter control
- Flash light control

Image Processing Engine

- Advanced image pipeline architecture for multi-purpose hardware acceleration
- Proprietary advanced anti-alias Bayer CFA color interpolation
- Advanced edge rendering control and continuity enhancement
- Powerful noise reduction technology for still and video recording
- Support advanced motion compensated temporal filtering (MCTF) for efficient video noise reduction
- Support temporal noise reduction with ghost reduction
- R/G/B Gamma LUT
- High precision color correction matrix for sRGB or specific color requirement
- Brightness/contrast and hue/saturation adjustment
- Specific color control technology (Patented)
- 3D color conversion for specific color preference tuning
- False color suppression

- Wide dynamic range (WDR) for global/local illumination enhancement
- HW acceleration for multiple frames HDR and night shot composition

Image Manipulation Engine

- High quality scaling engine for seamless digital zooming from 1/16x to 16x
- Advanced super resolution technology for digital zoom quality
- Support thumbnail image generation
- Forward/inverse color space transform

Face Detection Engine

- Very high speed face detection and tracking
- High accuracy under different light source
- Programmable target data base

Digital Image Stabilizer

- Remove unintended hand movement from an image sequence
- Single frame compensation for video (Total compensation)
- Accumulate frame compensation for video (Smart compensation)
- Programmable total compensation range
- Accommodate resolution 1080p

LCD/TV Display

- Support dual display including LCD panel and HDMI/TV display simultaneously
- High performance scaling up/down engine, programmable gamma correction, color transform and color management for LCD or TV display
- Separate OSD for LCD panel and TV
- Support digital LCD interface for AUO, Casio, CMI (all digital panels will be supported)
- Support 16-bit RGB parallel interface (RGB565 or Delta RGB) LCD panel up to 1024x1024 resolution
- Support 90° rotation/flip/mirror
- Support PAL / NTSC video encoder (CVBS format)
- Integrated 1 internal 10-bit video DACs
- Support digital interface BT.601/656/1120 output port
- 3.3V / 1.8V LCD / Digital video out

HDMI

- Support HDMI v1.3a
- Support DDC with maximum 100khz access rate for CEA-861-D format
- Support CEC

- Support 16 bits PCM 32 KHz, 44.1 KHz, 48KHz for maximum 2 channels audio output
- Support 1080p60 display

■ Graphic Engine

- Copy and paste
- Geometric operation including mirror, flip and rotation
- Arithmetic operation including addition, subtraction, color keying, logic operation and alpha blending
- Support anti-alias affine transform
- Support hardware acceleration for multi-frame processing

■ Cipher

- 64-bit DES, 3DES, and AES-128
- Both encryption and decryption
- Big and little endian of input data

■ H.264/AVC CODEC

- Support encoder BP/MP, level 4.1
- Support encoder HP, level 4.2
- Support real-time capability for 1080p60, 1080p30, 720p120, 720p60, 480p240, 480p120
- Support full frame still capture while video recording
- H.264 high/main profile
- 1 reference picture for P-frame, 2 reference pictures for B-frame
- Support video format MP4, AVI, MOV
- Support bit rate control
- Automatic frame sync for high frame rate

■ F/W Audio CODEC

- AAC encode / decode (32KHz, 48KHz @ 192kbps)
- ADPCM encode / decode

■ H/W Audio CODEC

- stereo 16-bits ADC audio recording
- stereo 16-bits DAC audio playback
- Programmable ALC / Noise Gate l
- Audio sampling rate : 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48kHz
- Support dual microphone inputs
- On-chip speaker driver / stereo headphone drive

■ JPEG CODEC

- Supports Motion JPEG 30fps@1080P30 video clip/playback function
- Max. pixel clock 240Mpixel / sec
- Support ISO/IEC 10918-1 baseline JPEG compression/decompression.
- Still image maximum resolutions will be up to 65536x65536 pixels
- Support input format: 422, 420, 411, 400, 211
- JPEG supports downloadable Quantization and Huffman tables
- Support Exchangeable Image File format (EXIF 2.2.3 and newer)
- Support MPO file format for 3D image

Digital Audio Interface

- Support I2S codec interface
- Audio clock generator

Dual Graphic-based OSD

- Support 8-bit palette and ARGB(8565 or 8888) OSD architecture
- 256 colors simultaneously out of true color at 8-bit palette OSD
- 8 levels of opacity for 8-bit palette OSD
- Programmable width & height to meet LCD/TV's resolution exactly
- Picture in picture function
- Dedicated 16 face frames for face detection function

Storage Memory Controller

- Secure Digital card and SDIO (3 sets)
- Support SD 3.0
- Support UHS-I: UHS50, UHS104 (Max. freq. 96MHz)
- Support eyeFi for wireless connection
- Multi-Media card
- SLC NAND type flash

USB

- Fully compliant with USB2.0 device/host (2 sets)
- High speed (480Mbps) supported
- Optionally switchable to be fully compliant with USB 1.1
- Support Control / Isochronous / Interrupt and Bulk transfer
- Support PC camera mode

Timers

- RTC can be powered by separate backup battery and operating from 1.5V to 3.6V
- Watch dog timer

- 20 programmable HW timers support resolution up to 3MHz and 32 bits counter

■ Peripheral Interface

- Support I2C interface (2 sets)
- Support 20 channels PWM including built-in 16 (4 sets) pattern generators for µ-Stepping motor control
- Support GPIO and flexible PWM interface with micro-stepping
- Support programmable 3-wired serial interface
- Support SPI interface (5 sets)
- Dedicated SPI for gyroscope reading
- Support NFC & BLE4.0 interface
- Support UART interface (4 sets)
- Support 8 channels of 10-bit ADC, the max. sample rate up to 12.5 KHz per channel
- Embed Ethernet 10M/100M MAC and RMII interface to PHY

■ On-chip Boot Strap Loader

- Built-in on-chip mask ROM
- User program can be stored in NAND-type flash and external static memory is not necessary
- On-chip mask ROM can be disabled
- System can boot from SPI NOR/Nand flash, NAND flash, memory cards, eMMC and USB

■ Triple Voltage Power Supply

- 1.1V core logic voltage
- 1.5V DDR3 or 1.35V DDR3L SDRAM interface voltage
- 3.3V I/O interface and analog circuit voltage

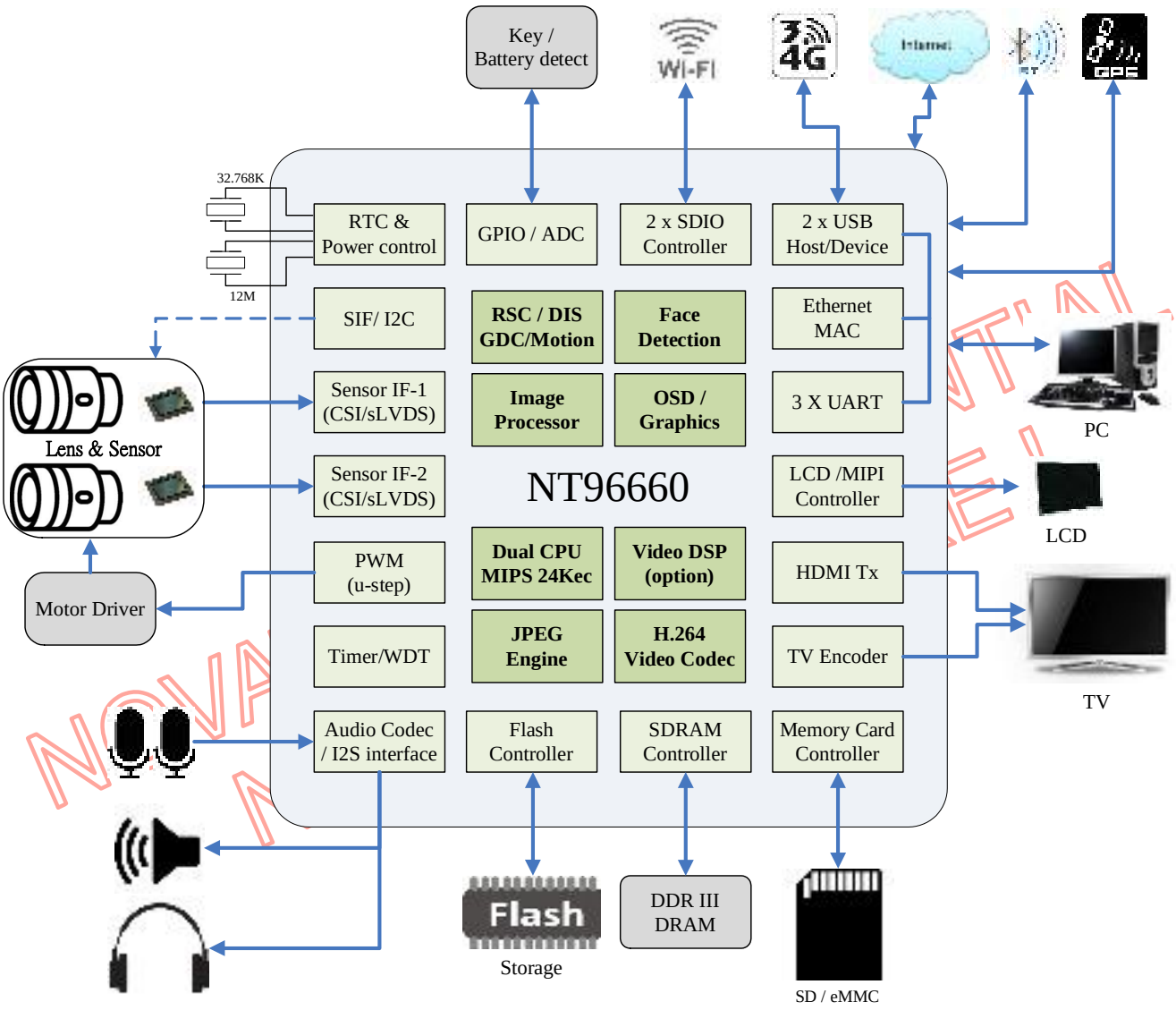
■ Package

- NT96660BG: 344 ball TFBGA, 14x14 mm^2

General Description

NT96660BG is a high image quality, high performance, power saving and cost effective digital still camera (DSC) and digital video camera (DV) controller with excellent digital still image capturing and video streaming capabilities. It is targeted for the application of VGA to 50M pixel DSC/DV resolutions. It can be easily adapted to many high speed CMOS and conventional CCD image sensors with on chip programmable interface timing approach. The controller provides sophisticated video processing methods with built-in hardware acceleration pipeline. This is essential for achieving high performance for per-shot, shot-to-shot, and continuous shooting pictures. The controller provides flexible mechanism for auto white balance, auto exposure and auto-focusing in order to better tradeoff hardware and software efforts over the performance. Embedded H.264 video CODEC supports video recording up to full-HD 1080p60/i60. The HDMI 1.3 Tx is also equipped for HDTV output. Rich storage interfaces are supported to make it ideal for the storage of still pictures and video streaming data. The USB2.0 high speed interface can upload/download the audio/video data efficiently to/from PC.

Block Diagram



Pin Configuration

1. TFBGA-344

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name

Note:

Pin Descriptions

I = input port with Schmitt trigger

O = output port with normal driving/sinking

I/O = bi-directional port with normal driving/sinking and Schmitt input

mvI/O = multi voltage bi-direction port with Schmitt input

HSI = high speed serial interface with multi voltage input port

I/Osw = bi-directional port with strong driving/sinking and wide Schmitt input range

I/Ow = bi-directional port with wide Schmitt input range

I/Os = bi-directional port with strong driving/sinking

I/Os_2 = bi-directional port with strong driving/sinking

I/Oss = bi-directional port with strong driving/sinking

I/Oz = bi-directional port with large pull/down resistor

I/O_{5VT} = bi-directional port with normal driving/sinking and Schmitt input

OD = open drain output with normal sinking

I/OD = bi-directional port, open drain output

LVD = low voltage detect function pin

p/u = internal pull-up

p/d = internal pull-down

AI = analog input port

AI_{5VT} = analog 5V tolerant input port

AO = analog output port

AI/O = analog bi-directional port

H = output high

L = output low

P = power or ground

Note: * means this pin has interrupted function.

1. NT96660BG 344 pins

Total: 344 pins

Alternative GPIO: 160 pins

1.1. System interface (9,9)

Pin No.	Name	Type	Reset	Descriptions
	XTAL_SYSI	AI	-	Crystal input for system oscillator. (12MHz)
	XTAL_SYSO	AO	-	Output for system oscillator.
	RESET#	LVD	p/u	System Reset. Connect a capacitor to ground for reset time control.
	TESTEN	I	I p/d	Test mode enable. Keep low for normal operation.
	JTAG_TRST# / DGPIO6*	IOs	I p/d	CPU's JTAG test logic reset(active low).
	JTAG_TMS / DGPIO7*	IOs	I p/d	CPU's JTAG test mode select.
	JTAG_TCK / DGPIO8*	IOs	I p/d	CPU's JTAG test clock input.
	JTAG_TDI / DGPIO9*	IOs	I p/d	CPU's JTAG test data input.
	JTAG_TDO / DGPIO10*	IOs	I p/d	CPU's JTAG test data output.

1.2. RTC & Power Button Controller (7,6)

Pin No.	Name	Type	Default	Descriptions
	XTAL_RTCI	AI	-	Crystal input for real time clock oscillator. (32.768KHz).
	XTAL_RTCO	AO	-	Output for real time clock oscillator.
	PWR_SW1*	AI	I p/d	Power on/off signal input. (ON/OFF switch use)
	PWR_SW2*#	AI	I p/u	Power on/off signal input. (falling edge trigger)
	PWR_SW3	AI	I p/d	Power on/off signal input.
	PWR_SW4	AI	I p/d	Power on/off signal input. (Bettery in use)
	PWR_EN	AO	-	Power enable signal output.

* PWR_SW can trigger interrupt (share RTC interrupt). If this pin isn't used, Novatek recommends connecting this pin to GND.

1.3. DRAM interface (50)

Pin No.	Name	Type	Reset	Descriptions
	DR_RESET#	O	-	Reset signal output for DDR3 DRAM.
	DR_CS#	O	-	DRAM chip select
	ODT	O	-	DRAM on die terminator control
	DR_CLK	O	-	DRAM differential clock output.
	DR_CLK#	O	-	

	DR_CKE	O	-	DRAM clock enable.
	DR_CAS#	O	-	DRAM control signals
	DR_RAS#			
	DR_WE#			
	DR_VREF	AI	-	DRAM reference voltage input.
	DR_BA0	O	-	DRAM bank select.
	DR_BA1			
	DR_BA2			
	DR_A0	O	-	DRAM address bus.
	DR_A1			
	DR_A2			
	DR_A3			
	DR_A4			
	DR_A5			
	DR_A6			
	DR_A7			
	DR_A8			
	DR_A9			
	DR_A10			
	DR_A11			
	DR_A12			
	DR_A13			
	DR_A14			
	DR_DQM0	O	-	DRAM data mask: DQM0 corresponds to DQ0-DQ7 and DQM1 corresponds to DQ8-DQ15.
	DR_DQM1			
	DR_DQS0	I/O	-	DRAM data strobe. DQS0 corresponds to DQ0-DQ7 and DQS1 corresponds to DQ8-DQ15.
	DR_DQS0#			
	DR_DQS1			
	DR_DQS1#			
	DR_D0	I/O	-	DRAM data bus input/output, lower byte. (Each bits of lower byte may be permuted to make routing simpler).
	DR_D1			
	DR_D2			
	DR_D3			
	DR_D4			
	DR_D5			
	DR_D6			
	DR_D7			
	DR_D8	I/O	-	DRAM data bus input/output, upper byte. (Each bits of upper byte may be permuted to make routing simpler)
	DR_D9			
	DR_D10			
	DR_D11			
	DR_D12			
	DR_D13			
	DR_D14			
	DR_D15			

1.4. Sensor interface (33,35)

Pin No.	Name	Type	Reset	Descriptions
	HSI_D0N / HSI_GPI[0]			
	HSI_D0P / HSI _GPI[1]			
	HSI_D1N / HSI _GPI[2]			
	HSI_D1P / HSI _GPI[3]			
	HSI_D2N / HSI _GPI[4]			
	HSI_D2P / HSI _GPI[5]			
	HSI_D3N / HSI _GPI[6]			
	HSI_D3P / HSI _GPI[7]			
	HSI_D4N / HSI _GPI[8]			
	HSI_D4P / HSI _GPI[9]			
	HSI_CK0N / HSI _GPI[10]			High speed differential sensor interface and parallel interface. (when sensor interface is configured as high speed differential sensor interface, the clock lane should be a dedicated differential lane. And each data lanes may be permuted in established group, refer to below table)
	HSI_CK0P / HSI _GPI[11]	HSI	I p/d	
	HSI_D5N / HSI _GPI[12]			
	HSI_D5P / HSI _GPI[13]			
	HSI_D6N / HSI _GPI[14]			
	HSI_D6P / HSI _GPI[15]			
	HSI_D7N / HSI _GPI[16]			
	HSI_D7P / HSI _GPI[17]			
	HSI_D8N / HSI _GPI[18]			
	HSI_D8P / HSI _GPI[19]			
	HSI_D9N / HSI _GPI[20]			
	HSI_D9P / HSI _GPI[21]			
	HSI_CK1N /			

	HSI _GPI[22]			
	HSI_CK1P / HSI _GPI[23]			
	SN_MCLK / S_GPIO[0]	mvI/Os	I p/d	Programmable Clock output for sensor
	SN_PXCLK / S_GPIO[1]	mvI/Os	I p/d	Sensor Pixel Clock Input
	SN_VD / S_GPIO[2]	mvI/O	I p/d	Sensor Vertical Sync input / output
	SN_HD / S_GPIO[3]	mvI/O	I p/d	Sensor Horizontal Sync input / output
	SN_CS / S_GPIO[4]	mvIOs	I p/u	General serial interface 0 Chip Select
	SN_SCK / I2C_SCL / S_GPIO[5]	mvIOD	I p/u	General serial interface 0 clock output. I2C-BUS clock output(Open Drain IO structure)
	SN_DAT / I2C_SDA / S_GPIO[6]	mvIOD	I p/u	General serial interface 0 data output. I2C-BUS data input / output(Open Drain IO structure)
	SN_RESET / S_GPIO[7]	mvIO	I p/d	Sensor reset control signal output
	SN_STBY / S_GPIO[8]	mvIO	I p/d	Sensor standby control signal output
	SN_FLASH / S_GPIO[9]	mvIO	I p/d	Flash Signal input from sensor
	SN_SHUT / S_GPIO[10]	mvIO	I p/d	Shutter signal input from sensor

Note*: The pin can trigger interrupt.

Note1 : The input voltage of HSI corresponds to GVDD_SN.

Note2 : The mvI/O voltage of Sensor interface corresponds to VDD_SN.

Name	LVDS (1C10D or 2C10D)		MIPI / HiSPi SIE1/2 (4 lanes)		Parallel SIE1/2 (RAW10)		CCIR601 SIE1/2 (8 bits)		Parallel SIE1 (RAW12)		CCIR601 SIE2 (16 bits)	
HSI_GPI[0]	HSI_D0N	I	HSI_D0N	I	SN_D0(LSB)	I			SN_D2	I		
HSI_GPI[1]	HSI_D0P	I	HSI_D0P	I	SN_D1	I			SN_D3	I		
HSI_GPI[2]	HSI_D1N	I	HSI_D1N	I	SN_D2	I	SN_YC0	I	SN_D4	I		
HSI_GPI[3]	HSI_D1P	I	HSI_D1P	I	SN_D3	I	SN_YC1	I	SN_D5	I		
HSI_GPI[4]	HSI_D2N	I	HSI_D2N	I	SN_D4	I	SN_YC2	I	SN_D6	I	SN2_Y0(LSB)	I
HSI_GPI[5]	HSI_D2P	I	HSI_D2P	I	SN_D5	I	SN_YC3	I	SN_D7	I	SN2_Y1	I
HSI_GPI[6]	HSI_D3N	I	HSI_D3N	I	SN_D6	I	SN_YC4	I	SN_D8	I	SN2_Y2	I
HSI_GPI[7]	HSI_D3P	I	HSI_D3P	I	SN_D7	I	SN_YC5	I	SN_D9	I	SN2_Y3	I
HSI_GPI[8]	HSI_D4N	I			SN_D8	I	SN_YC6	I	SN_D10	I	SN2_Y4	I
HSI_GPI[9]	HSI_D4P	I			SN_D9(MSB)	I	SN_YC7	I	SN_D11(MSB)	I	SN2_Y5	I
HSI_GPI[10]	**HSI_CK0N**	I	**HSI_CKN**	**I**	SN2_D0(LSB)	I		I	SN_D1	I	SN2_Y6	I
HSI_GPI[11]	**HSI_CK0P**	I	**HSI_CKP**	**I**	SN2_D1	I		I	SN_D0(LSB)	I	SN2_Y7(MSB)	I
HSI_GPI[12]	HSI_D5N	I	HSI2_D0N	I	SN2_D2		SN2_YC0	I			SN2_C0(LSB)	I
HSI_GPI[13]	HSI_D5P	I	HSI2_D0P	I	SN2_D3		SN2_YC1	I			SN2_C1	I
HSI_GPI[14]	HSI_D6N	I	HSI2_D1N	I	SN2_D4		SN2_YC2	I			SN2_C2	I
HSI_GPI[15]	HSI_D6P	I	HSI2_D1P	I	SN2_D5		SN2_YC3	I			SN2_C3	I
HSI_GPI[16]	HSI_D7N	I	HSI2_D2N	I	SN2_D6		SN2_YC4	I			SN2_C4	I
HSI_GPI[17]	HSI_D7P	I	HSI2_D2P	I	SN2_D7		SN2_YC5	I			SN2_C5	I

HSI_GPI[18]	HSI_D8N	I	HSI2_D3N	I	SN2_D8		SN2_YC6	I			SN2_C6	I
HSI_GPI[19]	HSI_D8P	I	HSI2_D3P	I	SN2_D9(MSB)		SN2_YC7	I			SN2_C7(MSB)	I
HSI_GPI[20]	HSI_D9N	I			SN2_VD		SN2_VD	I			SN2_VD	I
HSI_GPI[21]	HSI_D9P	I			SN2_HD		SN2_HD	I			SN2_HD	I
HSI_GPI[22]	HSI_CK1N	I	**HSI2_CKN**	I								
HSI_GPI[23]	HSI_CK1P	I	**HSI2_CKP**	I								
S_GPIO[0]	SN_MCLK	O	SN_MCLK	O	SN_MCLK	O	SN_MCLK	O	SN_MCLK	O		
S_GPIO[1]	SN_PXCLK	I			SN_PXCLK	I	SN_PXCLK	I	SN_PXCLK	I		
S_GPIO[2]	SN_VD	I/O			SN_VD	I	SN_VD	I	SN_VD	I		
S_GPIO[3]	SN_HD	I/O			SN_HD	I	SN_HD	I	SN_HD	I		
S_GPIO[4]			SN2_MCLK	O	SN2_MCLK	O	SN2_MLCK	I			SN2_MCLK	O
S_GPIO[7]					SN2_PXCLK	I	SN2_PXCLK	I			SN2_PXCLK	I

1.5. Memory Card interface (36,36)

Pin No.	Name	Type	Reset	Descriptions
	SD_CAP	P	-	Internal Supply Voltage decoupling for SDIO1 interface. (3.3/1.8V switchable, default 3.3V)
	SD_CAP2	P	-	Internal Supply Voltage decoupling for SDIO2 interface. (3.3/1.8V switchable, default 3.3V)
	MC0 / C_GPIO[0]	mvI/O	I p/u	Memory Card interface(see below table)
	MC1 / C_GPIO[1]	mvI/O	I p/u	
	MC2 / C_GPIO[2]	mvI/Os	I p/u	
	MC3 / C_GPIO[3]*	mvI/O	I p/u	
	MC4 / C_GPIO[4]	mvI/O	I p/u	
	MC5 / C_GPIO[5]	mvI/O	I p/u	
	MC6 / C_GPIO[6]	mvI/O	I p/u	
	MC7 / C_GPIO[7]	mvI/O	I p/u	
	MC8 / C_GPIO[8]	mvI/O	I p/u	
	MC9 / C_GPIO[9]*	mvI/O	I p/u	
	MC10 / C_GPIO[10]	mvI/O	I p/u	
	MC11 / C_GPIO[11]	mvI/O	I p/u	
	MC12 / C_GPIO[12]	mvI/O	I p/d	
	MC13 / C_GPIO[13]	mvI/O	I p/d	
	MC14 / C_GPIO[14]	mvI/O	I p/u	
	MC15 /	mvI/O	I p/u	

	C_GPIO[15]*			
	MC16 / C_GPIO[16]	I/Os	I p/d	
	MC17 / C_GPIO[17]	I/O	I p/u	
	MC18 / C_GPIO[18]	I/O	I p/u	
	MC19 / C_GPIO[19]	I/O	I p/u	
	MC20 / C_GPIO[20]	I/O	I p/u	
	MC21 / C_GPIO[21]*	I/O	I p/u	
	MC22 / C_GPIO[22]	I/Os	I p/d	
	MC23 / C_GPIO[23]	I/O	I p/u	
	MC24 / C_GPIO[24]	I/O	I p/u	
	MC25 / C_GPIO[25]*	I/O	I p/u	
	MC26 / C_GPIO[26]*	I/O	I p/u	
	MC27 / C_GPIO[27]*	I/O	I p/u	
	MC28 / C_GPIO[28]*	I/Os	I p/d	
	MC29 / C_GPIO[29]	I/O	I p/u	
	MC30 / C_GPIO[30]	I/O	I p/u	
	MC31 / C_GPIO[31]*	I/O	I p/u	
	MC32 / C_GPIO[32]	I/O	I p/u	
	MC33 / C_GPIO[33]*	I/O	I p/u	

Note*: The pin can trigger interrupt.

Note1: The mvI/O voltage of MC0~15 corresponds to VDD_MC.

Note2: The IO voltage of MC16~21 corresponds to SD_CAP, it could be switched between 3.3/1.8V by the register.

Note3: The IO voltage of MC22~27 corresponds to SD_CAP2, it could be switched between 3.3/1.8V by the register.

Memory card interface pinmux table

Name	NAND Flash (BS*)		SD/MMC/eMMC (BS*)		SPI flash(1~4 bits) (BS*)		SPI Nand Flash (BS*)		SD Card (BS*)		SDIO	
MC0	NAND_D0	I/O	eMMC_D0	I/O	SPI_DO/D0	I/O	SPI_D0					
MC1	NAND_D1	I/O	eMMC_D1	I/O	SPI_DI/D1	I/O	SPI_D1					
MC2	NAND_D2	I/O	eMMC_D2	I/O	SPI_CLK	O	SPI_CLK					
MC3	NAND_D3	I/O	eMMC_D3	I/O	SPI_WP/D2	I/O	SPI_D2					
MC4	NAND_D4	I/O	eMMC_D4	I/O	SPI_HOLD/D3	I/O	SPI_D3					
MC5	NAND_D5	I/O	eMMC_D5	I/O								
MC6	NAND_D6	I/O	eMMC_D6	I/O								
MC7	NAND_D7	I/O	eMMC_D7	I/O								
MC8	NAND_CS0#	O			SPI_CS#	O	SPI_CS#	O				
MC9	NAND_CS1#	O	eMMC_CLK	O								
MC10	NAND_WE#	O										
MC11	NAND_RE#	O	eMMC_CMD	I/O								
MC12	NAND_CLE	O										
MC13	NAND_ALE	O										
MC14	NAND_WP#	O										
MC15	NAND_RDY	I										
MC16									SD_CLK	O		
MC17									SD_CMD	I/O		
MC18									SD_D0	I/O		
MC19									SD_D1	I/O		
MC20									SD_D2	I/O		
MC21									SD_D3	I/O		
Name					DSP JTAG		SPI (3 wires)		SPI (4 wires)		SDIO	
MC22											SDIO2_CLK	O
MC23											SDIO2_CMD	I/O
MC24					DSP_TMS	I					SDIO2_D0	I/O
MC25					DSP_TCK	I					SDIO2_D1	I/O
MC26					DSP_TDI	I					SDIO2_D2	I/O
MC27					DSP_TDO	O					SDIO2_D3	I/O
MC28							SPI4_CLK	O	SPI4_CLK	O	SDIO3_CLK	O
MC29							SPI4_CS	O	SPI4_CS	O	SDIO3_CMD	I/O
MC30									SPI4_DI	I	SDIO3_D0	I/O
MC31							SPI4_DIO	I/O	SPI4_DO	O	SDIO3_D1	I/O
MC32							SPI4_RDY	I	SPI4_RDY	I	SDIO3_D2	I/O
MC33											SDIO3_D3	I/O

Note BS*: In general, it is a resident device. Please choose one of them as boot source(FW).

1.6. LCD interface (31,31)

Pin No.	Name	Type	Reset	Descriptions
	LCD0 / L_GPIO[0] / BS0	mvI/O	I p/d	LCD Signal Bus / BS2..0 : BOOT_SRC The boot source setting description: 0x0: NAND with RS ECC
	LCD1 / L_GPIO[1] / BS1	mvI/O	I p/d	0x1: Boot card (Select by BOOT_CARD) 0x2: eMMC (SDIO3_2) 0x3: USB full speed
	LCD2 / L_GPIO[2] / BS2	mvI/O	I p/d	0x4: SPI flash 0x5: USB high speed 0x6: SPI NAND 0x7: BMC (SPI)
	LCD3 / L_GPIO[3] / BS3	mvI/O	I p/d	LCD Signal Bus / BS3 : BOOT_APLL_RDY 0: normal 1: Boot when APLL ready

	LCD4 / L_GPIO[4] / BS4	mvI/O	I p/d	LCD Signal Bus / BS4 : BOOT_CARD Boot card select 0: SDIO 1: SDIO3 (SDIO3_1)
	LCD5 / L_GPIO[5] / BS5	mvI/O	I p/d	LCD Signal Bus / BS5 : EJTAG_SEL EJTAG select 0: GPIO (TRST, TMS, TCK, TDI, TDO are GPIO) 1: EJTAG
	LCD6 / L_GPIO[6] / BS6	mvI/O	I p/d	LCD Signal Bus / BS6 : MPLL_CLK_SEL Select clock source of PLL. 0: MPLL clock output (FromMPLL clock) 1: Bypass MPLL (From external clock)
	LCD7 / L_GPIO[7] / BS7	mvI/O	I p/d	LCD Signal Bus / BS7 : EMMC_BUSWIDTH eMMC boot bus width 0: 4 bits data bus 1: 8 bits data bus
	LCD8 / L_GPIO[8]	mvI/Os	I p/d	LCD Signal Bus
	LCD9 / L_GPIO[9]	mvI/O	I p/d	
	LCD10 / L_GPIO[10]	mvI/O	I p/d	
	LCD11 / L_GPIO[11]	mvI/O	I p/d	
	LCD12 / L_GPIO[12] / BS8	mvI/O	I p/d	LCD Signal Bus / BS8 : EMMC_BOOTMODE eMMC boot mode 0: single rate + backward timing 1: dual rate + high speed timing
	LCD13 / L_GPIO[13] / BS9	mvI/O	I p/d	LCD Signal Bus/ BS9 : EMMC_DDR_DATA_ORDER eMMC DDR data order 0: Odd byte (1st byte) first 1: Even byte (2nd byte) first
	LCD14 / L_GPIO[14]* / BS10	mvI/O	I p/d	LCD Signal Bus/ BS10 : MIPS_DEBUG_MODE_SEL Enable NT9666x enters CPU debug mode. Internal CPU state will be outputted to debug port on storage interface (MC[18..0]) 0: Normal mode 1: CPU debug mode BS10 for IC debugging setting. Please keep low at reset signal rising edge.
	LCD15/ L_GPIO[15]*	mvI/O	I p/d	LCD Signal Bus
	LCD16 / L_GPIO[16]	mvI/O	I p/d	
	LCD17 / L_GPIO[17]	mvI/O	I p/d	
	LCD18 / L_GPIO[18]	mvI/O	I p/d	

	LCD19 / L_GPIO[19]	mvI/O	I p/d	
	LCD20 / L_GPIO[20]*	mvI/Os	I p/d	
	LCD21 / L_GPIO[21]*	mvI/O	I p/d	
	LCD22 / L_GPIO[22]*	mvI/O	I p/d	
	LCD23 / L_GPIO[23]	mvI/O	I p/d	
	LCD24 / L_GPIO[24]	mvI/O	I p/d	
	LCD25 / L_GPIO[25]	mvI/O	I p/d	
	LCD26 / L_GPIO[26]*	mvI/O	I p/d	
	LCD27 / L_GPIO[27]	mvI/O	I p/d	
	LCD28 / L_GPIO[28]	mvI/O	I p/u	
	LCD29 / L_GPIO[29]	mvI/O	I p/d	
	LCD30 / L_GPIO[30]	mvI/O	I p/d	

Note1: The mvI/O voltage of LCD interface corresponds to VDD_LCD.

LCD interface pinmux table

Name	Parallel RGB (24 bits)		CCIR(16 bits)		i80/M68		CCIR & RGB Main / Secondary		CCIR & RGB (secondary panel)		Ethernet MAC* RMII	
LCD0	RGBC0_0	O	CCIR_Y0	O	MPU_D0	I/O	YCRGB_D0	O				
LCD1	RGBC0_1	O	CCIR_Y1	O	MPU_D1	I/O	YCRGB_D1	O				
LCD2	RGBC0_2	O	CCIR_Y2	O	MPU_D2	I/O	YCRGB_D2	O				
LCD3	RGBC0_3	O	CCIR_Y3	O	MPU_D3	I/O	YCRGB_D3	O				
LCD4	RGBC0_4	O	CCIR_Y4	O	MPU_D4	I/O	YCRGB_D4	O				
LCD5	RGBC0_5	O	CCIR_Y5	O	MPU_D5	I/O	YCRGB_D5	O				
LCD6	RGBC0_6	O	CCIR_Y6	O	MPU_D6	I/O	YCRGB_D6	O				
LCD7	RGBC0_7	O	CCIR_Y7	O	MPU_D7	I/O	YCRGB_D7	O				
LCD8	RGB_CLK	O	CCIR_CLK	O	MPU_TE	I	YCRGB_CLK	O				
LCD9	RGB_VD	O	CCIR_VD	O	MPU_CS#	O	YCRGB_VD	O				
LCD10	RGB_HD	O	CCIR_HD	O	MPU_RS	O	YCRGB_HD	O				
LCD11	RGB_DE	O	CCIR_DE	O	MPU_WR#	O					RMII_R_CLK	O
LCD12	RGBC1_0	O	CCIR_C0	O	MPU_RD#	O	LCD2_D0	O	MPU2_RS	O		
LCD13	RGBC1_1	O	CCIR_C1	O	MPU_D8	I/O	LCD2_D1	O	MPU2_CS	O		
LCD14	RGBC1_2	O	CCIR_C2	O	MPU_D9	I/O	LCD2_D2	O	MPU2_D0	I/O	RMII_RX_DV	I
LCD15	RGBC1_3	O	CCIR_C3	O	MPU_D10	I/O	LCD2_D3	O	MPU2_D1	I/O		
LCD16	RGBC1_4	O	CCIR_C4	O	MPU_D11	I/O	LCD2_D4	O	MPU2_D2	I/O	RMII_RX_ER	I
LCD17	RGBC1_5	O	CCIR_C5	O	MPU_D12	I/O	LCD2_D5	O	MPU2_D3	I/O		
LCD18	RGBC1_6	O	CCIR_C6	O	MPU_D13	I/O	LCD2_D6	O	MPU2_D4	I/O	RMII_RX_D0	I
LCD19	RGBC1_7	O	CCIR_C7	O	MPU_D14	I/O	LCD2_D7	O	MPU2_D5	I/O	RMII_RX_D1	I
LCD20	RGBC2_0	O			MPU_D15	I/O	LCD2_CLK	O	MPU2_D6	I/O		
LCD21	RGBC2_1	O			MPU_D16	I/O	LCD2_VD	O	MPU2_D7	I/O		
LCD22	RGBC2_2	O			MPU_D17	I/O	LCD2_HD	O	MPU2_WR#	O		
LCD23	RGBC2_3	O							MPU2_D8	I/O	RMII_TX_EN	O

LCD24	RGBC2_4	O							MPU2_RD#	O	RMII_TX_D0	O
LCD25	RGBC2_5	O							MPU2_TE	I	RMII_TX_D1	O
LCD26	RGBC2_6	O										
LCD27	RGBC2_7	O										
LCD28	**LCD_CS**	O										
LCD29	**LCD_CLK**	O										
LCD30	**LCD_DAT**	O										
P_GPIO[25]	SB_CK23										RMII_MDIO	I/O
P_GPIO[26]	SB_DAT23										RMII_MDC	O

Note 1*: There are two pins allocated in Peripheral I/O group. This chip also supports Ethernet MII interface.

1.7. PWM (20,20)

Pin No.	Name	Type	Reset	Descriptions
	P_GPIO[0] / PWM0	I/O	I p/d	PWM output pin. Mechanical Shutter control output. Micro-stepping control module 1.
	P_GPIO[1] / PWM0	I/O	I p/d	
	P_GPIO[2] / PWM2	I/O	I p/d	
	P_GPIO[3]* / PWM3	I/O	I p/d	
	P_GPIO[4] / PWM4	I/O	I p/d	PWM output pin. Micro-stepping control module 2. Serial Peripheral Interface
	P_GPIO[5] / PWM5	I/O	I p/d	
	P_GPIO[6]* / PWM6	I/O	I p/d	
	P_GPIO[7] / PWM7	I/O	I p/d	
	P_GPIO[8] / PWM8	I/O	I p/d	PWM output pin. Micro-stepping control module 3.
	P_GPIO[9] / PWM9	I/O	I p/d	
	P_GPIO[10] / PWM10	I/O	I p/d	
	P_GPIO[11]* / PWM11	I/O	I p/d	
	P_GPIO[12] / PWM12	I/O	I p/d	PWM output pin. Micro-stepping control module 4.
	P_GPIO[13] / PWM13	I/O	I p/d	
	P_GPIO[14] / PWM14	I/O	I p/d	
	P_GPIO[15]* / PWM15	I/O	I p/d	
	P_GPIO[16] / PWM16	I/O	I p/d	PWM output pin. Mechanical Shutter control output.
	P_GPIO[17] / PWM17	I/O	I p/d	

	P_GPIO[18] / PWM18	I/O	I p/d	PWM output pin.
	P_GPIO[19]* / PWM19	I/O	I p/d	PWM output pin.

Name	PWM		M-shutter		u-stepping		UART				CCIR input	
P_GPIO[0]	PWM0	O	ME_SHUT0	O	uSTP1_A	O					SIE3_YC0	I
P_GPIO[1]	PWM1	O	ME_SHUT1	O	uSTP1_B	O					SIE3_YC1	I
P_GPIO[2]	PWM2	O	ME2_SHUT0	O	uSTP1_C	O					SIE3_YC2	I
P_GPIO[3]	PWM3	O	ME2_SHUT1	O	uSTP1_D	O					SIE3_YC3	I
P_GPIO[4]	PWM4	O			uSTP2_A	O	UART4_TX	O			SIE3_YC4	I
P_GPIO[5]	PWM5	O			uSTP2_B	O	UART4_RX	I			SIE3_YC5	I
P_GPIO[6]	PWM6	O			uSTP2_C	O	UART4_RTS	O			SIE3_YC6	I
P_GPIO[7]	PWM7	O			uSTP2_D	O	UART4_CTS	I			SIE3_YC7	I
P_GPIO[8]	PWM8	O			uSTP3_A	O					SIE3_PCLK	I
P_GPIO[9]	PWM9	O			uSTP3_B	O					SIE3_VD	I
P_GPIO[10]	PWM10	O			uSTP3_C	O					SIE3_HD	I
P_GPIO[11]	PWM11	O			uSTP3_D	O					SIE4_PCLK	I
P_GPIO[12]	PWM12	O			uSTP4_A	O					SIE4_YC0	I
P_GPIO[13]	PWM13	O			uSTP4_B	O					SIE4_YC1	I
P_GPIO[14]	PWM14	O			uSTP4_C	O					SIE4_YC2	I
P_GPIO[15]	PWM15	O			uSTP4_D	O					SIE4_YC3	I
P_GPIO[16]	PWM16	O									SIE4_YC4	I
P_GPIO[17]	PWM17	O									SIE4_YC5	I
P_GPIO[18]	PWM18	O									SIE4_YC6	I
P_GPIO[19]	PWM19	O									SIE4_YC7	I
P_GPIO[39]											SIE4_VD	I
P_GPIO[40]											SIE4_HD	I

1.8. Peripheral I/O (23,19)

Pin No.	Name	Type	Reset	Descriptions
	P_GPIO[20] / SP_CLK	I/Oss	I p/d	Clock Output for peripheral device.
	P_GPIO[21]* / I2C_SDA	I/OD	I p/u	I2C-BUS clock output(Open Drain IO structure)
	P_GPIO[22] / I2C_SCL	I/OD	I p/u	I2C-BUS data input / output(Open Drain IO structure)
	P_GPIO[23] / SB_CS2 / SPI3_CS	I/O	I p/u	Serial Interface Chip Select 2 Serial Peripheral Interface 3 chip select output
	P_GPIO[24]* / SB_CS3 / SPI3_DI	I/O	I p/u	Serial Interface Chip Select 3 Serial Peripheral Interface 3 data input
	P_GPIO[25] / SB_CK23 / SPI3_CLK	I/O	I p/d	Serial Interface Clock 2 & 3 Serial Peripheral Interface 3 clock output
	P_GPIO[26] / SB_DAT23 / SPI3_DO	I/O	I p/d	Serial Interface Data 2 & 3 Serial Peripheral Interface 3 data output
	P_GPIO[27] / SB_CS4	I/O	I p/u	Serial Interface Chip Select 4
	P_GPIO[28] /	I/O	I p/u	Serial Interface Chip Select 5

	SB_CS5			
	P_GPIO[29] / SB_CK45	I/O	I p/d	Serial Interface Clock 4 & 5
	P_GPIO[30] / SB_DAT45	I/O	I p/d	Serial Interface Data 4 & 5
	P_GPIO[31] / UART2_TX SPI5_CS	I/O	I p/u	UART2 Transmit Serial Peripheral Interface 5 chip select output
	P_GPIO[32]* / UART2_RX / SPI5_CLK	I/O	I p/u	UART2 Receive Serial Peripheral Interface 5 clock output
	P_GPIO[33]* / UART2_RTS / SPI5_DO	I/O	I p/u	UART2 Request To Send Serial Peripheral Interface 5 data output
	P_GPIO[34]* / UART2_CTS / SPI5_DI	I/O	I p/u	UART2 Clear To Send Serial Peripheral Interface 5 data input
	P_GPIO[35] / SPI2_CS	I/O	I p/u	Serial Peripheral Interface 2 Chip Select output
	P_GPIO[36] / SPI2_CLK	I/O	I p/d	Serial Peripheral Interface 2 Clock output
	P_GPIO[37] / SPI2_DO	I/O	I p/d	Serial Peripheral Interface 2 Data Output
	P_GPIO[38]* / SPI2_DI	I/O	I p/u	Serial Peripheral Interface 2 Data Input
	P_GPIO[39]* / REMOTE_RX / PICNT3	I/Oss	I p/u	Infrared Remote-control Received Data Pulse Counter 3 input
	P_GPIO[40]* / FL_TRIG	I/Os	I p/d	Flash Light Trigger Control
	P_GPIO[41] / UART_TX	I/O	O	UART Transmit
	P_GPIO[42]* / UART_RX	I/O	I p/u	UART Receive

Name	Function 1		Function 2		Function 3		UART		SPI (4W/3W)		I2S	
P_GPIO[20]	SP_CLK	O	PICNT4	I							I2S_MCLK	O
P_GPIO[23]	SB_CS2						UART3_RX	O	SPI3_CS	O		
P_GPIO[24]	SB_CS3						UART3_TX	I	SPI3_DI/NULL	I		
P_GPIO[25]	SB_CK23				RMII_MDIO	I/O	UART3_RTS	O	SPI3_CLK	O		
P_GPIO[26]	SB_DAT23				RMII_MDC	O	UART3_CTS	I	SPI3_DO/DIO	I/O		
P_GPIO[31]							UART2_RX	O	SPI5_CS	O	I2S_BCLK	IO
P_GPIO[32]							UART2_TX	I	SPI5_CLK	O	I2S_SYNC	IO
P_GPIO[33]			PICNT1				UART2_RTS	O	SPI5_DO/DIO	I/O	I2S_SDO	O
P_GPIO[34]			PICNT2				UART2_CTS	I	SPI5_DI/NULL	I	I2S_SDI	I
P_GPIO[35]									SPI2_CS	O		
P_GPIO[36]									SPI2_CLK	O		
P_GPIO[37]									SPI2_DO/DIO	I/O		
P_GPIO[38]									SPI2_DI/NULL	O		
P_GPIO[39]	REMOTE_RX		PICNT3		SP_CLK2							

1.9. Dedicated I/O (2,2)

Pin No.	Name	Type	Reset	Descriptions
	DGPIO0*	I/Os	I p/u	Card detect input pin
	DGPIO1*	I/Os	I p/u	Write protect input pin

1.10. ADC interface (8,6)

Pin No.	Name	Type	Reset	Descriptions
	AD_IN0	AI	-	General ADC 0 Input with buffer
	AD_IN1*	AI	-	General ADC 1 Input with configurable trigger function
	AD_IN2*	AI	-	General ADC 2 Input with configurable trigger function
	AD_IN3	AI	-	General ADC 3 Input with buffer
	AD_IN4	AI	-	General ADC 4 Input
	AD_IN5	AI	-	General ADC 5 Input
	AD_IN6*	AI	-	General ADC 6 Input with configurable trigger function
	AD_IN7	AI	-	General ADC 7 Input

1.11. Audio Codec(12,9)

Pin No.	Name	Type	Reset	Descriptions
	AUD_CAP	AI	-	Internal Supply Voltage decoupling for audio circuit
	MIC_BIAS	AO	-	Microphone working bias output.
	MIC_RINP	AI	-	Right channel microphone differential input positive side.
	MIC_RINN	AI	-	Right channel microphone differential input negative side.
	MIC_LINP	AI	-	Left channel microphone differential input positive side.
	MIC_LINN	AI	-	Left channel microphone differential input negative side.
	AUD_VMIDX	AO	-	Decoupling for audio codec reference voltage.
	AUD_VRP	AO	-	Decoupling for audio codec positive reference voltage.
	HP_R	AO	-	Right channel headphone output. (or Line out)
	HP_L	AO	-	Left channel headphone output. (or Line out)
	SPK_P	AO	-	Speaker Output of Right Channel
	SPK_N	AO	-	Speaker Output of Left Channel

1.12. TV interface (1,1)

Pin No.	Name	Type	Reset	Descriptions
	TV_CVBS	AO	-	Video Data Output Composite video output.

1.13. Vx1 (0,5)

Pin No.	Name	Type	Reset	Descriptions
	Vx1_RxP	AI	-	Vx1 Main Link differential input
	Vx1_RxN	AI	-	

	Vx1_SLP	AIO	-	Vx1 Sub Link differential signal
	Vx1_SLN	AIO	-	
	Vx1_REXT	AI		Vx1 reference resistor

1.14. MIPI DSI (7,11)

Pin No.	Name	Type	Reset	Descriptions
	DSI_CAP	P	-	Internal Supply Voltage decoupling for DSI LP mode circuit.
	DSI_CKP	AO	-	MIPI DSI differential clock lane output
	DSI_CKN	AO	-	
	DSI_D0P	AO	-	MIPI DSI differential data lane input / output
	DSI_D0N	AO	-	
	DSI_D1P	AO	-	
	DSI_D1N	AO	-	
	DSI_D2P	AO	-	
	DSI_D2N	AO	-	
	DSI_D3P	AO	-	
	DSI_D3N	AO	-	

1.15. HDMI (12,11)

Pin No.	Name	Type	Reset	Descriptions
	HDMI_TXCP	AO	-	TMDS Low Voltage Differential Signal Output Clock
	HDMI_TXCN			
	HDMI_TX0P	AO	-	TMDS Low Voltage Differential Signal Output Data
	HDMI_TX0N			
	HDMI_TX1P			
	HDMI_TX1N			
	HDMI_TX2P			
	HDMI_TX2N			
	HDMI_CEC / P_GPIO[27]*	I/O_{5VT}	I p/u	Consumer Electronics Control. CEC is 5V tolerance input.
	DDC_SDA / P_GPIO[28]	I/OD_{5VT}	I p/u	Display Data Channel SDA. DDCSDA is 5V tolerance input.
	DDC_SCL / P_GPIO[29]	I/OD_{5VT}	I p/u	Display Data Channel SCL. DDCSCL is 5V tolerance input.
	HDMI_PLUG / P_GPIO[30]*	I/O_{5VT}	I p/d	Hot Plug Detect. HOTPLUG is 5V tolerance input.

1.16. USB device interface (6,3)

Pin No.	Name	Type	Reset	Descriptions
	VBUS	I_{5VTZ}	I p/d	USB1 V_{BUS} Input. This pin is 5V tolerance input
	VBUS2	I_{5VTZ}	I p/d	USB2 V_{BUS} Input. This pin is 5V tolerance input
	USB_DP	AI/O	-	USB1 FS/HS Differential Data Plus (D+)

	USB_DM	AI/O	-	USB1 FS/HS Differential Data Minus (D-)
	USB2_DP	AI/O	-	USB2 FS/HS Differential Data Plus (D+)
	USB2_DM	AI/O	-	USB2 FS/HS Differential Data Minus (D-)

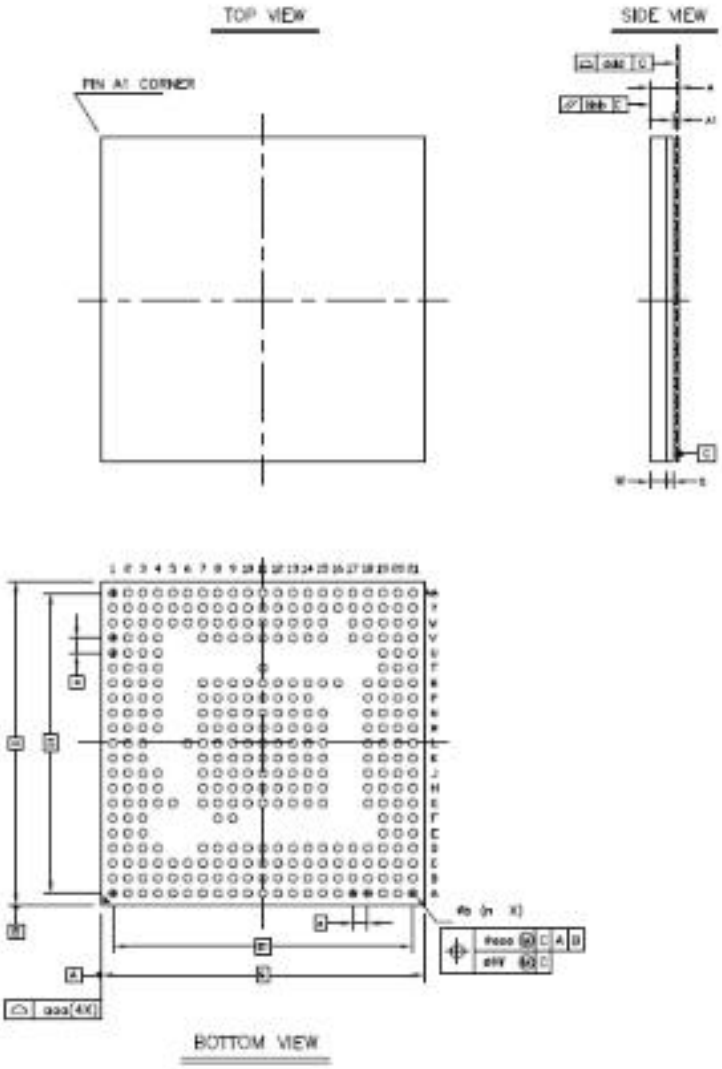
1.17. Power (90)

Pin No.	Name	Type	Descriptions
	VDDK(17)	P	Core Power
	VDD_IO(5)	P	I/O Pad Power
	GND(26)	P	Digital Ground
	VDD_DRCLK	P	DDR clock I/O Power
	VDD_DRCA(2)	P	DDR command and address I/O Power
	VDD_DRDQ(3)	P	DDR data bus IO Power
	GND_CLK	P	Ground for DRAM clock
	AVDD_DR_1V	P	Analog 1.0V power for DDR PHY
	AVDD_DLL	P	DLL power for core circuit
	AVDD_HDLL	P	DLL power for analog block
	AGND_HDLL	P	Gorund for DLL
	VDD_RTC(1)	P	RTC Power
	VDD_VBAT(1)	P	Battery input for power button controller
	VDD_MC(1)	P	Multi-level IO power for Memory Card
	AVDD_HSI_K	P	Analog 1.0V power for HSI core power
	AVDD_HSI_RX	P	Analog 3.3V power for HSI receiver
	VDD_HSI_IO	P	Multi-level input power of HSI
	AGND_HSI(2)	P	Ground for High Speed Interface
	VDD_SN	P	Multi-level IO Power for sensor interface
	VDD_LCD(2)	P	Multi-level IO power for LCD interface
	VDD_Vx1	P	NC(reserved for test)
	AVDD_Vx1	P	
	AGND_Vx1	P	
	AVDD_DSI_K	P	Analog power for MIPI DSI core
	VDD_DSI_IO	P	LDO's input power for MIPI DSI LP IO
	AGND_DSI	P	Ground for MIPI DSI
	AVDD_ADC	P	Analog 3.3V power for ADC
	AGND_ADC	P	Ground for ADC
	AVDD_DAC	P	Analog 3.3V power for TV DAC
	AGND_DAC	P	Ground for TV DAC
	AVDD_AUD	P	Analog 3.3V power for Audio Codec
	AGND_AUD	P	Ground for Audio Codec
	AVDD_SPK	P	Analog 3.3V power for Speaker Amplifier
	AGND_SPK	P	Ground for Speaker Amplifier
	AVDD_HDMI	P	Analog HDMI interface Power
	AGND_HDMI	P	Ground for HDMI interface
	AVDD_USB	P	Analog USB interface Power
	AGND_USB	P	Ground for USB
	AVDD_MPLL	P	Multiple PLL analog Power
	AGND_MPLL	P	PLL analog Power

Package Information

1.

TFBGA-344



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package			HS LFBGA		
Body Size	X	E		14.000	
	Y	D		14.000	
Ball Pitch		e		0.650	
Total Thickness		A			1.400
Mold Thickness		M		0.700 Ref.	
Substrate Thickness		S		0.260 Ref.	
Ball Diameter				0.350	
Stand Off		A1	0.220	–	0.320
Ball Width		b	0.320	–	0.420
Package Edge Tolerance		aaa		0.150	
Mold Flatness		bbb		0.080	
Coplanarity		ddd		0.080	
Ball Offset (Package)		eee		0.150	
Ball Offset (Ball)		fff		0.080	
Ball Count		n		344	
Edge Ball Center to Center	X	e1		13.000	
	Y	e1		13.000	

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Electrical Characteristics

1.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage of 1.0V Core power	V_{DDK}	-0.3 ~ +1.2	V
Supply Voltage of DRAM I/O	V_{DD_DR}	-0.3 ~ +2.1	V
Supply Voltage of 3.3V Digital I/O	V_{DD_VBAT}, V_{DD_RTC}, V_{DD_IO}, $V_{DD\_DSI\_IO}$	-0.3 ~ +3.8	V
Supply Voltage of multi-level I/O	V_{DD_MC}, $V_{DD\_HSI\_IO}$, V_{DD_SN}, V_{DD_LCD}	-0.3 ~ +3.8	V
Supply Voltage of 1.0V analog block	$AV_{DD\_DR\_1V}$, $AV_{DD\_HSI\_K}$, $AV_{DD\_DSI\_K}$,	-0.3 ~ +1.2	V
Supply Voltage of 1.5/1.8V analog block	AV_{DD_DLL} AV_{DD_MPLL} AV_{DD_HDMI}	-0.3 ~ +2.1	V
Supply Voltage of 3.3V analog block	AV_{DD_HDLL}, $AV_{DD\_HSI\_RX}$, AV_{DD_USB}, AV_{DD_ADC}, AV_{DD_DAC}, AV_{DD_AUD}, AV_{DD_SPK}, AV_{DD_VX1}	-0.3 ~ +3.8	V
Input/Output Voltage	I/O	-0.3 ~ V_{DD_IO} +0.3	V
Input Voltage(5V Tolerant)	I/O_{5VT}	-0.3 ~ +5.8	V
Operating Ambient Temperature	T_{OPR}	-20 ~ 85	^{0}C
Operating Ambient Temperature (Industrial grade version)	T_{OPR}	-40 ~ 85	^{0}C
Storage Temperature	T_{STG}	-55 ~ 125	^{0}C

*

Comment

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

2. ESD performance

Model	Standard	Classification	Note
Human Body Mode(HBM)	MIL-STD-883G Method 3015.7	Class : 2	2K~4KV
Machine Mode(MM)	JEDEC Specification EIA/JESD22-A115	Class : B	200~400V
CDM Mode(CDM)	JEDEC Specification JESD22-C101		

3. Latch-up Immunity

Model	Standard	Classification	Note
Latch up	JEDEC Specification JESD-78A	Class : I	±200mA

4. Recommended Operating Conditions

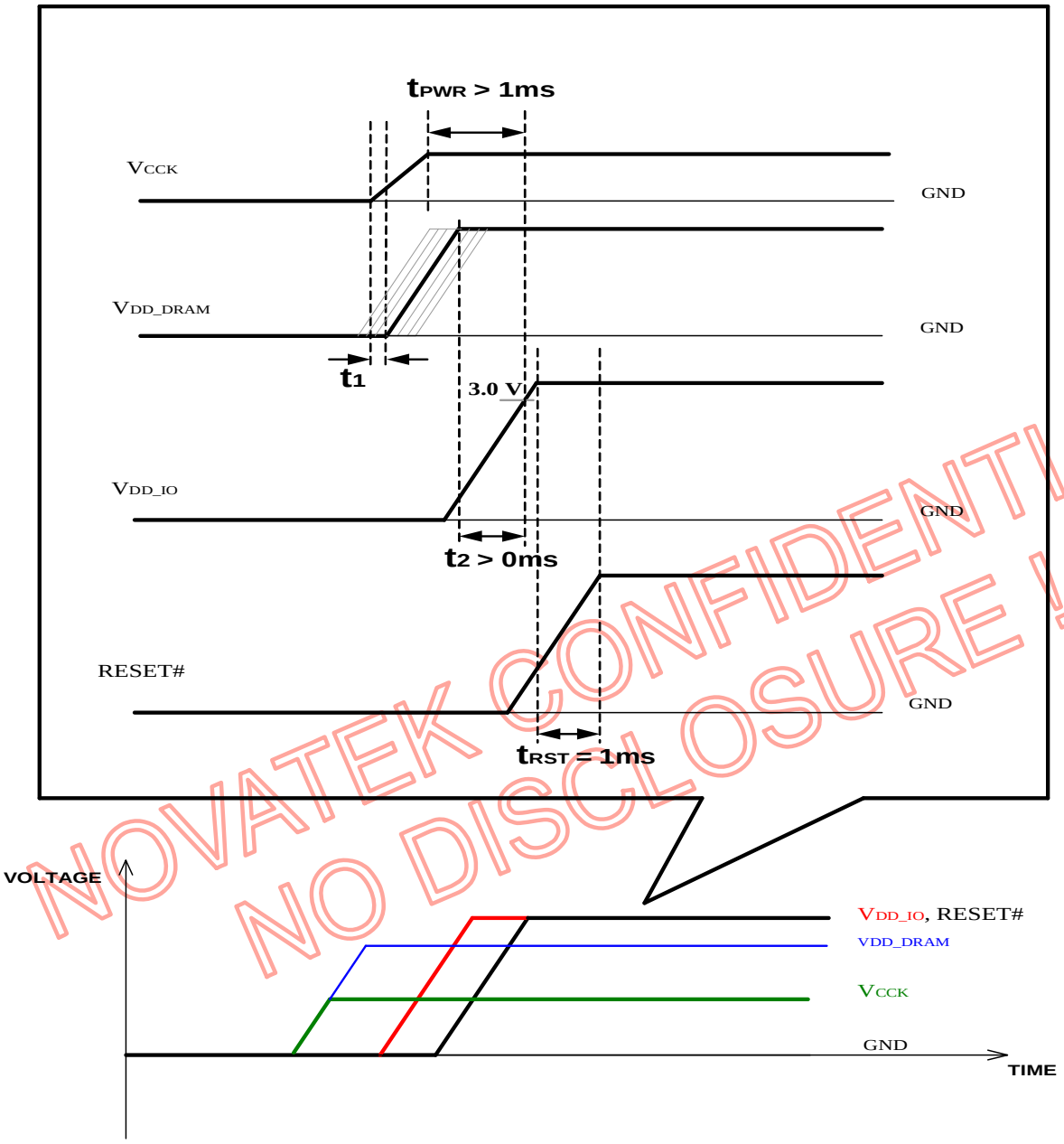
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DDK}	Core Logic Operating Voltage	1.0	1.1	1.2	V	
$AV_{DD\_DR\_1V}$	Core Logic of DDR PHY Operating Voltage	1.0	1.1	1.2	V	
V_{DD_DR}	DDR PHY I/O Interface Operating Voltage	1.425	1.5	1.575	V	DDR3 DRAM
		1.283	1.35	1.45	V	DDR3L DRAM
AV_{DD_HDLL}	DDR PHY Analog 3.3V Power	3.0	3.3	3.6	V	
AV_{DD_DLL}	DDR PHY Analog 1.5V Power	1.425	1.5	1.65	V	
AV_{DD_MPLL}	MPLL Operating Voltage	1.35	1.5	1.65	V	
V_{DD_RTC}	RTC Operating Voltage	1.5	-	3.6	V	
V_{DD_RTC}	RTC Maintenance Voltage	1	-	3.6	V	
V_{DD_VBAT}	Power Controller Operating Voltage	2.2	-	3.6	V	
V_{DD_IO}	General I/O Interface Operating Voltage	3.0	3.3	3.6	V	
V_{DD_MC}	I/O of Memory Card Interface Operating Voltage	1.62	3.3	3.6	V	1.8V~3.3V
$AV_{DD\_DSI\_K}$	Core Logic of MIPI DSI Operating Voltage	1.0	1.1	1.2	V	
$V_{DD\_DSI\_IO}$	LDO of MIPI DSI	3.0	3.3	3.6	V	

	Operating Voltage					
V_{DD_LCD}	I/O of LCD Interface Operating Voltage	1.62	3.3	3.6	V	1.8V~3.3V
AV_{DD_HDMI}	Transceiver of HDMI Operating Voltage	1.35	1.5	1.65	V	
AV_{DD_DAC}	Video DAC Operating Voltage	3.0	3.3	3.6	V	
$AV_{DD\_HSI\_K}$	Core Logic of High Speed Interface Operating Voltage	1.0	1.1	1.2	V	
$AV_{DD\_HSI\_RX}$	Receiver of High Speed Interface Operating Voltage	3.0	3.3	3.6	V	
$V_{DD\_HSI\_IO}$	Input of High Speed Interface Operating Voltage	1.62	3.3	3.6	V	1.8V~3.3V
V_{DD_SN}	I/O of Sensor Interface Operating Voltage	1.62	3.3	3.6	V	1.8V~3.3V
AV_{DD_VX1}	Vx1 Operating Voltage	3.0	3.3	3.6	V	
AV_{DD_ADC}	ADC Operating Voltage	3.0	3.3	3.6	V	
AV_{DD_USB}	USB PHY Operating Voltage	3.0	3.3	3.6	V	
AV_{DD_AUD}	Audio Codec Operating Voltage	3.2	3.3	3.6	V	
AV_{DD_SPK}	Speaker Amplifier Operating Voltage	3.0	3.3	3.6	V	

5. AC/DC Characteristics

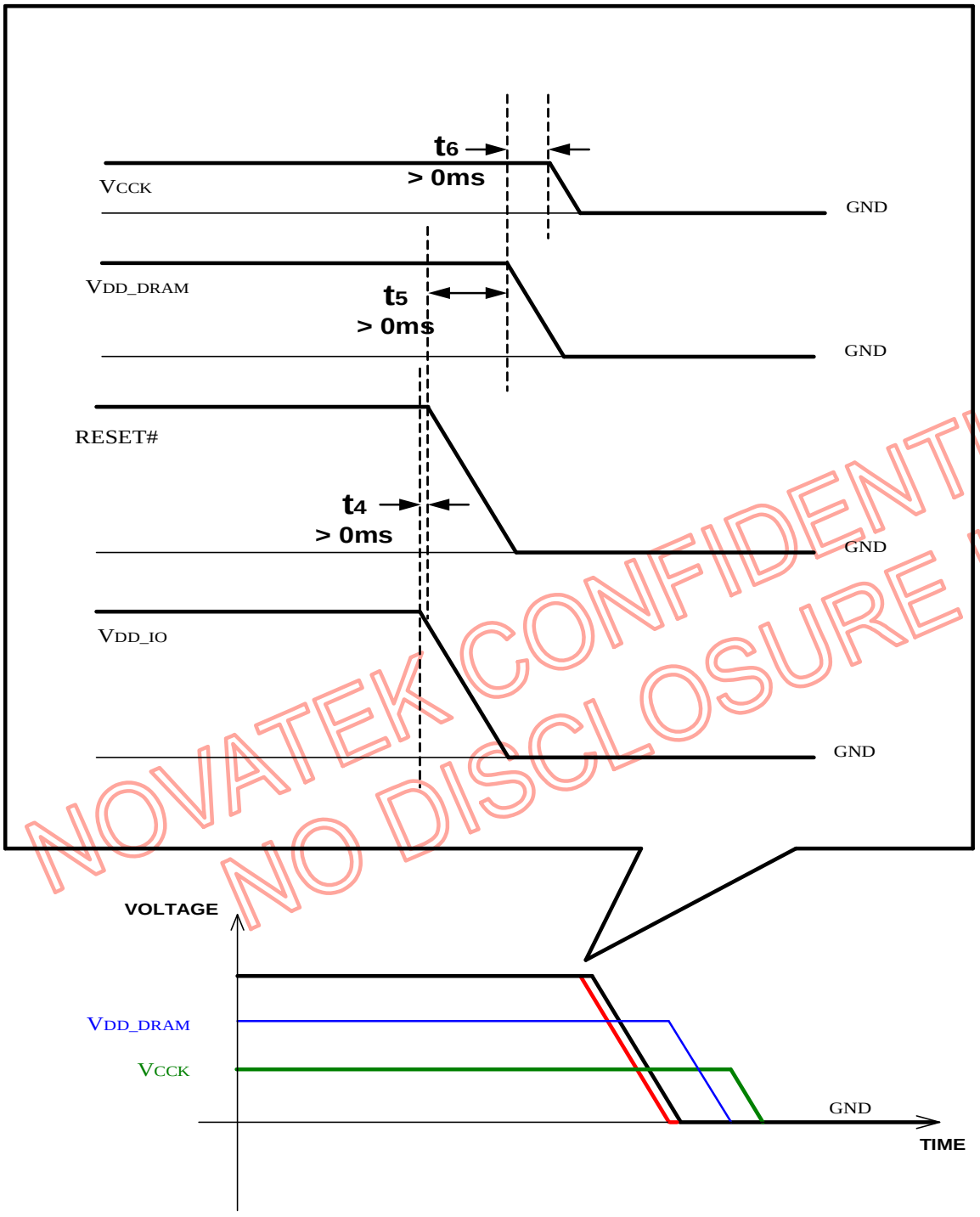
5.1. Power on Sequence

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Power on sequence and Reset						
T_{RST}	RESET# sustained time	1	-	-	ms	After power being stable
T_{PWR}	Core power prior to I/O power time	1	-	-	ms	



POWER-ON SQUENCE

Note： Even $t_1 \geqq 0$ ms or $t_1 < 0$ ms is acceptable, but it is necessary to make sure $t_2 > 0$ ms .



POWER-OFF SEQUENCE

Note：

Novatek recommends that $t_4 > 0$ ms, $t_5 > 0$ ms, and $t_6 > 0$ ms for a stable system application. But they are not the required restrictions for Novatek's DSP.

5.2. General I/O

(V_{DDK}=1.1V, Temp=25^{0}C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
3.3V I/O General characteristic						
V_{P_IO}	IO power supply	3.0	3.3	3.6	V	
V_{IH}	Input high voltage	2.0	-	-	V	
V_{IL}	Input low voltage	-	-	0.8	V	
V_{T+}	Schmitt trigger high threshold	-	1.625	-	V	
V_{T-}	Schmitt trigger low threshold	-	1.325	-	V	
V_{HYST}	Hysteresis	0.25	-	0.34	V	
V_{OH}	Output high voltage	V_{P_IO} -0.4	-	-	V	
V_{OL}	Output low voltage	-	-	0.4	V	
I_{LI}	Input leakage current	-10	-	+10	uA	
I_{LO}	Output leakage current	-10	-	+10	uA	
R_{PU}	Pull-up resistor	-	44	-	kΩ	
R_{PD}	Pull-down resistor	-	44	-	kΩ	
I_{OH}	Output high driving current	2.4	-	-	mA	Level setting 0
		4.8	-	-	mA	Level setting 1
		7.2	-	-	mA	Level setting 2
		9.6	-	-	mA	Level setting 3
I_{OL}	Output low driving current	2.4	-	-	mA	Level setting 0
		4.8	-	-	mA	Level setting 1
		7.2	-	-	mA	Level setting 2
		9.6	-	-	mA	Level setting 3
3.3V I/O_S (strong driving/sinking output capacity)						
I_{OH}	Output high driving current	4.8	-	-	mA	Level setting 0
		9.6	-	-	mA	Level setting 1
		14.4	-	-	mA	Level setting 2
		19.2	-	-	mA	Level setting 3
I_{OL}	Output low driving current	4.8	-	-	mA	Level setting 0
		9.6	-	-	mA	Level setting 1
		14.4	-	-	mA	Level setting 2
		19.2	-	-	mA	Level setting 3
3.3V I/O_{S2} (double strong driving/sinking output capacity)						
R_{PU}	Pull-up resistor	-	22	-	kΩ	
R_{PD}	Pull-down resistor	-	22	-	kΩ	
I_{OH}	Output high driving current	4.8	-	-	mA	Level setting 0
		9.6	-	-	mA	Level setting 1
		14.4	-	-	mA	Level setting 2
		19.2	-	-	mA	Level setting 3
		24	-	-	mA	Level setting 4

		28.8	-	-	mA	Level setting 5
		33.6	-	-	mA	Level setting 6
		38.4	-	-	mA	Level setting 7
I_{OL}	Output low driving current	4.8	-	-	mA	Level setting 0
		9.6	-	-	mA	Level setting 1
		14.4	-	-	mA	Level setting 2
		19.2	-	-	mA	Level setting 3
		24	-	-	mA	Level setting 4
		28.8	-	-	mA	Level setting 5
		33.6	-	-	mA	Level setting 6
		38.4	-	-	mA	Level setting 7
2.5V I/O General characteristic						
V_{P_IO}	IO power supply	2.25	2.5	2.75	V	
V_{IH}	Input high voltage	1.7	-	-	V	
V_{IL}	Input low voltage	-	-	0.7	V	
V_{t+}	Schmitt trigger high threshold	-	1.295	-	V	
V_{t-}	Schmitt trigger low threshold	-	1.025	-	V	
V_{HYST}	Hysteresis	0.21	-	0.31	V	
V_{OH}	Output high voltage	V_{P_IO} -0.4	-	-	V	
V_{OL}	Output low voltage	-	-	0.4	V	
I_{LI}	Input leakage current	-10	-	+10	uA	
I_{LO}	Output leakage current	-10	-	+10	uA	
R_{PU}	Pull-up resistor	-	58	-	kΩ	
R_{PD}	Pull-down resistor	-	58	-	kΩ	
I_{OH}	Output high driving current	1.8	-	-	mA	Level setting 0
		3.6	-	-	mA	Level setting 1
		5.4	-	-	mA	Level setting 2
		7.2	-	-	mA	Level setting 3
I_{OL}	Output low driving current	1.8	-	-	mA	Level setting 0
		3.6	-	-	mA	Level setting 1
		5.4	-	-	mA	Level setting 2
		7.2	-	-	mA	Level setting 3
2.5V I/O_S (strong driving/sinking output capacity)						
I_{OH}	Output high driving current	3.6	-	-	mA	Level setting 0
		7.2	-	-	mA	Level setting 1
		10.8	-	-	mA	Level setting 2
		14.4	-	-	mA	Level setting 3
I_{OL}	Output low driving current	3.6	-	-	mA	Level setting 0
		7.2	-	-	mA	Level setting 1
		10.8	-	-	mA	Level setting 2
		14.4	-	-	mA	Level setting 3
1.8V I/O General characteristic						
V_{P_IO}	IO power supply	1.62	1.8	1.98	V	

V_{IH}	Input high voltage	1.2	-	-	V	
V_{IL}	Input low voltage	-	-	0.6	V	
V_{t+}	Schmitt trigger high threshold	-	1.005	-	V	
V_{t-}	Schmitt trigger low threshold	-	0.745	-	V	
V_{HYST}	Hysteresis	0.2	-	0.3	V	
V_{OH}	Output high voltage	V_{P_IO} -0.4	-	-	V	
V_{OL}	Output low voltage	-	-	0.4	V	
I_{LI}	Input leakage current	-10	-	+10	uA	
I_{LO}	Output leakage current	-10	-	+10	uA	
R_{PU}	Pull-up resistor	-	98	-	kΩ	
R_{PD}	Pull-down resistor	-	98	-	kΩ	
I_{OH}	Output high driving current	1.2	-	-	mA	Level setting 0
		2.2	-	-	mA	Level setting 1
		3.3	-	-	mA	Level setting 2
		4.4	-	-	mA	Level setting 3
I_{OL}	Output low driving current	1.2	-	-	mA	Level setting 0
		2.2	-	-	mA	Level setting 1
		3.3	-	-	mA	Level setting 2
		4.4	-	-	mA	Level setting 3
1.8V I/O_S (strong driving/sinking output capacity)						
I_{OH}	Output high driving current	2.2	-	-	mA	Level setting 0
		4.4	-	-	mA	Level setting 1
		6.6	-	-	mA	Level setting 2
		8.8	-	-	mA	Level setting 3
I_{OL}	Output low driving current	2.2	-	-	mA	Level setting 0
		4.4	-	-	mA	Level setting 1
		6.6	-	-	mA	Level setting 2
		8.8	-	-	mA	Level setting 3

5.3. Specific function I/O(RTC, Reset, LVD and PBC)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
RTC						
$T_{START-UP}$	RTC 32768Hz crystal start up time	-	250	-	ms	V_{DD_RTC} = 3V
I_{RTC}	Operating current of RTC	-	-	1	uA	V_{DD_RTC} = 2.5V
V_{DD_RTCO}	Operating voltage of RTC	1.5	-	3.6	V	V_{DD_BAT} >= 2.2V
V_{DD_RTCM}	Maintenance voltage of RTC	1	-	3.6	V	no V_{DD_BAT}
RESET# & Low Voltage Detector						
R_{PU_RST}	Pull-Up Resistor of RESET#	-	124	-	KΩ	VDD_IO=3.3V
R_{PD_RST}	Pull-Down Resistor of	-	730	-	Ω	VDD_IO=3.3V

	RESET#					
V_{LVD_DET+}	LVD Logic 1 Detect Level	-	2.55	2.7	V	
V_{LVD_DET-}	LVD Logic 0 Detect Level	2.25	2.4	-	V	
V_{T+_RESET}	Schmitt Trigger Positive Going Threshold (RESET)	-	2.3	-	V	
V_{T-_RESET}	Schmitt Trigger Negative Going Threshold (RESET)	-	1.7	-	V	
Power Button Controller						
V_{T+}	Schmitt Trigger Positive Going Threshold (PWR_SW1,PWR_SW2, PWR_SW3,PWR_SW4)	-	1.5	1.8	V	V_{DD_RTC} = 3.0V
V_{T-}	Schmitt Trigger Negative Going Threshold (PWR_SW1,PWR_SW2, PWR_SW3,PWR_SW4)	1	1.3	-	V	V_{DD_RTC} = 3.0V
V_{PFD+}	PFD Positive Going Threshold Voltage (Core power)	-	0.9	0.95	V	
V_{PFD-}	PFD Negative Going Threshold Voltage (Core power)	0.80	0.85	-	V	
I_{SW1-pd}	Pull-Down Current (PWR_SW1)	-	10	-	uA	V_{DD_RTC} = 3.0V
I_{SW2-pu}	Pull-Up Current (PWR_SW2)	-	10	-	uA	V_{DD_RTC} = 3.0V
I_{SW3-pd}	Pull-Down Current (PWR_SW3)	-	3	-	uA	V_{DD_RTC} = 3.0V
I_{SW4-pd}	Pull-Down Current (PWR_SW4)	-	1	-	uA	V_{DD_RTC} = 3.0V
R_{OH}	Resistor of PWR_EN Output High	1100	1300	1500	Ω	V_{OH}=2.9V, V_{DD_VBAT}=3.3V
R_{OL}	Resistor of PWR_EN Output Low	180	250	320	Ω	V_{OL}=0.4V, V_{DD_VBAT}=3.3V
V_{OH}	PWR_EN Output High Voltage	V_{DD_VBAT} - 0.2	-	-	V	@ I_{OH} = 100uA
V_{OL}	PWR_EN Output Low Voltage	-	-	0.1	V	@ I_{OL} = -100uA

5.4. DDR3 / DDR3L Interfance

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DC specification						
V_{REF}	DDR PHY I/O Reference Voltage	0.49* V_{DD_DR}	-	0.51* V_{DD_DR}	V	
DDR3 Single-Ended Output logic level						
$V_{OH(DC)}$	DC Output High (Logic 1) Voltage	V_{REF} +0.100	-	V_{DD_DR}	V	

$V_{OL(DC)}$	DC Output Low (Logic 0) Voltage	V_{SS}	-	V_{REF} -0.100	V	
$V_{OH(AC)}$	AC Output High (Logic 1) Voltage	V_{REF} +0.15	-	Note1	V	
$V_{OL(AC)}$	AC Output Low (Logic 0) Voltage	Note1	-	V_{REF} -0.15	V	
DDR3L Single-Ended Output logic level						
$V_{OH(DC)}$	DC Output High (Logic 1) Voltage	V_{REF} +0.09	-	V_{DD_DR}	V	
$V_{OL(DC)}$	DC Output Low (Logic 0) Voltage	V_{SS}	-	V_{REF} -0.09	V	
$V_{OH(AC)}$	AC Output High (Logic 1) Voltage	V_{REF} +0.135	-	Note1	V	
$V_{OL(AC)}$	AC Output Low (Logic 0) Voltage	Note1	-	V_{REF} -0.135	V	
DDR3 Differential Output logic level						
$V_{OH(Diff)}$	Differential output high voltage	0.200	-	Note2	V	
$V_{OL(Diff)}$	Differential output low voltage	Note2	-	-0.200	V	
$V_{OHDiff(AC)}$	Differential output high AC voltage	2 * ($V_{OH(AC)}$ - V_{REF})	-	Note2	V	
$V_{OLDiff(AC)}$	Differential input low AC voltage	Note2	-	2 * (V_{REF} -$V_{OL(AC)}$)	V	
$V_{OX(DQS)}$	Differential output cross point relative to V_{DD_DR}/2 for DQS, DQS#	-150	-	150	mV	
$V_{OX(CK)}$	Differential output cross point relative to V_{DD_DR}/2 for CK, CK#	-175	-	175	mV	
DDR3L Differential Output logic level						
$V_{OH(Diff)}$	Differential output high voltage	0.180	-	Note2	V	
$V_{OL(Diff)}$	Differential output low voltage	Note2	-	-0.180	V	
$V_{OHDiff(AC)}$	Differential output high AC voltage	2 * ($V_{OH(AC)}$ - V_{REF})	-	Note2	V	
$V_{OLDiff(AC)}$	Differential input low AC voltage	Note2	-	2 * (V_{REF} -$V_{OL(AC)}$)	V	
$V_{OX(DQS)}$	Differential output cross point relative to V_{DD_DR}/2 for DQS, DQS#	-150	-	150	mV	
$V_{OX(CK)}$	Differential output cross point relative to V_{DD_DR}/2	-150	-	150	mV	

	for CK, CK#					
AC specification						
F_{CLK}	DDR3 Clock Frequency	300	-	600	Mhz	
t_{CH}	clock high pulse width	0.43	-	-	t_{CK}	
t_{CL}	clock low pulse width	0.43	-	-	t_{CK}	
t_{DQSH}	DQS,DQS# differential optput high time	0.45	-	0.55	t_{CK}	
t_{DQSL}	DQS,DQS# differential optput low time	0.45	-	0.55	t_{CK}	
t_{DQSS}	DQS,DQS# rising edge output access time from rising CK,CK#	-0.25		0.25	t_{CK}	
Note	1. Refer to JESD79-3F "Overshoot and Undershoot Specifications" 2. These values are not defined; however, the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to JESD79-3F "Overshoot and Undershoot Specifications"					

5.5. High speed serial interface(MIPI CSI, LVDS, HiSPi)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Input Impedance						
Z_{ID}	Impedance of Differential Terminator	80	100	125	Ohm	(check resistor's accuracy)
LVDS/HiSPi(Sub-LVDS/HiVCM) HS Receiver DC Specifications						
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	600	900	1200	mV	
V_{IDTH}	Differential input high threshold	-	-	70	mV	("Z" : 25mV)
V_{IDTL}	Differential input low threshold	-70	-	-	mV	("Z" : -25mV)
V_{IHHS}	Single-ended input high voltage	-	-	1500	mV	(1200+300)
V_{ILHS}	Single-ended input low voltage	400	-	-	mV	
HiSPi(SLVS) HS Receiver DC Specifications						
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	150	200	250	mV	
V_{IDTH}	Differential input high threshold	-	-	70	mV	("Z" : 25mV)
V_{IDTL}	Differential input low threshold	-70	-	-	mV	("Z" : -25mV)
V_{IHHS}	Single-ended input high voltage	-	-	490	mV	(360+130))
V_{ILHS}	Single-ended input low voltage	-10	-	-	mV	(120-130)
MIPI HS Receiver DC Specifications						
$V_{CMRX(DC)}$	Common-mode voltage	70	-	330	mV	Note 1,2

	HS receive mode					
V_{IDTH}	Differential input high threshold	-	-	70	mV	
V_{IDTL}	Differential input low threshold	-70	-	-	mV	
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	Note 1
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	Note 1
Note	1. Excluding possible additional RF interface of 100mV peak sine wave beyond 450MHz. 2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variation below 450MHz.					
MIPI LP Receiver DC specifications						
V_{IH}	Logic 1 input voltage	880	-	-	mV	
V_{IL}	Logic 0 input voltage, not in ULP State	-	-	500	mV	
V_{HYST}	Input Hysteresis	25	-	-	mV	
General Purpose Input DC specifications						
V_{T+}	Schmitt Trigger Positive Going Threshold	--	-	2.0	V	$V_{DD\_HSI\_IO}$ = 3.3V
V_{T-}	Schmitt Trigger Negative Going Threshold	0.8	-	-	V	$V_{DD\_HSI\_IO}$ = 3.3V
R_{PD}	Pull Down Resistance	-	103K	-	Ohm	$V_{DD\_HSI\_IO}$ = 3.3V
V_{HYST}	Input Hysteresis	0.2	-	-	V	$V_{DD\_HSI\_IO}$ = 3.3V
V_{T+}	Schmitt Trigger Positive Going Threshold	-	-	1.85	V	$V_{DD\_HSI\_IO}$ = 2.8V
V_{T-}	Schmitt Trigger Negative Going Threshold	0.75	-	-	V	$V_{DD\_HSI\_IO}$ = 2.8V
V_{HYST}	Input Hysteresis	0.2	-	-	V	$V_{DD\_HSI\_IO}$ = 2.8V
R_{PD}	Pull Down Resistance	-	136K	-	Ohm	$V_{DD\_HSI\_IO}$ = 2.8V
V_{T+}	Schmitt Trigger Positive Going Threshold	-	-	1.2	V	$V_{DD\_HSI\_IO}$ = 1.8V
V_{T-}	Schmitt Trigger Negative Going Threshold	0.6	-	-	V	$V_{DD\_HSI\_IO}$ = 1.8V
V_{HYST}	Input Hysteresis	0.2	-	-	V	$V_{DD\_HSI\_IO}$ = 1.8V
R_{PD}	Pull Down Resistance	-	218K	-	Ohm	$V_{DD\_HSI\_IO}$ = 1.8V
LVDS/HiSPi Receiver AC Specifications						
F_{CLK}		-	-	750	MHz	
C_{CM}	Common-mode termination	-	10	-	pF	(5pF option)
MIPI HS Receiver AC specifications						
F_{CLK}		40	-	750	MHz	
ΔV_{CMRX_HF}	Common-mode interference beyond 450MHz	-	-	100	mV	Note 2
ΔV_{CMRX_LF}	Common-mode interference	-50	-	50	mV	Note 1,4

	50MHz-450MHz					
C_{CM}	Common-mode termination	-	10	60	pF	Note 3 (5pF option)
Note	1. Excluding 'static' ground shift of 50mV 2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs. 3. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification. 4. Voltage difference compared to DC average common-mode potential.					
MIPI LP Receiver AC specifications						
e_{SPIKE}	Input pulse rejection	-	-	300	V·ps	Note 1,2,4
T_{MIN-RX}	Minimum pulse width response	20	-	-	nS	Note 4
V_{INT}	Peak interference amplitude	-	-	200	mV	
f_{INT}	Interference frequency	450	-	-	MHz	
Note	1. Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state. 2. An impulse less than this will not change the receiver state. 3. In addition to the required glitch rejection, implements shall ensure rejection of known RF-interferences. 4. An input pulse greater than this shall toggle the output.					

5.6. ADC

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
RES	ADC Effective Resolution	-	8	-	Bits	10bits SAR ADC structure ≦125KSPS
V_{IN}	Input signal level	0	-	V_{DD-ADC}	V	
INL	Integral nonlinearity	-2	-	+2	LSB	
DNL	Differential nonlinearity	-1	-	+1	LSB	
C_{IN}	Input capacitance of channel	-	20	-	pF	
$C_{IN-buffer}$	Input capacitance of buffer	-	1	-	pF	

5.7. Audio Codec

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Microphone						
V_{MIC_BIAS}	Mic Bias Output Level	-	2.0	-	V	Setting 0
		-	2.5	-	V	Setting 1
V_{IN}	Input Full Scale Level	-	1.2	-	Vpp	0dB gain
SNR	Signal to Noise Ratio	-	85	-	dBA	0dB gain, A-weighting..
THD+N	Total Harmonic Distortion Plus Noise Ratio	-	-84	-	dBA	0dB gain, A-weighting.
R_{IN}	Input Resistance	-	2.38	-	KΩ	PGA gain set to +25.5 dB
		-	24	-	KΩ	PGA gain set to 0 dB
		-	44.2	-	KΩ	PGA gain set to -21 dB
G_{PGA}	Programable Gain Amplifier Range	-21	-	+25.5	dB	32 steps
G_{STEP}	Programable Gain Amplifier Step Size	-	1.5	-	dB	
G_{Boost}	Boost Gain	-	20	-	dB	0/10/20/30 dB
Headphone or Line Out @16Ω Load						
SNR	Signal to Noise Ratio	-	88	-	dBA	
THD+N	Total Harmonic Distortion Plus Noise Ratio	-	-81	-	dBA	
G_{PGA}	Programable Gain Amplifier Range	-31.6	-	+6	dB	
G_{STEP}	Programable Gain Amplifier Step Size	-	1.2	-	dB	
C_R	Crosstalk Ratio	-	-80	-	dB	
Speaker BTL Output @ 8Ω (Class-AB)						
SNR	Signal to Noise Ratio	-	90	-	dBA	
THD+N	Total Harmonic Distortion Plus Noise Ratio	-	-80	-	dBA	
G_{PGA}	Programable Gain Amplifier Range	-31.6	-	+6	dB	32 steps
G_{STEP}	Programable Gain Amplifier Step Size	-	1.2	-	dB	
P_{SPK}	BTL Speaker Output Power	-	280	-	mW	@THD10%
		-	180	-	mW	@THD1%
Speaker BTL Output @ 8Ω (Class-D)						
SNR	Signal to Noise Ratio	-	70	-	dBA	
THD+N	Total Harmonic Distortion Plus Noise Ratio	-	50	-	dBA	
P_{SPK}	BTL Speaker Output Power	-	400	-	mW	0dBFS input, 0dB gain.

5.8. TV encoder

(R_{LOAD} = 37.5Ω, Conversion rate = 27MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
RES	Video DAC Effective Resolution	-	10	-	bits	10-Bits I-Steering DAC structure
INL	Integral Nonlinearity, INL	-3.5	-	+3.5	LSB	
DNL	Differential Nonlinearity, DNL	-1		+1	LSB	
I_{CODE}	Output Current-DAC Code 1023 (Iout FS)	-	34	-	mA	R_{load} = 37.5 Ohm
V_{CODE}	Out Voltage-DAC Code 1023	-	1.275	-	V	R_{load} = 37.5 Ohm
VLE	Video Level Error	-5	-	+5	%	
V_{OC}	Output Compliance Range	0	-	1.4	V	
F_{CLK}	Conversion rate	-	27	-	MHz	

5.9. MIPI DSI Tx

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
MIPI D-PHY DC specifications						
HS Transmitter						
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV	Note. 1
$\|\Delta V_{CMTX(1,0)}\|$	VCMTX mismatch when output is Differential-1 or Differential-0	-	-	5	mV	Note. 2
$\|V_{OD}\|$	HS transmit differential voltage	140	200	270	mV	Note. 1
$\|\Delta V_{OD}\|$	VOD mismatch when output is Differential-1 or Differential-0	-	-	10	mV	Note. 2
V_{OHHS}	HS output high voltage	-	-	360	mV	Note. 1
Z_{OS}	Single ended output impedance	40	50	62.5	Ω	
ΔZ_{OS}	Single ended output impedance Mismatch	-	-	10	%	
Note	1. Value when driving into load impedance anywhere in the Z_{ID} range. 2. It is recommended the implementer minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation and optimize signal integrity.					
LP Transmitter						
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	VOH
V_{OL}	Thevenin output low level	-50	-	50	mV	VOL
Z_{OLP}	Output impedance of LP transmitter	110	-	-	Ω	Note. 1,2
Note	1. See Figure 42 and Figure 43. in MIPI D-PHY specification.					

	2. Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the T_{RLP}/T_{FLP} specification is met.						
LP Receiver							
V_{IH}	Logic 1 input voltage		880	-	-	mV	
V_{IL}	Logic 0 input voltage, not in ULP State		-	-	500	mV	
V_{IL_ULPS}	Logic 0 input voltage, ULP State		-	-	300	mV	
V_{HYST}	Input Hysteresis		25	-	-	mV	
Note	1. See Figure 42 and Figure 43. in MIPI D-PHY specification. 2. Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the T_{RLP}/T_{FLP} specification is met.						
Contention Detector (LP-CD)							
V_{IHCD}	Logic 1 contention threshold		450	-	-	mV	
V_{ILCD}	Logic 0 contention threshold		-	-	200	mV	
MIPI D-PHY AC specifications							
HS Transmitter							
$\Delta V_{CMTX(HF)}$	Common-level variations above 450MHz		-	-	15	mV RMS	
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450MHz		-	-	25	mV PEAK	
t_{R} and t_{F}	20%-80% rise time and fall time		-	-	0.3	UI	Note. 1
			150	-	-	ps	
Note	1. UI is equal to 1/(2*fh). See section 7.3 for the definition of fh						
LP Transmitter							
T_{RLP}/T_{FLP}	15%-85% rise time and fall time		-	-	25	ns	Note. 1
T_{REOT}	30%-85% rise time and fall time		-	-	35	ns	Note. 1, 5, 6
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	-	-	ns	Note. 4
		ALL other pulses	20	-	-	ns	Note 4
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock		90	-	-	ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF		-	-	500	mV/ns	Note 1, 3, 7, 8
	Slew rate @ CLOAD = 5pF		-	-	300	mV/ns	Note 1, 3, 7, 8

	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	Note 1, 3, 7, 8
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	Note 1, 3, 7, 8
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	Note 1, 2, 3
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	Note 1, 3, 9
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST – 700)	-	-	mV/ns	Note. 1, 10, 11
C_{LOAD}	Load capacitance	0	-	70	pF	Note 1
Note	1. C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. 2. When the output voltage is between 400 mV and 930 mV. 3. Measured as average across any 50 mV segment of the output signal transition. 4. This parameter value can be lower than T_{LPX} due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in section 8.2.2. 5. The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive. 6. With an additional load capacitance CCM between 0 and 60pF on the termination center tap at RX side of the Lane 7. This value represents a corner point in a piecewise linear curve. See Figure 45 and Figure 46. 8. When the output voltage is in the range specified by V_{PIN}(absmax). 9. When the output voltage is between 400 mV and 700 mV. 10. Where $V_{O,INST}$ is the instantaneous output voltage, V_{DP} or V_{DN}, in millivolts. 11. When the output voltage is between 700 mV and 930 mV.					
LP Receiver						
e_{SPIKE}	Input pulse rejection	-	-	300	V·ps	Note 1,2,3
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns	Note 4
V_{INT}	Peak interference amplitude	-	-	200	mV	
f_{INT}	Interference frequency	450	-	-	MHz	
Note	1. Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state. 2. An impulse less than this will not change the receiver state. 3. In addition to the required glitch rejection, implements shall ensure rejection of known RF-interferences. 4. An input pulse greater than this shall toggle the output.					

Pin Characteristic Specifications						
V_{PIN}	Pin signal voltage range	-50	-	1350	mV	
I_{LEAK}	Pin leakage current	-10	-	10	uA	
V_{GNDSH}	Ground shift	-50	-	50	mV	
V_{PIN} (absmax)	Transient pin voltage level	-0.15	-	1.45	V	
T_{VPIN} (absmax)	Maximum transient time above VPIN(max) or below VPIN(min)	-	-	20	ns	
Note	1. When the pad voltage is in the signal voltage range from V_{GNDSH},MIN to VOH + V_{GNDSH}, MAX and the Lane Module is in LP receive mode. 2. The voltage overshoot and undershoot beyond the V_{PIN} is only allowed during a single 20ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range. 3. This value includes ground shift.					

Figure. D-PHY signaling level

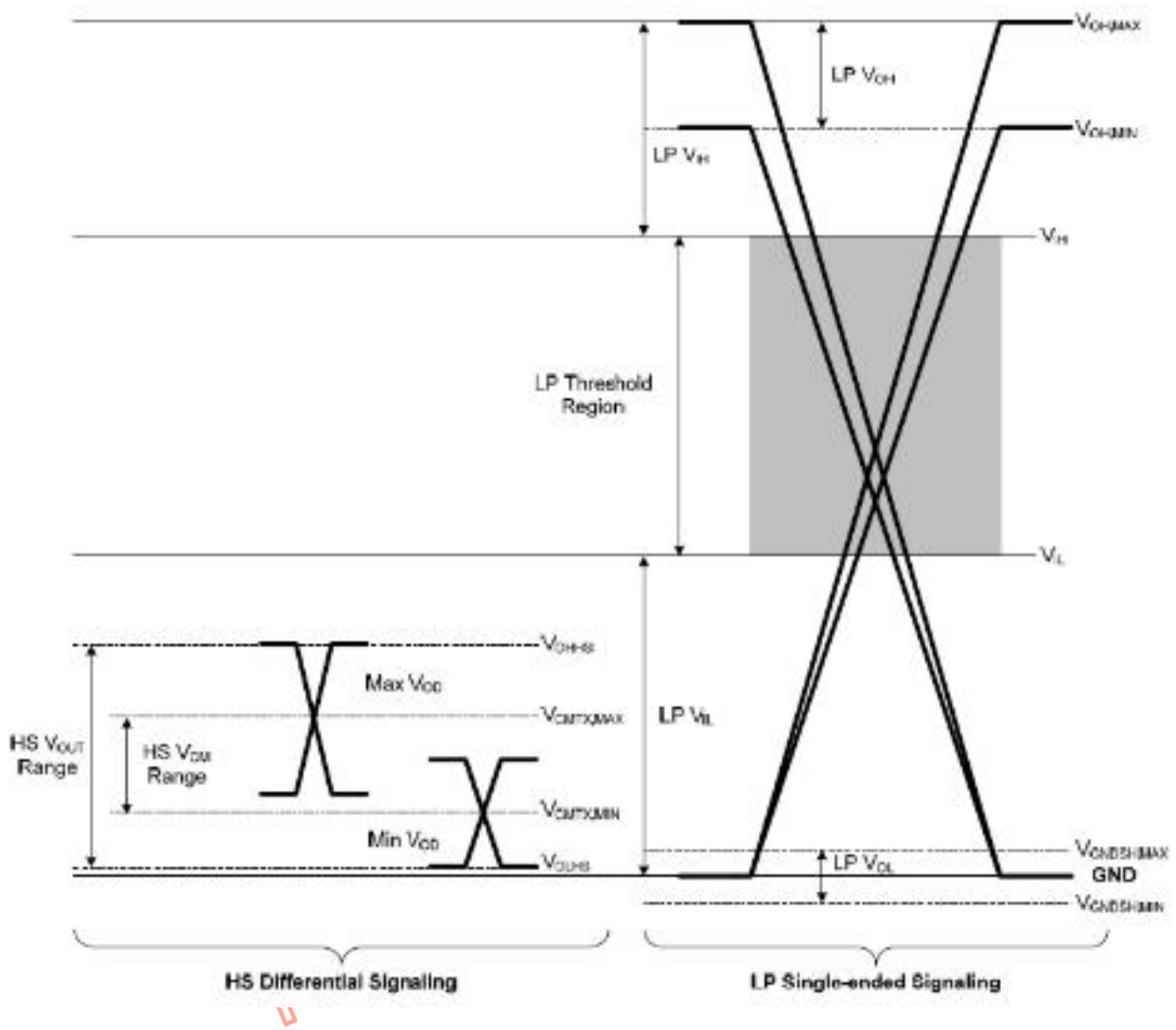
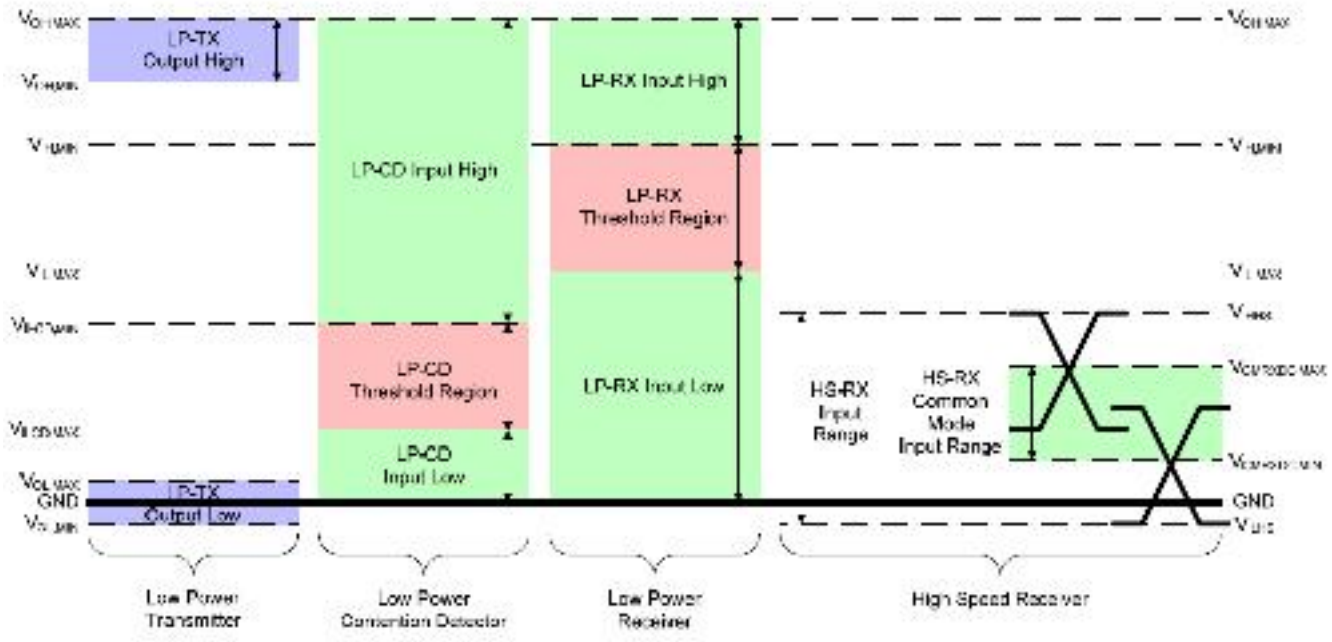


Figure. Signaling and contention Voltage levels



5.10. HDMI Tx

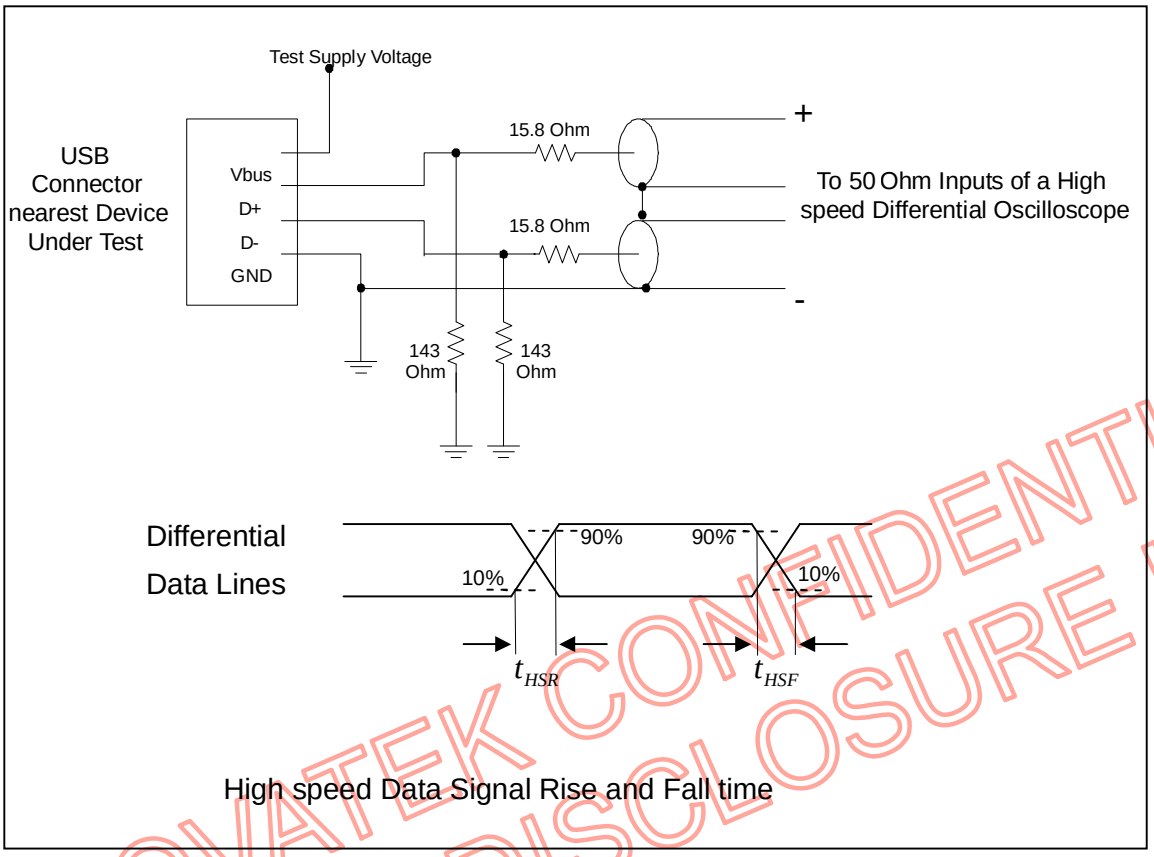
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Transmitter DC Specifications						
V_{OFF}	Single-ended standby output voltage	AV_{CC} -10		AV_{CC} +10	mV	AV_{CC}: Termination Supply Voltage
V_{SWING}	Single-ended output swing voltage	400	500	600	mV	
V_L	Single-ended low level output voltage	2.7	-	2.9	V	
Transmitter AC Specifications						
t_R / t_F	Rise/fall time	75	-	-	ps	
T_{Skew_inter}	Inter-Pair Skew at source connector	-	-	0.20	$T_{char.}$	
T_{Skew_intra}	Intra-Pair Skew at source connector	-	-	0.15	T_{bit}	
Duty	Clock duty cycle	40	50	60	%	
T_{cj}	TMDS Differential Clock Jitter	-	-	0.25	T_{bit}	
Hot Plug Detection Signal						
V_{IH}	Input High Voltage (HDMI_PLUG)	2.0	-	-	V	Max 5.3V
V_{IL}	Input Low Voltage (HDMI_PLUG)	-	-	0.8	V	

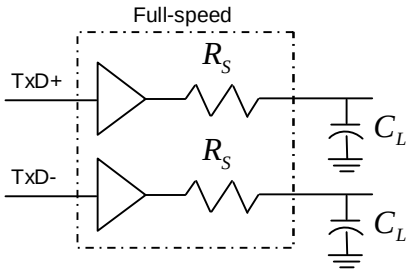
5.11. USB

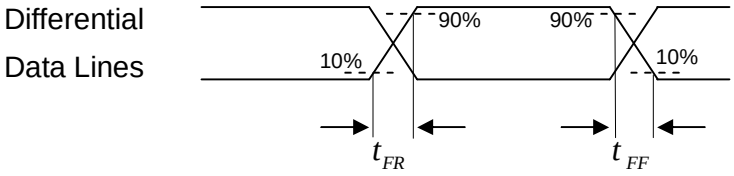
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
High Speed DC Specifications						
Input Levels (differential receiver)						
V_{HSDIFF}	High speed differential input sensitivity	300	-	-	mV	$\|V_{I(DP)}-V_{I(DM)}\|$ measured at the connection as application circuit
V_{HSCM}	High speed data signaling common mode voltage range	-50	-	500	mV	
V_{HSSQ}	High speed squelch detection threshold	-	-	100	mV	squelch detected
		150	-	-	mV	no squelch detected
V_{HSDSC}	High speed disconnection detection threshold	625	-	-	mV	disconnection detected
		-	-	525	mV	disconnection not detected
Output Levels						
V_{HSOI}	High speed idle level output voltage (differential)	-10	-	10	mV	
V_{HSOL}	High speed low level output voltage (differential)	-10	-	10	mV	
V_{HSOH}	High speed high level output voltage (differential)	-360	-	400	mV	
V_{CHRPJ}	Chirp-J output voltage (differential)	700	-	1100	mV	
V_{CHIRPK}	Chirp-K output voltage (differential)	-900	-	-500	mV	
Resistance						
R_{DRV}	Driver output impedance	3	6	9	Ω	equivalent resistance used as internal chip only
		40.5	45	49.5	Ω	overall resistance including external resistor
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU	3.0	-	3.6	V	
Full Speed DC Specifications						
Input Levels (differential receiver)						
V_{DI}	Differential input sensitivity	0.2	-	-	V	$\|V_{I(DP)}-V_{I(DM)}\|$
V_{CM}	Differential common mode voltage	0.8	-	2.5	V	
Input Levels (single-ended receivers)						
V_{SE}	Single ended receiver threshold	0.8	-	2.0	V	
Output Levels						
V_{OL}	Low-level output voltage	0	-	0.3	V	

V_{OH}	High-level output voltage	2.8	-	3.6	V	
High Speed AC Specifications						
Driver Characteristics						
$T_{HSDRATE}$	High speed TX data rate	479.76	-	480.24	Mbps	
$T_{HSRDRATE}$	High speed RX data rate	479.76	-	480.24	Mbps	
t_{HSR}	High speed differential rise time	500	-	-	ps	
t_{HSF}	High speed differential fall time	500	-	-	ps	
Driving timing						
	Driver waveform requirement	see eye pattern of template 1				Follow template1 described in USB2.0 spec
Receiver timing						
	Data source jitter and receiver jitter tolerance	see eye pattern of template 4				Follow template 4 described in USB2.0 spec
Full Speed AC Specifications						
Driver Characteristics						
$T_{FSDRATE}$	Full speed TX data rate	11.994	-	12.006	Mbps	
$T_{FSRDRATE}$	Full speed RX data rate	11.97	-	12.03	Mbps	
t_{FR}	Rise time	4	-	20	ns	CL=50pF; 10 to 90% of $\|V_{OH}-V_{OL}\|$
t_{FF}	Fall time	4	-	20	ns	CL=50pF; 90 to 10% of $\|V_{OH}-V_{OL}\|$
t_{FRMA}	Differential rise/fall time matching (t_{FR}/t_{FF})	90	-	110	%	Excluding the first transition from idle mode
V_{CRS}	Output signal crossover voltage	1.3	-	2.0	V	Excluding the first transition from idle mode
Driving timing						
	VI, FSE0, OE to DP, DN propagation delay	-	-	15	ns	for detailed description of VI, FSE0 and OE, please refer to USB1.1 spec
T_{FDEOP}	Source jitter for differential transition to SE0 transition	-2	-	5	ns	
T_{JR1}	Receiver jitter	-18.5	-	18.5	ns	To next transition
T_{JR2}	Receiver jitter	-9	-	9	ns	For paired transition
T_{FEOPT}	Source SE0 interval of EOP	160	-	175	ns	
T_{FEOPR}	Receiver SE0 interval of EOP	82	-	-	ns	
T_{FST}	Width of SE0 interval during differential transition	-	-	14	ns	
Receiver timing						
$t_{PLH(RCV)}$ $t_{PHL(RCV)}$	Receiver propagation delay (DP; DM to RCV)	-	-	15	ns	for detailed description of RCV, please refer to USB1.1 spec
$t_{PLH(single)}$ $t_{PHL(single)}$	Receiver propagation delay (DP; DM to VOP,	-	-	15	ns	

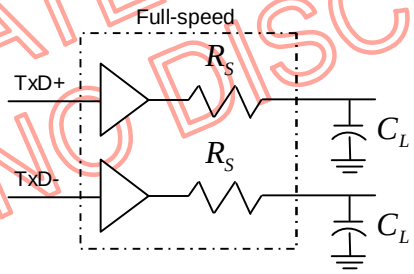
	VON)					

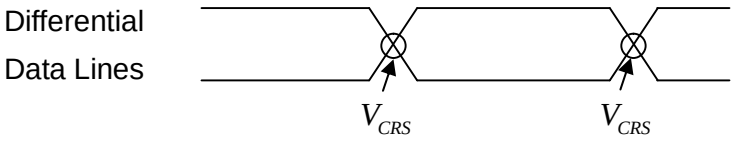






Full speed Data Signal Rise and Fall time





Full speed Output Signal Crossover Voltage

5.12. USB Charging Port Detect

USB charging port detect						
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DAT_REF}	Data Detect Voltage	0.25	-	0.4	V	
V_{DM_SRC}	D- Source Voltage	0.5	-	0.7	V	
V_{DP_SRC}	D+ Source Voltage	0.5	-	0.7	V	
V_{LGC}	Logic Threshold	0.8	-	2.0	V	
V_{LGC_HI}	Logic High	2.0	-	3.6	V	
V_{LGC_LOW}	Logic Low	0	-	0.8	V	
I_{DM_SINK}	D- Sink Current	25	-	175	uA	
I_{DP_SINK}	D+ Sink Current	25	-	175	uA	
I_{DP_SRC}	Data Contact Detect Current Source	7	-	13	uA	
R_{DM_DWN}	D- Pull-down resistance	14.25	-	24.8	kΩ	

5.13. Vx1

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
HS Receiver Specification						
V_{RTH}	CML Differential Input High Threshold	-	-	50	mV	
V_{RTL}	CML Differential Input Low Threshold	-50	-	-	mV	
V_{RCT}	CML Common mode Bias Voltage	-	0	-	V	
R_{RIN}	CML Differential Input Resistance	80	100	120	Ohm	
t_{RISK_INTRA}	Allowable Inter-pair Skew	-	0.3	-	UI	
Sub_Link Specifications						
OBUF Default SPEC						
R_{TERM}	Termination Resistance	37.5	50	62.5	Ohm	PHY_OEX=L, Default Setting at TX Mode
		150	200	250	Ohm	PHY_OEX=H, Default Setting at RX Mode
I_{DRIVE}	Drive Current	4	12	16	mA	Default Setting at TX Mode
V_{BIC}	Bi-Directional Buffer Input Terminated Common Voltage	1.55	1.65	1.85	mV	
ΔV_{BIC}	Undesirable change of Bi-Directional Buffer Input Terminated Voltages	-	-	20	mV	AC chatacteristics should be taken care
V_{BOD}	Bi-Directional Buffer Differential Output Voltage	640	1920	2560	mV	VBOD = 2 * IDRIVE * (RXerm // TXterm)
V_{BOC}	Bi-Directional Buffer Common Output Voltage	1.55	1.65	1.85	mV	
OBUF Optional SPEC						
R_{TERM}	Termination Resistance	-	50	-	Ohm	TERM[4:0] PHY_OEX=L

						=5'b10100	
		-	100	-	Ohm	TERM[4:0] =5'b01011	PHY_OEX=H
		-	50	-	Ohm	TERM[4:0] =5'b10100	PHY_OEX=L Default settings at TX Mode
		-	200	-	Ohm	TERM[4:0] =5'b00101	PHY_OEX=H Default settings at RX Mode
		-	50	-	Ohm	TERM[4:0]	PHY_OEX=L
		-	50	-	Ohm	=5'b10100	PHY_OEX=H
		-	75	-	Ohm	TERM[4:0]	PHY_OEX=L
		-	75	-	Ohm	=5'b01111	PHY_OEX=H
I_{DRIVE}	Drive Current	-	16	-	mA	DRIVE[1:0]=2'b11	
		-	12	-	mA	DRIVE[1:0]=2'b10 Default settings at TX Mode	
		-	8	-	mA	DRIVE[1:0]=2'b01	
		-	4	-	mA	DRIVE[1:0]=2'b00	
IBUF Default SPEC							
V_{BTH}	Bi-Directional Buffer Differential Input High Threshold	-	-	50	mV	HYS = 3'b000	
V_{BTL}	Bi-Directional Buffer Differential Input Low Threshold	-50	-	-	mV	HYS = 3'b000	
V_{HYS}	Differential Hysteresis voltage	50	-	-	mV	HYS = 3'b000	
IBUF Optional SPEC							
V_{BTH}	Bi-Directional Buffer Differential Input High Threshold	-	-	175	mV	HYS = 3'b001	
V_{BTL}	Bi-Directional Buffer Differential Input Low Threshold	-175	-	-	mV	HYS = 3'b001	
V_{HYS}	Differential Hysteresis voltage	175	-	-	mV	HYS = 3'b001	
AC Characteristics							
t_{BRF}	tR, tF of differential output(20-80%)	150	-	1000	ps	See Fig B.1	
t_{BPJTX}	Bi-Directional Buffer Transmitter Period Jitter Accuracy	-	-	1	ns	See Fig B.2	
t_{BPRX}	Bi-Directional Buffer Receiver Period Jitter Tolerance(peak to peak)	8	-	-	ns	See Fig B.2	
TX/RX mode (Common) Timing							
f_{OSC}	Frequency of Oscillator	70	80	90	MHz		

	used as CLK_I on Sub-Link					
t_{OSC}	Period of Oscillator	-	$1/f_{OSC}$	-	us	
t_{BUI}	Unit Interval of Manchester Codes	-	$16*t_{OSC}$	-	us	
TX mode Timing						
t_{RDY_Tx}	Set-up time for transmitting data from the time when PHY_OEX becoming H from L	-	-	$2*t_{OSC}$	us	
tPWL_DIN_E	Delay time to make PHY_OEX H from the time when valid data finishes.	-	-	$4*t_{OSC}$	us	
RX mode Timing						
t_{PUP_RX}	Set-up time for receiving data from time when PDX becoming H form L	-	-	150	us	
t_{RDY_RX}	Set-up time for receiving data from the time when PHY_OEX becoming H from L	-	-	$3*t_{OSC}$	us	
ΔV_{PUP_RX}	Difference between CMLP and CMLN, during set-up time	-	-	+/-20	mV	

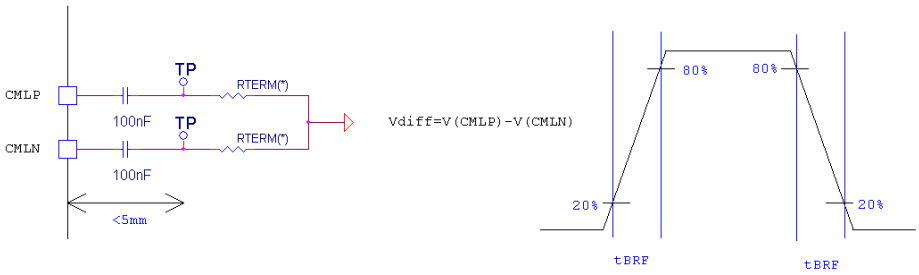
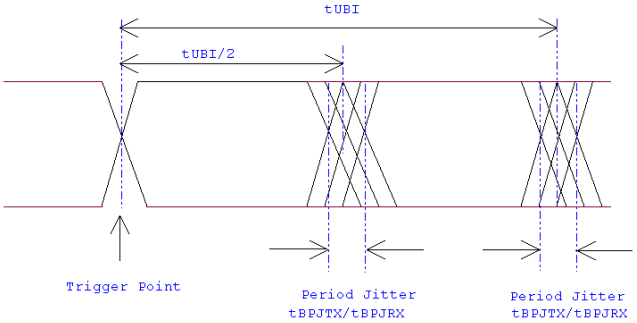


Fig B.1 Bi-directional CML Test Circuit for TX Mode and Switching Timing Diagram

(*)RTERM is set as the same valus as RDIFF/2 ; 200 ohm



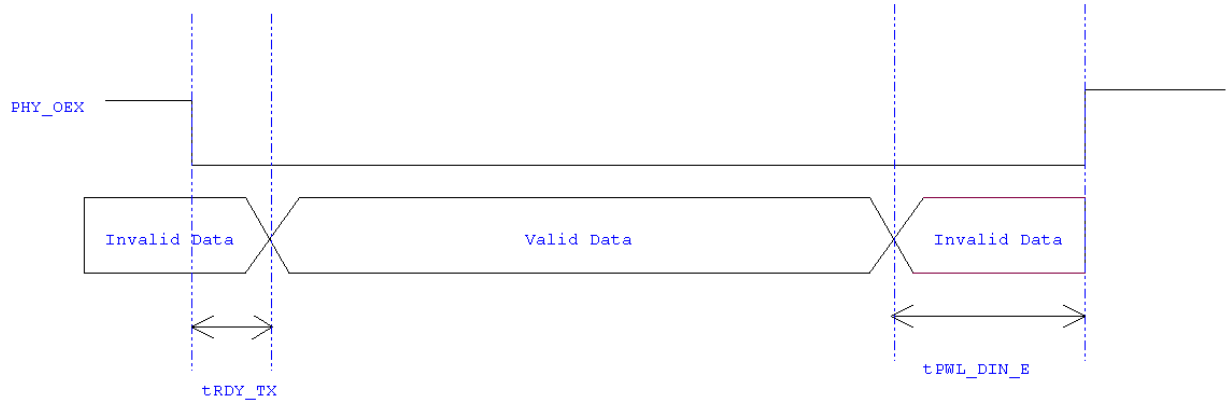


Fig B.3 Timing chart of PHY_OEX and PHY_DINP

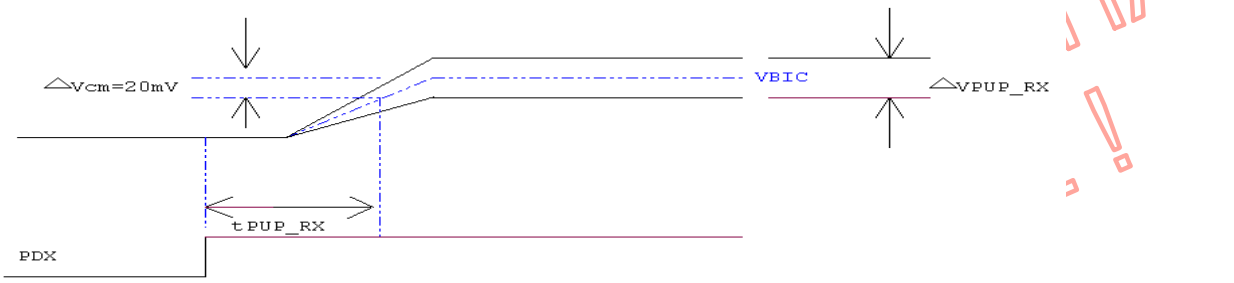


Fig B.4 Timing chart of tPUP_RX

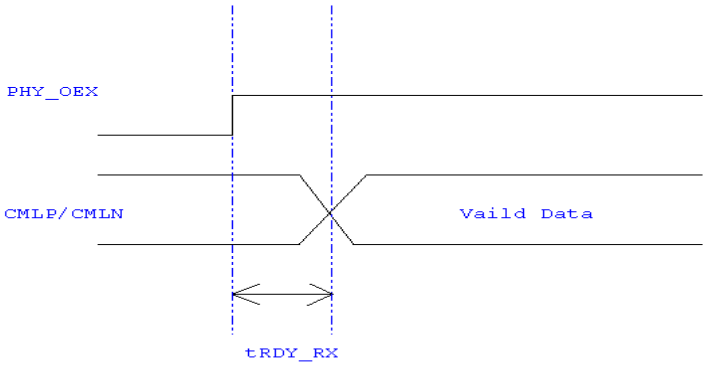


Fig B.5 Timing chart of tRDY_RX

Ordering Information