

# 1 MHz, Low-Power Op Amp

### Features

- Available in SC-70-5 and SOT-23-5 packages
- Gain Bandwidth Product: 1 MHz (typical)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8V to 6.0V
- Supply Current: I<sub>Q</sub> = 100 μA (typical)
- Phase Margin: 90° (typical)
- Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C
- · Available in Single, Dual and Quad Packages

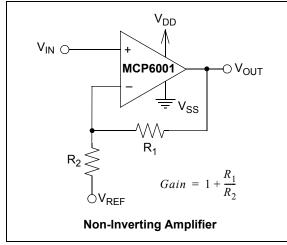
# Applications

- Automotive
- Portable Equipment
- · Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

### **Design Aids**

- · SPICE Macro Models
- FilterLab<sup>®</sup> Software
- Mindi™ Circuit Designer & Simulator
- Microchip Advanced Part Selector (MAPS)
- · Analog Demonstration and Evaluation Boards
- Application Notes

# **Typical Application**

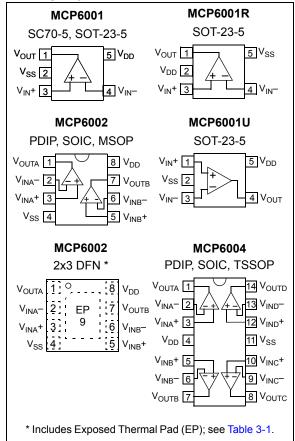


## Description

The Microchip Technology Inc. MCP6001/2/4 family of operational amplifiers (op amps) is specifically designed for general-purpose applications. This family has a 1 MHz Gain Bandwidth Product (GBWP) and 90° phase margin (typical). It also maintains 45° phase margin (typical) with a 500 pF capacitive load. This family operates from a single supply voltage as low as 1.8V, while drawing 100  $\mu$ A (typical) quiescent current. Additionally, the MCP6001/2/4 supports rail-to-rail input and output swing, with a Common-mode input voltage range of V<sub>DD</sub> + 300 mV to V<sub>SS</sub> – 300 mV. This family of op amps is designed with Microchip's advanced CMOS process.

The MCP6001/2/4 family is available in the industrial and extended temperature ranges, with a power supply range of 1.8V to 6.0V.

## Package Types



NOTES:

# 1.0 ELECTRICAL CHARACTERISTICS

# Absolute Maximum Ratings †

| V <sub>DD</sub> – V <sub>SS</sub>  |
|--|
| Current at Analog Input Pins (V <sub>IN</sub> +, V <sub>IN</sub> -)±2 mA   |
| Analog Inputs (V <sub>IN</sub> +, V <sub>IN</sub> -) $\uparrow\uparrow$ V <sub>SS</sub> – 1.0V to V <sub>DD</sub> + 1.0V |
| All Other Inputs and Outputs $V_{SS}$ – 0.3V to $V_{DD}$ + 0.3V  |
| Difference Input Voltage $ V_{DD} - V_{SS} $   |
| Output Short Circuit CurrentContinuous   |
| Current at Output and Supply Pins±30 mA  |
| Storage Temperature65°C to +150°C  |
| Maximum Junction Temperature (T <sub>J</sub> )+150°C   |
| ESD Protection On All Pins (HBM; MM) $\geq$ 4 kV; 200V   |

**†** Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**††** See Section 4.1.2 "Input Voltage and Current Limits".

# DC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics**: Unless otherwise indicated,  $T_A = +25^{\circ}C$ ,  $V_{DD} = +1.8V$  to +5.5V,  $V_{SS} = GND$ ,  $V_{CM} = V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10 \text{ k}\Omega \text{ to } V_L$ , and  $V_{OUT} \approx V_{DD}/2$  (refer to Figure 1-1).

| Parameters                          | Sym                               | Min                  | Тур                  | Max                   | Units | Conditions  |
|-------------------------------------|-----------------------------------|----------------------|----------------------|-----------------------|-------|---|
| Input Offset                        | •                                 | •                    |                      | •                     |       | ·   |
| Input Offset Voltage                | V <sub>OS</sub>                   | -4.5                 | _                    | +4.5                  | mV    | V <sub>CM</sub> = V <sub>SS</sub> (Note 1)                      |
| Input Offset Drift with Temperature | $\Delta V_{OS} / \Delta T_A$      | —                    | ±2.0                 | —                     | µV/°C | $T_A$ = -40°C to +125°C,<br>V <sub>CM</sub> = V <sub>SS</sub>   |
| Power Supply Rejection Ratio        | PSRR                              | _                    | 86                   | _                     | dB    | $V_{CM} = V_{SS}$   |
| Input Bias Current and Impedance    |                                   | •                    |                      |                       |       | ·   |
| Input Bias Current:                 | Ι <sub>Β</sub>                    | _                    | ±1.0                 | _                     | pА    |   |
| Industrial Temperature              | Ι <sub>Β</sub>                    | _                    | 19                   | _                     | pА    | T <sub>A</sub> = +85°C  |
| Extended Temperature                | Ι <sub>Β</sub>                    | _                    | 1100                 | _                     | pА    | T <sub>A</sub> = +125°C   |
| Input Offset Current                | I <sub>OS</sub>                   | _                    | ±1.0                 | _                     | pА    |   |
| Common-mode Input Impedance         | Z <sub>CM</sub>                   | _                    | 10 <sup>13</sup>   6 | _                     | Ω  pF |   |
| Differential Input Impedance        | Z <sub>DIFF</sub>                 | _                    | 10 <sup>13</sup>   3 | _                     | Ω  pF |   |
| Common-mode                         |                                   | •                    |                      |                       |       |   |
| Common-mode Input Range             | V <sub>CMR</sub>                  | $V_{SS} - 0.3$       | _                    | V <sub>DD</sub> + 0.3 | V     |   |
| Common-mode Rejection Ratio         | CMRR                              | 60                   | 76                   | —                     | dB    | $V_{CM}$ = -0.3V to 5.3V,<br>$V_{DD}$ = 5V                      |
| Open-Loop Gain                      | •                                 |                      |                      |                       |       | •   |
| DC Open-Loop Gain (Large Signal)    | A <sub>OL</sub>                   | 88                   | 112                  | —                     | dB    | $V_{OUT}$ = 0.3V to $V_{DD}$ – 0.3V,<br>$V_{CM}$ = $V_{SS}$     |
| Output                              | -                                 |                      |                      |                       |       |   |
| Maximum Output Voltage Swing        | V <sub>OL</sub> , V <sub>OH</sub> | V <sub>SS</sub> + 25 | —                    | V <sub>DD</sub> – 25  | mV    | V <sub>DD</sub> = 5.5V,<br>0.5V Input Overdrive                 |
| Output Short Circuit Current        | I <sub>SC</sub>                   | _                    | ±6                   | _                     | mA    | V <sub>DD</sub> = 1.8V  |
|                                     |                                   | —                    | ±23                  | —                     | mA    | V <sub>DD</sub> = 5.5V  |
| Power Supply                        |                                   |                      |                      |                       |       |   |
| Supply Voltage                      | V <sub>DD</sub>                   | 1.8                  | _                    | 6.0                   | V     | Note 2  |
| Quiescent Current per Amplifier     | ا <sub>م</sub>                    | 50                   | 100                  | 170                   | μA    | I <sub>O</sub> = 0, V <sub>DD</sub> = 5.5V, V <sub>CM</sub> = 5 |

Note 1: MCP6001/1R/1U/2/4 parts with date codes prior to December 2004 (week code 49) were tested to ±7 mV minimum/maximum limits.

2: All parts with date codes November 2007 and later have been screened to ensure operation at

 $V_{DD}$  = 6.0V. However, the other minimum and maximum specifications are measured at 1.8V and 5.5V.

# **AC ELECTRICAL SPECIFICATIONS**

Thermal Resistance, 5L-SC70

Thermal Resistance, 8L-PDIP

Thermal Resistance, 8L-MSOP

Thermal Resistance, 14L-PDIP

Thermal Resistance, 14L-SOIC

Thermal Resistance, 14L-TSSOP

Thermal Resistance, 8L-DFN (2x3)

Thermal Resistance, 5L-SOT-23

Thermal Resistance, 8L-SOIC (150 mil)

| Electrical Characteristics: Unless other $V_L = V_{DD}/2$ , $V_{OUT} \approx V_{DD}/2$ , $R_L = 10$ ks |                  |                       |          |           | .5V, V <sub>SS</sub> = | GND, $V_{CM} = V_{DD}/2$ |
|--|------------------|-----------------------|----------|-----------|------------------------|--------------------------|
| Parameters   | Sym              | Min                   | Тур      | Max       | Units                  | Conditions               |
| AC Response  |                  |                       |          |           |                        |                          |
| Gain Bandwidth Product   | GBWP             |                       | 1.0      | _         | MHz                    |                          |
| Phase Margin   | PM               |                       | 90       |           | 0                      | G = +1 V/V               |
| Slew Rate  | SR               | _                     | 0.6      | _         | V/µs                   |                          |
| Noise  | •                |                       | · •      |           |                        |                          |
| Input Noise Voltage  | E <sub>ni</sub>  | _                     | 6.1      | _         | µVp-p                  | f = 0.1 Hz to 10 Hz      |
| Input Noise Voltage Density  | e <sub>ni</sub>  | _                     | 28       | _         | nV/√Hz                 | f = 1 kHz                |
| Input Noise Current Density  | i <sub>ni</sub>  | _                     | 0.6      | _         | fA/√Hz                 | f = 1 kHz                |
| TEMPERATURE SPECIFICA  |                  |                       |          |           |                        |                          |
| Electrical Characteristics: Unless of  | therwise indicat | ed, V <sub>DD</sub> = | +1.8V to | +5.5V and | I V <sub>SS</sub> = GN | ID.                      |
| Parameters   | Sym              | Min                   | Тур      | Max       | Units                  | Conditions               |
| Temperature Ranges   |                  |                       |          |           |                        |                          |
| Industrial Temperature Range   | T <sub>A</sub>   | -40                   |          | +85       | °C                     |                          |
| Extended Temperature Range   | T <sub>A</sub>   | -40                   | —        | +125      | °C                     |                          |
| Operating Temperature Range  | T <sub>A</sub>   | -40                   |          | +125      | °C                     | Note                     |
| Storage Temperature Range  | T <sub>A</sub>   | -65                   |          | +150      | °C                     |                          |
| Thermal Package Resistances  | •                |                       | •        | •         |                        | •                        |

 $\theta_{\mathsf{JA}}$ The industrial temperature devices operate over this extended temperature range, but with reduced Note: performance. In any case, the internal Junction Temperature (T<sub>1</sub>) must not exceed the Absolute Maximum specification of +150°C.

\_

\_\_\_\_

\_\_\_\_

\_\_\_\_

\_\_\_\_

 $\theta_{\text{JA}}$ 

 $\theta_{\text{JA}}$ 

 $\theta_{\mathsf{JA}}$ 

 $\theta_{\mathsf{JA}}$ 

 $\theta_{\text{JA}}$ 

 $\theta_{\text{JA}}$ 

 $\theta_{\text{JA}}$ 

 $\theta_{\mathsf{JA}}$ 

331

256

85

163

206

68

70

120

100

\_\_\_\_

\_\_\_

\_

\_\_\_\_

\_

°C/W

°C/W

°C/W

°C/W

°C/W

°C/W

°C/W

°C/W

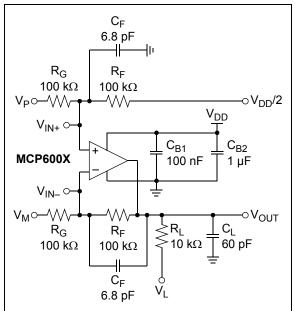
°C/W

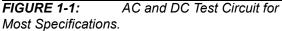
# 1.1 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set V<sub>CM</sub> and V<sub>OUT</sub>; see Equation 1-1. Note that V<sub>CM</sub> is not the circuit's Common-mode voltage ((V<sub>P</sub> + V<sub>M</sub>)/2), and that V<sub>OST</sub> includes V<sub>OS</sub> plus the effects (on the input offset error, V<sub>OST</sub>) of temperature, CMRR, PSRR and A<sub>OL</sub>.

### **EQUATION 1-1:**

$$\begin{split} G_{DM} &= R_F / R_G \\ V_{CM} &= (V_P + V_{DD} / 2) / 2 \\ V_{OST} &= V_{IN-} - V_{IN+} \\ V_{OUT} &= (V_{DD} / 2) + (V_P - V_M) + V_{OST} (1 + G_{DM}) \\ \end{split}$$
Where: 
$$\begin{split} G_{DM} &= \text{Differential Mode Gain} \qquad (V/V) \\ V_{CM} &= \text{Op Amp's Common-mode} \qquad (V) \\ \text{Input Voltage} \\ V_{OST} &= \text{Op Amp's Total Input Offset} \qquad (mV) \\ \text{Voltage} \end{split}$$





NOTES:

#### 2.0 TYPICAL PERFORMANCE CURVES

The graphs and tables provided following this note are a statistical summary based on a limited number of Note: samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T<sub>A</sub> = +25°C, V<sub>DD</sub> = +1.8V to +5.5V, V<sub>SS</sub> = GND, V<sub>CM</sub> = V<sub>DD</sub>/2, V<sub>OUT</sub>  $\approx$  V<sub>DD</sub>/2,  $V_L = V_{DD}/2$ ,  $R_L = 10 \text{ k}\Omega$  to  $V_L$ , and  $C_L = 60 \text{ pF}$ .

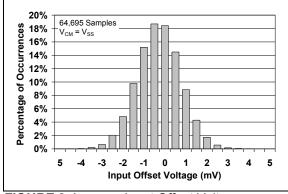
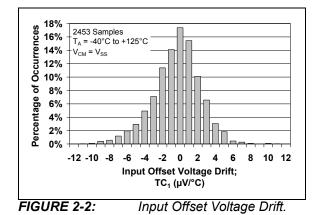


FIGURE 2-1:

Input Offset Voltage.



s 45% 2453 Samples T<sub>A</sub> = -40°C to +125°C urren 35% V<sub>CM</sub> = V<sub>SS</sub> 30% 0 25% ቴ 20% Percentage 10% 5% 0% \_\_\_\_ -0.02 0.0 0.0 0.02 0.03 0.04 0.05 0.06 0.0 0.0 Input Offset Quadratic Temp. Co.;  $TC_2 (\mu V/°C^2)$ FIGURE 2-3: Input Offset Quadratic Temp. Co.

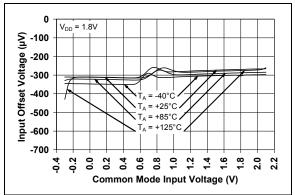


FIGURE 2-4: Input Offset Voltage vs. Common-mode Input Voltage at  $V_{DD}$  = 1.8V.

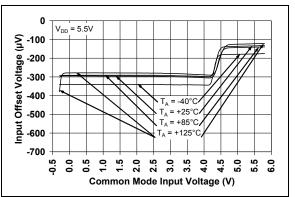
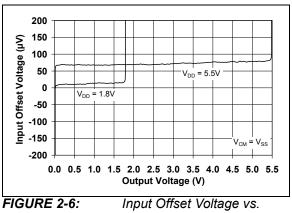
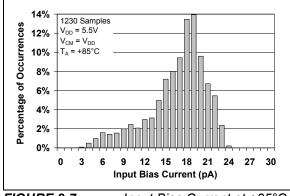


FIGURE 2-5: Input Offset Voltage vs. Common-mode Input Voltage at  $V_{DD}$  = 5.5V.

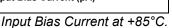


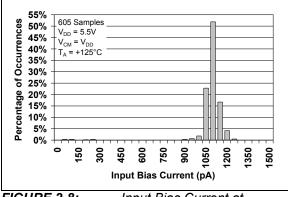
Output Voltage.

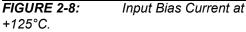
Note: Unless otherwise indicated, T<sub>A</sub> = +25°C, V<sub>DD</sub> = +1.8V to +5.5V, V<sub>SS</sub> = GND, V<sub>CM</sub> = V<sub>DD</sub>/2, V<sub>OUT</sub>  $\approx$  V<sub>DD</sub>/2,  $V_L = V_{DD}/2$ ,  $R_L = 10 \text{ k}\Omega$  to  $V_L$ , and  $C_L = 60 \text{ pF}$ .











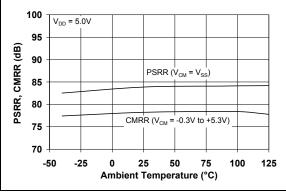
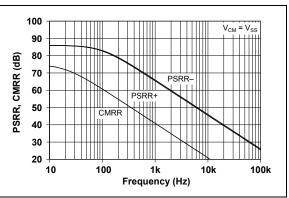


FIGURE 2-9: CMRR, PSRR vs. Ambient Temperature.



**FIGURE 2-10:** Frequency.

PSRR, CMRR vs.

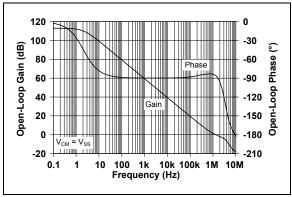
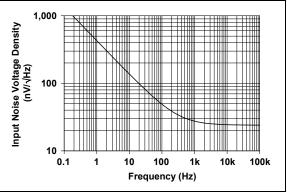
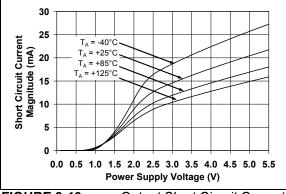


FIGURE 2-11: Open-Loop Gain, Phase vs. Frequency.



**FIGURE 2-12:** Input Noise Voltage Density vs. Frequency.

**Note:** Unless otherwise indicated,  $T_A = +25^{\circ}C$ ,  $V_{DD} = +1.8V$  to +5.5V,  $V_{SS} = GND$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10 \text{ k}\Omega$  to  $V_L$ , and  $C_L = 60 \text{ pF}$ .



**FIGURE 2-13:** Output Short Circuit Current vs. Power Supply Voltage.

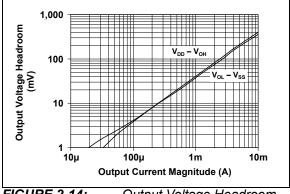
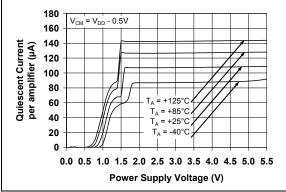
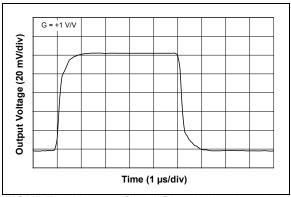


FIGURE 2-14: Output Voltage Headroom vs. Output Current Magnitude.



**FIGURE 2-15:** Quiescent Current vs. Power Supply Voltage.



*FIGURE 2-16:* Small-Signal, Non-Inverting Pulse Response.

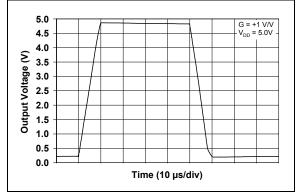


FIGURE 2-17: Large-Signal, Non-Inverting Pulse Response.

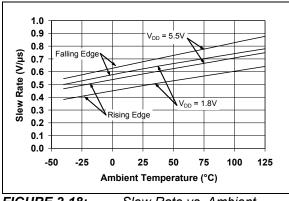


FIGURE 2-18: Temperature.

Slew Rate vs. Ambient

**Note:** Unless otherwise indicated,  $T_A = +25^{\circ}C$ ,  $V_{DD} = +1.8V$  to +5.5V,  $V_{SS} = GND$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10 \text{ k}\Omega$  to  $V_L$ , and  $C_L = 60 \text{ pF}$ .

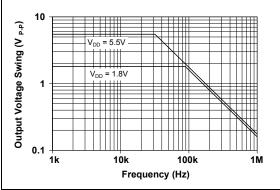
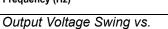
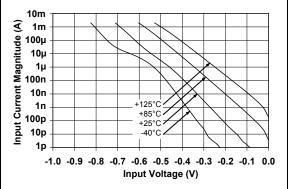


FIGURE 2-19: Frequency.



Oulput Voltage Swill



**FIGURE 2-20:** Measured Input Current vs. Input Voltage (below V<sub>SS</sub>).

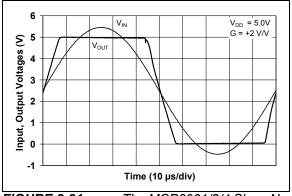


FIGURE 2-21: The MCP6001/2/4 Show No Phase Reversal.

# 3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

| MCP6001             | MCP6001R | MCP6001U | MCP6                   | 002        | MCP6004                 |                                       |  |
|---------------------|----------|----------|------------------------|------------|-------------------------|---------------------------------------|--|
| SC70-5,<br>SOT-23-5 | SOT-23-5 | SOT-23-5 | MSOP,<br>PDIP,<br>SOIC | DFN<br>2x3 | PDIP,<br>SOIC,<br>TSSOP | Symbol                                | Description  |
| 1                   | 1        | 4        | 1                      | 1          | 1                       | V <sub>OUT</sub> , V <sub>OUTA</sub>  | Analog Output (op amp A)                               |
| 4                   | 4        | 3        | 2                      | 2          | 2                       | V <sub>IN</sub> -, V <sub>INA</sub> - | Inverting Input (op amp A)                             |
| 3                   | 3        | 1        | 3                      | 3          | 3                       | V <sub>IN</sub> +, V <sub>INA</sub> + | Non-inverting Input (op amp A)                         |
| 5                   | 2        | 5        | 8                      | 8          | 4                       | V <sub>DD</sub>                       | Positive Power Supply                                  |
| —                   | —        | —        | 5                      | 5          | 5                       | V <sub>INB</sub> +                    | Non-inverting Input (op amp B)                         |
| —                   | —        | —        | 6                      | 6          | 6                       | V <sub>INB</sub> –                    | Inverting Input (op amp B)                             |
| _                   | _        | —        | 7                      | 7          | 7                       | V <sub>OUTB</sub>                     | Analog Output (op amp B)                               |
| —                   | —        | —        | _                      | _          | 8                       | V <sub>OUTC</sub>                     | Analog Output (op amp C)                               |
| —                   | —        | —        | —                      | _          | 9                       | V <sub>INC</sub> -                    | Inverting Input (op amp C)                             |
| —                   | —        | —        | —                      | —          | 10                      | V <sub>INC</sub> +                    | Non-inverting Input (op amp C)                         |
| 2                   | 5        | 2        | 4                      | 4          | 11                      | V <sub>SS</sub>                       | Negative Power Supply                                  |
| —                   | —        | —        | _                      | _          | 12                      | V <sub>IND</sub> +                    | Non-inverting Input (op amp D)                         |
| —                   |          | —        |                        | _          | 13                      | V <sub>IND</sub> -                    | Inverting Input (op amp D)                             |
| _                   | _        |          |                        |            | 14                      | V <sub>OUTD</sub>                     | Analog Output (op amp D)                               |
| —                   | —        | —        | —                      | 9          | —                       | EP                                    | Exposed Thermal Pad (EP);<br>must be connected to VSS. |

# TABLE 3-1: PIN FUNCTION TABLE

# 3.1 Analog Outputs

The output pins are low-impedance voltage sources.

# 3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

# 3.3 Power Supply Pins

The positive power supply (V<sub>DD</sub>) is 1.8V to 6.0V higher than the negative power supply (V<sub>SS</sub>). For normal operation, the other pins are at voltages between V<sub>SS</sub> and V<sub>DD</sub>.

Typically, these parts are used in a single (positive) supply configuration. In this case,  $V_{SS}$  is connected to ground and  $V_{DD}$  is connected to the supply.  $V_{DD}$  will need bypass capacitors.

# 3.4 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the  $V_{SS}$  pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

NOTES:

# 4.0 APPLICATION INFORMATION

The MCP6001/2/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-cost, low-power and general-purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6001/2/4 ideal for battery-powered applications. This device has high phase margin, which makes it stable for larger capacitive load applications.

## 4.1 Rail-to-Rail Inputs

### 4.1.1 PHASE REVERSAL

The MCP6001/1R/1U/2/4 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-21 shows the input voltage exceeding the supply voltage without any phase reversal.

### 4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current ( $I_B$ ). The input ESD diodes clamp the inputs when they try to go more than one diode drop below  $V_{SS}$ . They also clamp any voltages that go too far above  $V_{DD}$ ; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

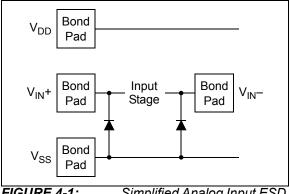
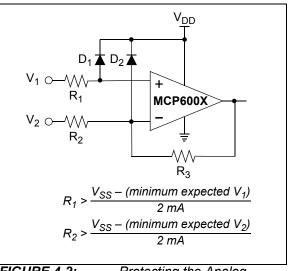


FIGURE 4-1: Simplified Analog Input ESD Structures.

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the V<sub>IN</sub>+ and V<sub>IN</sub>- pins (see **Absolute Maximum Ratings †** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V<sub>IN</sub>+ and V<sub>IN</sub>-) from going too far below ground, and the resistors R<sub>1</sub> and R<sub>2</sub> limit the possible current drawn out of the input pins. Diodes D<sub>1</sub> and D<sub>2</sub> prevent the input pins (V<sub>IN</sub>+ and V<sub>IN</sub>-) from going too far above

 $V_{DD}$ , and dump any currents onto  $V_{DD}$ . When implemented as shown, resistors  $R_1$  and  $R_2$  also limit the current through  $D_1$  and  $D_2$ .



# FIGURE 4-2: Protecting the Analog Inputs.

It is also possible to connect the diodes to the left of resistors R<sub>1</sub> and R<sub>2</sub>. In this case, current through the diodes D<sub>1</sub> and D<sub>2</sub> needs to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V<sub>IN</sub><sup>+</sup> and V<sub>IN</sub><sup>-</sup>) should be very small.

A significant amount of current can flow out of the inputs when the Common-mode voltage ( $V_{CM}$ ) is below ground ( $V_{SS}$ ); see Figure 2-20. Applications that are high impedance may need to limit the usable voltage range.

# 4.1.3 NORMAL OPERATION

The input stage of the MCP6001/1R/1U/2/4 op amps use two differential CMOS input stages in parallel. One operates at low Common-mode input voltage (V<sub>CM</sub>), while the other operates at high V<sub>CM</sub>. With this topology, the device operates with V<sub>CM</sub> up to 0.3V above V<sub>DD</sub> and 0.3V below V<sub>SS</sub>.

The transition between the two input stages occurs when  $V_{CM} = V_{DD} - 1.1V$ . For the best distortion and gain linearity, with non-inverting gains, avoid this region of operation.

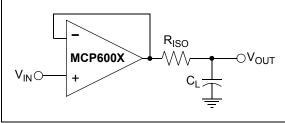
# 4.2 Rail-to-Rail Output

The output voltage range of the MCP6001/2/4 op amps is  $V_{DD} - 25 \text{ mV}$  (minimum) and  $V_{SS} + 25 \text{ mV}$  (maximum) when  $R_L = 10 \text{ k}\Omega$  is connected to  $V_{DD}/2$  and  $V_{DD} = 5.5$ V. Refer to Figure 2-14 for more information.

# 4.3 Capacitive Loads

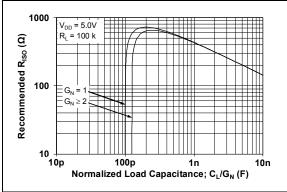
Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1), a small series resistor at the output ( $R_{ISO}$  in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.



**FIGURE 4-3:** Output resistor, R<sub>ISO</sub> stabilizes large capacitive loads.

Figure 4-4 gives recommended  $R_{ISO}$  values for different capacitive loads and gains. The x-axis is the normalized load capacitance ( $C_L/G_N$ ), where  $G_N$  is the circuit's noise gain. For non-inverting gains,  $G_N$  and the Signal Gain are equal. For inverting gains,  $G_N$  is 1+|Signal Gain| (e.g., -1 V/V gives  $G_N = +2$  V/V).



**FIGURE 4-4:** Recommended R<sub>ISO</sub> values for Capacitive Loads.

After selecting  $R_{ISO}$  for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify  $R_{ISO}$ 's value until the response is reasonable. Bench evaluation and simulations with the MCP6001/1R/1U/2/4 SPICE macro model are very helpful.

# 4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (V<sub>DD</sub> for single-supply) should have a local bypass capacitor (i.e., 0.01  $\mu$ F to 0.1  $\mu$ F) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1  $\mu$ F or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

# 4.5 Unused Op Amps

An unused op amp in a quad package (MCP6004) should be configured as shown in Figure 4-5. These circuits prevent the output from toggling and causing crosstalk. Circuits A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

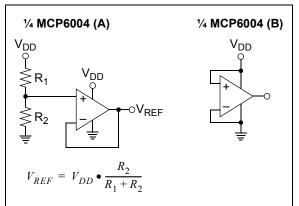


FIGURE 4-5: Unused Op Amps.

# 4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is  $10^{12}\Omega$ . A 5V difference would cause 5 pA of current to flow; which is greater than the MCP6001/1R/1U/2/4 family's bias current at 25°C (typically 1 pA).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-6.

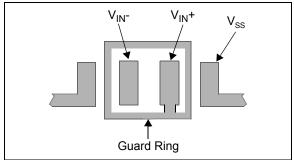


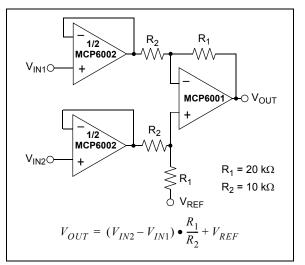
FIGURE 4-6: Example Guard Ring Layout for Inverting Gain.

- 1. Non-inverting Gain and Unity-Gain Buffer:
  - a.Connect the non-inverting pin (V<sub>IN</sub>+) to the input with a wire that does not touch the PCB surface.
  - b.Connect the guard ring to the inverting input pin (V\_{IN}-). This biases the guard ring to the Common-mode input voltage.
- 2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
  - a.Connect the guard ring to the non-inverting input pin ( $V_{IN}$ +). This biases the guard ring to the same reference voltage as the op amp (e.g.,  $V_{DD}$ /2 or ground).
  - b.Connect the inverting pin (V<sub>IN</sub>-) to the input with a wire that does not touch the PCB surface.

# 4.7 Application Circuits

### 4.7.1 UNITY-GAIN BUFFER

The rail-to-rail input and output capability of the MCP6001/2/4 op amp is ideal for unity-gain buffer applications. The low quiescent current and wide bandwidth makes the device suitable for a buffer configuration in an instrumentation amplifier circuit, as shown in Figure 4-7.



**FIGURE 4-7:** Instrumentation Amplifier with Unity-Gain Buffer Inputs.

### 4.7.2 ACTIVE LOW-PASS FILTER

The MCP6001/2/4 op amp's low input bias current makes it possible for the designer to use larger resistors and smaller capacitors for active low-pass filter applications. However, as the resistance increases, the noise generated also increases. Parasitic capacitances and the large value resistors could also modify the frequency response. These trade-offs need to be considered when selecting circuit elements.

Usually, the op amp bandwidth is 100x the filter cutoff frequency (or higher) for good performance. It is possible to have the op amp bandwidth 10X higher than the cutoff frequency, thus having a design that is more sensitive to component tolerances.

Figure 4-8 shows a second-order Butterworth filter with 100 kHz cutoff frequency and a gain of +1 V/V; the op amp bandwidth is only 10x higher than the cutoff frequency. The component values were selected using Microchip's FilterLab<sup>®</sup> software.

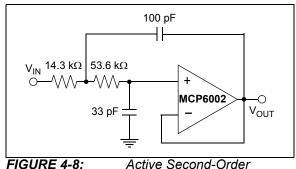


FIGURE 4-8: Active S Low-Pass Filter.

# 4.7.3 PEAK DETECTOR

The MCP6001/2/4 op amp has a high input impedance, rail-to-rail input/output and low input bias current, which makes this device suitable for peak detector applications. Figure 4-9 shows a peak detector circuit with clear and sample switches. The peak-detection cycle uses a clock (CLK), as shown in Figure 4-9.

At the rising edge of CLK, Sample Switch closes to begin sampling. The peak voltage stored on C<sub>1</sub> is sampled to C<sub>2</sub> for a sample time defined by t<sub>SAMP</sub>. At the end of the sample time (falling edge of Sample Signal), Clear Signal goes high and closes the Clear Switch. When the Clear Switch closes, C<sub>1</sub> discharges through R<sub>1</sub> for a time defined by t<sub>CLEAR</sub>. At the end of the clear time (falling edge of Clear Signal), op amp A begins to store the peak value of V<sub>IN</sub> on C<sub>1</sub> for a time defined by t<sub>DETECT</sub>.

In order to define  $t_{SAMP}$  and  $t_{CLEAR}$ , it is necessary to determine the capacitor charging and discharging period. The capacitor charging time is limited by the amplifier source current, while the discharging time ( $\tau$ ) is defined using  $R_1$  ( $\tau = R_1C_1$ ).  $t_{DETECT}$  is the time that the input signal is sampled on  $C_1$  and is dependent on the input voltage change frequency.

The op amp output current limit, and the size of the storage capacitors (both C<sub>1</sub> and C<sub>2</sub>), could create slewing limitations as the input voltage (V<sub>IN</sub>) increases. Current through a capacitor is dependent on the size of the capacitor and the rate of voltage change. From this relationship, the rate of voltage change or the slew rate can be determined. For example, with an op amp short circuit current of I<sub>SC</sub> = 25 mA and a load capacitor of C<sub>1</sub> = 0.1  $\mu$ F, then:

### **EQUATION 4-1:**

$$I_{SC} = C_1 \frac{dV_{C1}}{dt}$$
$$\frac{dV_{C1}}{dt} = \frac{I_{SC}}{C_1}$$
$$= \frac{25mA}{0.1\,\mu F}$$
$$\frac{dV_{C1}}{dt} = 250mV/\mu s$$

This voltage rate of change is less than the MCP6001/2/4 slew rate of 0.6 V/ $\mu$ s. When the input voltage swings below the voltage across C<sub>1</sub>, D<sub>1</sub> becomes reverse-biased. This opens the feedback loop and rails the amplifier. When the input voltage increases, the amplifier recovers at its slew rate. Based on the rate of voltage change shown in the above equation, it takes an extended period of time to charge a 0.1  $\mu$ F capacitor. The capacitors need to be selected so that the circuit is not limited by the amplifier slew rate. Therefore, the capacitors should be less than 40  $\mu$ F and a stabilizing resistor (R<sub>ISO</sub>) needs to be properly selected. (Refer to **Section 4.3 "Capacitive Loads"**).

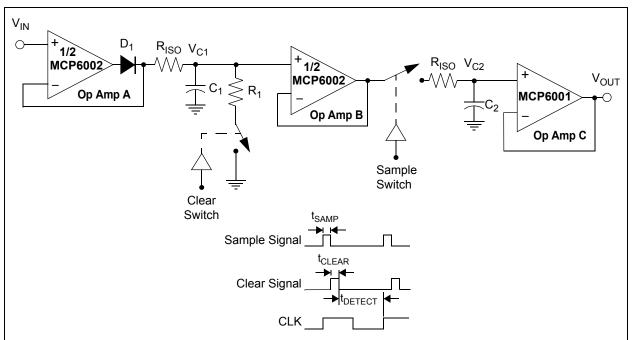


FIGURE 4-9: Peak Detector with Clear and Sample CMOS Analog Switches.

# 5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6001/1R/1U/2/4 family of op amps.

# 5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6001/1R/1U/2/4 op amps is available on the Microchip web site at www.microchip.com. The model was written and tested in official Orcad (Cadence) owned PSPICE. For the other simulators, it may require translation.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current, and resistance of the op amp, but it also covers the temperature and noise effects on the behavior of the op amp. The model has not been verified outside of the specification range listed in the op amp data sheet. The model behaviors under these conditions can not be guaranteed that it will match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

# 5.2 FilterLab<sup>®</sup> Software

Microchip's FilterLab<sup>®</sup> software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

# 5.3 Mindi™ Circuit Designer & Simulator

Microchip's Mindi<sup>™</sup> Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online circuit designer & simulator available from the Microchip web site at www.microchip.com/mindi. This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

# 5.4 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/ maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase, and Sampling of Microchip parts.

# 5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
- 14-Pin SOIC/TSSOP/DIP Evaluation Board, P/N SOIC14EV

# 5.6 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip web site at www.microchip. com/appnotes and are recommended as supplemental reference resources.

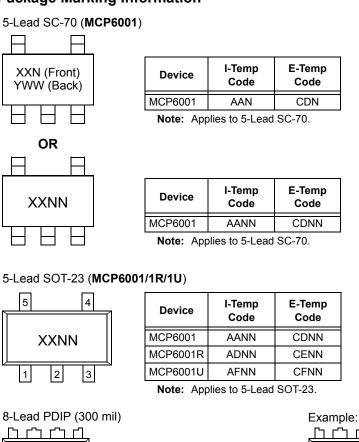
- ADN003: "Select the Right Operational Amplifier for your Filtering Circuits," DS21821
- AN722: "Operational Amplifier Topologies and DC Specifications," DS00722
- AN723: "Operational Amplifier AC Specifications and Applications," DS00723
- AN884: "Driving Capacitive Loads With Op Amps," DS00884
- AN990: "Analog Sensor Conditioning Circuits An Overview," DS00990
- AN1177: "Op Amp Precision Design: DC Errors," DS01177
- AN1228: "Op Amp Precision Design: Random Noise," DS01228
- AN1297: "Microchip 's Op Amp SPICE Macro Models"

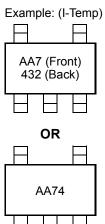
These application notes and others are listed in the design guide:

• "Signal Chain Design Guide," DS21825

#### 6.0 PACKAGING INFORMATION

#### 6.1 **Package Marking Information**





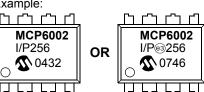
Example: (E-Temp)

|   | 5 |      | 4 | _ |
|---|---|------|---|---|
|   |   | CD25 |   | Í |
| - | 1 | 2    | 3 |   |



8-Lead DFN (2 x 3)

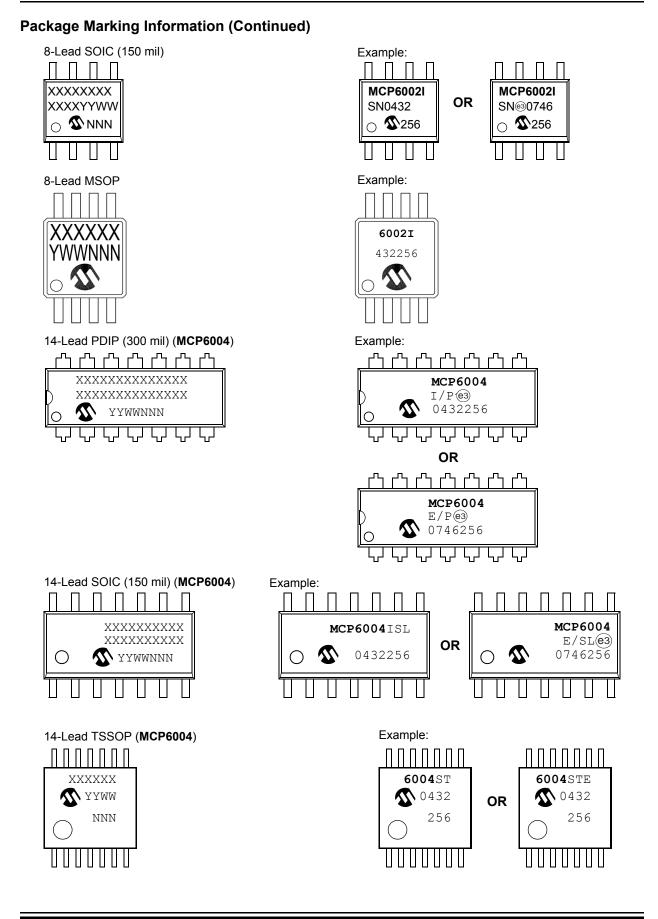
| XXX<br>YWW<br>NN |   |     |
|------------------|---|-----|
| NN               |   | XXX |
|                  |   | YWW |
|                  | 0 | NN  |



Example:

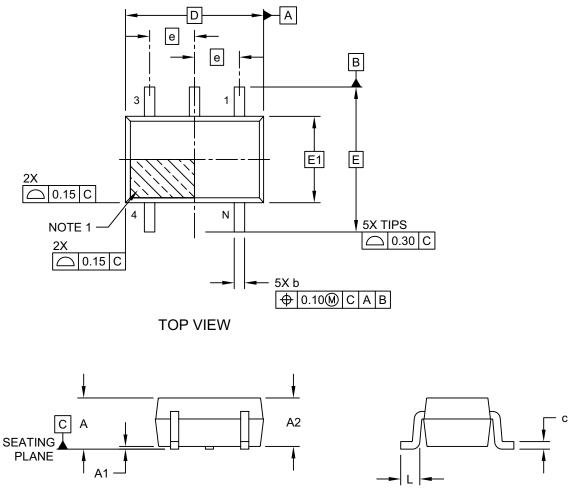
|   |     | _ |
|---|-----|---|
|   |     |   |
|   | ABY |   |
|   | 944 |   |
| _ | 25  |   |
| S |     |   |

Customer-specific information Legend: XX...X Year code (last digit of calendar year) Y YY Year code (last 2 digits of calendar year) WW Week code (week of January 1 is week '01') NNN Alphanumeric traceability code (e3) Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.



# 5-Lead Plastic Small Outline Transistor (LT) [SC70]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



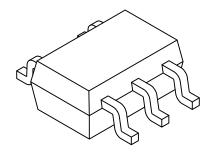
SIDE VIEW

END VIEW

Microchip Technology Drawing C04-061D Sheet 1 of 2

# 5-Lead Plastic Small Outline Transistor (LT) [SC70]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



|                          | MILLIMETERS |      |          |      |
|--------------------------|-------------|------|----------|------|
| Dimension                | Limits      | MIN  | NOM      | MAX  |
| Number of Pins           | N           |      | 5        |      |
| Pitch                    | е           |      | 0.65 BSC |      |
| Overall Height           | A           | 0.80 | -        | 1.10 |
| Standoff                 | A1          | 0.00 | -        | 0.10 |
| Molded Package Thickness | A2          | 0.80 | -        | 1.00 |
| Overall Length           | D           |      | 2.00 BSC |      |
| Exposed Pad Length       | D2          | 2.50 | 2.60     | 2.70 |
| Overall Width            | E           |      | 2.10 BSC |      |
| Exposed Pad Width        | E1          |      | 1.25 BSC |      |
| Terminal Width           | b           | 0.15 | -        | 0.40 |
| Terminal Length          | L           | 0.10 | 0.20     | 0.46 |
| Lead Thickness           | С           | 0.08 | -        | 0.26 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

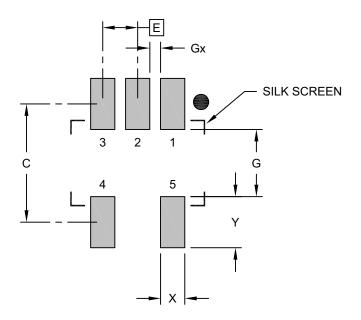
- 2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or
- protrusions shall not exceed 0.15mm per side. 3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-061D Sheet 2 of 2

# 5-Lead Plastic Small Outline Transistor (LT) [SC70]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



### RECOMMENDED LAND PATTERN

|                       | Units       | 1    | MILLIMETER | S    |
|-----------------------|-------------|------|------------|------|
| Dimen                 | sion Limits | MIN  | NOM        | MAX  |
| Contact Pitch         | E           |      | 0.65 BSC   |      |
| Contact Pad Spacing   | С           |      | 2.20       |      |
| Contact Pad Width     | Х           |      |            | 0.45 |
| Contact Pad Length    | Y           |      |            | 0.95 |
| Distance Between Pads | G           | 1.25 |            |      |
| Distance Between Pads | Gx          | 0.20 |            |      |

Notes:

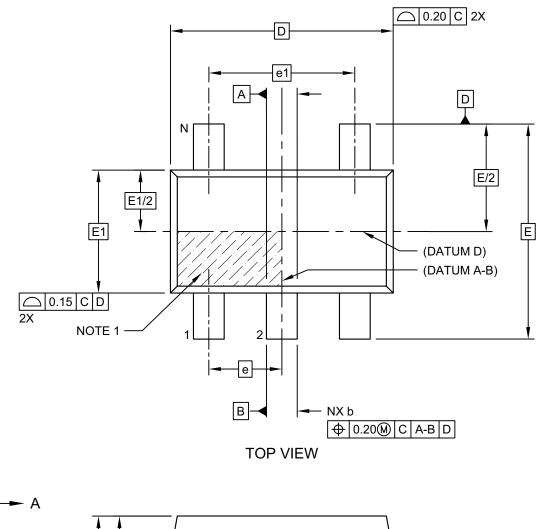
1. Dimensioning and tolerancing per ASME Y14.5M

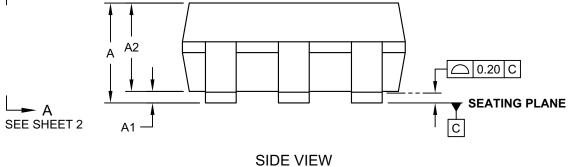
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061B

# 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

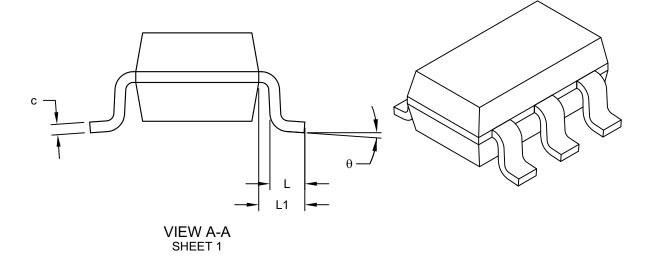




Microchip Technology Drawing C04-091-OT Rev E Sheet 1 of 2

# 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



|                          | Units | MILLIMETERS |          |      |  |
|--------------------------|-------|-------------|----------|------|--|
| Dimension Limits         |       | MIN         | NOM      | MAX  |  |
| Number of Pins           | Ν     |             | 5        |      |  |
| Pitch                    | е     |             | 0.95 BSC |      |  |
| Outside lead pitch       | e1    |             | 1.90 BSC |      |  |
| Overall Height           | Α     | 0.90        | -        | 1.45 |  |
| Molded Package Thickness | A2    | 0.89        | -        | 1.30 |  |
| Standoff                 | A1    | -           | -        | 0.15 |  |
| Overall Width            | E     |             | 2.80 BSC |      |  |
| Molded Package Width     | E1    |             | 1.60 BSC |      |  |
| Overall Length           | D     |             | 2.90 BSC |      |  |
| Foot Length              | L     | 0.30        | -        | 0.60 |  |
| Footprint                | L1    |             | 0.60 REF |      |  |
| Foot Angle               | ¢     | 0°          | -        | 10°  |  |
| Lead Thickness           | С     | 0.08        | -        | 0.26 |  |
| Lead Width               | b     | 0.20        | -        | 0.51 |  |

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

2. Dimensioning and tolerancing per ASME Y14.5M

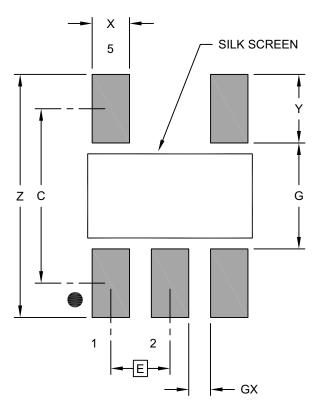
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev E Sheet 2 of 2

# 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



# RECOMMENDED LAND PATTERN

|                         | Units  |      |          | S    |
|-------------------------|--------|------|----------|------|
| Dimension               | Limits | MIN  | NOM      | MAX  |
| Contact Pitch           | E      |      | 0.95 BSC |      |
| Contact Pad Spacing     | С      |      | 2.80     |      |
| Contact Pad Width (X5)  | Х      |      |          | 0.60 |
| Contact Pad Length (X5) | Y      |      |          | 1.10 |
| Distance Between Pads   | G      | 1.70 |          |      |
| Distance Between Pads   | GX     | 0.35 |          |      |
| Overall Width           | Z      |      |          | 3.90 |

Notes:

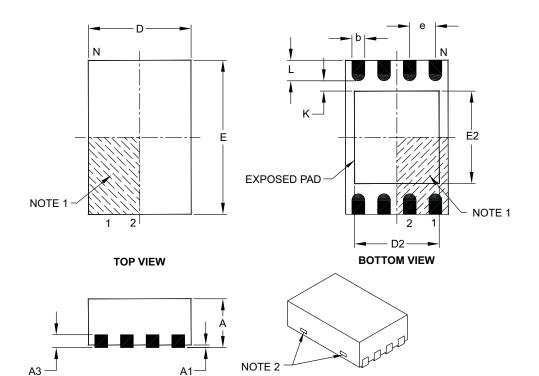
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091B [OT]

# 8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



|                        | Units            | MILLIMETERS |          |      |
|------------------------|------------------|-------------|----------|------|
|                        | Dimension Limits | MIN         | NOM      | MAX  |
| Number of Pins         | N                |             | 8        |      |
| Pitch                  | e                |             | 0.50 BSC |      |
| Overall Height         | A                | 0.80        | 0.90     | 1.00 |
| Standoff               | A1               | 0.00        | 0.02     | 0.05 |
| Contact Thickness      | A3               |             | 0.20 REF |      |
| Overall Length         | D                | 2.00 BSC    |          |      |
| Overall Width          | E                |             | 3.00 BSC |      |
| Exposed Pad Length     | D2               | 1.30        | _        | 1.55 |
| Exposed Pad Width      | E2               | 1.50        | -        | 1.75 |
| Contact Width          | b                | 0.20        | 0.25     | 0.30 |
| Contact Length         | L                | 0.30        | 0.40     | 0.50 |
| Contact-to-Exposed Pad | K                | 0.20        | _        | -    |

#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

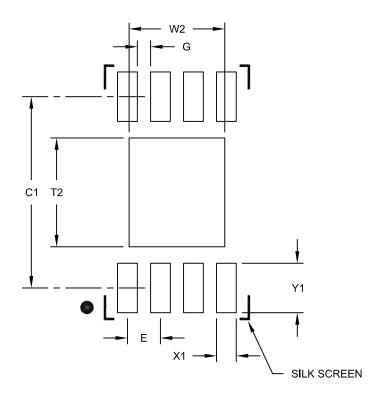
- 2. Package may have one or more exposed tie bars at ends.
- 3. Package is saw singulated.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



# RECOMMENDED LAND PATTERN

| Units                      |    | MILLIMETERS |     |      |  |
|----------------------------|----|-------------|-----|------|--|
| Dimension Limits           |    | MIN         | NOM | MAX  |  |
| Contact Pitch              | E  | 0.50 BSC    |     |      |  |
| Optional Center Pad Width  | W2 |             |     | 1.45 |  |
| Optional Center Pad Length | T2 |             |     | 1.75 |  |
| Contact Pad Spacing        | C1 | 2.90        |     |      |  |
| Contact Pad Width (X8)     | X1 |             |     | 0.30 |  |
| Contact Pad Length (X8)    | Y1 |             |     | 0.75 |  |
| Distance Between Pads      | G  | 0.20        |     |      |  |

### Notes:

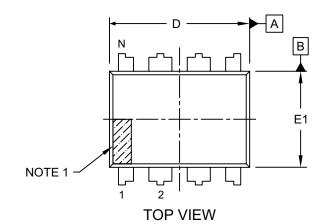
1. Dimensioning and tolerancing per ASME Y14.5M

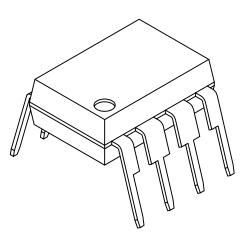
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

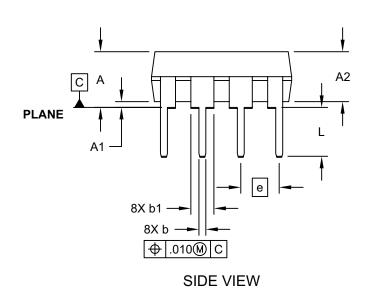
Microchip Technology Drawing No. C04-2123B

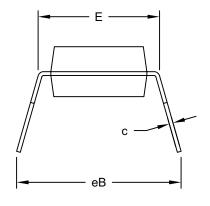
# 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







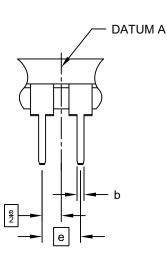


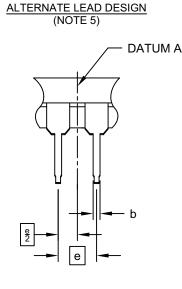


Microchip Technology Drawing No. C04-018-P Rev E Sheet 1 of 2

# 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





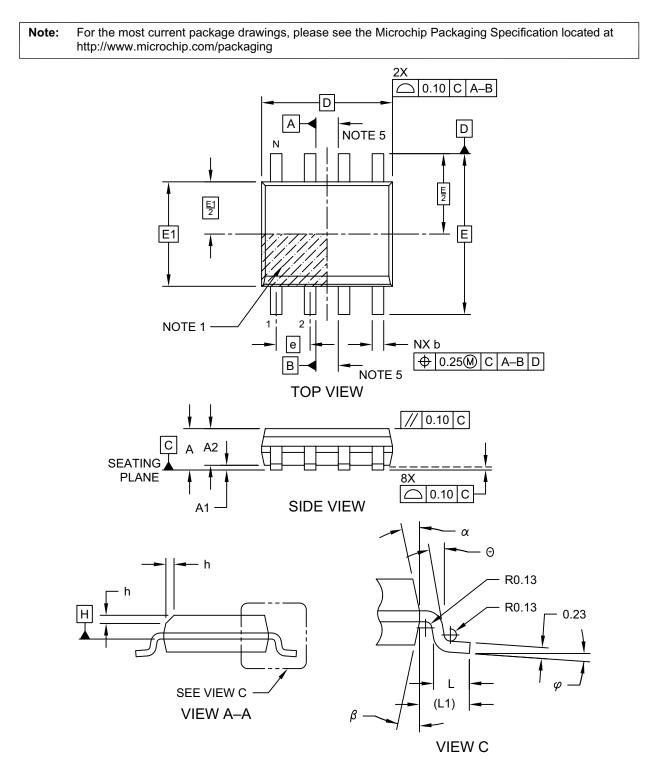
| Units                      |    | INCHES   |      |      |  |
|----------------------------|----|----------|------|------|--|
| Dimension Limits           |    | MIN      | NOM  | MAX  |  |
| Number of Pins             | N  | 8        |      |      |  |
| Pitch                      | е  | .100 BSC |      |      |  |
| Top to Seating Plane       | Α  | -        | -    | .210 |  |
| Molded Package Thickness   | A2 | .115     | .130 | .195 |  |
| Base to Seating Plane      | A1 | .015     | -    | -    |  |
| Shoulder to Shoulder Width | E  | .290     | .310 | .325 |  |
| Molded Package Width       | E1 | .240     | .250 | .280 |  |
| Overall Length             | D  | .348     | .365 | .400 |  |
| Tip to Seating Plane       | L  | .115     | .130 | .150 |  |
| Lead Thickness             | С  | .008     | .010 | .015 |  |
| Upper Lead Width           | b1 | .040     | .060 | .070 |  |
| Lower Lead Width           | b  | .014     | .018 | .022 |  |
| Overall Row Spacing §      | eВ | -        | -    | .430 |  |

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- 5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev E Sheet 2 of 2

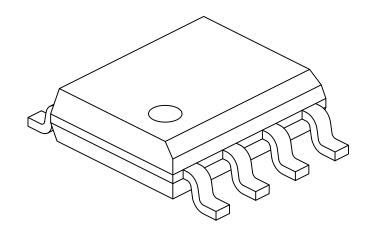
# 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]



Microchip Technology Drawing No. C04-057-SN Rev E Sheet 1 of 2

# 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



|                          | MILLIMETERS |             |     |      |
|--------------------------|-------------|-------------|-----|------|
| Dimension Limits         |             | MIN         | NOM | MAX  |
| Number of Pins           | Ν           | 8           |     |      |
| Pitch                    | е           | 1.27 BSC    |     |      |
| Overall Height           | Α           | -           | -   | 1.75 |
| Molded Package Thickness | A2          | 1.25        | -   | -    |
| Standoff §               | A1          | 0.10        | -   | 0.25 |
| Overall Width            | E           | 6.00 BSC    |     |      |
| Molded Package Width     | E1          | 3.90 BSC    |     |      |
| Overall Length           | D           | 4.90 BSC    |     |      |
| Chamfer (Optional)       | h           | 0.25 - 0.50 |     |      |
| Foot Length              | L           | 0.40        | -   | 1.27 |
| Footprint                | L1          | 1.04 REF    |     |      |
| Foot Angle               | φ           | 0°          | -   | 8°   |
| Lead Thickness           | С           | 0.17        | -   | 0.25 |
| Lead Width               | b           | 0.31        | -   | 0.51 |
| Mold Draft Angle Top     | α           | 5°          | -   | 15°  |
| Mold Draft Angle Bottom  | β           | 5°          | -   | 15°  |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

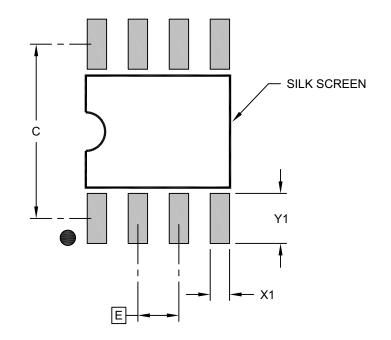
REF: Reference Dimension, usually without tolerance, for information purposes only.

5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev E Sheet 2 of 2

# 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



# RECOMMENDED LAND PATTERN

| Units                   |    | MILLIMETERS |      |      |
|-------------------------|----|-------------|------|------|
| Dimension Limits        |    | MIN         | NOM  | MAX  |
| Contact Pitch           | Е  | 1.27 BSC    |      |      |
| Contact Pad Spacing     | С  |             | 5.40 |      |
| Contact Pad Width (X8)  | X1 |             |      | 0.60 |
| Contact Pad Length (X8) | Y1 |             |      | 1.55 |

Notes:

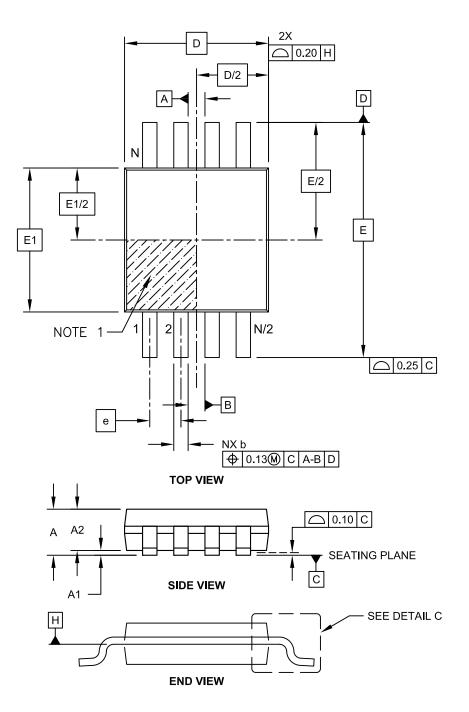
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev E

# 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

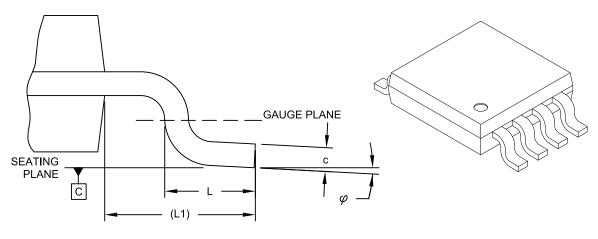
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

### 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

|                          | MILLIMETERS |          |      |      |
|--------------------------|-------------|----------|------|------|
| Dimension Limits         |             | MIN      | NOM  | MAX  |
| Number of Pins           | N           | 8        |      |      |
| Pitch                    | е           | 0.65 BSC |      |      |
| Overall Height           | A           | 1.10     |      |      |
| Molded Package Thickness | A2          | 0.75     | 0.85 | 0.95 |
| Standoff                 | A1          | 0.00     | -    | 0.15 |
| Overall Width            | E           | 4.90 BSC |      |      |
| Molded Package Width     | E1          | 3.00 BSC |      |      |
| Overall Length           | D           | 3.00 BSC |      |      |
| Foot Length              | L           | 0.40     | 0.60 | 0.80 |
| Footprint                | L1          | 0.95 REF |      |      |
| Foot Angle               | φ           | 0°       | -    | 8°   |
| Lead Thickness           | С           | 0.08     | -    | 0.23 |
| Lead Width               | b           | 0.22     | -    | 0.40 |

#### Notes:

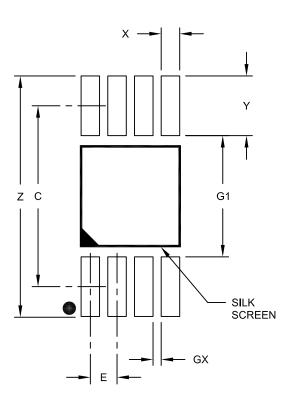
- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- protrusions shall not exceed 0.15mm per side. 3. Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

# 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



# RECOMMENDED LAND PATTERN

|                         | Units      |      | MILLIMETERS |      |  |  |
|-------------------------|------------|------|-------------|------|--|--|
| Dimension Limits        |            | MIN  | NOM         | MAX  |  |  |
| Contact Pitch           | E 0.65 BSC |      |             |      |  |  |
| Contact Pad Spacing     | С          |      | 4.40        |      |  |  |
| Overall Width           | Z          |      |             | 5.85 |  |  |
| Contact Pad Width (X8)  | X1         |      |             | 0.45 |  |  |
| Contact Pad Length (X8) | Y1         |      |             | 1.45 |  |  |
| Distance Between Pads   | G1         | 2.95 |             |      |  |  |
| Distance Between Pads   | GX         | 0.20 |             |      |  |  |

### Notes:

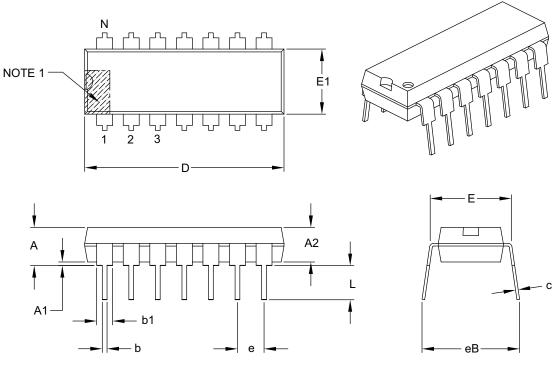
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

#### 14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



|                            | Units            |          | INCHES |      |
|----------------------------|------------------|----------|--------|------|
|                            | Dimension Limits | MIN      | NOM    | MAX  |
| Number of Pins             | N                | 14       |        |      |
| Pitch                      | е                | .100 BSC |        |      |
| Top to Seating Plane       | A                | _        | -      | .210 |
| Molded Package Thickness   | A2               | .115     | .130   | .195 |
| Base to Seating Plane      | A1               | .015     | -      | -    |
| Shoulder to Shoulder Width | E                | .290     | .310   | .325 |
| Molded Package Width       | E1               | .240     | .250   | .280 |
| Overall Length             | D                | .735     | .750   | .775 |
| Tip to Seating Plane       | L                | .115     | .130   | .150 |
| Lead Thickness             | С                | .008     | .010   | .015 |
| Upper Lead Width           | b1               | .045     | .060   | .070 |
| Lower Lead Width           | b                | .014     | .018   | .022 |
| Overall Row Spacing §      | eB               | _        | -      | .430 |

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.

2. § Significant Characteristic.

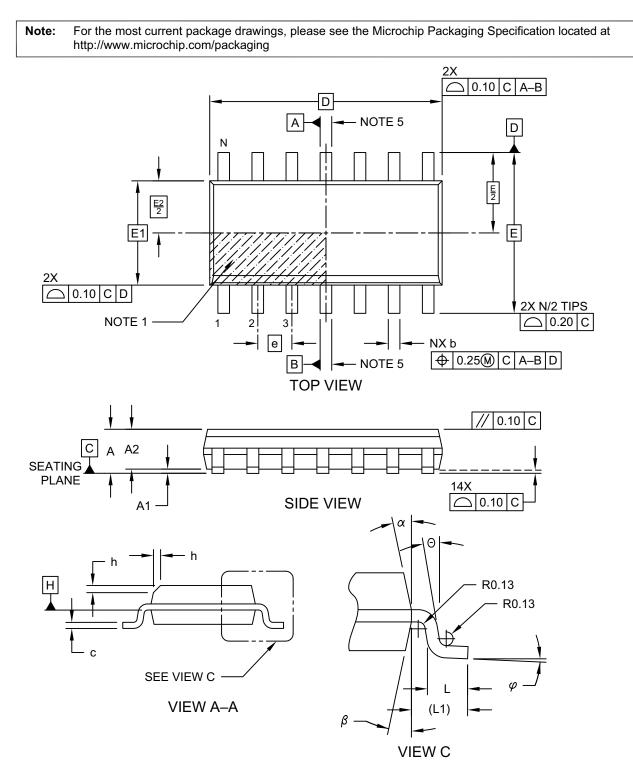
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

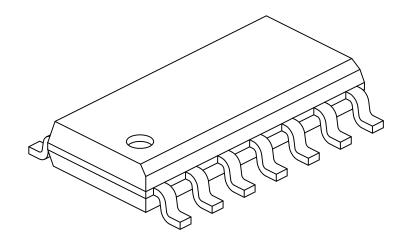
### 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]



Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

#### 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units                    |    | N           | <b>IILLIMETER</b> | ILLIMETERS<br>NOM MAX<br>14 |  |  |
|--------------------------|----|-------------|-------------------|-----------------------------|--|--|
| Dimension Limits         |    | MIN         | NOM               | MAX                         |  |  |
| Number of Pins           | N  | 14          |                   |                             |  |  |
| Pitch                    | е  | 1.27 BSC    |                   |                             |  |  |
| Overall Height           | Α  | -           | -                 | 1.75                        |  |  |
| Molded Package Thickness | A2 | 1.25        | -                 | -                           |  |  |
| Standoff §               | A1 | 0.10        | -                 | 0.25                        |  |  |
| Overall Width            | E  | 6.00 BSC    |                   |                             |  |  |
| Molded Package Width     | E1 | 3.90 BSC    |                   |                             |  |  |
| Overall Length           | D  | 8.65 BSC    |                   |                             |  |  |
| Chamfer (Optional)       | h  | 0.25 - 0.50 |                   | 0.50                        |  |  |
| Foot Length              | L  | 0.40 - 1.2  |                   | 1.27                        |  |  |
| Footprint                | L1 | 1.04 REF    |                   |                             |  |  |
| Lead Angle               | Θ  | 0°          | -                 | -                           |  |  |
| Foot Angle               | φ  | 0°          | -                 | 8°                          |  |  |
| Lead Thickness           | С  | 0.10        | -                 | 0.25                        |  |  |
| Lead Width               | b  | 0.31        | -                 | 0.51                        |  |  |
| Mold Draft Angle Top     | α  | 5° - 15°    |                   | 15°                         |  |  |
| Mold Draft Angle Bottom  | β  | 5° - 15°    |                   |                             |  |  |

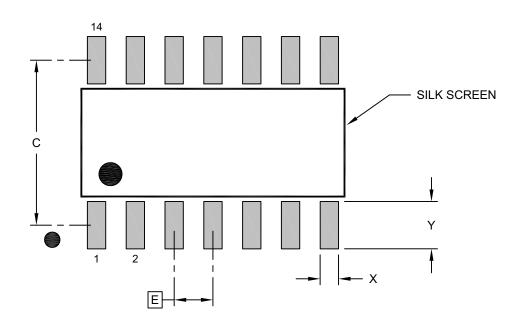
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

## 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



#### RECOMMENDED LAND PATTERN

| Units                    |   | MILLIMETERS |          |      |
|--------------------------|---|-------------|----------|------|
| Dimension Limits         |   | MIN         | NOM      | MAX  |
| Contact Pitch            | E |             | 1.27 BSC |      |
| Contact Pad Spacing      | С |             | 5.40     |      |
| Contact Pad Width (X14)  | Х |             |          | 0.60 |
| Contact Pad Length (X14) | Y |             |          | 1.55 |

Notes:

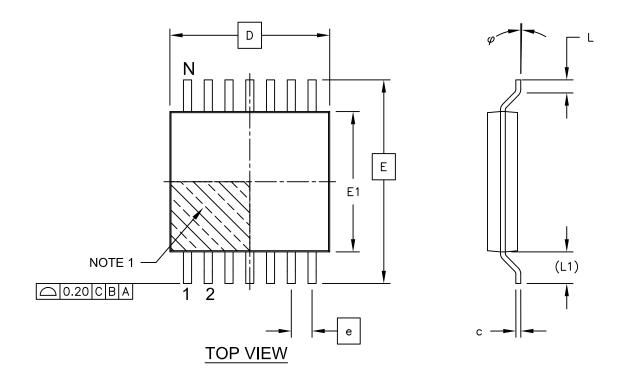
1. Dimensioning and tolerancing per ASME Y14.5M

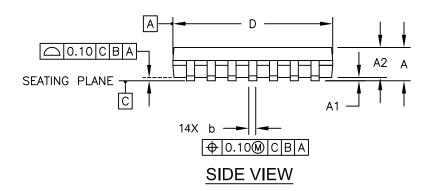
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

#### 14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

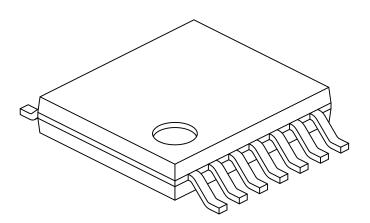




Microchip Technology Drawing C04-087C Sheet 1 of 2

#### 14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units                    |      | N        | MILLIMETERS |      |  |
|--------------------------|------|----------|-------------|------|--|
| Dimension Limits         |      | MIN      | NOM         | MAX  |  |
| Number of Pins           | N    | 14       |             |      |  |
| Pitch                    | е    | 0.65 BSC |             |      |  |
| Overall Height           | A    | -        | -           | 1.20 |  |
| Molded Package Thickness | A2   | 0.80     | 1.00        | 1.05 |  |
| Standoff                 | A1   | 0.05     | -           | 0.15 |  |
| Overall Width            | E    | 6.40 BSC |             |      |  |
| Molded Package Width     | E1   | 4.30     | 4.40        | 4.50 |  |
| Molded Package Length    | D    | 4.90     | 5.00        | 5.10 |  |
| Foot Length              | L    | 0.45     | 0.60        | 0.75 |  |
| Footprint                | (L1) | 1.00 REF |             |      |  |
| Foot Angle               | φ    | 0°       | -           | 8°   |  |
| Lead Thickness           | С    | 0.09     | -           | 0.20 |  |
| Lead Width               | b    | 0.19     | -           | 0.30 |  |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.

3. Dimensioning and tolerancing per ASME Y14.5M

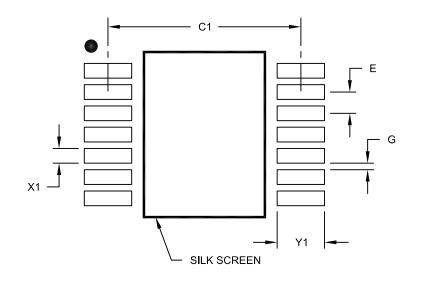
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

#### 14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



#### RECOMMENDED LAND PATTERN

| Units                    |    | MILLIMETERS |      |      |
|--------------------------|----|-------------|------|------|
| Dimension Limits         |    | MIN         | NOM  | MAX  |
| Contact Pitch            | E  | 0.65 BSC    |      |      |
| Contact Pad Spacing      | C1 |             | 5.90 |      |
| Contact Pad Width (X14)  | X1 |             |      | 0.45 |
| Contact Pad Length (X14) | Y1 |             |      | 1.45 |
| Distance Between Pads    | G  | 0.20        |      |      |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

# MCP6001/1R/1U/2/4

NOTES:

#### APPENDIX A: REVISION HISTORY

#### **Revision K (November 2019)**

The following is the list of modifications:

1. Updated Section 6.0 "Packaging Information".

#### **Revision J (November 2009)**

The following is the list of modifications:

- 1. Added new 2x3 DFN 8-Lead package on page 1.
- 2. Updated the Temperature Specifications table with 2x3 DFN thermal resistance information.
- 3. Updated Section 1.1 "Test Circuits".
- 4. Updated Figure 2-15.
- 5. Added the 2x3 DFN column to Table 3-1.
- 6. Added new Section 3.4 "Exposed Thermal Pad (EP)".
- 7. Updated Section 5.1 "SPICE Macro Model".
- 8. Updated Section 5.5 "Analog Demonstration and Evaluation Boards".
- 9. Updated Section 5.6 "Application Notes".
- 10. Updated **Section 6.1 "Package Marking Information**" with the new 2x3 DFN package marking information.
- 11. Updated the package drawings.
- 12. Updated the Product Identification System section with new 2x3 DFN package information.

#### Revision H (May 2008)

The following is the list of modifications:

- 1. **Design Aids:** Name change for Mindi Simulation Tool.
- 2. Package Types: Correct device labeling error.
- 3. Section 1.0 "Electrical Characteristics", DC Electrical Specifications: Changed "Maximum Output Voltage Swing" condition from 0.9V Input Overdrive to 0.5V Input Overdrive.
- Section 1.0 "Electrical Characteristics", AC Electrical Specifications: Changed Phase Margin condition from G = +1 to G= +1 V/V.
- 5. Section 5.0 "Design AIDS": Name change for Mindi Simulation Tool.

#### **Revision G (November 2007)**

The following is the list of modifications:

- 1. Updated notes to Section 1.0 "Electrical Characteristics".
- 2. Increased Absolute Maximum Voltage range at input pins.
- 3. Increased maximum operating supply voltage  $(V_{DD})$ .
- 4. Added test circuits.
- 5. Added Figure 2-3 and Figure 2-20.
- 6. Added Section 4.1.1 "Phase Reversal", Section 4.1.2 "Input Voltage and Current Limits", Section 4.1.3 "Normal Operation" and Section 4.5 "Unused Op Amps".
- 7. Updated Section 5.0 "Design AIDS",
- 8. Updated Section 6.0 "Packaging Information"
- 9. Updated Package Outline Drawings.

#### **Revision F (March 2005)**

The following is the list of modifications:

1. Updated Section 6.0 "Packaging Information" to include old and new packaging examples.

#### **Revision E (December 2004)**

The following is the list of modifications:

- V<sub>OS</sub> specification reduced to ±4.5 mV from ±7.0 mV for parts starting with date code YYWW = 0449
- 2. Corrected package markings in Section 6.0 "Packaging Information".
- 3. Added Appendix A: Revision History.

#### Revision D (May 2003)

• Undocumented changes.

#### **Revision C (December 2002)**

• Undocumented changes.

#### **Revision B (October 2002)**

· Undocumented changes.

#### Revision A (June 2002)

Original data sheet release.

NOTES:

### **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>ΡΑRT ΝΟ. Χ /ΧΧ</u> |  | Examples:  |
|-----------------------|--|--|
| Device Temp           | erature Package<br>nge   | a) MCP6001T-I/LT:Tape and Reel,<br>Industrial Temperature,<br>5LD SC-70 package<br>b) MCP6001T-I/OT: Tape and Reel,  |
| Device:               | MCP6001T:       Single Op Amp (Tape and Reel)<br>(SC-70, SOT-23)         MCP6001RT:       Single Op Amp (Tape and Reel) (SOT-23)         MCP6001UT:       Single Op Amp (Tape and Reel) (SOT-23)         MCP6002:       Dual Op Amp<br>(Tape and Reel) (SOT-23)         MCP6002:       Dual Op Amp<br>(SOIC_MSOP)         MCP60041:       Quad Op Amp<br>(SOIC, MSOP)         MCP60041:       Quad Op Amp<br>(SOIC, MSOP)                                | <ul> <li>b) MCP600114/01. Industrial Temperature,<br/>5LD SOT-23 package.</li> <li>c) MCP6001RT-I/OT: Tape and Reel,<br/>Industrial Temperature,<br/>5LD SOT-23 package.</li> <li>d) MCP6001UT-E/OT: Tape and Reel,<br/>Extended Temperature,<br/>5LD SOT-23 package.</li> <li>a) MCP6002-I/MS:Industrial Temperature, 8LD<br/>MSOP package.</li> </ul>  |
| Temperature Range:    | $I = -40^{\circ}C \text{ to } +85^{\circ}C$<br>E = -40^{\circ}C to +125^{\circ}C   | <ul> <li>b) MCP6002-I/P:Industrial Temperature, 8LD<br/>PDIP package.</li> <li>c) MCP6002-E/P:Extended Temperature, 8LD</li> </ul>   |
| Package:              | <ul> <li>LT = Plastic Package (SC-70), 5-lead (MCP6001 only)</li> <li>OT = Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6001, MCP6001R, MCP6001U)</li> <li>MS = Plastic MSOP, 8-lead</li> <li>MC = Plastic DFN, 8-lead</li> <li>P = Plastic DIP (300 mil body), 8-lead, 14-lead</li> <li>SN = Plastic SOIC, (3.99 mm body), 8-lead</li> <li>SL = Plastic SOIC (3.99 body), 14-lead</li> <li>ST = Plastic TSSOP (4.4mm body), 14-lead</li> </ul> | PDIP package.<br>d) MCP6002-E/MC:Extended Temperature,<br>8LD DFN package.<br>e) MCP6002-I/SN:Industrial Temperature, 8LD<br>SOIC package.<br>f) MCP6002T-I/MS:Tape and Reel,<br>Industrial Temperature,<br>8LD MSOP package.<br>g) MCP6002T-E/MC:Tape and Reel,<br>Extended Temperature,<br>8LD DFN package.  |
|                       |  | <ul> <li>a) MCP6004-I/P:Industrial Temperature, 14LD PDIP package.</li> <li>b) MCP6004-I/SL:Industrial Temperature, 14LD SOIC package.</li> <li>c) MCP6004-E/SL:Extended Temperature, 14LD SOIC package.</li> <li>d) MCP6004-I/ST:Industrial Temperature, 14LD TSSOP package.</li> <li>e) MCP6004T-I/SL:Tape and Reel, Industrial Temperature, 14LD SOIC package.</li> <li>f) MCP6004T-I/ST:Tape and Reel, Industrial Temperature, 14LD SOIC package.</li> </ul> |

# MCP6001/1R/1U/2/4

NOTES:

#### Note the following details of the code protection feature on Microchip devices:

- · Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

#### Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PackeTime, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TempTrackr, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, FlashTec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, Vite, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet Iogo, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified Iogo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2019, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-5331-4

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.



## Worldwide Sales and Service

#### AMERICAS

**Corporate Office** 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: http://www.microchip.com/ support

Web Address: www.microchip.com

Atlanta Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455

Austin, TX Tel: 512-257-3370

**Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088

Chicago Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075

Dallas Addison, TX Tel: 972-818-7423 Fax: 972-818-2924

Detroit Novi, MI Tel: 248-848-4000

Houston, TX Tel: 281-894-5983

Indianapolis Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380

Los Angeles Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800

Raleigh, NC Tel: 919-844-7510

New York NY Tel: 631-435-6000

San Jose, CA Tel: 408-735-9110 Tel: 408-436-4270

Canada - Toronto Tel: 905-695-1980 Fax: 905-695-2078

#### ASIA/PACIFIC

Australia - Sydney Tel: 61-2-9868-6733

China - Beijing Tel: 86-10-8569-7000 China - Chengdu

Tel: 86-28-8665-5511 China - Chongqing Tel: 86-23-8980-9588

China - Dongguan Tel: 86-769-8702-9880

China - Guangzhou Tel: 86-20-8755-8029

China - Hangzhou Tel: 86-571-8792-8115

China - Hong Kong SAR Tel: 852-2943-5100

China - Nanjing Tel: 86-25-8473-2460

China - Qingdao Tel: 86-532-8502-7355

China - Shanghai Tel: 86-21-3326-8000

China - Shenyang Tel: 86-24-2334-2829

China - Shenzhen Tel: 86-755-8864-2200

China - Suzhou Tel: 86-186-6233-1526

China - Wuhan Tel: 86-27-5980-5300

China - Xian Tel: 86-29-8833-7252

China - Xiamen Tel: 86-592-2388138 China - Zhuhai

#### ASIA/PACIFIC

India - Bangalore Tel: 91-80-3090-4444

India - New Delhi Tel: 91-11-4160-8631 India - Pune

Tel: 91-20-4121-0141 Japan - Osaka

Tel: 81-6-6152-7160 Japan - Tokyo

Tel: 81-3-6880- 3770 Korea - Daegu

Tel: 82-53-744-4301 Korea - Seoul

Tel: 82-2-554-7200

Malaysia - Kuala Lumpur Tel: 60-3-7651-7906

Tel: 60-4-227-8870

Tel: 63-2-634-9065

Tel: 65-6334-8870

Taiwan - Hsin Chu

Taiwan - Kaohsiung Tel: 886-7-213-7830

Thailand - Bangkok

Vietnam - Ho Chi Minh Tel: 84-28-5448-2100

**Netherlands - Drunen** Tel: 31-416-690399

Fax: 31-416-690340

EUROPE

Austria - Wels

Tel: 43-7242-2244-39

Tel: 45-4450-2828

Fax: 45-4485-2829

Tel: 358-9-4520-820

Tel: 33-1-69-53-63-20

Fax: 33-1-69-30-90-79

Germany - Garching

Tel: 49-2129-3766400

Germany - Heilbronn

Germany - Karlsruhe

Tel: 49-7131-72400

Tel: 49-721-625370

Germany - Munich

Tel: 49-89-627-144-0

Fax: 49-89-627-144-44

Germany - Rosenheim

Tel: 49-8031-354-560

Israel - Ra'anana

Italy - Milan

Italy - Padova

Tel: 972-9-744-7705

Tel: 39-0331-742611

Fax: 39-0331-466781

Tel: 39-049-7625286

Tel: 49-8931-9700

Germany - Haan

Finland - Espoo

France - Paris

Fax: 43-7242-2244-393

Denmark - Copenhagen

Norway - Trondheim Tel: 47-7288-4388

Poland - Warsaw Tel: 48-22-3325737

Romania - Bucharest Tel: 40-21-407-87-50

Spain - Madrid Tel: 34-91-708-08-90 Fax: 34-91-708-08-91

Sweden - Gothenberg Tel: 46-31-704-60-40

Sweden - Stockholm Tel: 46-8-5090-4654

**UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820

Malaysia - Penang

Philippines - Manila

Singapore

Tel: 886-3-577-8366

Taiwan - Taipei Tel: 886-2-2508-8600

Tel: 66-2-694-1351

Tel: 86-756-3210040