OPAx348-Q1 1-MHz 45-µA CMOS Rail-to-Rail Operational Amplifier

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Low Quiescent Current (I_Q): 45 µA (Typ)
- Low Cost
- Rail-to-Rail Input and Output
- Single Supply: 2.1 V to 5.5 V
- Input Bias Current: 0.5 pA (Typ)
- High Speed: Power With Bandwidth: 1 MHz

2 Applications

- Portable Equipment
- Battery-Powered Equipment
- Smoke Alarms
- CO Detectors
- HEV/EV and Power Train
- Infotainment and Cluster
- Medical Instrumentation

3 Description

The OPAx348-Q1 series of devices are single-supply, low-power CMOS operational amplifiers. Featuring an extended bandwidth of 1 MHz and a supply current of 45 µA, the OPAx348-Q1 family of devices is useful for low-power applications on single supplies of 2.1 V to 5.5 V.

Low supply current of 45 µA and an input bias current of 0.5 pA make the OPAx348-Q1 family of devices an optimal candidate for low-power, high-impedance applications such as smoke detectors and other sensors.

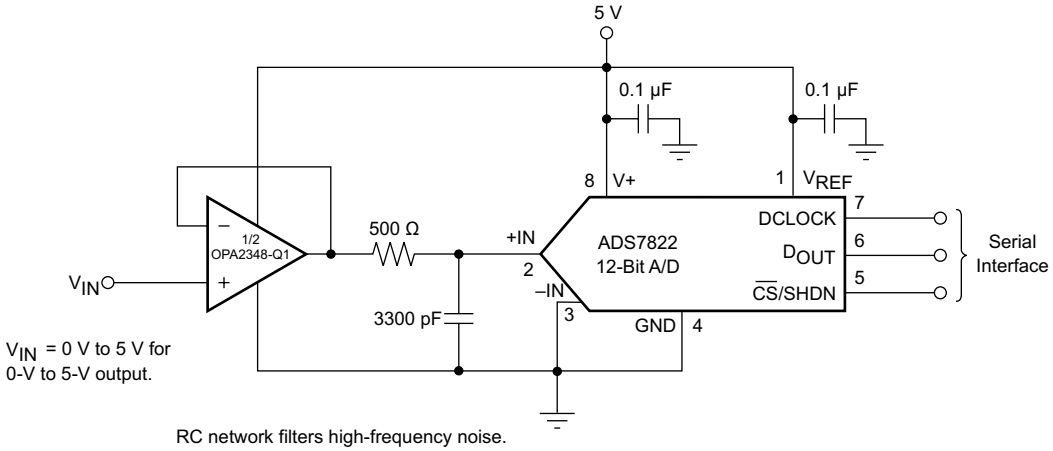
The OPA348-Q1 device is available in both the SOT23-5 (DBV) and the SOIC (D) packages. The OPA2348-Q1 device is available in the SOIC-8 (D) package. The OPA4348-Q1 device is available in the TSSOP-14 (PW) package. The automotive temperature range of –40°C to +125°C over all supply voltages offers additional design flexibility.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA348-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
	SOIC (8)	4.90 mm × 3.91 mm
OPA2348-Q1	SOIC (8)	4.90 mm × 3.91 mm
OPA4348-Q1	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Noninverting Configuration Driving ADS7822



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2014) to Revision C **Page**

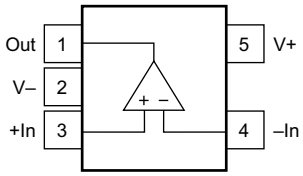
- Added the OPA348-Q1 SOIC (D) package option to document ... 1

Changes from Revision A (January 2009) to Revision B **Page**

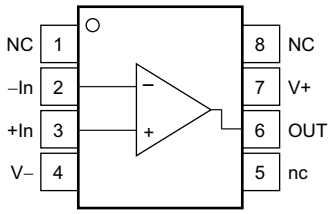
- Added two new applications to the *Applications* section ... 1
- Added the *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added the OPA348-Q1 device to the data sheet ... 1
- Changed the name for pin 3 in the PW (TSSOP) package drawing ... 4

5 Pin Configuration and Functions

DBV Package: OPA348-Q1
5-Pin SOT-23
Top View



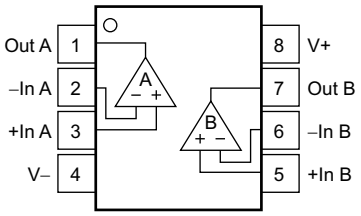
D Package: OPA348-Q1
8-Pin SOIC
Top View



Pin Functions: OPA348-Q1

PIN			I/O	DESCRIPTION
NAME	NO.			
	SOT-23	SOIC		
+IN	3	3	I	Noninverting input
–IN	4	2	I	Inverting input
OUT	1	6	O	Output
V+	5	7	—	Positive (highest) supply
V–	2	4	—	Negative (lowest) supply
NC	—	1	—	Do not connect
		5		
		8		

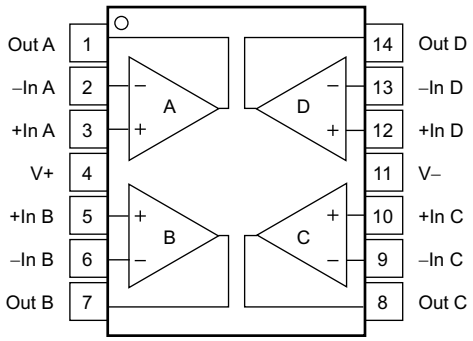
D Package: OPA2348-Q1
8-Pin SOIC
Top View



Pin Functions: OPA2348-Q1

PIN		I/O	DESCRIPTION
NAME	NO		
+IN A	3	I	Noninverting input, Channel A
–IN A	2	I	Inverting input, Channel A
+IN B	5	I	Noninverting input, Channel B
–IN B	6	I	Inverting input, Channel B
OUT A	1	O	Output, Channel A
OUT B	7	O	Output, Channel B
V+	8	—	Positive (highest) supply
V–	4	—	Negative (lowest) supply

PW Package: OPA4348-Q1
14-Pin TSSOP
Top View



Pin Functions: OPA4348-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, Channel A
–IN A	2	I	Inverting input, Channel A
+IN B	5	I	Noninverting input, Channel B
–IN B	6	I	Inverting input, Channel B
+IN C	10	I	Noninverting input, Channel C
–IN C	9	I	Inverting input, Channel C
+IN D	12	I	Noninverting input, Channel D
–IN D	13	I	Inverting input, Channel D
OUT A	1	O	Output, Channel A
OUT B	7	O	Output, Channel B
OUT C	8	O	Output, Channel C
OUT D	14	O	Output, Channel D
V+	4	—	Positive (highest) supply
V–	11	—	Negative (lowest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S	V– to V+		7.5	V
Input voltage, V_{IN}	Signal input terminals(2)	(V–) – 0.5 V	(V+) + 0.5 V	V
Input current, I_{IN}	Signal input terminals(2)		10	mA
Output short-circuit duration(3)		Continuous		
Operating free-air temperature, T_A		–40	150	°C
Operating virtual-junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 7, 8, and 14)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, V– to V+	2.1	5.5	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information: OPA348-Q1

THERMAL METRIC(1)		OPA348-Q1		UNIT
		DBV (SOT-23)	D (SOIC)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.5	142.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.1	90.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.6	82.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.7	39.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	82.0	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: OPA2348-Q1, OPA4348-Q1

THERMAL METRIC(1)		OPA2348-Q1	OPA4348-Q1	UNIT
		D (SOIC)	PW (TSSOP)	
		8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.4	121	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.5	49.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.9	5.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.1	62.2	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

At V_S = 2.5 V to 5.5 V, R_L = 100 kΩ connected to V_S / 2, V_{OUT} = V_S / 2 (unless otherwise noted).

PARAMETER			TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage		V_S = 5 V, V_{CM} = (V–) + 0.8 V	25°C		1	5	mV
				Full range			6	
$\Delta V_{OS}/\Delta T$	Offset voltage drift over temperature			Full range		4		µV/°C
PSRR	Offset voltage drift vs power supply		V_S = 2.5 V to 5.5 V, V_{CM} < (V+) – 1.7 V	25°C		60	175	µV/V
				Full range			300	
	Channel separation		dc	25°C		0.2		µV/V
			f = 1 kHz	25°C		134		dB
V_{CM}	Input common-mode voltage range			25°C	(V–) – 0.2		(V+) + 0.2	V
CMRR	Input common-mode rejection ratio		(V–) – 0.2 V < V_{CM} < (V+) – 1.7 V	25°C	70	82		dB
				Full range	66			
			V_S = 5.5 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V	25°C	60	71		
			V_S = 5.5 V, (V–) < V_{CM} < (V+)	Full range	56			
I_B	Input bias current			25°C		±0.5	±10	pA
I_{OS}	Input offset current			25°C		±0.5	±10	pA
Z_I	Input impedance		Differential	25°C		10^{13}|| 3		Ω || pF
			Common-mode			10^{13}|| 3		
	Input voltage noise		V_{CM} < (V+) – 1.7 V, f = 0.1 Hz to 10 Hz	25°C		10		μV_{PP}
V_n	Input voltage noise density		V_{CM} < (V+) – 1.7 V, f = 1 kHz	25°C		35		nV/√Hz
I_n	Input current noise density		V_{CM} < (V+) – 1.7 V, f = 1 kHz	25°C		4		fA/√Hz
A_{OL}	Open-loop voltage gain		V_S = 5 V, R_L = 100 kΩ, 0.025 V < V_O < 4.975 V	25°C	94	108		dB
				Full range	90			
			V_S = 5V, R_L = 5 kΩ, 0.125 V < V_O < 4.875 V	25°C	90	98		
				Full range	88			
	Voltage output swing from rail		RL = 100 kΩ, A_{OL} > 94 dB	25°C		18	25	mV
				Full range			25	
			RL = 5 kΩ, A_{OL} > 90 dB	25°C		100	125	mV
				Full range			125	
I_{SC}	Output short-circuit current			25°C		±10		mA
C_{LOAD}	Capacitive load drive		See the *Typical Characteristics* section	25°C				
GBW	Gain-bandwidth product		C_L = 100 pF	25°C		1		MHz
SR	Slew rate		C_L = 100 pF, G = +1	25°C		0.5		V/µs
t_s	Settling time	0.1%	C_L = 100 pF, V_S = 5.5 V, 2V- step, G = +1	25°C		5		µs
		0.01%				7		
	Overload recovery time		V_{IN} × Gain > V_S	25°C		1.6		µs
THD+N	Total harmonic distortion plus noise		C_L = 100 pF, V_S = 5.5 V, V_O = 3 V_{PP}, G = +1, f = 1 kHz	25°C		0.0023%		
I_Q	Quiescent current		Per amplifier	25°C		45	65	µA
				Full range			75	

(1) Full range T_A = –40°C to +125°C.

6.7 Typical Characteristics

At T_A = 25°C, R_L = 100 kΩ connected to V_S / 2, V_{OUT} = V_S / 2 (unless otherwise noted).

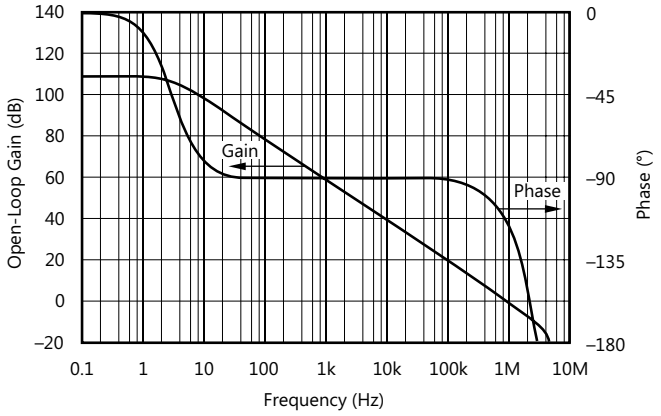


Figure 1. Open-Loop Gain and Phase vs Frequency

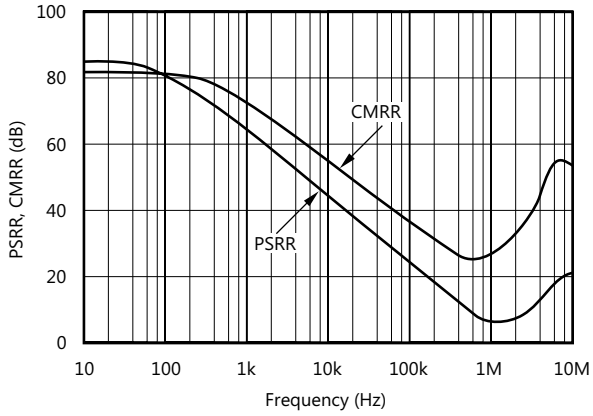


Figure 2. PSRR and CMRR vs Frequency

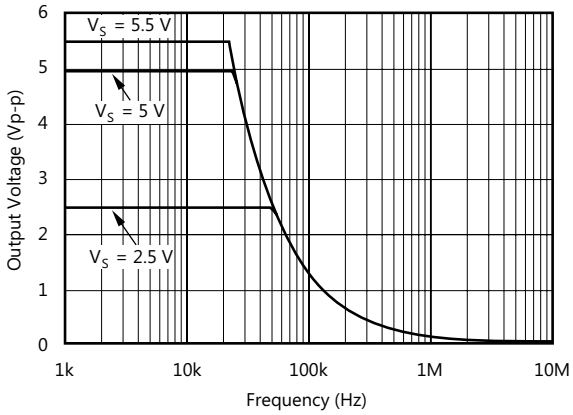


Figure 3. Maximum Output Voltage vs Frequency

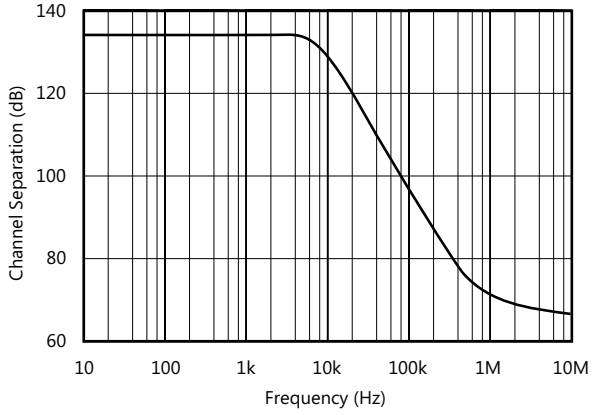


Figure 4. Channel Separation vs Frequency

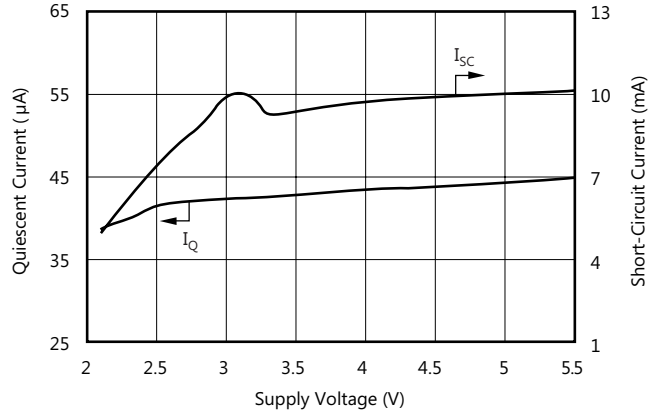


Figure 5. Quiescent and Short-Circuit Current vs Supply Voltage

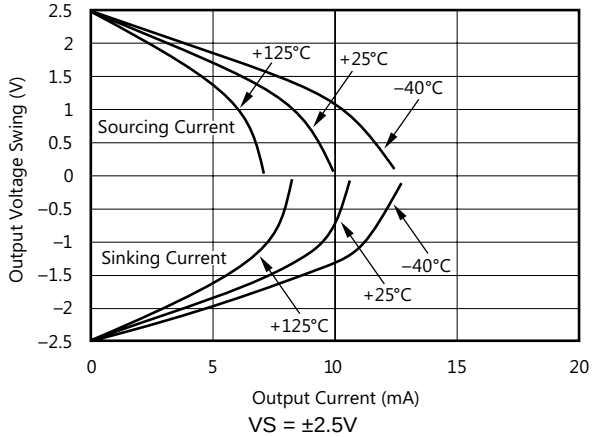


Figure 6. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

At T_A = 25°C, R_L = 100 kΩ connected to V_S / 2, V_{OUT} = V_S / 2 (unless otherwise noted).

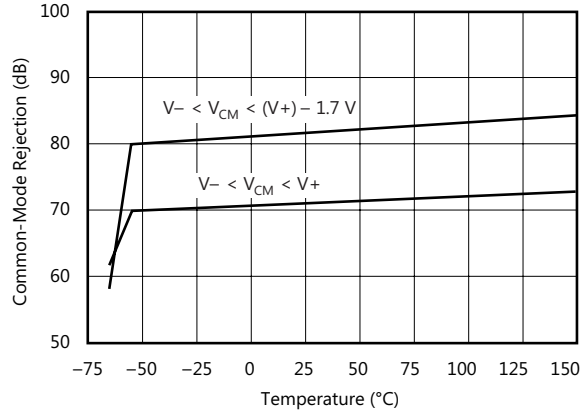


Figure 7. Common-Mode Rejection vs Temperature

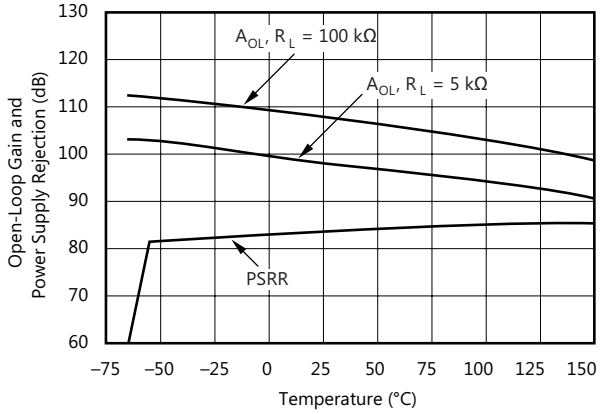


Figure 8. Open-Loop Gain and PSRR vs Temperature

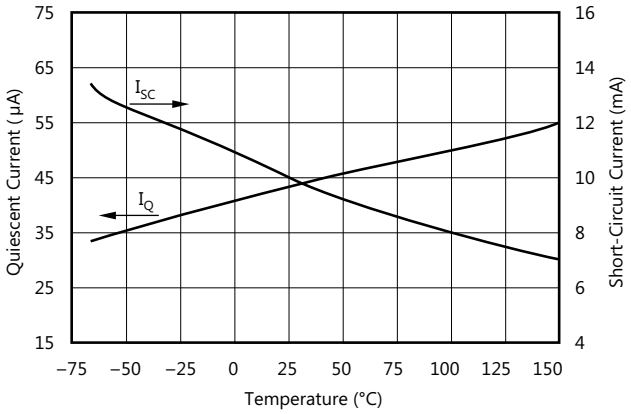


Figure 9. Quiescent and Short-Circuit Current vs Temperature

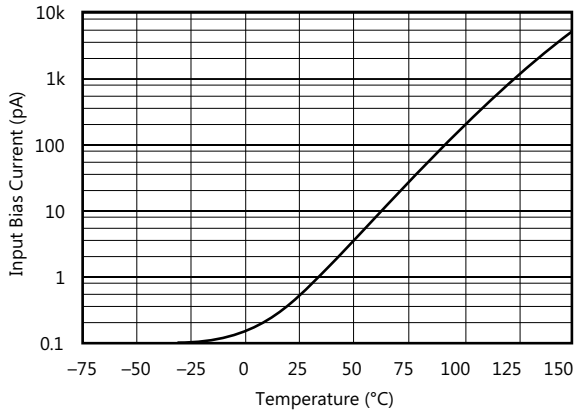
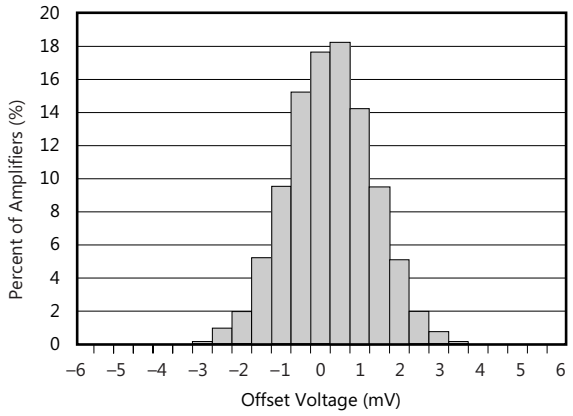
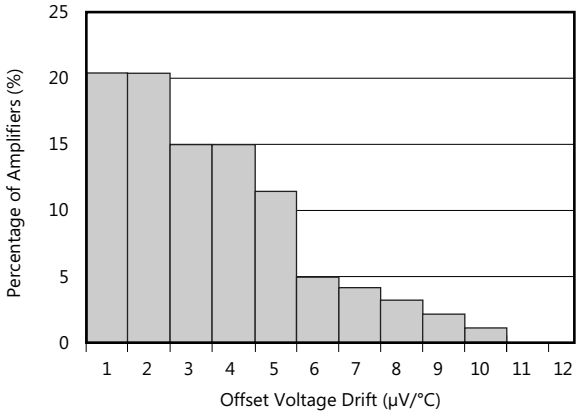


Figure 10. Input Bias (I_B) Current vs Temperature



Typical production distribution of packaged units.

Figure 11. Offset Voltage Production Distribution



Typical production distribution of packaged units.

Figure 12. Offset Voltage Drift Magnitude Production Distribution

Typical Characteristics (continued)

At T_A = 25°C, R_L = 100 kΩ connected to V_S / 2, V_{OUT} = V_S / 2 (unless otherwise noted).

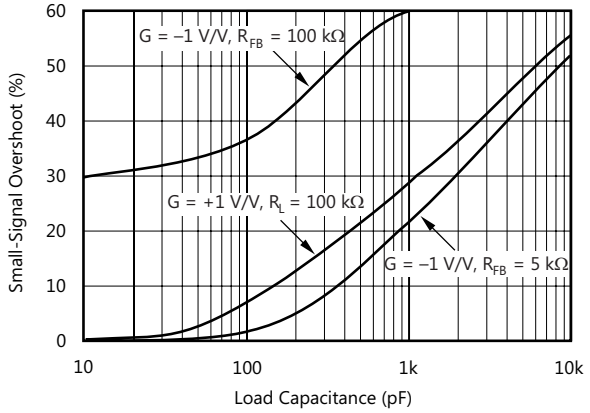
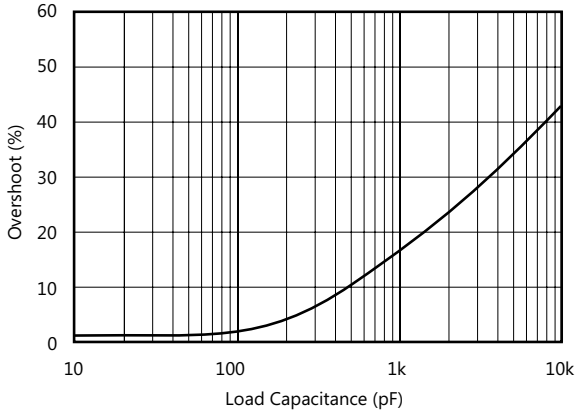
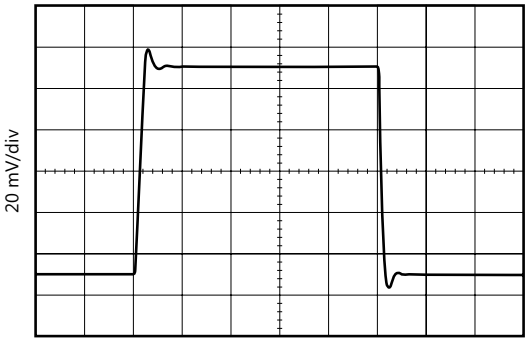


Figure 13. Small-Signal Overshoot vs Load Capacitance



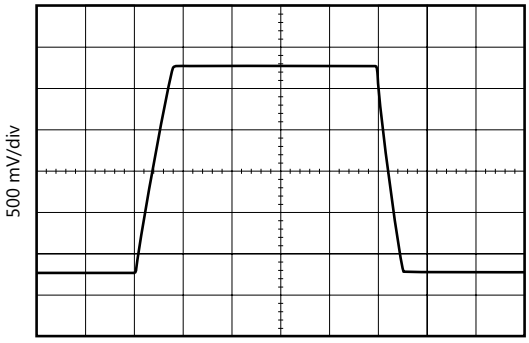
G = ±5 V/V, R_{FB} = 100 kΩ

Figure 14. Percent Overshoot vs Load Capacitance



G = 1 V/V R_L = 100 kΩ C_L = 100 pF

Figure 15. Small-Signal Step Response



G = 1 V/V R_L = 100 kΩ C_L = 100 pF

Figure 16. Large-Signal Step Response

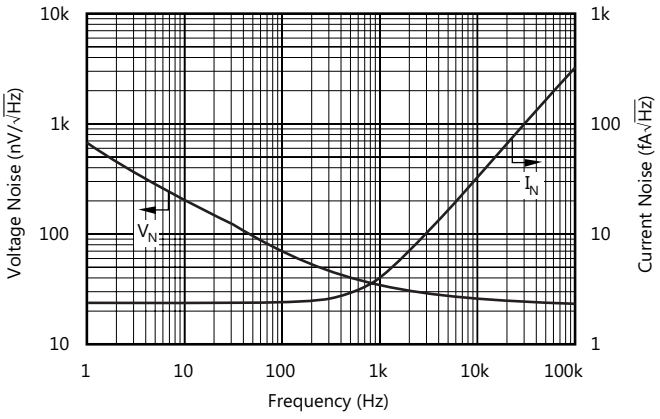


Figure 17. Input Current and Voltage Noise Spectral Density vs Frequency

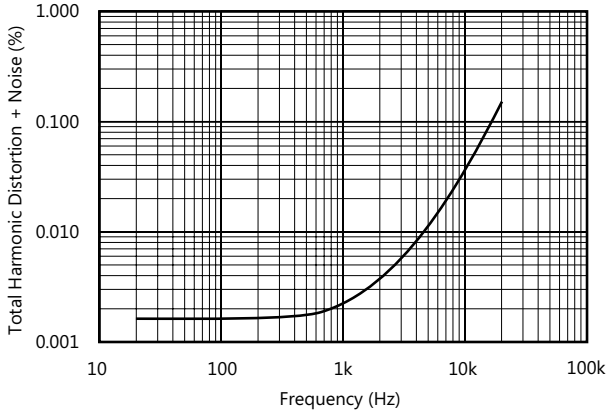


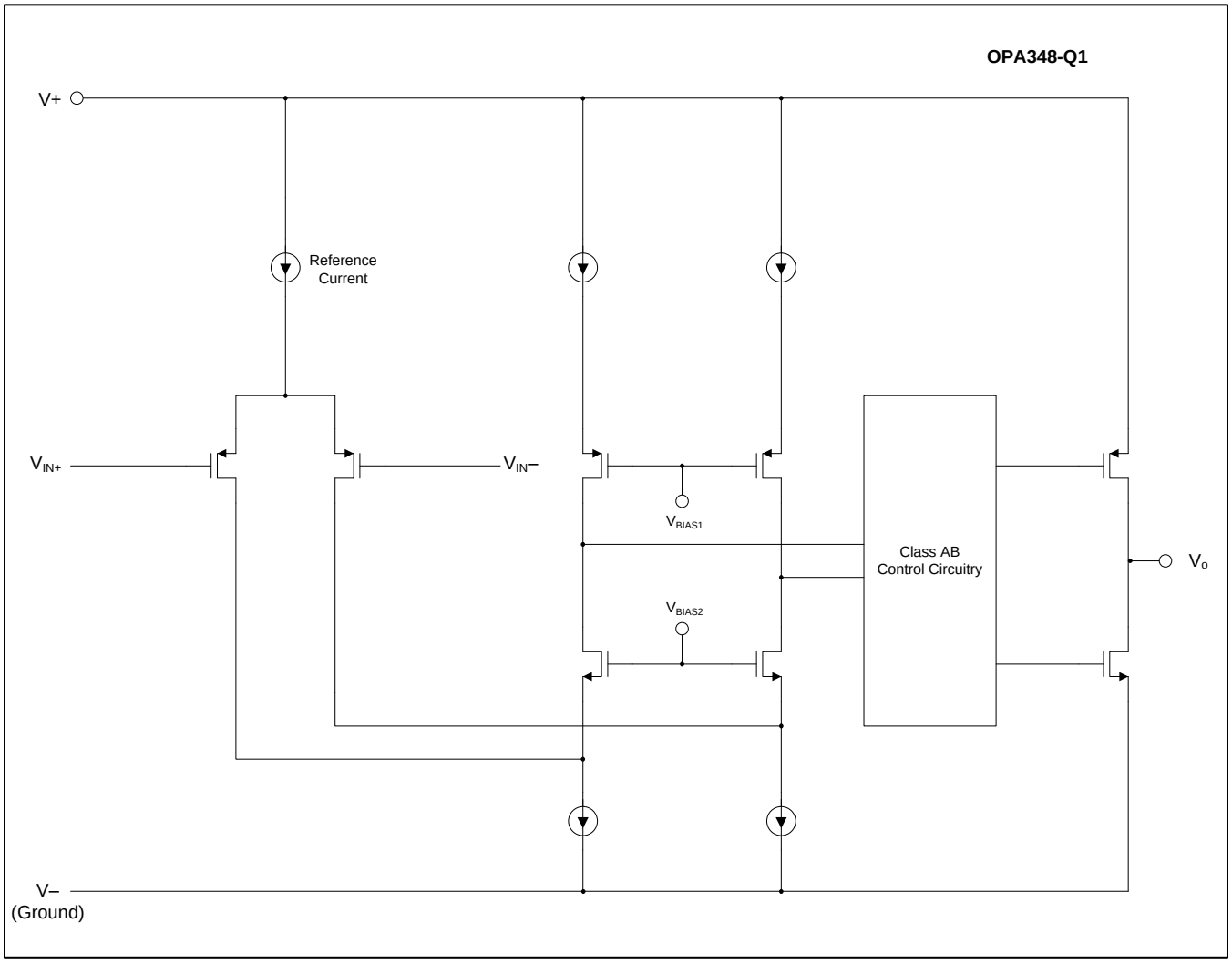
Figure 18. Total Harmonic Distortion + Noise vs Frequency

7 Detailed Description

7.1 Overview

The OPAx348-Q1 family of devices is a low-power, rail-to-rail input and output operational amplifier. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails and allows the OPAx348-Q1 family of devices to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPAx348-Q1 op amp is fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* graphs. Power-supply pins should be bypassed with 0.01-µF ceramic capacitors.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPAx348-Q1 family of devices extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3 V to 200 mV above the positive supply. The P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 1.3 V. A small transition region exists, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region can vary up to 300 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to device operation outside this region.

7.3.3 Rail-to-Rail Input

The input common-mode range extends from (V–) – 0.2 V to (V+) + 0.2 V. For normal operation, the inputs should be limited to this range. The absolute maximum input voltage is 500 mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, do not cause any damage to the op amp. Unlike some other op amps, if the input current is limited, the inputs may go beyond the power supplies without phase inversion, as shown in Figure 19.

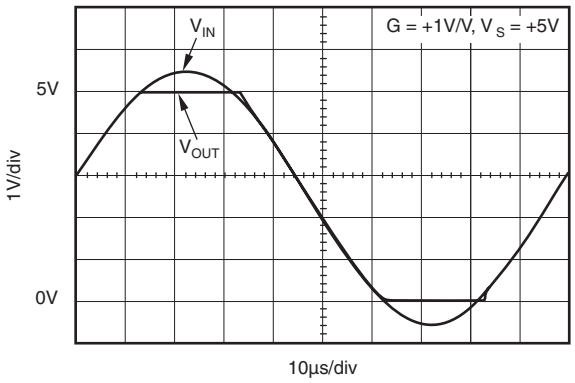


Figure 19. No Phase Inversion with Inputs Greater Than Power-Supply Voltage

Normally, input currents are 0.5 pA. However, large inputs (greater than 500 mV beyond the supply rails) can cause excessive current to flow in or out of the input pins. Therefore, limiting the input current to less than 10 mA is important as well as keeping the input voltage below the maximum rating. This limiting is easily accomplished with an input voltage resistor, as shown in Figure 20.

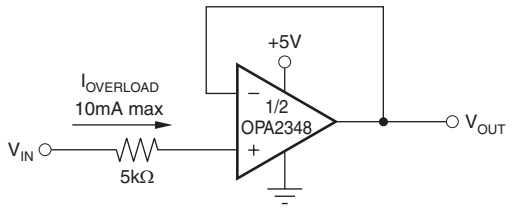


Figure 20. Input Current Protection for Voltages Exceeding the Supply Voltage

Feature Description (continued)

7.3.4 Input and ESD Protection

The OPAx348-Q1 family of devices incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table. Figure 21 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value should be kept to a minimum in noise-sensitive applications.

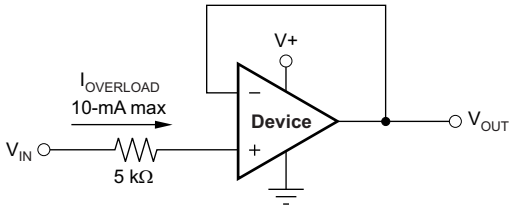


Figure 21. Input Current Protection

7.3.5 Common-Mode Rejection Ratio (CMRR)

CMRR for the OPAx348-Q1 family of devices is specified in several ways so the best match for a given application may be used; see the *Electrical Characteristics* table. First, the CMRR of the device in the common-mode range below the transition region [V_{CM} < (V+) – 1.3 V] is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at (V_{CM} = –0.2 V to 5.7 V). This last value includes the variations seen through the transition region (see Figure 22).

7.3.6 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx348-Q1 device extends 200 mV beyond the supply rails. This extended range is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.2 V to 300 mV above the positive supply, while the P-channel pair is on for inputs from 300 mV below the negative supply to approximately (V+) – 1.4 V. A small transition region exists, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region, shown in Figure 22, can vary ±300 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within the 200-mV transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

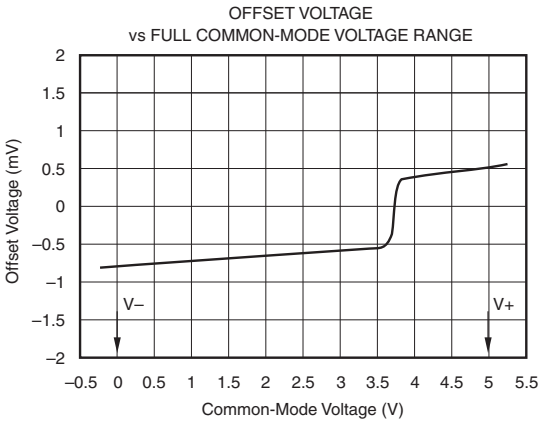


Figure 22. Behavior of Typical Transition Region at Room Temperature

Feature Description (continued)

7.3.7 EMI Susceptibility and Input Filtering

Op amps vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op amp, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op amp pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The OPAx348-Q1 family of devices incorporates an internal input, low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by this filter. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. Detailed information can also be found in the application report, *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

7.3.8 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the OPAx348-Q1 family of devices delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 10 kΩ, the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; refer to the graph, *Output Voltage Swing vs Output Current*.

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving 5-kΩ loads connected to any potential between V+ and ground. For light resistive loads (>100 kΩ), the output voltage can typically swing to within 18 mV from supply rail. With moderate resistive loads (10 kΩ to 50 kΩ), the output voltage can typically swing to within 100 mV of the supply rails while maintaining high open-loop gain (see Figure 6 in the *Typical Characteristics* section).

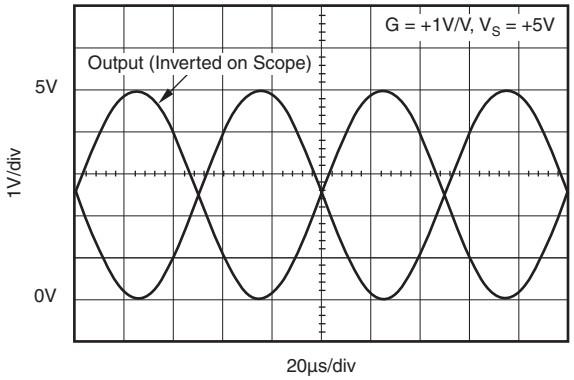


Figure 23. Rail-to-Rail I/O

Feature Description (continued)

7.3.9 Capacitive Load and Stability

The OPAx348-Q1 family of devices in a unity-gain configuration can directly drive up to 250-pF pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads (see Figure 13 in the *Typical Characteristics* section). In unity-gain configurations, capacitive load drive can be improved by inserting a small (10-Ω to 20-Ω) resistor, R_S, in series with the output, as shown in Figure 24. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if a resistive load exists in parallel with the capacitive load, a voltage divider is created, introducing a direct current (dc) error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S/R_L and is generally negligible.

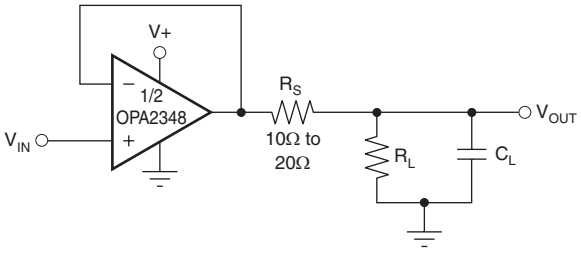


Figure 24. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive

In unity-gain inverter configuration, the phase margin can be reduced by the reaction between the capacitance at the op amp input and the gain setting resistors, thus degrading capacitive load drive. The best performance is achieved by using small-valued resistors. For example, when driving a 500-pF load, reducing the resistor values from 100 kΩ to 5 kΩ decreases overshoot from 55% to 13% (see Figure 13 in the *Typical Characteristics* section). However, when large-valued resistors cannot be avoided, a small (4-pF to 6-pF) capacitor, C_{FB}, can be inserted in the feedback loop, as shown in Figure 25. This small capacitor significantly reduces overshoot by compensating the effect of capacitance, C_{IN}, which includes the input capacitance of the amplifier and printed circuit board (PCB) parasitic capacitance.

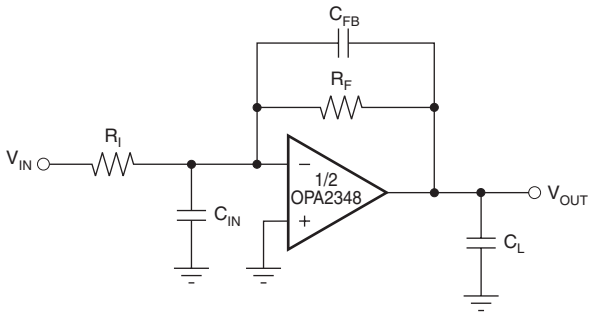


Figure 25. Improving Capacitive Load Drive

7.4 Device Functional Modes

The OPAx348-Q1 family of devices is powered on when the supply is connected. The device can be operated as a single-supply operational amplifier or a dual-supply amplifier, depending on the application.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx348-Q1 operational amplifiers (op amps) are unity-gain stable and suitable for a wide range of general-purpose applications.

The OPAx348-Q1 device features wide bandwidth and unity-gain stability with rail-to-rail input and output for increased dynamic range. Figure 23 shows the input and output waveforms for the OPAx348-Q1 device in unity-gain configuration. Operation is from a single 5-V supply with a 100-kΩ load connected to V_S / 2. The input is a 5-V_{PP} sinusoid. Output voltage is approximately 4.98 V_{PP}.

The power-supply pins should be bypassed with 0.01-µF ceramic capacitors.

8.1.1 Driving Analog-to-Digital Converters (ADCs)

The OPAx348-Q1 op amps are optimized for driving medium-speed sampling ADCs. The OPAx348-Q1 op amps buffer the ADC input capacitance and resulting charge injection while providing signal gain.

Figure 26 shows the OPA2348 in a basic noninverting configuration driving the ADS7822 device. The ADS7822 device is a 12-bit, micropower sampling converter in the MSOP-8 package. When used with the low-power miniature packages of the OPAx348-Q1 family of devices, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the ADC input can be used to provide for anti-aliasing filtering and charge injection current.

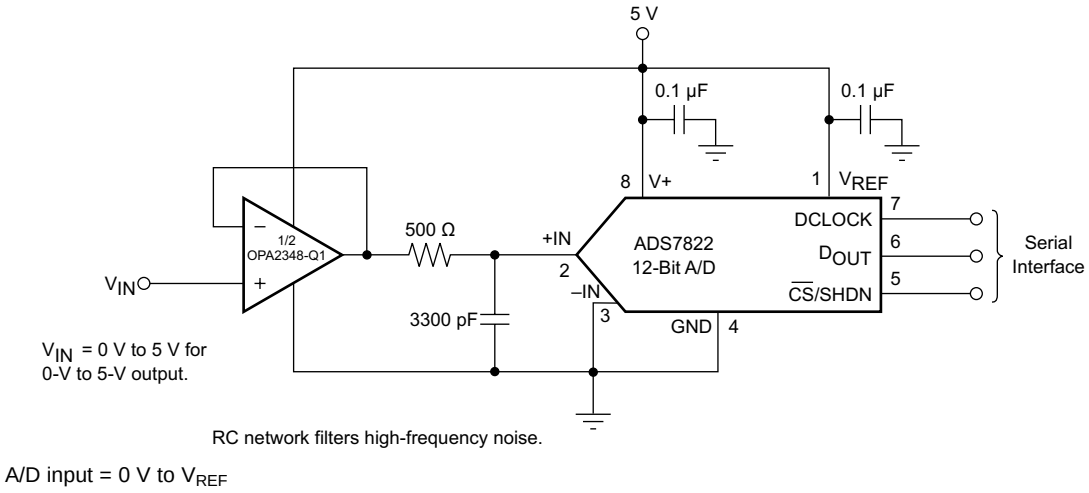
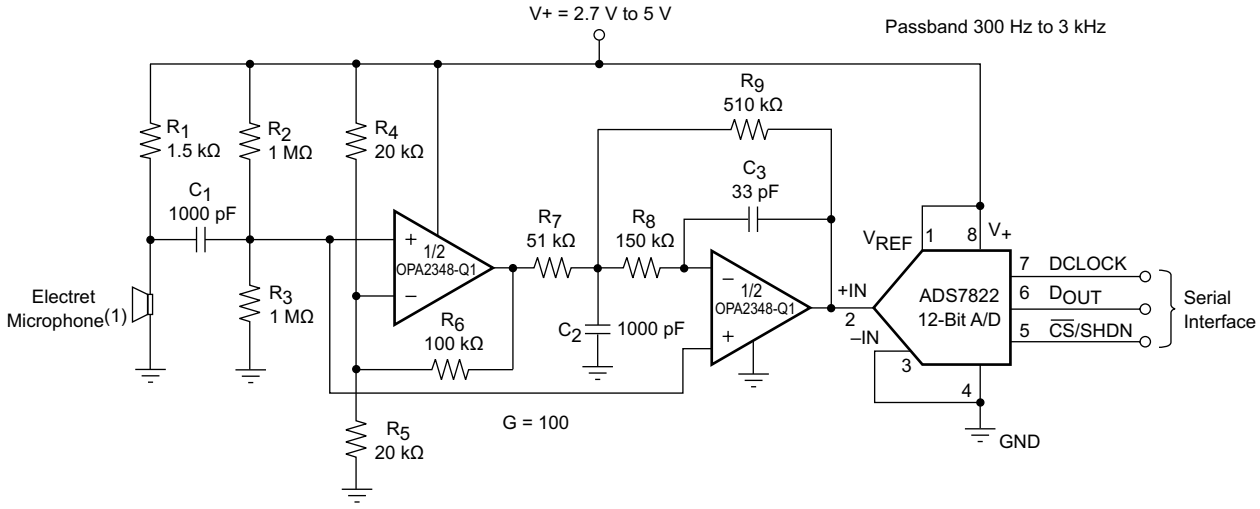


Figure 26. Noninverting Configuration Driving ADS7822

The OPAx348-Q1 family of devices can also be used in noninverting configuration to drive the ADS7822 device in limited low-power applications. In this configuration, an RC network at the ADC input can be used to provide for anti-aliasing filtering and charge injection current. See Figure 26 for the OPAx348-Q1 driving an ADS7822 device in a speech bandpass filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit operates with V_S = 2.7 V to 5 V with less than 250-µA typical quiescent current.

Application Information (continued)



(1) Electret microphone powered by R_1.

Figure 27. Speech Bandpass Filtered Data Acquisition System

8.2 Typical Application

Some applications require differential signals. Figure 28 shows a simple circuit to convert a single-ended input of 0.1 V to 2.4 V into a differential output of ±2.3 V on a single 2.7-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier functions as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate $V_{OUT–}$. Both V_{OUT+} and $V_{OUT–}$ range from 0.1 V to 2.4 V. The difference, V_{DIFF}, is the difference between V_{OUT+} and $V_{OUT–}$. This configuration makes the differential output voltage range to be 2.3 V.

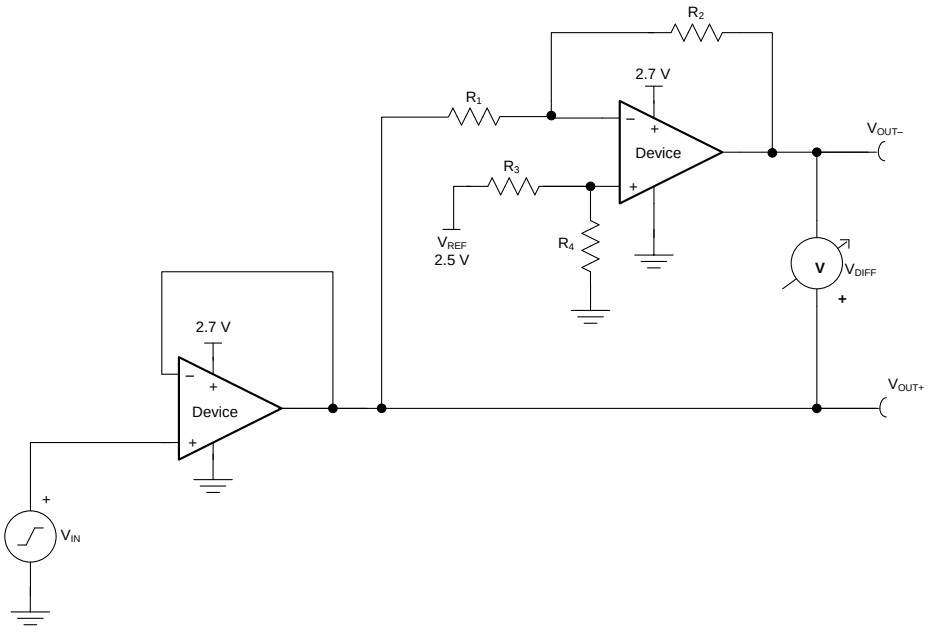


Figure 28. Schematic for a Single-Ended Input to Differential Output Conversion

Typical Application (continued)

8.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 2.7 V
- Reference voltage: 2.5 V
- Input: 0.1 V to 2.4 V
- Output differential: ±2.3 V
- Output common-mode voltage: 1.25 V
- Small-signal bandwidth: 1 MHz

8.2.2 Detailed Design Procedure

The circuit in Figure 28 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and V_{OUT-} using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (as shown in Equation 1). V_{OUT-} is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for V_{OUT-} is given in Equation 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT-} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) - V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

The differential output signal, V_{DIFF}, is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-}. Equation 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to V_{REF}. The differential output range is 2 × V_{REF}. Furthermore, the common-mode voltage (V_{CM}) is one half of V_{REF} (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) \tag{3}$$

$$V_{OUT+} = V_{IN} \tag{4}$$

$$V_{OUT-} = V_{REF} - V_{IN} \tag{5}$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \tag{6}$$

$$V_{CM} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2} V_{REF} \tag{7}$$

8.2.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common-mode input range and output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design, so the OPAx348-Q1 family of devices is selected because its bandwidth is greater than the target of 1 MHz. The bandwidth and power ratio makes this device power-efficient, and the low offset and drift ensure good accuracy for moderate precision applications.

8.2.2.2 Passive Component Selection

Because the transfer function of V_{OUT-} relies heavily upon resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design uses resistors with resistance values of 49.9 kΩ and tolerances of 0.1%. However, if the noise of the system is a key parameter, smaller resistance values (6 kΩ or lower) can be selected to keep the overall system noise low. This technique ensures that the noise from the resistors is lower than the amplifier noise.

Typical Application (continued)

8.2.3 Application Curves

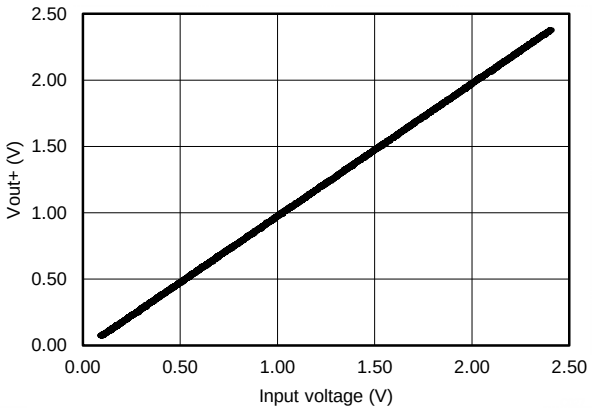


Figure 29. V_{OUT+} vs Input Voltage

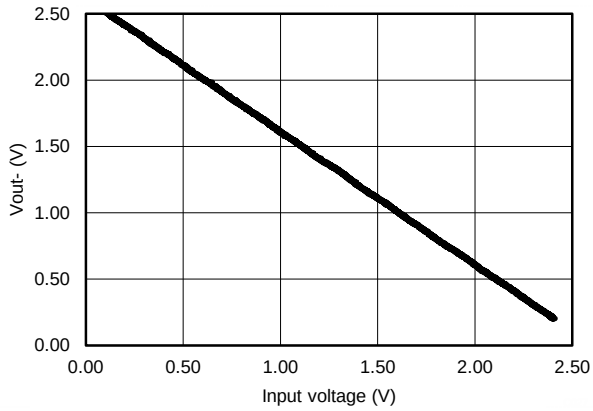


Figure 30. V_{OUT-} vs Input Voltage

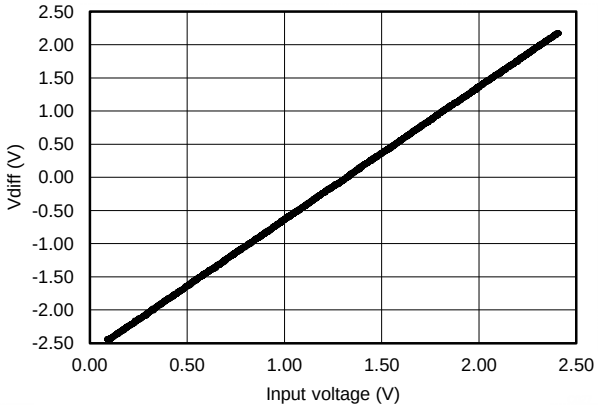


Figure 31. V_{DIFF} vs Input Voltage

9 Power Supply Recommendations

The OPAx348-Q1 family of devices is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines* section.

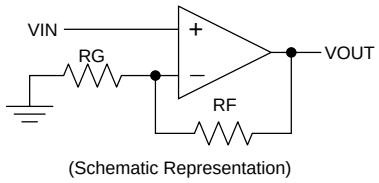
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep RF and RG close to the inverting input to minimize parasitic capacitance, as shown in Figure 32.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example



(Schematic Representation)

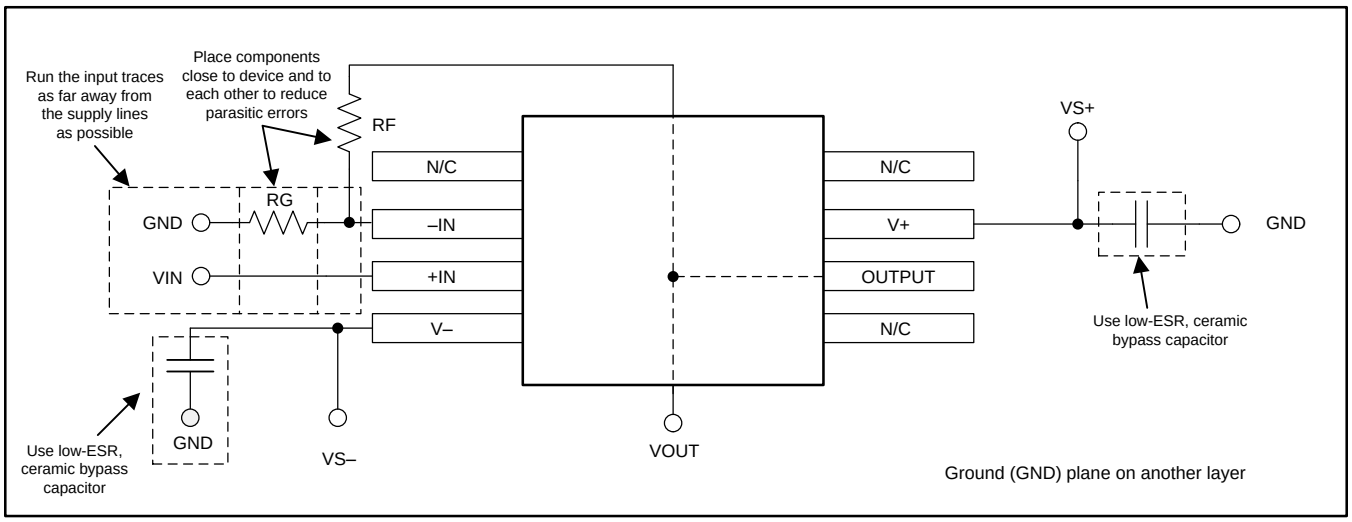


Figure 32. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- ADS7822: 12-Bit, 200kHz, microPower Sampling Analog-to-Digital Converter, SBAS062
- Application report: *Circuit Board Layout Techniques*, SLOA089
- Application report: *EMI Rejection Ratio of Operational Amplifiers*, SBOA128

11.2 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA348-Q1	Click here	Click here	Click here	Click here	Click here
OPA2348-Q1	Click here	Click here	Click here	Click here	Click here
OPA4348-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2348AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2348Q	Samples
OPA348AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A48	Samples
OPA348AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	348Q1	Samples
OPA4348AQPWRQ1	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	OP4348Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA2348-Q1, OPA348-Q1, OPA4348-Q1 :

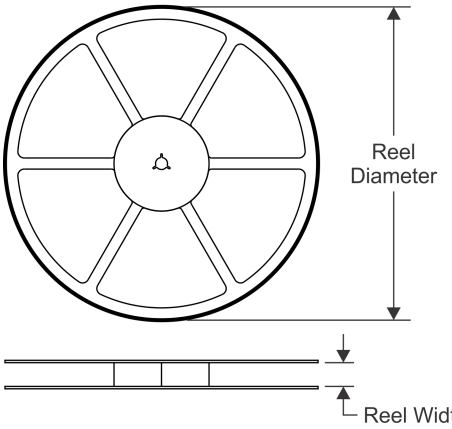
- Catalog: OPA2348, OPA348, OPA4348

NOTE: Qualified Version Definitions:

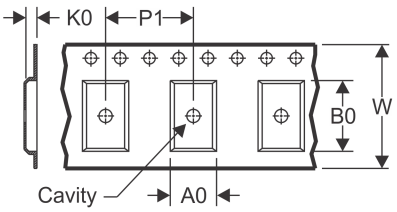
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

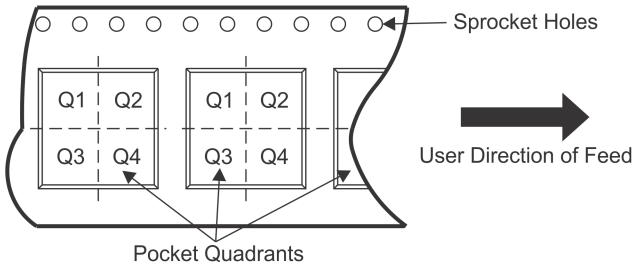


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

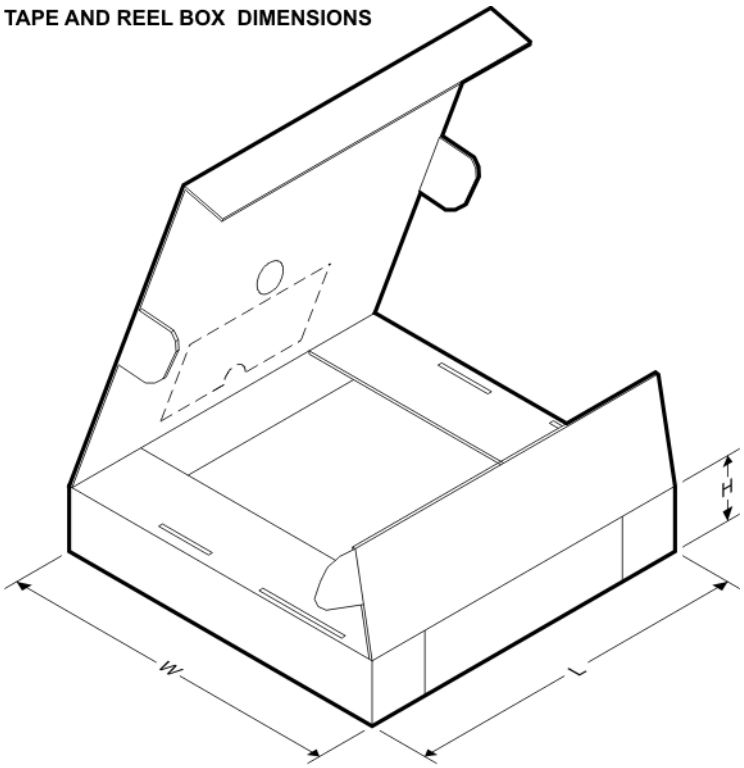
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2348AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA348AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA348AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4348AQPWRQ1	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

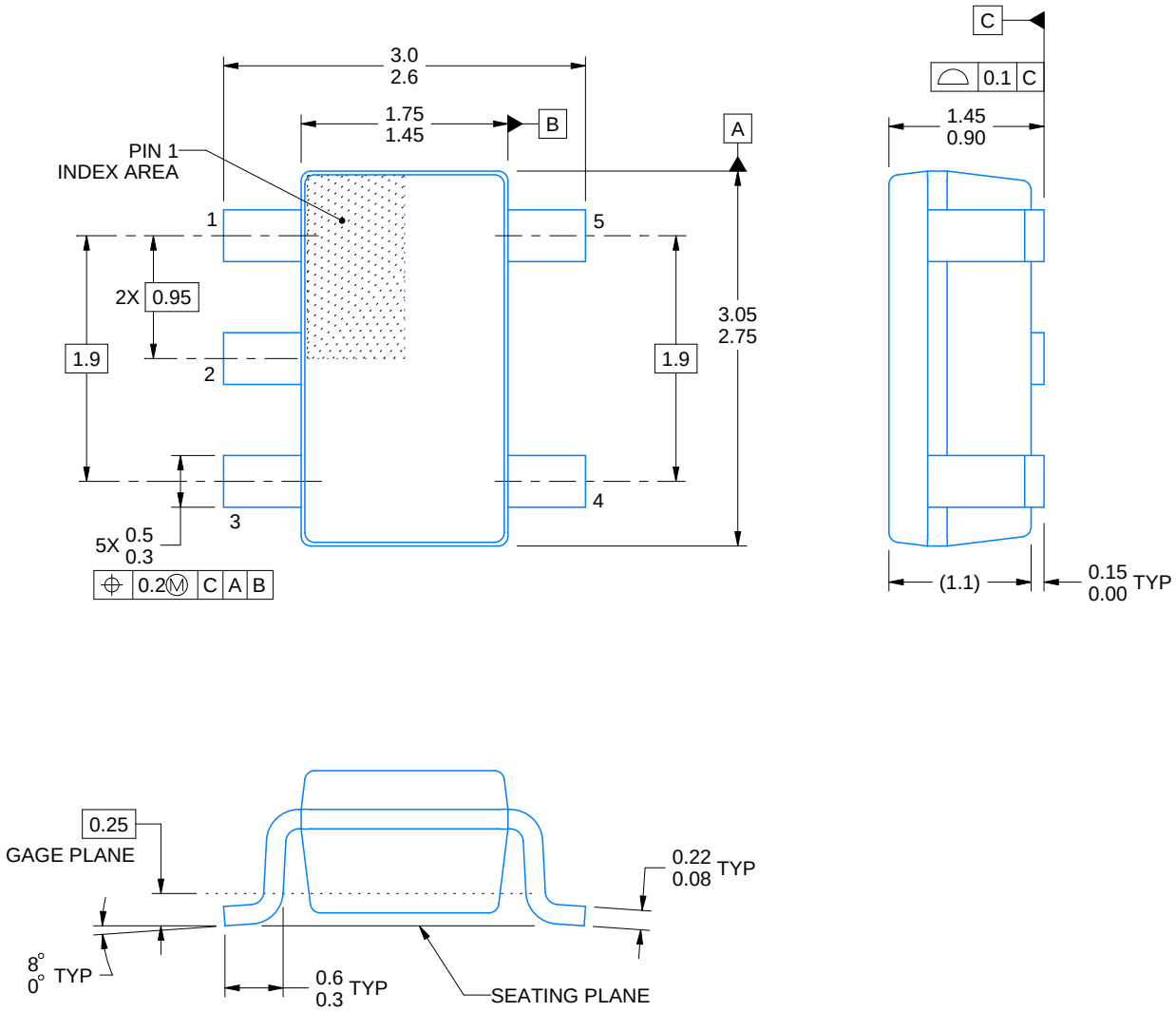
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2348AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
OPA348AQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA348AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
OPA4348AQPWRQ1	TSSOP	PW	14	2500	367.0	367.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

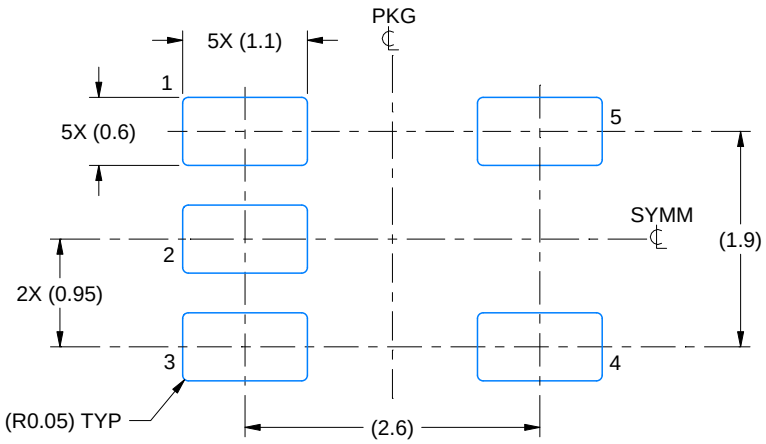
SMALL OUTLINE TRANSISTOR



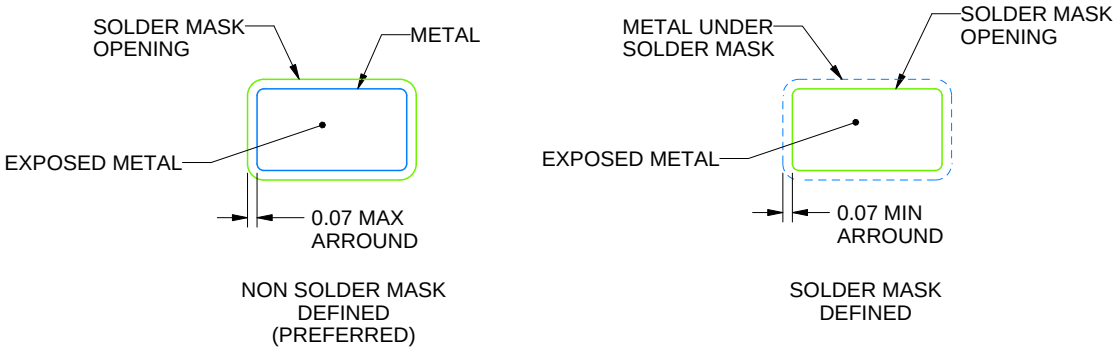
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

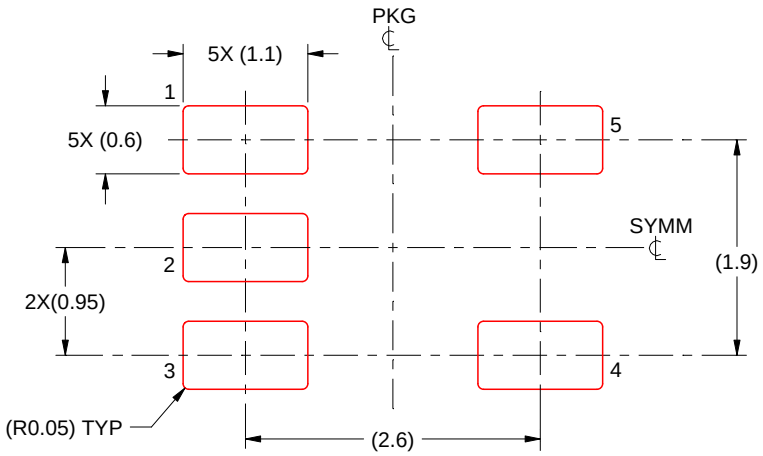


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



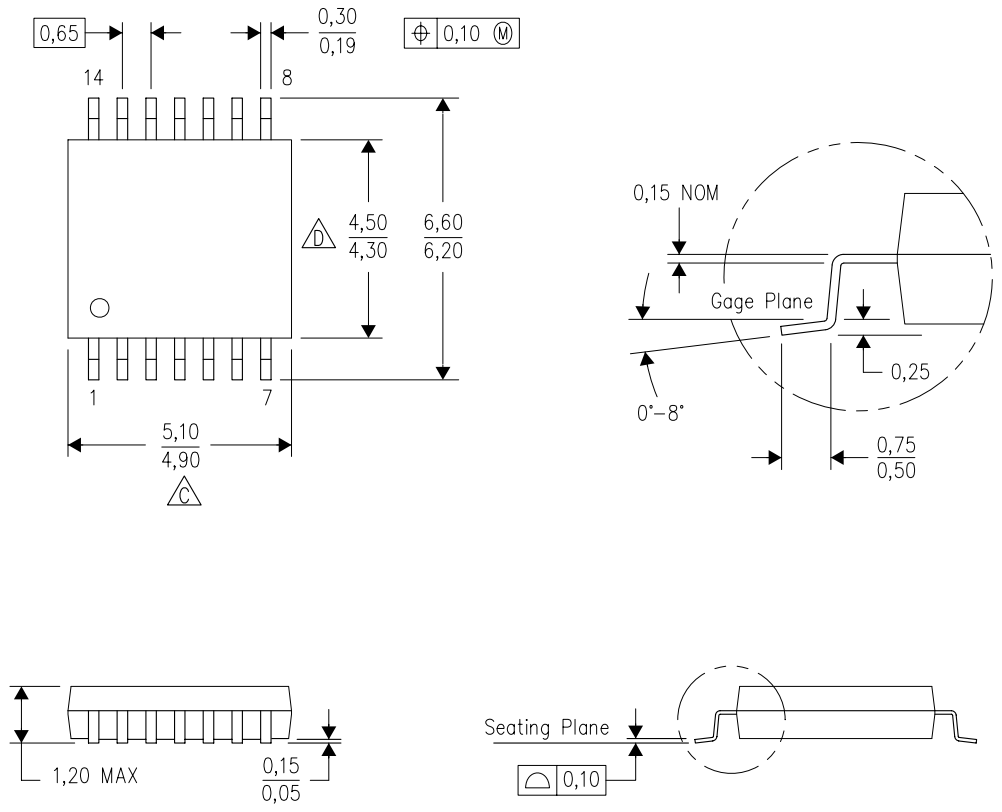
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

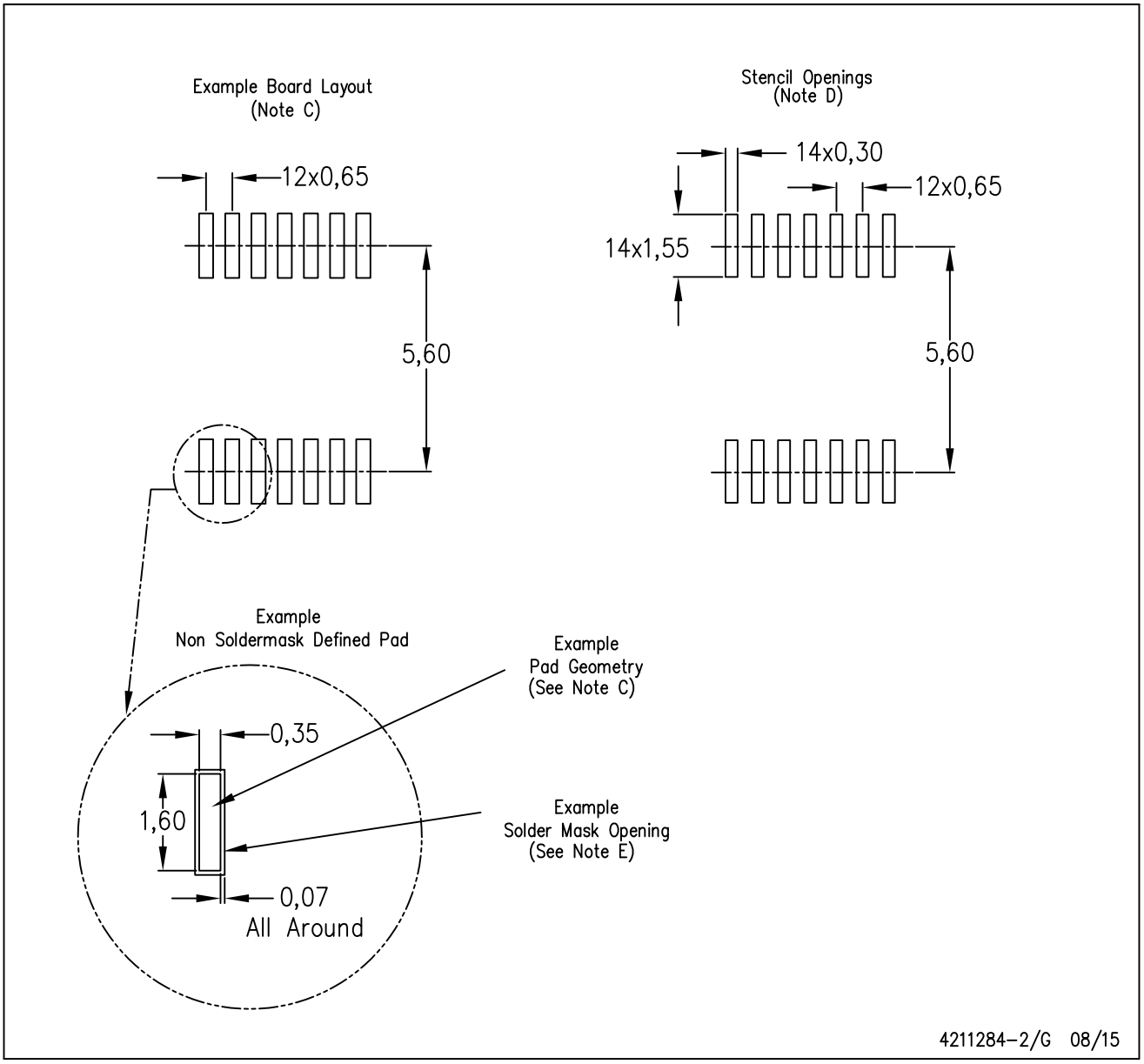
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



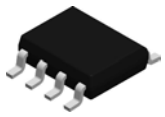
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

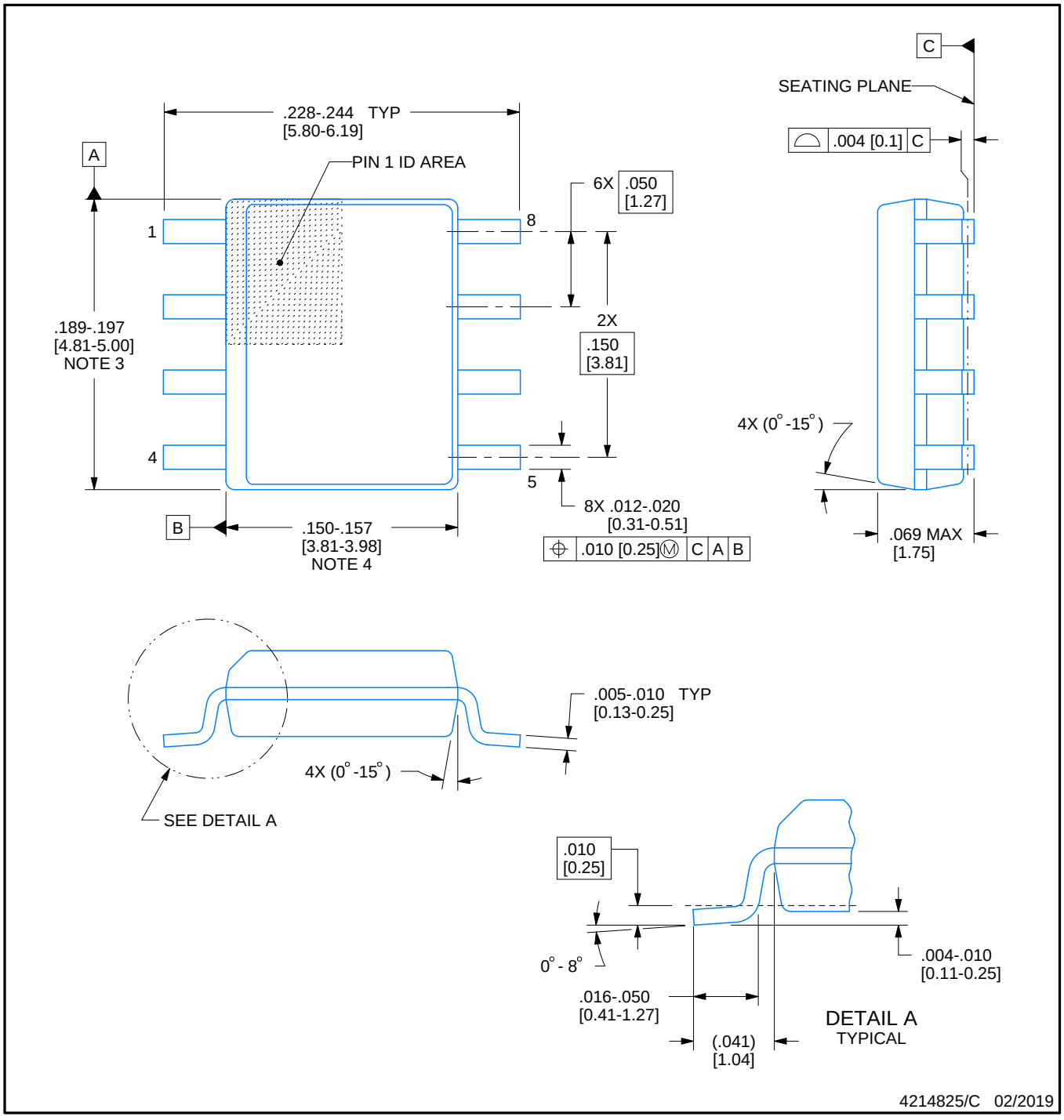


PACKAGE OUTLINE

D0008A

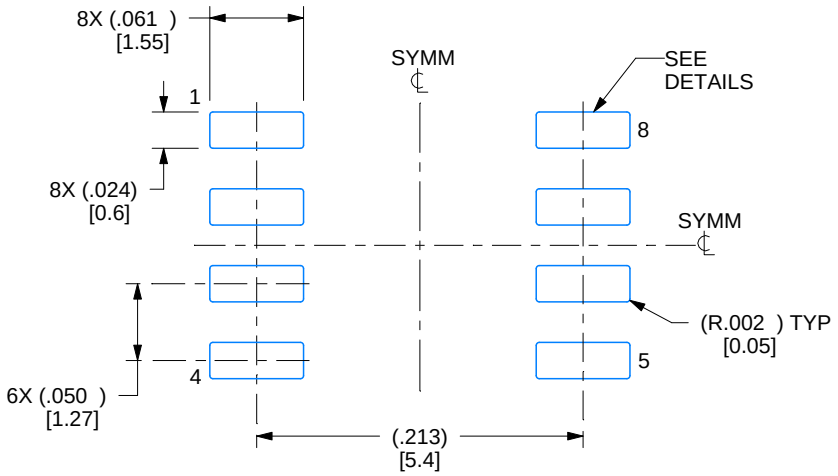
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

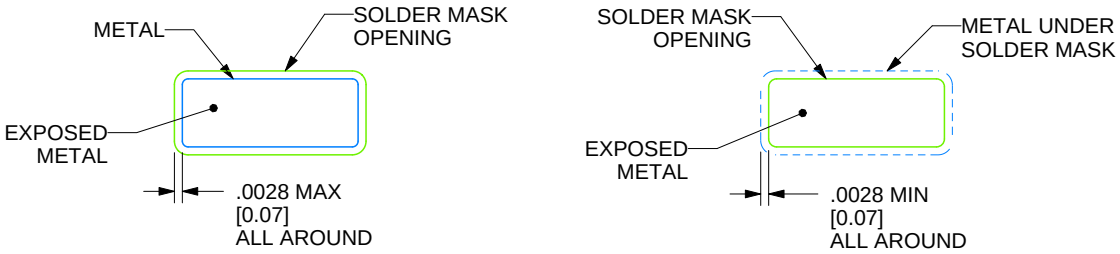


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

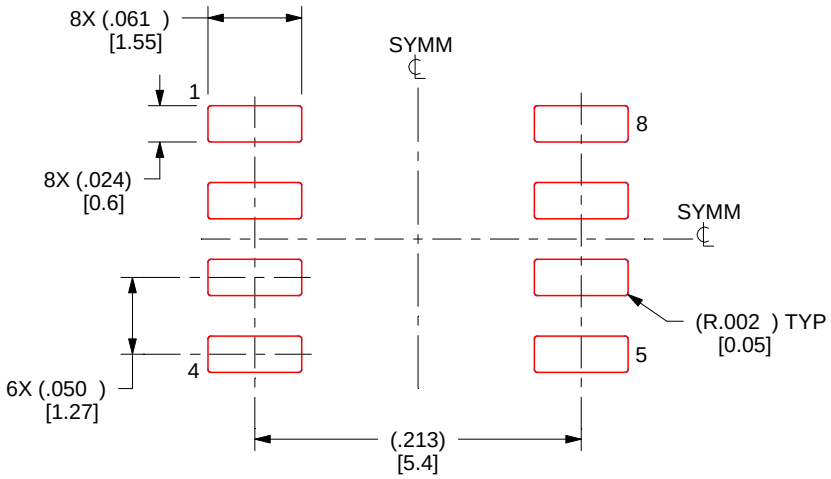
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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