PESD3V3S1BL

Low capacitance bidirectional ESD protection diode

31 May 2017 Product data sheet

1. General description

Low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a leadless ultra small SOD882 (DFN1006-2) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Bidirectional ESD protection of one line
- Ultra small SMD plastic package
- Reverse standoff voltage V_{RWM} = 3.3 V
- Low clamping voltage: V_{CL} = 9.3 V @ 15 A 8/20 µs
- Ultra low leakage current: I_{RM} < 1 nA
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); I_{PPM} = 15 A
- IEC 61000-4-5 (surge); I_{PPM} = 17.5 A (average measured)
- AEC-Q101 qualified

3. Applications

ESD and surge protection for:

- very sensitive interface lines
- generic interface lines

in portable electronics, communication, consumer and computing devices.

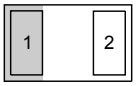
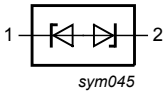
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	3.3	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	35	40	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view **DFN1006-2 (SOD882)**	
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD3V3S1BL	DFN1006-2	plastic, leadless ultra small package; 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.48 mm body	SOD882

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD3V3S1BL	F1

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	t_p = 8/20 µs	[1]	-	15	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2] [3]	-	30	kV

[1] According to IEC 61000-4-5.
[2] Device stressed with ten non-repetitive ESD pulses.
[3] Measured from pin 1 to pin 2.

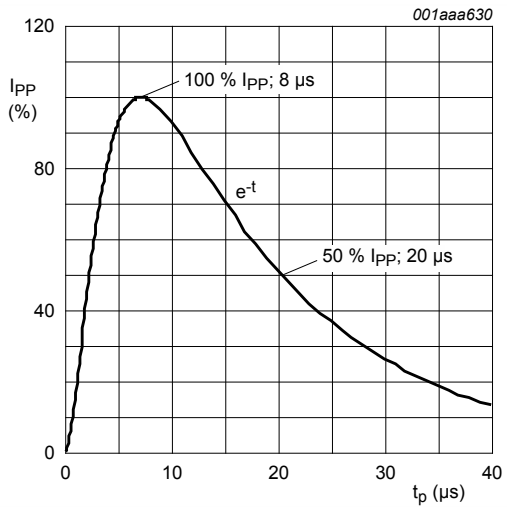


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

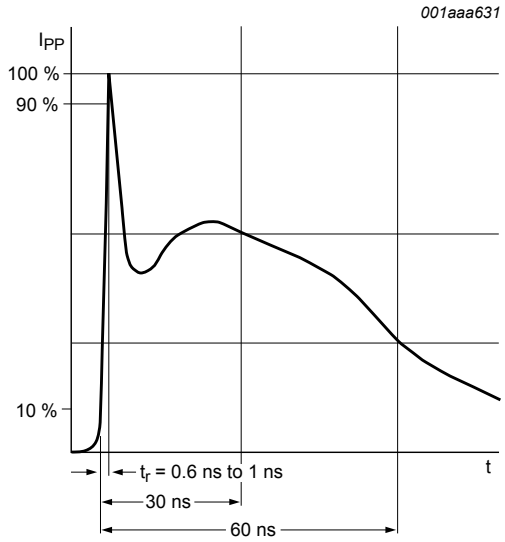


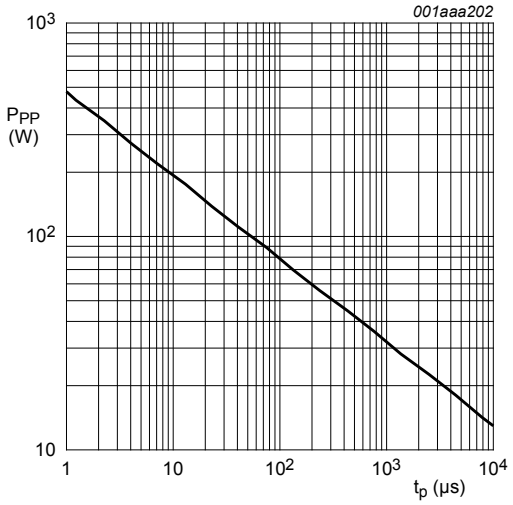
Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	3.3	V
V_{BR}	breakdown voltage	I_R = 1 mA; T_{amb} = 25 °C		4.5	-	-	V
I_R	reverse current	T_{amb} = 25 °C		-	1	-	A
I_{RM}	reverse leakage current	V_{RWM} = 3.3 V; T_{amb} = 25 °C		-	1	100	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	35	40	pF
V_{CL}	clamping voltage	I_{PP} = 1 A; T_{amb} = 25 °C	[1] [2]	-	6.5	-	V
		I_{PP} = 15 A	[1] [2]	-	9.3	11.5	V
R_{dyn}	dynamic resistance	I_R = 10 A; T_{amb} = 25 °C	[3] [2]	-	0.1	-	Ω
		I_R = -10 A	[3] [2]	-	0.15	-	Ω

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[2] Measured from pin 1 to pin 2.
[3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.



T_{amb} = 25 °C

Fig. 3. Peak pulse power as a function of exponential pulse duration; typical values

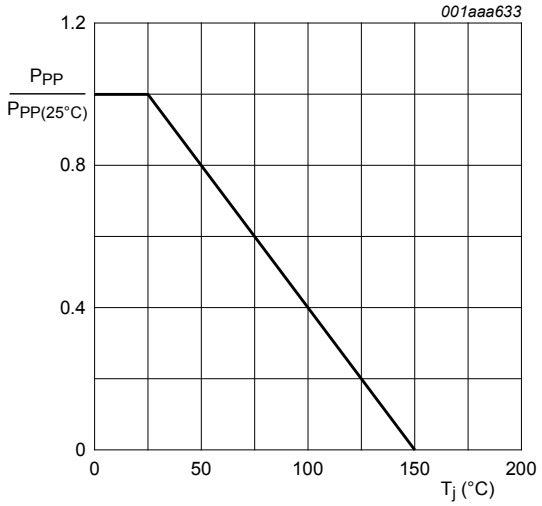
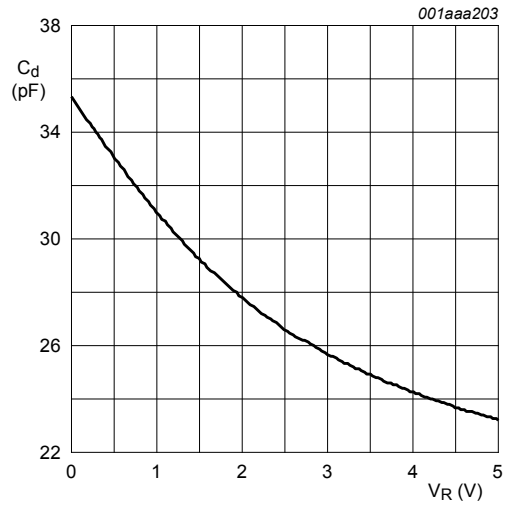


Fig. 4. Relative variation of peak pulse power as a function of junction temperature; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig. 5. Diode capacitance as a function of reverse voltage; typcial values

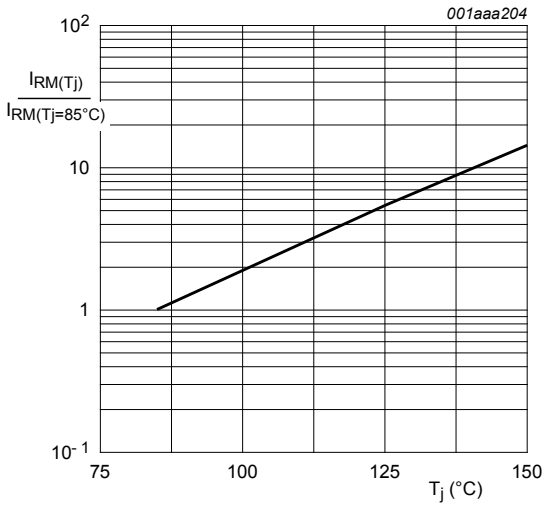


Fig. 6. Relative variation of reverse leakage current as a function of junction temperature; typical values

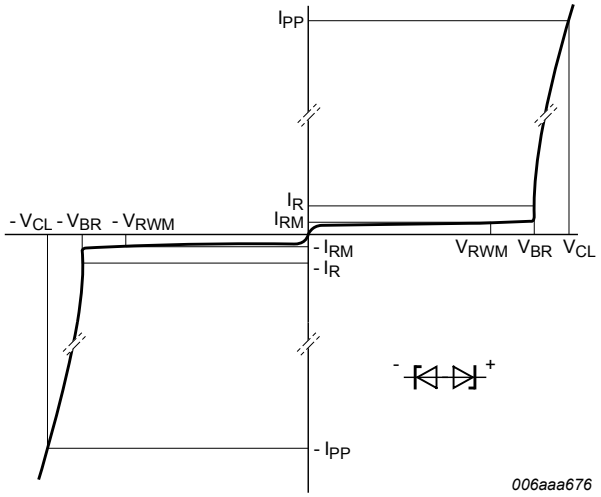


Fig. 7. V-I characteristics for a bidirectional ESD protection diode

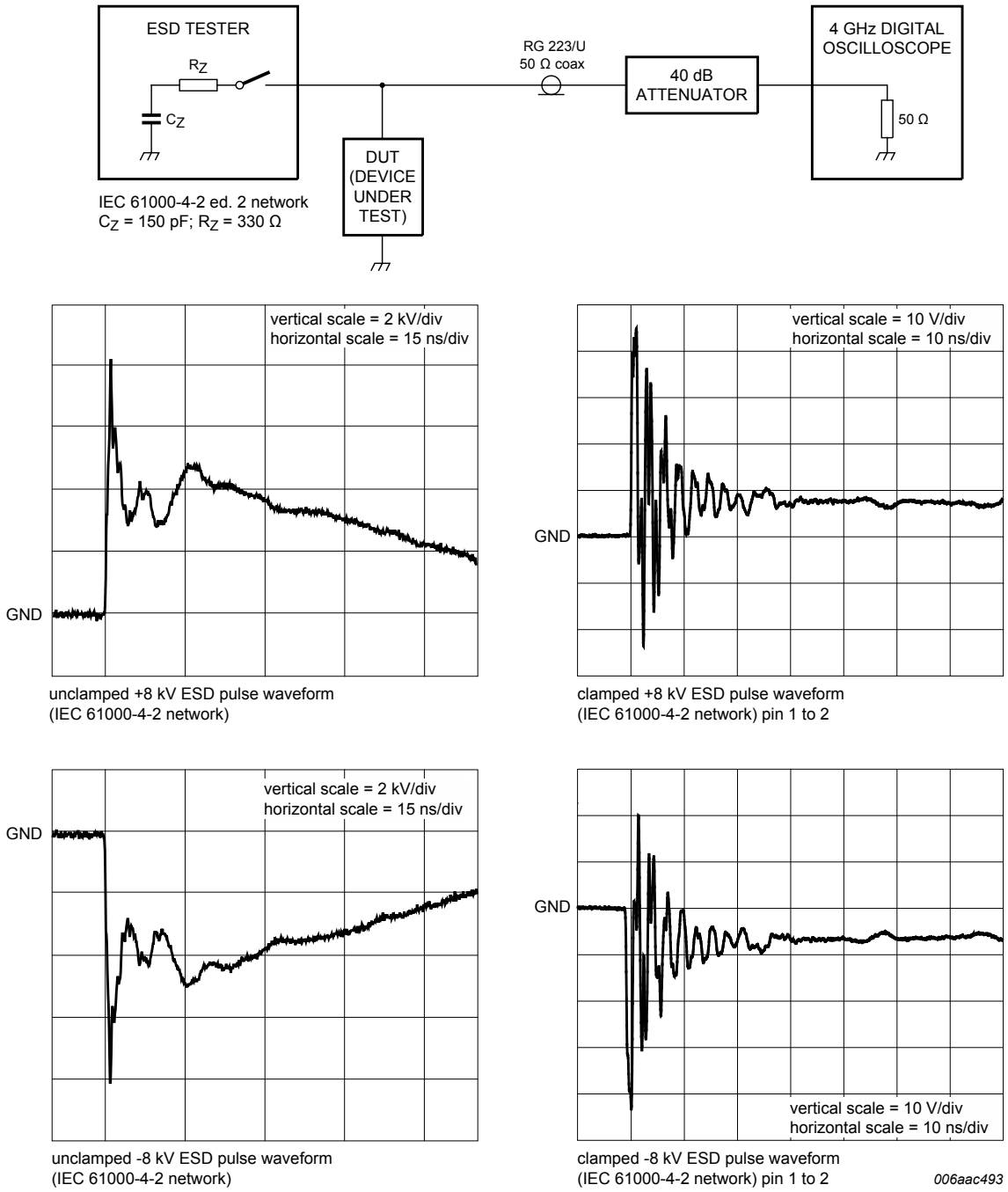
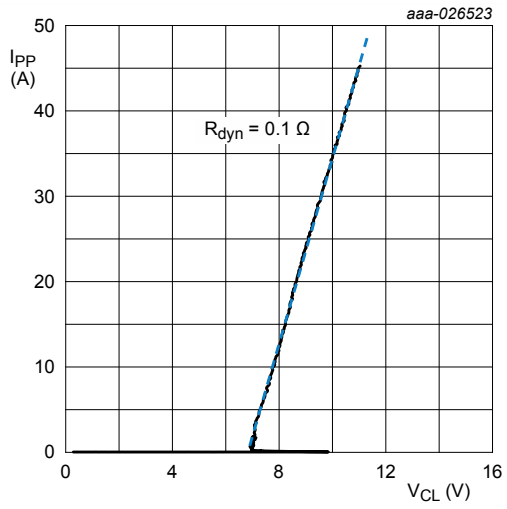
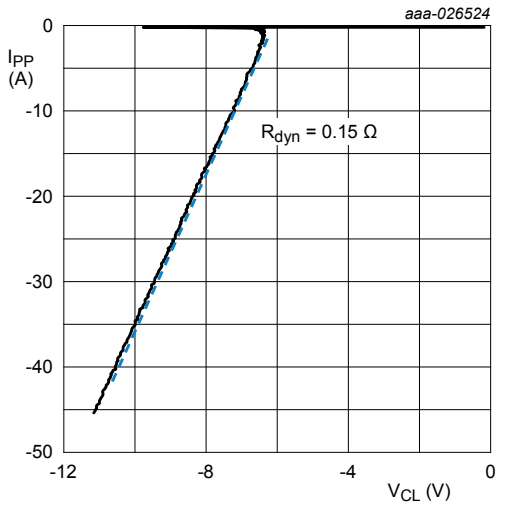


Fig. 8. ESD clamping test setup and waveforms



Transmission Line Pulse (TLP) = 100 ns

Fig. 9. Dynamic resistance with positive clamping; typical values



Transmission Line Pulse (TLP) = 100 ns

Fig. 10. Dynamic resistance with negative clamping; typical values

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

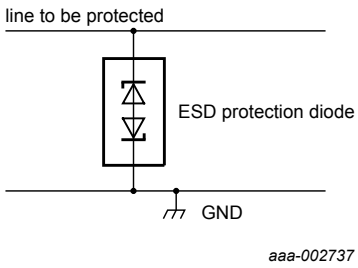


Fig. 11. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

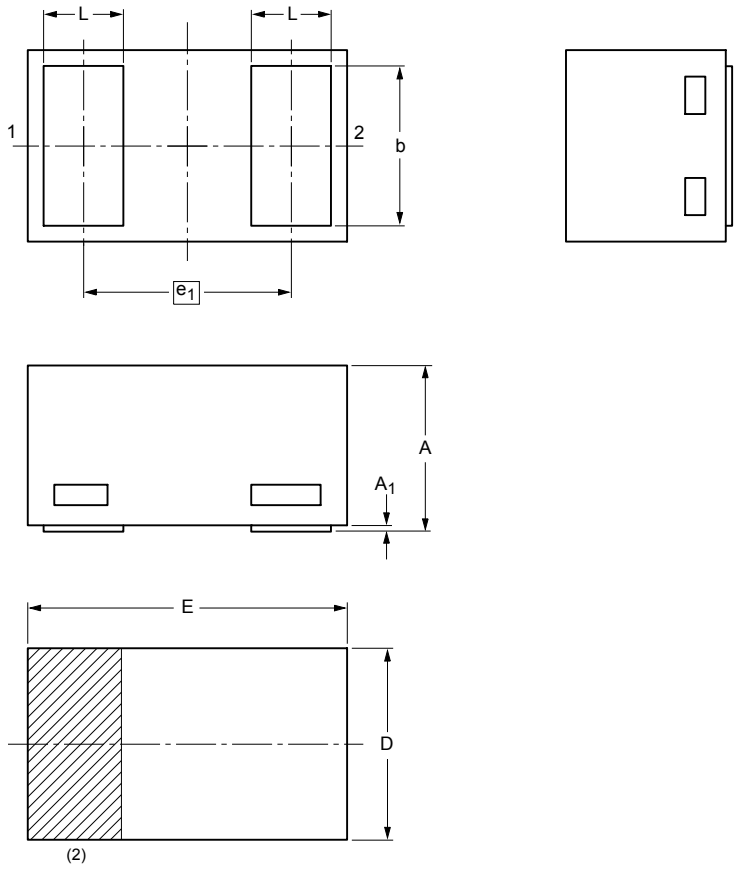
11. Test information

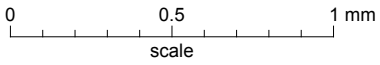
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

DFN1006-2: Leadless ultra small plastic package; 2 terminals; body 1.0 x 0.6 x 0.5 mm **SOD882**





Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	D	E	e_1	L
mm	max	0.50	0.03	0.55	0.62	1.02		0.30
	nom						0.65	
	min	0.46		0.47	0.55	0.95		0.22

Note
1. Including plating thickness
2. The marking bar indicates the cathode (if applicable)

sod882_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD882						~~14-08-26~~ 14-08-27

Fig. 12. Package outline DFN1006-2 (SOD882)

13. Soldering

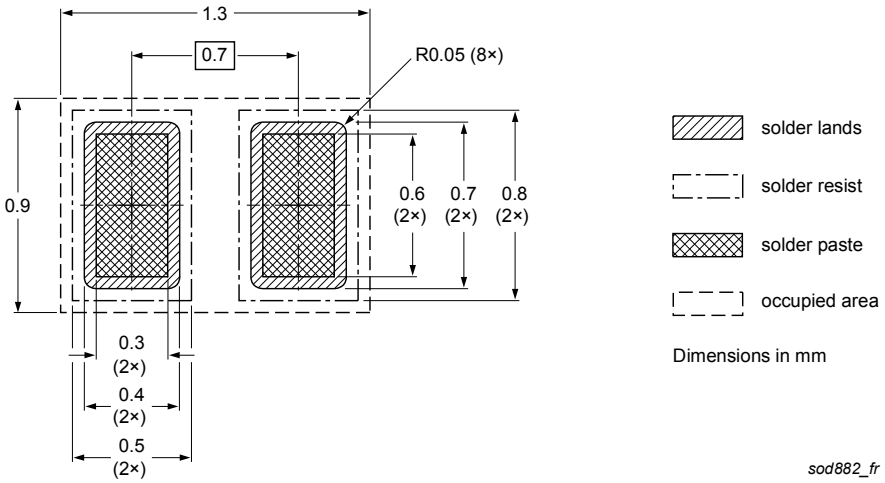


Fig. 13. Reflow soldering footprint for DFN1006-2 (SOD882)

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD3V3S1BL v.1	20170531	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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