



# PESD3V3Y1BSF

## Extremely low capacitance bidirectional ESD protection diode

29 March 2019

Product data sheet

## 1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS protection family. This device is housed in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

## 2. Features and benefits

- Bidirectional ESD protection of one line
- Extremely low trigger-voltage  $V_{t1}$  of 7 V TLP
- Extremely low diode capacitance  $C_d = 0.24$  pF
- Extremely low clamping voltage to protect sensitive I/Os
- Extremely low-inductance protection path to ground
- ESD protection up to  $\pm 15$  kV according to IEC 61000-4-2
- Ultra small SMD package

## 3. Applications

- USB 3.2, HDMI2, and Universal Flash Storage (UFS) data lines
- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals

## 4. Quick reference data

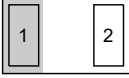
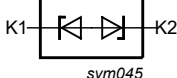
Table 1. Quick reference data

| Symbol    | Parameter                | Conditions                                  |     | Min | Typ  | Max  | Unit |
|-----------|--------------------------|---|-----|-----|------|------|------|
| $C_d$     | diode capacitance        | $f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C | [1] | -   | 0.24 | 0.29 | pF   |
| $V_{RWM}$ | reverse standoff voltage |   |     | -   | -    | 3.3  | V    |

[1] Guaranteed by design.

## 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description       | Simplified outline   | Graphic symbol   |
|-----|--------|-------------------|--|--|
| 1   | K1     | cathode (diode 1) |  <p>Transparent<br/>top view</p> <p><b>DSN0603-2 (SOD962-2)</b></p> |  <p><i>sym045</i></p> |
| 2   | K2     | cathode (diode 2) |  |  |

## 6. Ordering information

Table 3. Ordering information

| Type number  | Package   |   |          |
|--------------|-----------|---|----------|
|              | Name      | Description   | Version  |
| PESD3V3Y1BSF | DSN0603-2 | silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body | SOD962-2 |

## 7. Marking

Table 4. Marking codes

| Type number  | Marking code |
|--------------|--------------|
| PESD3V3Y1BSF | C5           |

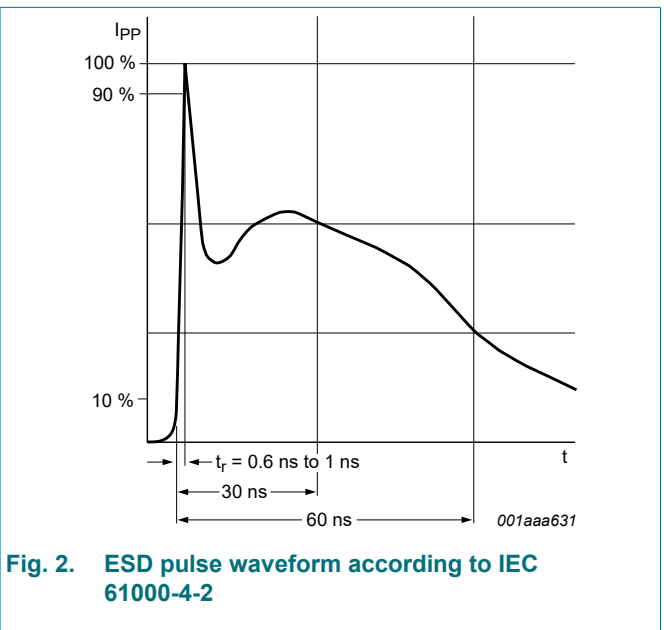
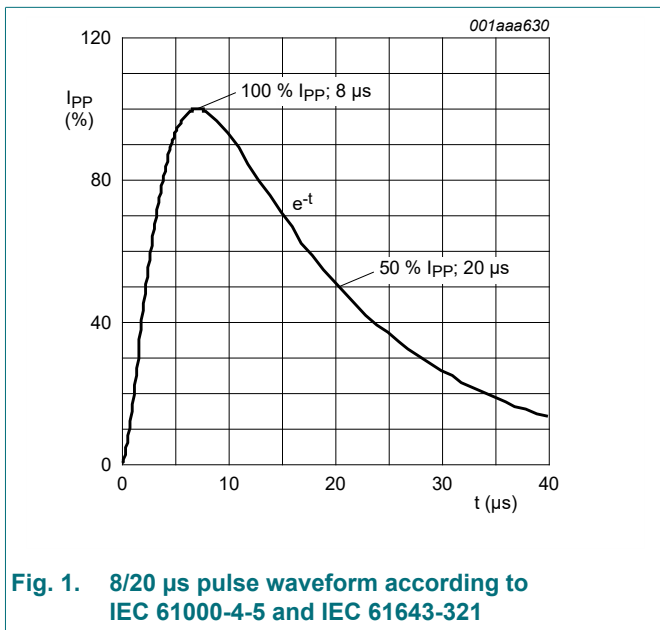
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                     | Parameter                       | Conditions                       |     | Min | Max | Unit |
|----------------------------|---------------------------------|----------------------------------|-----|-----|-----|------|
| $V_{RWM}$                  | reverse standoff voltage        |                                  |     | -   | 3.3 | V    |
| $T_{amb}$                  | ambient temperature             |                                  |     | -40 | 125 | °C   |
| $T_{stg}$                  | storage temperature             |                                  |     | -65 | 150 | °C   |
| <b>ESD maximum ratings</b> |                                 |                                  |     |     |     |      |
| $V_{ESD}$                  | electrostatic discharge voltage | IEC 61000-4-2; contact discharge | [1] | -15 | 15  | kV   |
|                            |                                 | IEC 61000-4-2; air discharge     | [1] | -15 | 15  | kV   |

[1] Device stressed with ten non-repetitive ESD pulses.



## 9. Characteristics

Table 6. Characteristics

| Symbol     | Parameter               | Conditions  | Min | Typ  | Max  | Unit     |
|------------|-------------------------|---|-----|------|------|----------|
| $V_{BR}$   | breakdown voltage       | $I_R = 1 \text{ mA}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$                      | 4.2 | 6.2  | 8    | V        |
| $I_{RM}$   | reverse leakage current | $V_{RWM} = 3.3 \text{ V}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$                 | -   | 1    | 50   | nA       |
| $C_d$      | diode capacitance       | $f = 1 \text{ MHz}$ ; $V_R = 0 \text{ V}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$ | [1] | 0.24 | 0.29 | pF       |
| $V_{CL}$   | clamping voltage        | $I_{PPM} = 4 \text{ A}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$                   | [2] | 3.7  | -    | V        |
| $R_{dyn}$  | dynamic resistance      | $I_R = 10 \text{ A}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$                      | [3] | 0.25 | -    | $\Omega$ |
|            |                         | $I_R = -10 \text{ A}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$                     | [3] | 0.25 | -    | $\Omega$ |
| $f_{-3dB}$ | -3 dB cut-off frequency | $T_{amb} = 25 \text{ }^\circ\text{C}$ ; normalized to attenuation at 1 MHz        | -   | 19.6 | -    | GHz      |

- [1] Guaranteed by design.
- [2] Device stressed with 8/20  $\mu\text{s}$  exponential decay waveform according to IEC 61000-4-5.
- [3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.1-2008.

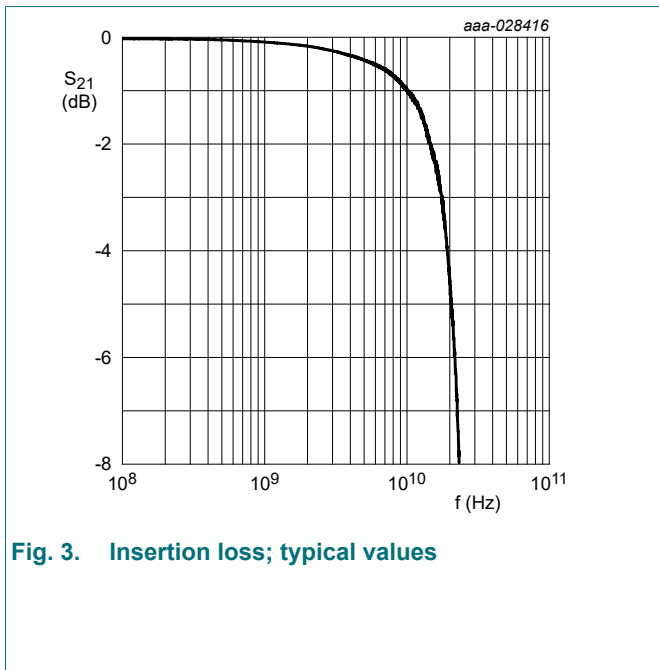


Fig. 3. Insertion loss; typical values

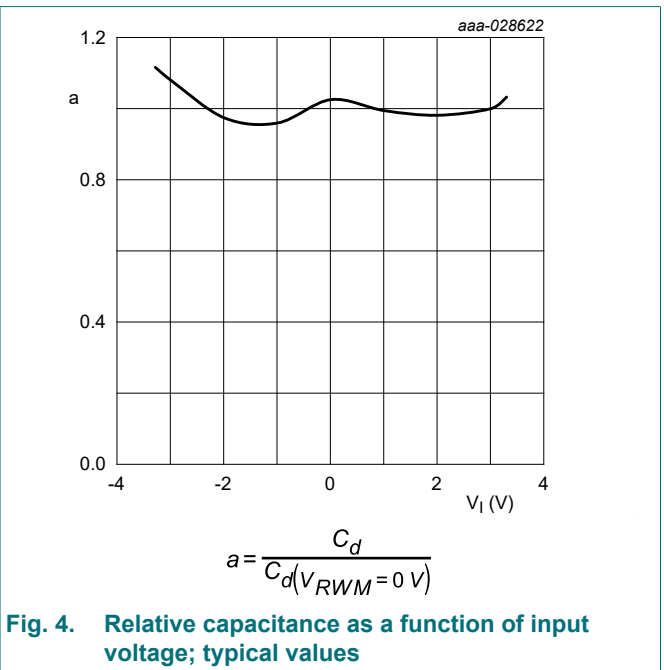
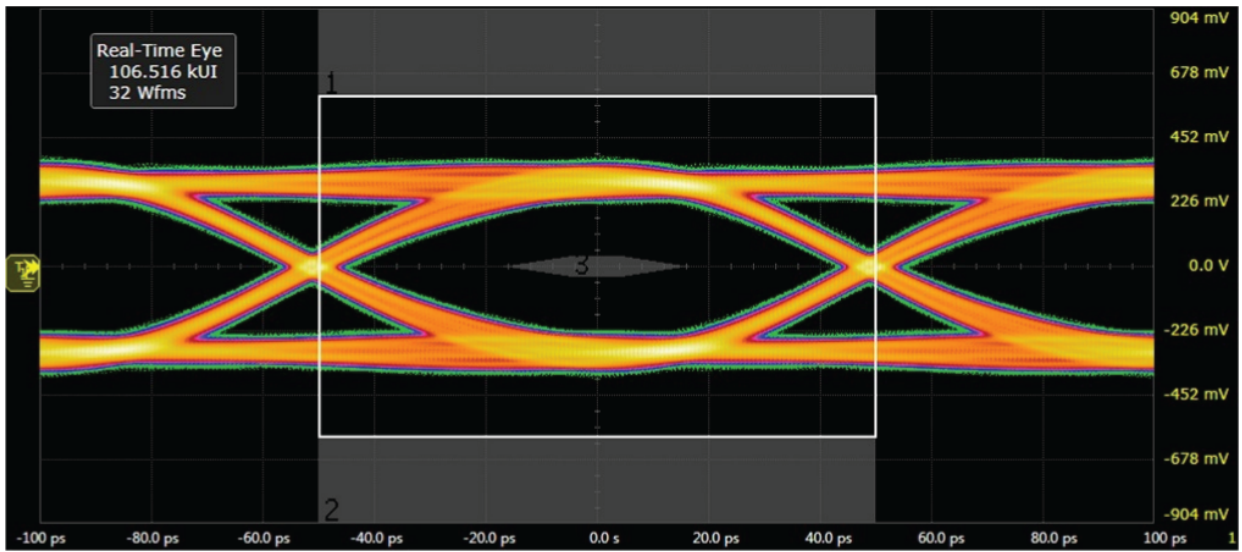


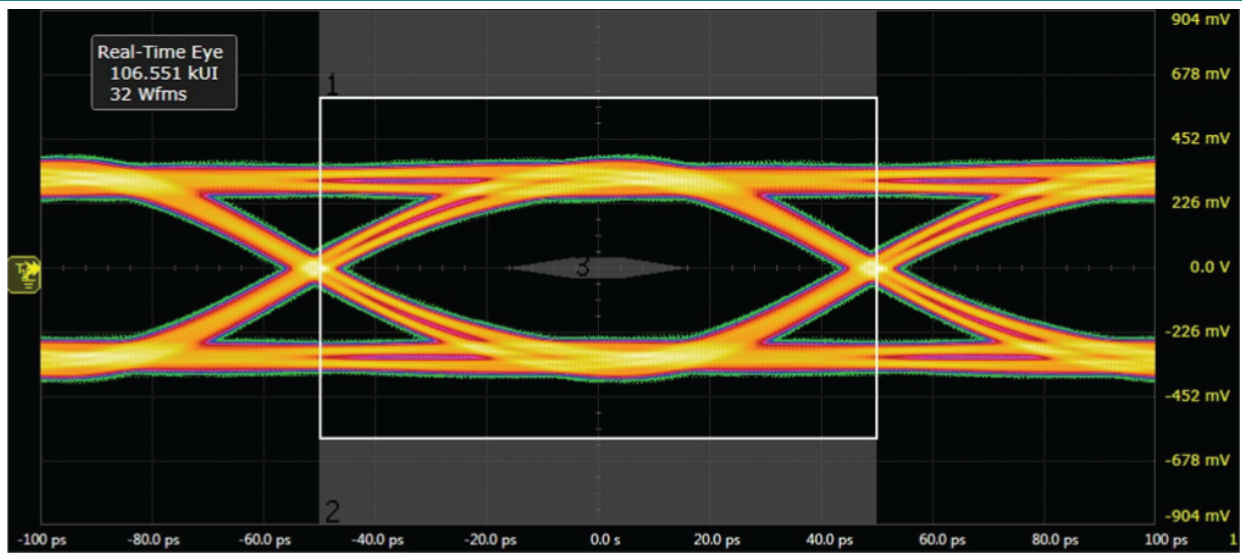
Fig. 4. Relative capacitance as a function of input voltage; typical values



aaa-028417

Data rate: 10 Gbit/s

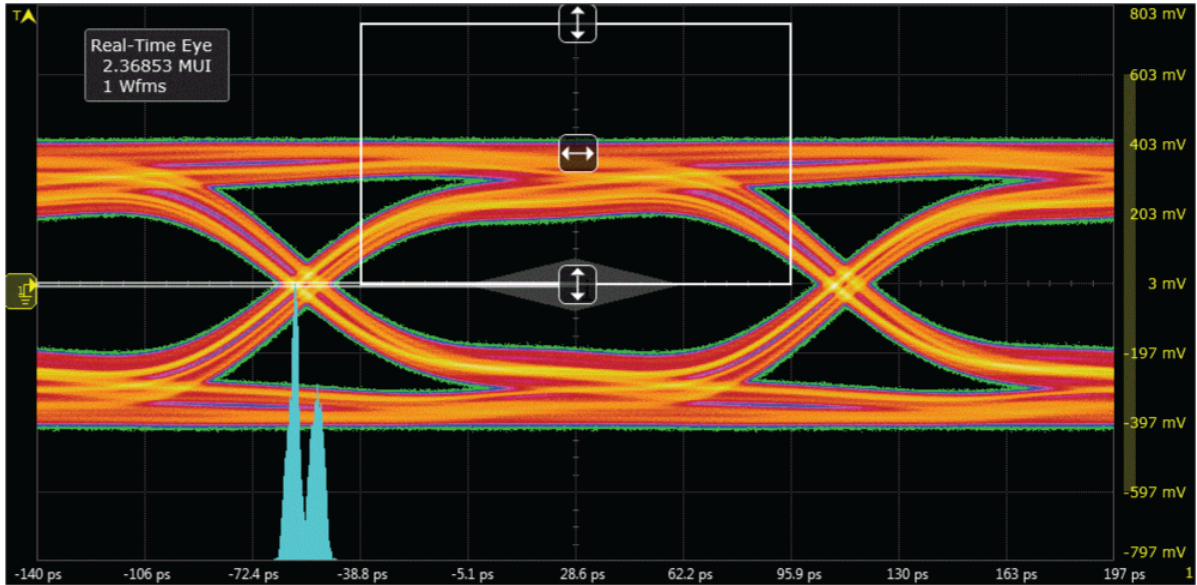
Fig. 5. USB 3.2 eye diagram, PCB with device; typical values



aaa-028418

Data rate: 10 Gbit/s

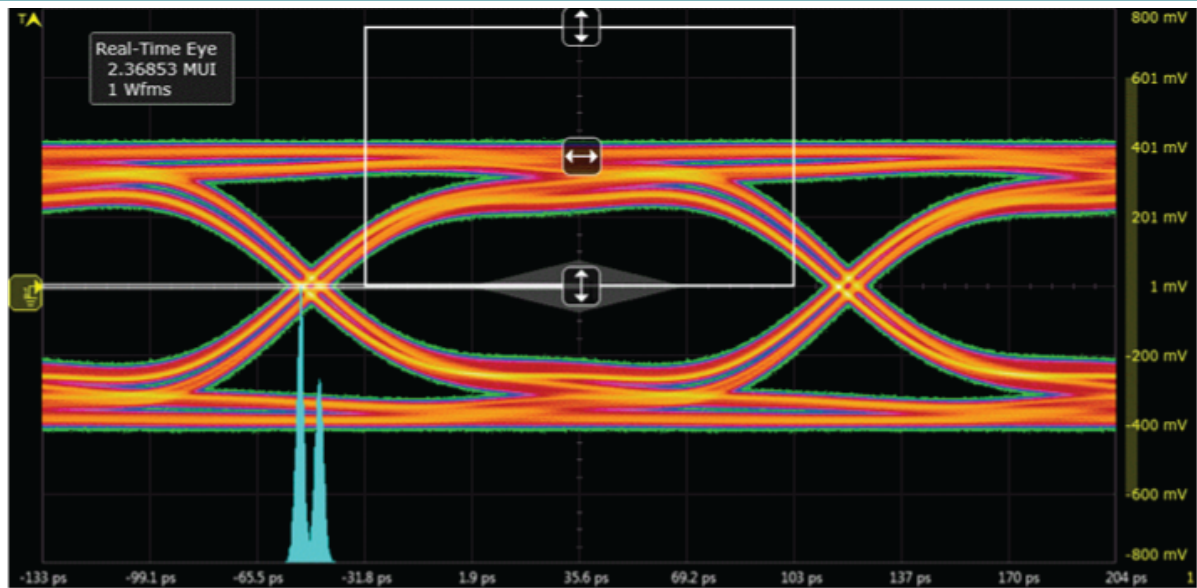
Fig. 6. USB 3.2 eye diagram, PCB without device; typical values



aaa-028419

1080p  
Data rate: 6 Gbit/s

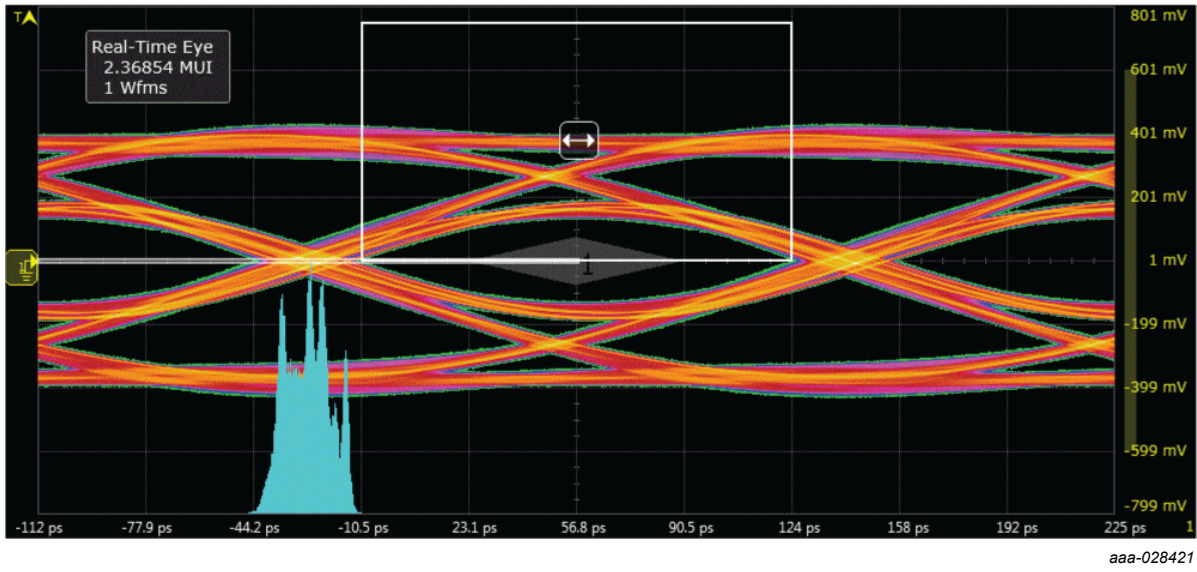
Fig. 7. HDMI TP1 eye diagram, PCB with device; typical values



aaa-028420

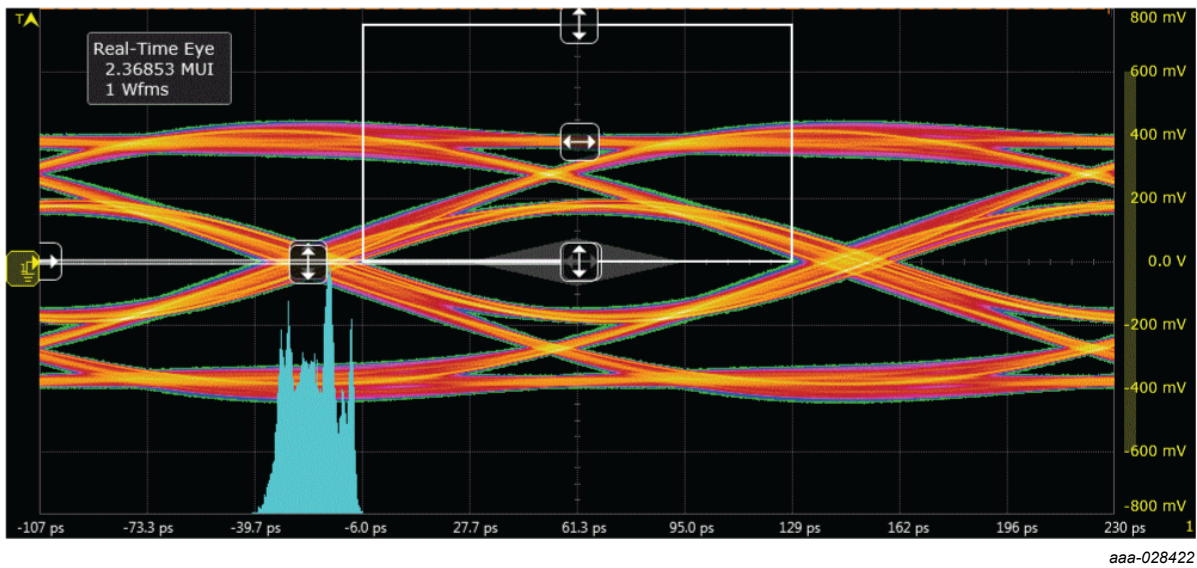
1080p  
Data rate: 6 Gbit/s

Fig. 8. HDMI TP1 eye diagram, PCB without device; typical values



1080p  
Data rate: 6 Gbit/s

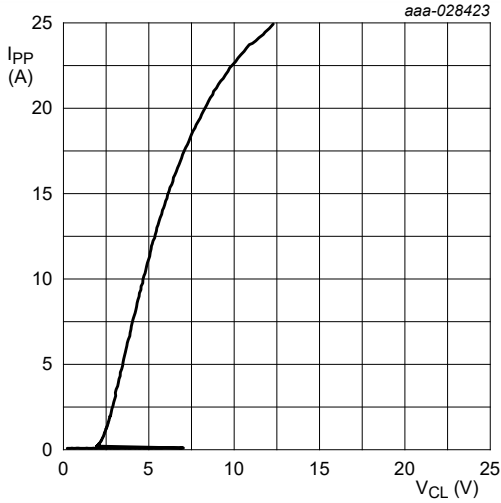
Fig. 9. HDMI TP2 eye diagram, PCB with device; typical values



1080p  
Data rate: 6 Gbit/s

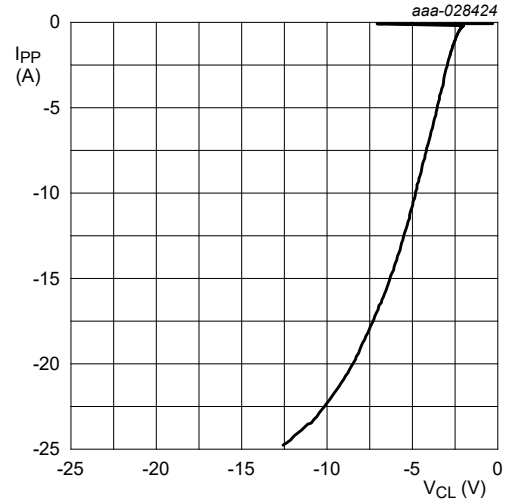
Fig. 10. HDMI TP2 eye diagram, PCB without device; typical values





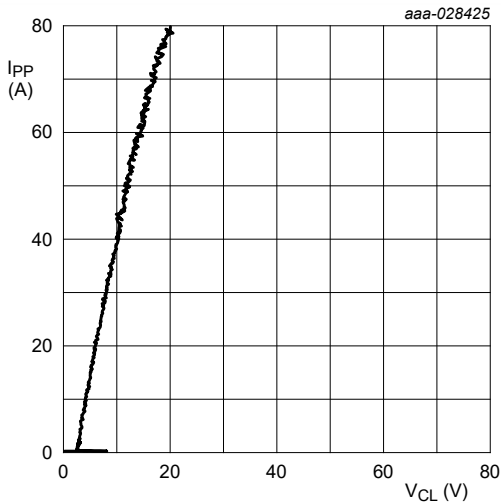
$t_r = 1 \text{ ns}$   
 $t_p = 100 \text{ ns}$ ; Transmission Line Pulse (TLP)

**Fig. 11. Dynamic resistance with positive clamping; typical values**



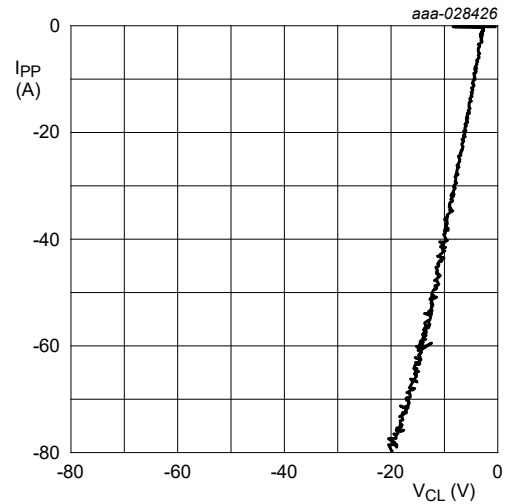
$t_r = 1 \text{ ns}$   
 $t_p = 100 \text{ ns}$ ; Transmission Line Pulse (TLP)

**Fig. 12. Dynamic resistance with negative clamping; typical values**



$t_r = 600 \text{ ps}$   
 $t_p = 5 \text{ ns}$ ; Very-Fast Transmission Line Pulse (VF-TLP)

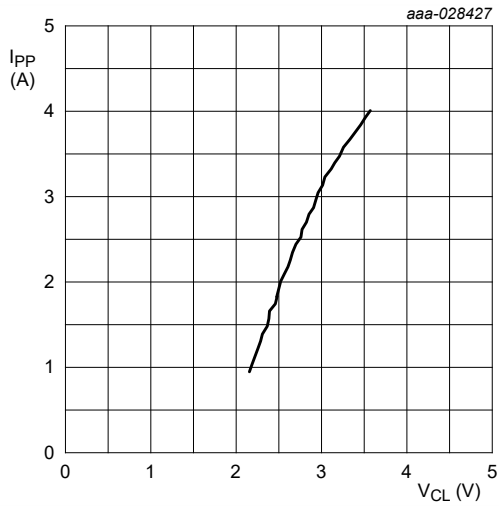
**Fig. 13. Dynamic resistance with positive clamping; typical values**



$t_r = 600 \text{ ps}$   
 $t_p = 5 \text{ ns}$ ; Very Fast Transmission Line Pulse (VF-TLP)

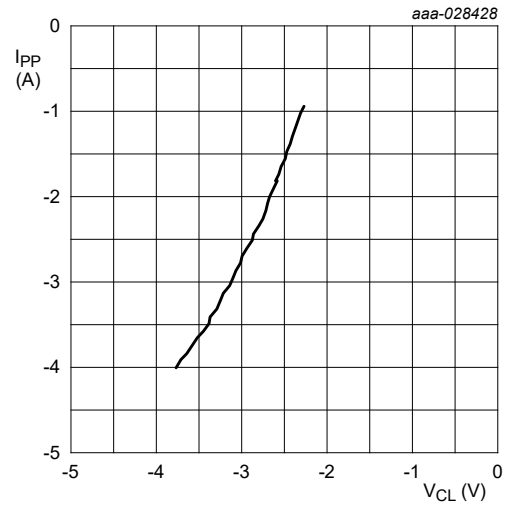
**Fig. 14. Dynamic resistance with negative clamping; typical values**





IEC 61000-4-5;  $t_p = 8/20 \mu s$ ; positive pulse

**Fig. 15. Dynamic resistance with positive clamping; typical values**



IEC 61000-4-5;  $t_p = 8/20 \mu s$ ; negative pulse

**Fig. 16. Dynamic resistance with negative clamping; typical values**

## 10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

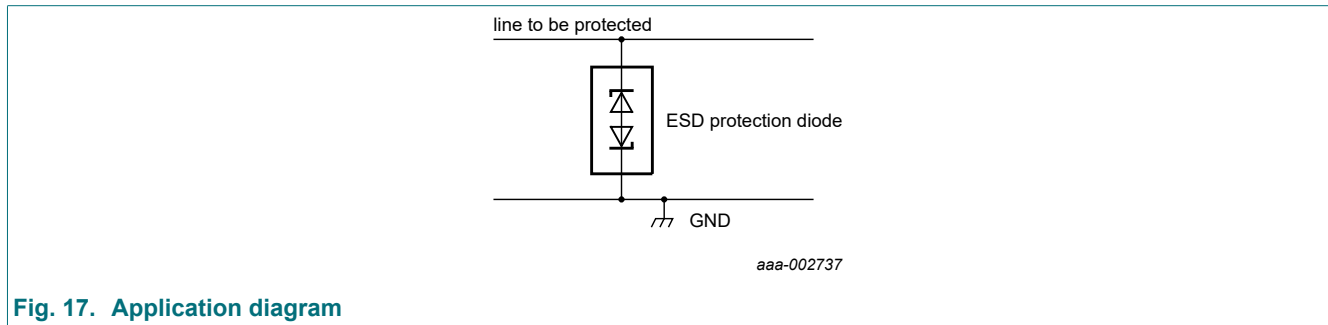


Fig. 17. Application diagram

### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

### 11. Package outline

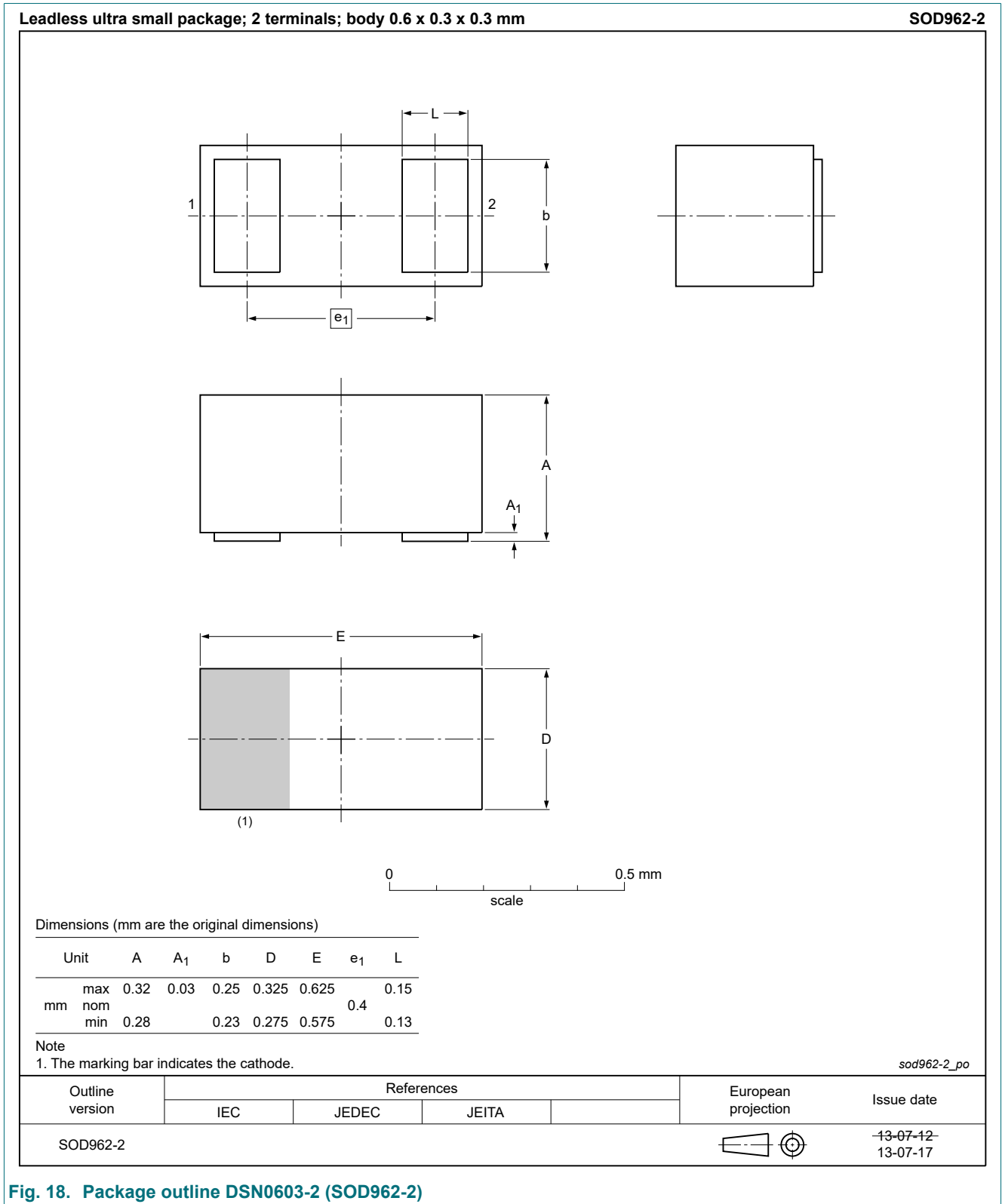
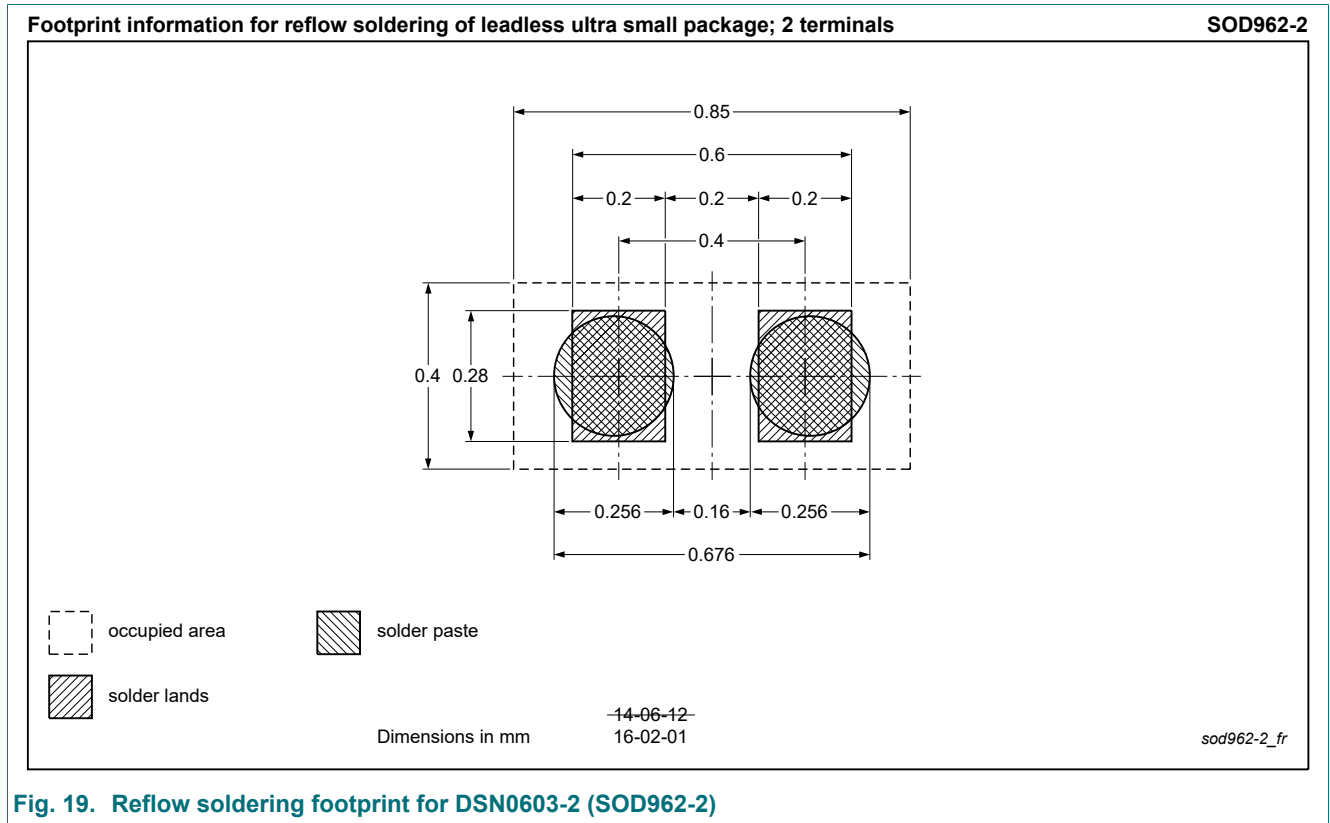


Fig. 18. Package outline DSN0603-2 (SOD962-2)

## 12. Soldering



## 13. Revision history

Table 7. Revision history

| Data sheet ID    | Release date      | Data sheet status  | Change notice | Supersedes       |
|------------------|-------------------|--------------------|---------------|------------------|
| PESD3V3Y1BSF v.2 | 20190329          | Product data sheet | -             | PESD3V3Y1BSF v.1 |
| Modifications:   | • Updated package |                    |               |                  |
| PESD3V3Y1BSF v.1 | 20180607          | Product data sheet | -             | -                |

## 14. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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