

74LVC1G38-Q100

2-input NAND gate; open drain

Rev. 2 — 9 December 2016

Product data sheet

1. General description

The 74LVC1G38-Q100 provides a 2-input NAND function.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device as translator in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V).
- $\pm 24\text{ mA}$ output drive ($V_{CC} = 3.0\text{ V}$)
- CMOS low power consumption
- Open drain outputs
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|------------------|-------------------|--------|--|----------|
| | Temperature range | Name | Description | |
| 74LVC1G38GW-Q100 | -40 °C to +125 °C | TSSOP5 | plastic thin shrink small outline package; 5 leads; body width 1.25 mm | SOT353-1 |
| 74LVC1G38GV-Q100 | -40 °C to +125 °C | SC-74A | plastic surface-mounted package; 5 leads | SOT753 |

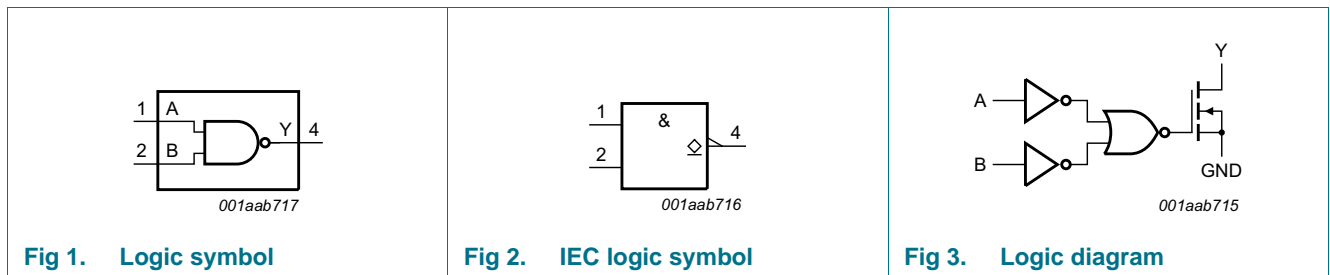
4. Marking

Table 2. Marking

| Type number | Marking code ^[1] |
|------------------|-----------------------------|
| 74LVC1G38GW-Q100 | YB |
| 74LVC1G38GV-Q100 | YB |

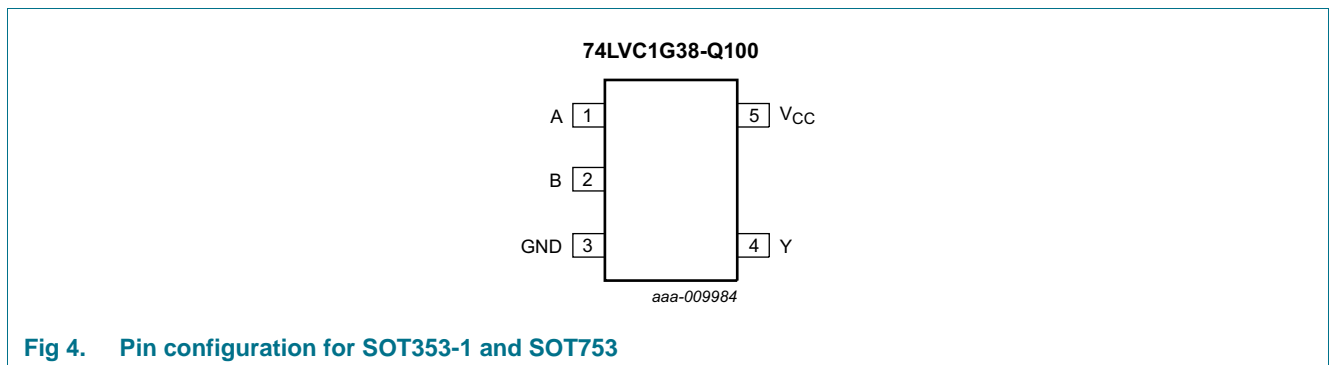
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|-----------------|-----|----------------|
| A | 1 | data input |
| B | 2 | data input |
| GND | 3 | ground (0 V) |
| Y | 4 | data output |
| V _{CC} | 5 | supply voltage |

7. Functional description

Table 4. Function table^[1]

| Input | | Output |
|-------|---|--------|
| A | B | Y |
| L | L | Z |
| L | H | Z |
| H | L | Z |
| H | H | L |

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|--|-------------|------|------|
| V _{CC} | supply voltage | | -0.5 | +6.5 | V |
| I _{IK} | input clamping current | V _I < 0 V | -50 | - | mA |
| V _I | input voltage | | [1] -0.5 | +6.5 | V |
| I _{OK} | output clamping current | V _O > V _{CC} or V _O < 0 V | - | ±50 | mA |
| V _O | output voltage | Active mode | [1][2] -0.5 | +6.5 | V |
| | | Power-down mode | [1][2] -0.5 | +6.5 | V |
| I _O | output current | V _O = 0 V to V _{CC} | - | ±50 | mA |
| I _{CC} | supply current | | - | 100 | mA |
| I _{GND} | ground current | | -100 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C | [3] - | 300 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|--|------|-----|------|------|
| V_{CC} | supply voltage | | 1.65 | - | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | Active mode | 0 | - | 5.5 | V |
| | | Disable mode; $V_{CC} = 1.65$ V to 5.5 V | 0 | - | 5.5 | V |
| | | Power-down mode; $V_{CC} = 0$ V | 0 | - | 5.5 | V |
| T_{amb} | ambient temperature | | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65$ V to 2.7 V | - | - | 20 | ns/V |
| | | $V_{CC} = 2.7$ V to 5.5 V | - | - | 10 | ns/V |

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---------------------------|--|--------------|-----------|--------------|---------|
| $T_{amb} = -40$ °C to $+85$ °C [1] | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 1.65$ V to 1.95 V | $0.65V_{CC}$ | - | - | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | 1.7 | - | - | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 2.0 | - | - | V |
| | | $V_{CC} = 4.5$ V to 5.5 V | $0.7V_{CC}$ | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 1.65$ V to 1.95 V | - | - | $0.35V_{CC}$ | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | - | - | 0.7 | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | - | - | 0.8 | V |
| | | $V_{CC} = 4.5$ V to 5.5 V | - | - | $0.3V_{CC}$ | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH}$ or V_{IL} | - | - | - | |
| | | $I_O = 100$ μ A; $V_{CC} = 1.65$ V to 5.5 V | - | - | 0.1 | V |
| | | $I_O = 4$ mA; $V_{CC} = 1.65$ V | - | - | 0.45 | V |
| | | $I_O = 8$ mA; $V_{CC} = 2.3$ V | - | - | 0.3 | V |
| | | $I_O = 12$ mA; $V_{CC} = 2.7$ V | - | - | 0.4 | V |
| | | $I_O = 24$ mA; $V_{CC} = 3.0$ V | - | - | 0.55 | V |
| | | $I_O = 32$ mA; $V_{CC} = 4.5$ V | - | - | 0.55 | V |
| I_I | input leakage current | $V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V | - | ± 0.1 | ± 1 | μ A |
| I_{OZ} | OFF-state output current | $V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5$ V | - | ± 0.1 | ± 2 | μ A |
| I_{OFF} | power-off leakage current | V_I or $V_O = 5.5$ V; $V_{CC} = 0$ V | - | ± 0.1 | ± 2 | μ A |
| I_{CC} | supply current | $V_I = 5.5$ V or GND; $V_{CC} = 1.65$ V to 5.5 V; $I_O = 0$ A | - | 0.1 | 4 | μ A |
| ΔI_{CC} | additional supply current | $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 2.3$ V to 5.5 V; per pin | - | 5 | 500 | μ A |
| C_I | input capacitance | | - | 2.5 | - | pF |

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------|---|---------------------|-----|---------------------|------|
| T_{amb} = -40 °C to +125 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65V _{CC} | - | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | V |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7V _{CC} | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | V |
| | | V _{CC} = 4.5 V to 5.5 V | - | - | 0.3V _{CC} | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | - | - | - | |
| | | I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V | - | - | 0.1 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | - | 0.70 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | - | 0.45 | V |
| | | I _O = 12 mA; V _{CC} = 2.7 V | - | - | 0.60 | V |
| | | I _O = 24 mA; V _{CC} = 3.0 V | - | - | 0.80 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | ±1 | μA |
| | | | | | | |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±2 | μA |
| I _{OFF} | power-off leakage current | V _I or V _O = 5.5 V; V _{CC} = 0 V | - | - | ±2 | μA |
| I _{CC} | supply current | V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A | - | - | 4 | μA |
| ΔI _{CC} | additional supply current | V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V; per pin | - | - | 500 | μA |

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------------------|--|------------------|--------------------|------|-------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| t _{pd} | propagation delay | A, B to Y; see Figure 5 ^[2] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.0 | 3.0 | 10.0 | 1.0 | 12.5 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.5 | 1.8 | 6.0 | 0.5 | 7.5 | ns |
| | | V _{CC} = 2.7 V | 0.5 | 2.5 | 5.0 | 0.5 | 6.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 0.5 | 2.3 | 4.5 | 0.5 | 5.7 | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 0.5 | 1.5 | 3.9 | 0.5 | 4.9 | ns |
| C _{PD} | power dissipation capacitance | V _{CC} = 3.3 V; V _I = GND to V _{CC} ^[3] | - | 6 | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PZL} and t_{PLZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

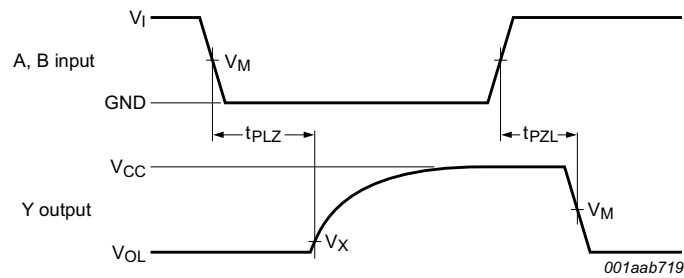
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

∑(C_L × V_{CC}² × f_o) = sum of outputs.

12. Waveform and test circuit



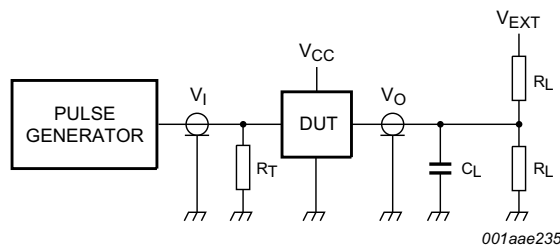
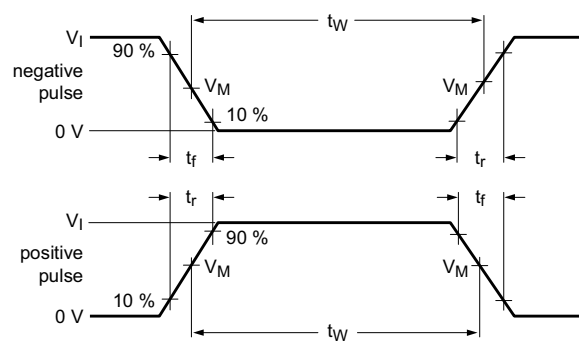
Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. The input (A, B) to output (Y) propagation delays

Table 9. Measurement points

| Supply voltage | Input | Output | V_X |
|------------------|-------------|-------------|-------------------|
| V_{CC} | V_M | V_M | $V_{OL} + 0.15 V$ |
| 1.65 V to 1.95 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL} + 0.15 V$ |
| 2.3 V to 2.7 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL} + 0.15 V$ |
| 2.7 V | 1.5 V | 1.5 V | $V_{OL} + 0.3 V$ |
| 3.0 V to 3.6 V | 1.5 V | 1.5 V | $V_{OL} + 0.3 V$ |
| 4.5 V to 5.5 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL} + 0.3 V$ |



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 6. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Input | Load | V_{EXT} |
|------------------|------------|---------------|--------------------------------|
| V_{CC} | V_I | C_L | t_{PZL}, t_{PLZ} |
| | t_r, t_f | R_L | |
| 1.65 V to 1.95 V | V_{CC} | $\leq 2.0 ns$ | 30 pF, 1 k Ω , V_{CC} |
| 2.3 V to 2.7 V | V_{CC} | $\leq 2.0 ns$ | 30 pF, 500 Ω , V_{CC} |
| 2.7 V | 2.7 V | $\leq 2.5 ns$ | 50 pF, 500 Ω , V_{CC} |
| 3.0 V to 3.6 V | 2.7 V | $\leq 2.5 ns$ | 50 pF, 500 Ω , V_{CC} |
| 4.5 V to 5.5 V | V_{CC} | $\leq 2.5 ns$ | 50 pF, 500 Ω , V_{CC} |

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

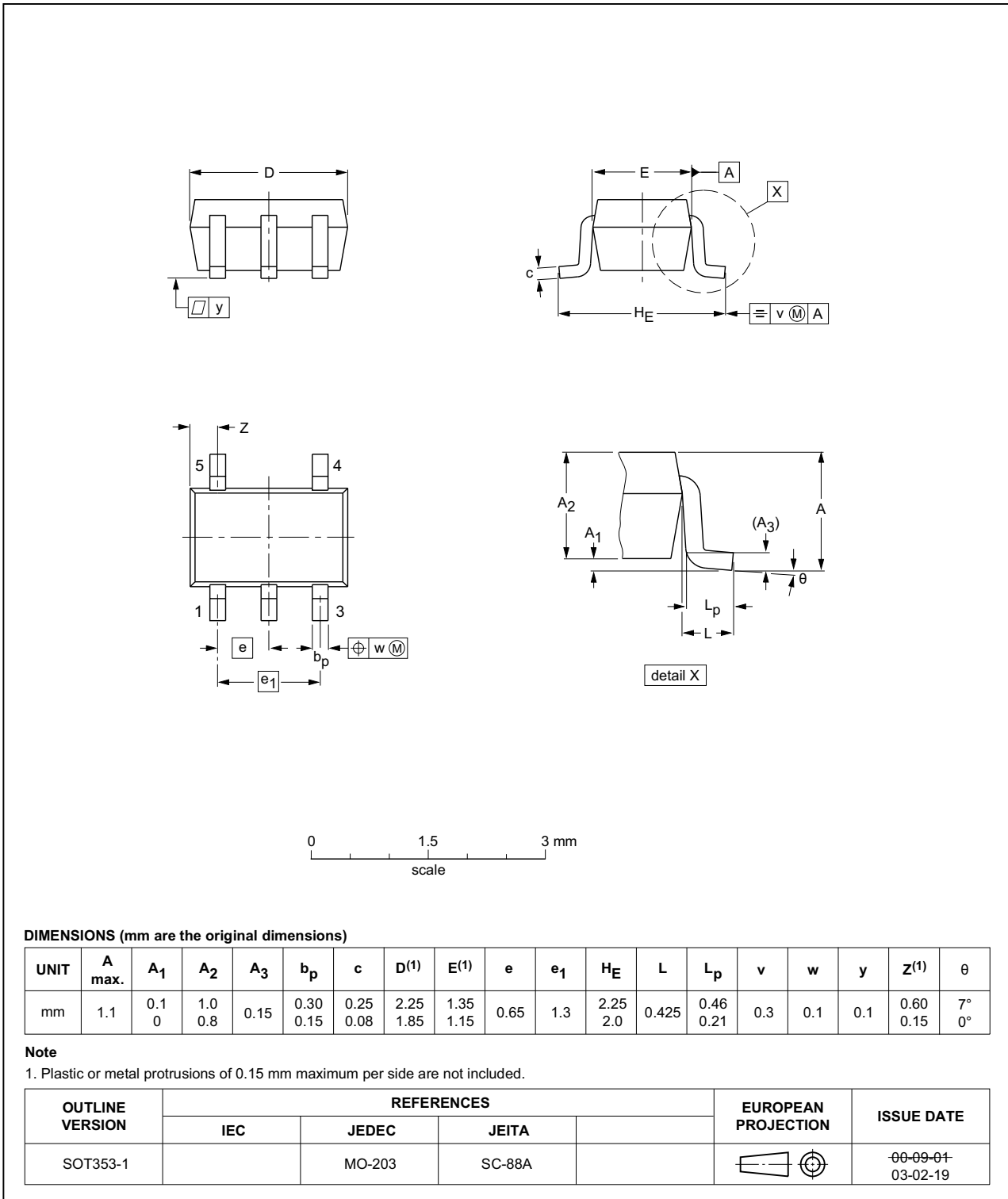


Fig 7. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

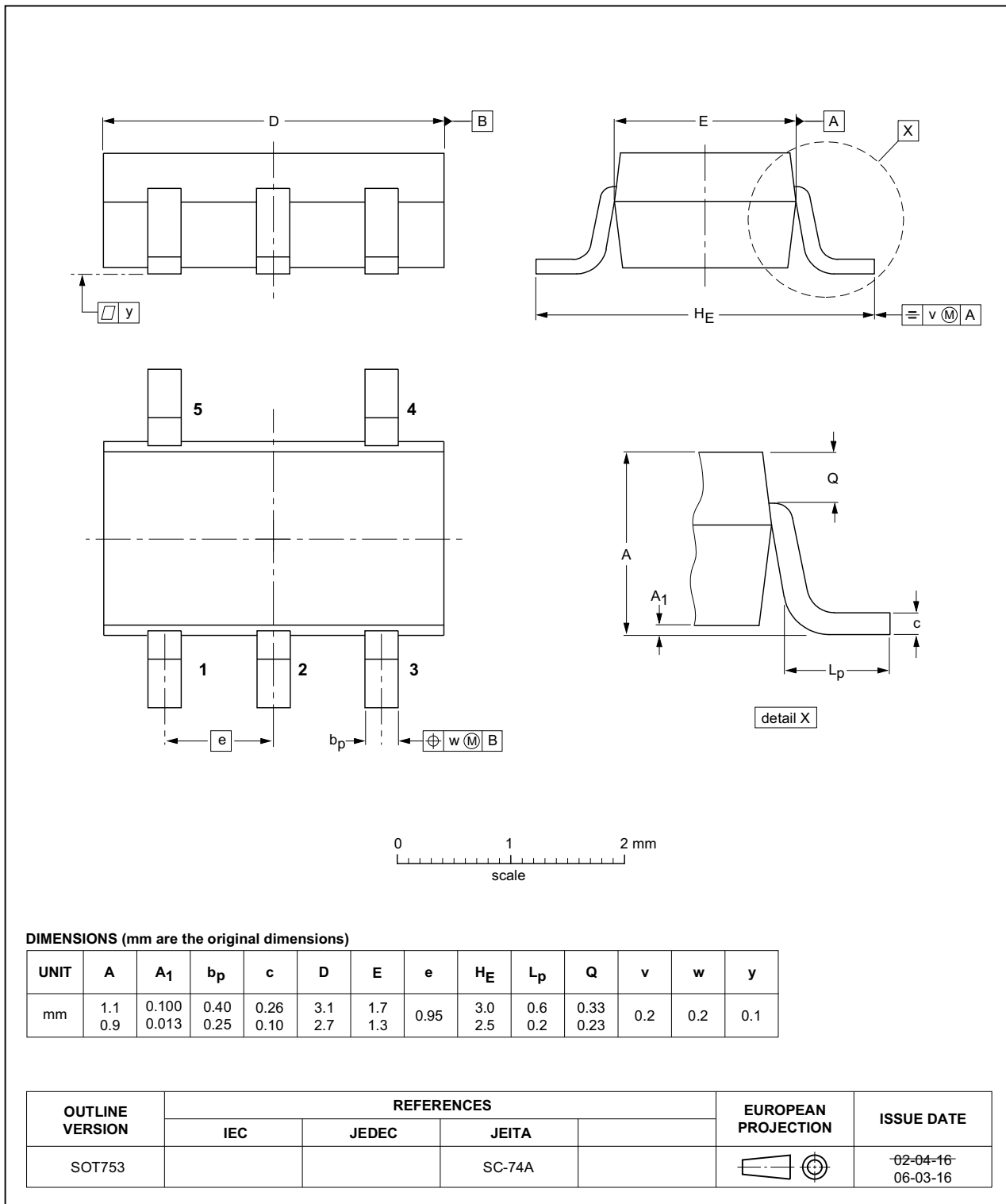


Fig 8. Package outline SOT753 (SC-74A)

14. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MIL | Military |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

15. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------------|--|--------------------|---------------|--------------------|
| 74LVC1G38_Q100 v.1 | 20161209 | Product data sheet | - | 74LVC1G38_Q100 v.1 |
| Modifications: | <ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. | | | |
| 74LVC1G38_Q100 v.1 | 20131127 | Product data sheet | - | - |

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16.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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