# 74AHC123A; 74AHCT123A

## Dual retriggerable monostable multivibrator with reset

Rev. 4 — 8 November 2011 Product data sheet

## 1. General description

The 74AHC123A; 74AHCT123A are high-speed Si-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74AHC123A; 74AHCT123A are dual retriggerable monostable multivibrators with output pulse width control by three methods. The basic pulse time is programmed by selection of an external resistor ($R_{EXT}$) and capacitor ($C_{EXT}$). The external resistor and capacitor are normally connected as shown in Figure 11.

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input $n\overline{RD}$, which also inhibits the triggering.

An internal connection from $n\overline{RD}$ to the input gate makes it possible to trigger the circuit by a positive-going signal at input $n\overline{RD}$ as shown in Table 3. Figure 8 and Figure 9 illustrate pulse control by retriggering and early reset. The basic output pulse width is essentially determined by the value of the external timing components $R_{EXT}$ and $C_{EXT}$. When $C_{EXT} \geq 10$ nF, the typical output pulse width is defined as: $t_W = R_{EXT} \times C_{EXT}$ where $t_W$ = pulse width in ns; $R_{EXT}$ = external resistor in kΩ; $C_{EXT}$ = external capacitor in pF. Schmitt-trigger action at all inputs makes the circuit highly tolerant to slower input rise and fall times.

## 2. Features and benefits

- All inputs have a Schmitt-trigger action
- Inputs accept voltages higher than $V_{CC}$
- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- For 74AHC123A only: operates with CMOS input levels
- For 74AHCT123A only: operates with TTL input levels
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74AHC123AD | −40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74AHCT123AD | | | | |
| 74AHC123APW | −40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74AHCT123APW | | | | |
| 74AHC123ABQ | −40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |
| 74AHCT123ABQ | | | | |

## 4. Functional diagram

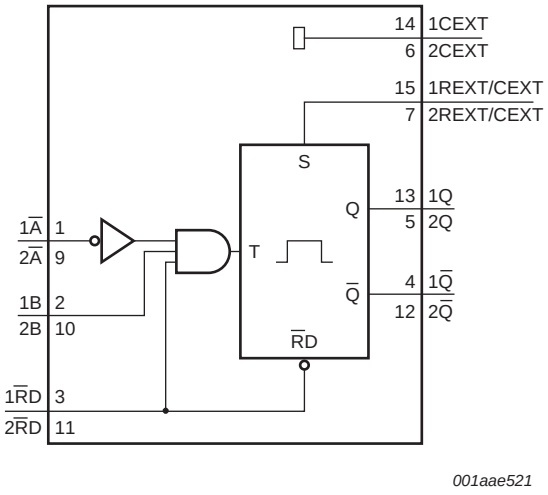



**Fig 1. Logic symbol**

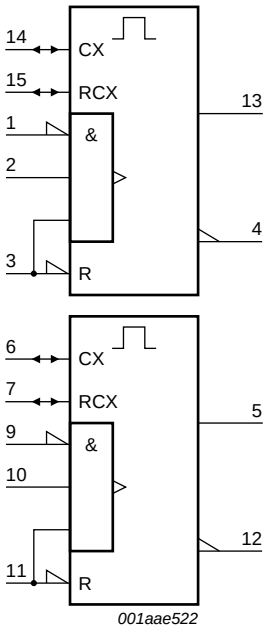



**Fig 2. IEC logic symbol**

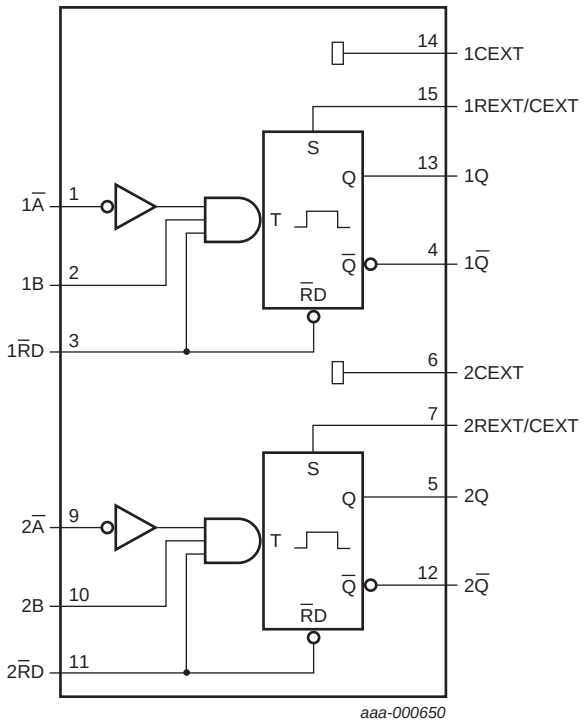
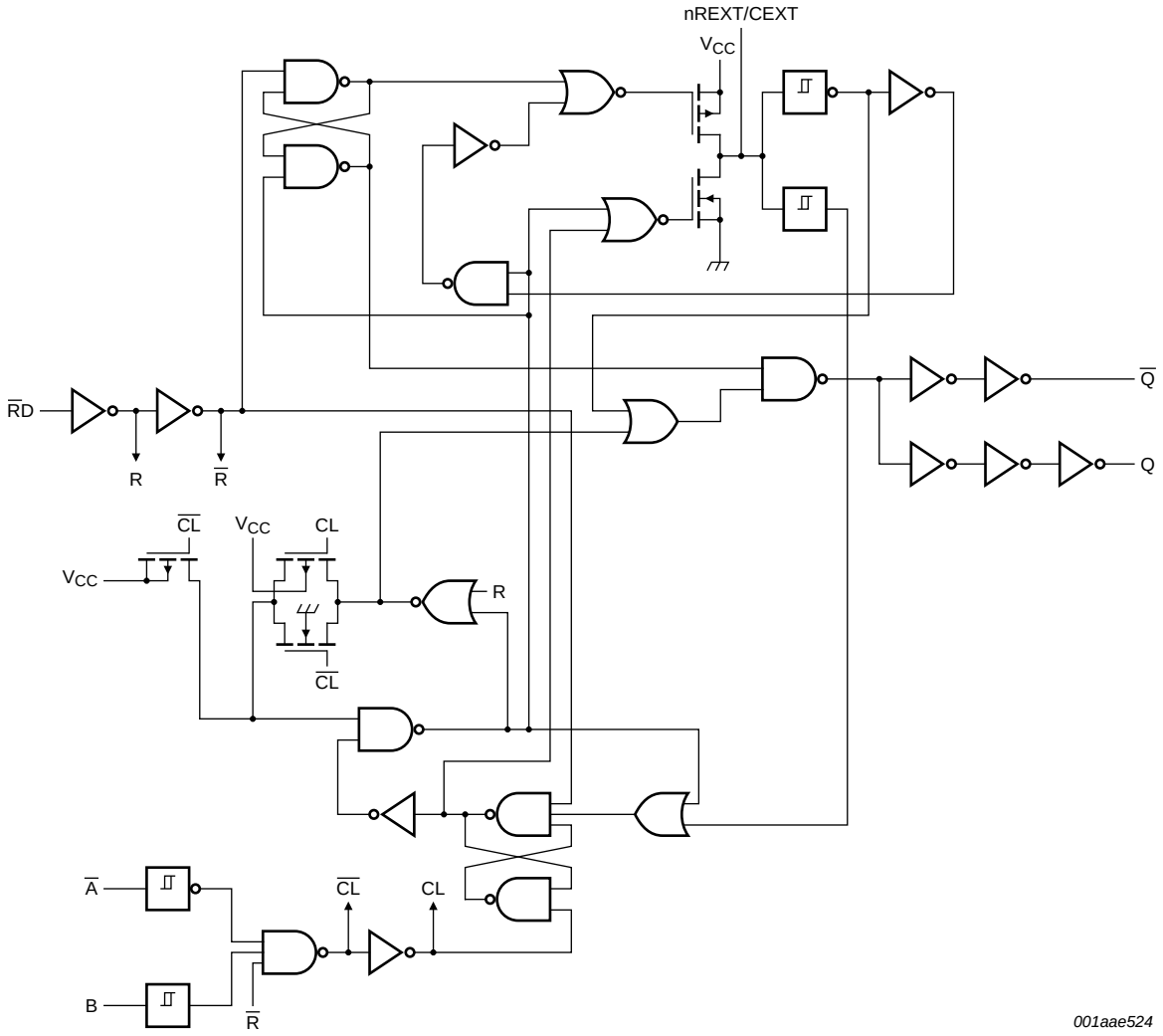



**Fig 3. Functional diagram**




For minimum noise generation it is recommended to ground pins 6 (2CEXT) and 14 (1CEXT) externally to pin 8 (GND).

**Fig 4. Functional diagram**

# 5. Pinning information

## 5.1 Pinning

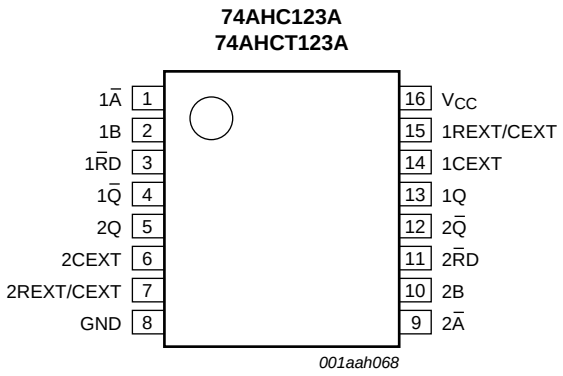
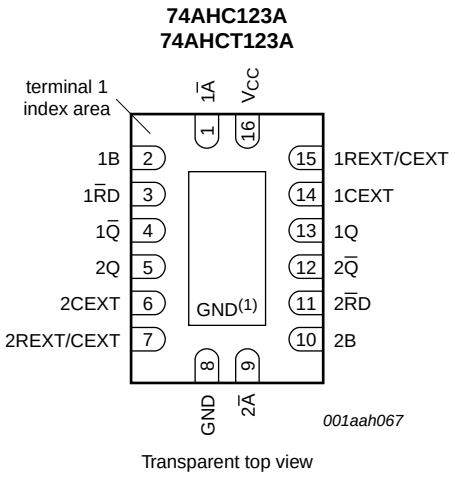



Fig 5. Pin configuration SO16, TSSOP16




Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 6. Pin configuration DHVQFN16

## 5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---|---|---|
| 1Ā | 1 | negative-edge triggered input 1 |
| 1B | 2 | positive-edge triggered input 1 |
| 1R̄D | 3 | direct reset LOW and positive-edge triggered input 1 |
| 1Q̄ | 4 | active LOW output 1 |
| 2Q | 5 | active HIGH output 2 |
| 2CEXT | 6 | external capacitor connection 2 |
| 2REXT/CEXT | 7 | external resistor and capacitor connection 2 |
| GND | 8 | ground (0 V) |
| 2Ā | 9 | negative-edge triggered input 2 |
| 2B | 10 | positive-edge triggered input 2 |
| 2R̄D | 11 | direct reset LOW and positive-edge triggered input 2 |
| 2Q̄ | 12 | active LOW output 2 |
| 1Q | 13 | active HIGH output 1 |
| 1CEXT | 14 | external capacitor connection 1 |
| 1REXT/CEXT | 15 | external resistor and capacitor connection 1 |
| $V_{CC}$ | 16 | supply voltage |

## 6. Functional description

**Table 3. Function table[1]**

| Input | | | Output | |
|---|---|---|---|---|
| $\overline{nRD}$ | $n\overline{A}$ | nB | nQ | $n\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L[2] | H[2] |
| X | X | L | L[2] | H[2] |
| H | L | ↑ | ⎍ | ⎍ |
| H | ↓ | H | ⎍ | ⎍ |
| ↑ | L | H | ⎍ | ⎍ |

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH transition;
↓ = HIGH-to-LOW transition;
⎍ = one HIGH level output pulse;
⎍ = one LOW level output pulse.

[2] If the monostable multivibrator was triggered before this condition was established, the pulse will continue as programmed.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +7.0 | V |
| $V_I$ | input voltage | | | –0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V | [1] | –20 | - | mA |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] | - | ±20 | mA |
| $I_O$ | output current | $V_O = -0.5$ V to $(V_{CC} + 0.5$ V) | | - | ±25 | mA |
| $I_{CC}$ | supply current | | | - | 75 | mA |
| $I_{GND}$ | ground current | | | –75 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb} = -40$ °C to +125 °C | | | | |
| | SO16 package | | [2] | - | 500 | mW |
| | TSSOP16 package | | [3] | - | 500 | mW |
| | DHVQFN16 package | | [4] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

[3] $P_{tot}$ derates linearly with 5.5 mW/K above 60 °C.

[4] $P_{tot}$ derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 74AHC123A | | | 74AHCT123A | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | 0 | - | 5.5 | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | –40 | +25 | +125 | –40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | - | - | 100 | - | - | - | ns/V |
| | | $V_{CC}$ = 5.0 V ± 0.5 V | - | - | 20 | - | - | 20 | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74AHC123A** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | $V_{CC}$ = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | $V_{CC}$ = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = –50 μA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = –50 μA; $V_{CC}$ = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | $I_O$ = –50 μA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –4.0 mA; $V_{CC}$ = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| | | $I_O$ = –8.0 mA; $V_{CC}$ = 4.5 V | 3.94 | - | - | 3.8 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 50 μA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 μA; $V_{CC}$ = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | | $I_O$ = 8.0 mA; $V_{CC}$ = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | | | | | | | | |
| | | nREXT/CEXT [1] | - | - | ±0.25 | - | ±2.5 | - | ±10.0 | μA |
| | | pins $n\overline{A}$, nB, $n\overline{RD}$ | - | - | ±0.1 | - | ±1.0 | - | ±2.0 | μA |

**Table 6. Static characteristics** *…continued*

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | μA |
| | | active state (per circuit); [1] $V_I = V_{CC}$ or GND | | | | | | | | |
| | | $V_{CC}$ = 3.0 V | - | 160 | 250 | - | 280 | - | 280 | μA |
| | | $V_{CC}$ = 4.5 V | - | 380 | 500 | - | 650 | - | 650 | μA |
| | | $V_{CC}$ = 5.5 V | - | 560 | 750 | - | 975 | - | 975 | μA |
| $C_I$ | input capacitance | | - | 5.0 | 10 | - | 10 | - | 10 | pF |
| $C_O$ | output capacitance | | - | 4.0 | - | - | - | - | - | pF |
| **74AHCT123A** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = –50 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –8.0 mA | 3.94 | - | - | 3.8 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = 50 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| $I_I$ | input leakage current | nREXT/CEXT; [1] $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | - | ±0.25 | - | ±2.5 | - | ±10.0 | μA |
| | | pins $n\overline{A}$, nB, $n\overline{RD}$; $V_I = V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | ±0.1 | - | ±1.0 | - | ±2.0 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | μA |
| | | active state (per circuit); [1] $V_I = V_{CC}$ or GND | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | - | 380 | 500 | - | 650 | - | 650 | μA |
| | | $V_{CC}$ = 5.5 V | - | 560 | 750 | - | 975 | - | 975 | μA |
| $C_I$ | input capacitance | | - | 3 | 10 | - | 10 | - | 10 | pF |
| $C_O$ | output capacitance | | - | 4.0 | - | - | - | - | - | pF |

[1] Voltage on nREXT/CEXT = 0.5 × $V_{CC}$ and pin nREXT/CEXT in OFF-state during test.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND = 0 V; For test circuit see Figure 12.*

| Symbol | Parameter | Conditions | | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| **74AHC123A** | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | $n\overline{A}$ and nB to nQ and $n\overline{Q}$; see Figure 7 | [2] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 7.4 | 20.6 | 1.0 | 24.0 | 1.0 | 26.0 | ns |
| | | $C_L$ = 50 pF | | - | 10.5 | 24.1 | 1.0 | 27.5 | 1.0 | 30.0 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 5.1 | 12.0 | 1.0 | 14.0 | 1.0 | 15.5 | ns |
| | | $C_L$ = 50 pF | | - | 7.3 | 14.0 | 1.0 | 16.0 | 1.0 | 17.5 | ns |
| | | $n\overline{RD}$ to nQ and $n\overline{Q}$; see Figure 7 | [2] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 8.2 | 22.4 | 1.0 | 26.0 | 1.0 | 28.0 | ns |
| | | $C_L$ = 50 pF | | - | 11.7 | 25.9 | 1.0 | 29.5 | 1.0 | 32.0 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 5.6 | 12.9 | 1.0 | 15.0 | 1.0 | 16.5 | ns |
| | | $C_L$ = 50 pF | | - | 8.1 | 14.9 | 1.0 | 17.0 | 1.0 | 19.0 | ns |
| | | $n\overline{RD}$ to nQ and $n\overline{Q}$ (reset); see Figure 7 | [2] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 6.4 | 15.8 | 1.0 | 18.5 | 1.0 | 20.0 | ns |
| | | $C_L$ = 50 pF | | - | 9.2 | 19.3 | 1.0 | 22.0 | 1.0 | 24.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.4 | 9.4 | 1.0 | 11.0 | 1.0 | 12.0 | ns |
| | | $C_L$ = 50 pF | | - | 6.3 | 11.4 | 1.0 | 13.0 | 1.0 | 14.5 | ns |

**Table 7. Dynamic characteristics** *...continued*

*GND = 0 V; For test circuit see Figure 12.*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| $t_W$ | pulse width | inputs; $n\overline{A}$ = LOW; see Figure 7 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | inputs; nB = HIGH; see Figure 7 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | inputs; $n\overline{R}D$ = LOW; see Figure 7 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | outputs; $n\overline{Q}$ = LOW and nQ = HIGH; $C_L$ = 50 pF; see Figure 7, Figure 8, Figure 9 and Figure 10 [3] | | | | | | | | |
| | | $C_{EXT}$ = 28 pF; $R_{EXT}$ = 2 kΩ | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | 115 | 240 | - | 300 | - | 300 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | 100 | 200 | - | 240 | - | 240 | ns |
| | | $C_{EXT}$ = 0.01 μF; $R_{EXT}$ = 10 kΩ | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 90 | 100 | 110 | 90 | 110 | 85 | 115 | μs |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 90 | 100 | 110 | 90 | 110 | 85 | 115 | μs |
| | | $C_{EXT}$ = 0.1 μF; $R_{EXT}$ = 10 kΩ; | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 0.9 | 1 | 1.1 | 0.9 | 1.1 | 0.85 | 1.15 | ms |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0.9 | 1 | 1.1 | 0.9 | 1.1 | 0.85 | 1.15 | ms |
| $t_{rtrig}$ | retrigger time | $n\overline{A}$ to nB; $C_{EXT}$ = 100 pF; $R_{EXT}$ = 1 kΩ; $C_L$ = 50 pF; see Figure 8 and Figure 10 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | 60 | - | - | - | - | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | 39 | - | - | - | - | - | ns |
| | | $n\overline{A}$ to nB; $C_{EXT}$ = 0.01 μF; $R_{EXT}$ = 1 kΩ; $C_L$ = 50 pF; see Figure 8 and Figure 10 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | 1.5 | - | - | - | - | - | μs |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | 1.2 | - | - | - | - | - | μs |
| $C_{PD}$ | power dissipation capacitance | $C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ [4] | - | 57 | - | - | - | - | - | pF |

**Table 7. Dynamic characteristics** *...continued*

*GND = 0 V; For test circuit see Figure 12.*

| Symbol | Parameter | Conditions | | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| **74AHCT123A** | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | $n\overline{A}$ and nB to nQ and $n\overline{Q}$; see Figure 7 | [2] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 5.0 | 12.0 | 1.0 | 14.0 | 1.0 | 15.5 | ns |
| | | $C_L$ = 50 pF | | - | 7.1 | 14.0 | 1.0 | 16.0 | 1.0 | 17.5 | ns |
| | | $n\overline{RD}$ to nQ and $n\overline{Q}$; see Figure 7 | [2] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 5.2 | 12.9 | 1.0 | 15.0 | 1.0 | 16.5 | ns |
| | | $C_L$ = 50 pF | | - | 7.5 | 14.9 | 1.0 | 17.0 | 1.0 | 18.5 | ns |
| | | $n\overline{RD}$ to nQ and $n\overline{Q}$ (reset); see Figure 7 | [2] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.7 | 9.4 | 1.0 | 11.0 | 1.0 | 12.0 | ns |
| | | $C_L$ = 50 pF | | - | 6.7 | 11.4 | 1.0 | 13.0 | 1.0 | 14.5 | ns |
| $t_W$ | pulse width | inputs; $n\overline{A}$ = LOW; $C_L$ = 50 pF; see Figure 7 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | inputs; nB = HIGH; $C_L$ = 50 pF; see Figure 7 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | inputs; $n\overline{RD}$ = LOW; $C_L$ = 50 pF; see Figure 7 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | outputs; $n\overline{Q}$ = LOW and nQ = HIGH; $C_L$ = 50 pF; $C_{EXT}$ = 28 pF; $R_{EXT}$ = 2 kΩ; see Figure 7, Figure 8, Figure 9 and Figure 10 | [3] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | - | 100 | 200 | - | 240 | - | 240 | ns |
| | | $C_{EXT}$ = 0.01 μF; $R_{EXT}$ = 10 kΩ | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 90 | 100 | 110 | 90 | 110 | 85 | 115 | μs |
| | | $C_{EXT}$ = 0.1 μF; $R_{EXT}$ = 10 kΩ | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 0.9 | 1 | 1.1 | 0.9 | 1.1 | 0.85 | 1.15 | ms |

**Table 7. Dynamic characteristics** *...continued*

*GND = 0 V; For test circuit see Figure 12.*

| Symbol | Parameter | Conditions | | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| $t_{rtrig}$ | retrigger time | $\overline{nA}$ to nB; $C_{EXT}$ = 100 pF; $R_{EXT}$ = 1 kΩ; $C_L$ = 50 pF; see Figure 8 and Figure 10 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | - | 60 | - | - | - | - | - | ns |
| | | $\overline{nA}$ to nB; $C_{EXT}$ = 0.01 μF; $R_{EXT}$ = 1 kΩ; $C_L$ = 50 pF; see Figure 8 and Figure 10 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | - | 1.5 | - | - | - | - | - | μs |
| $C_{PD}$ | power dissipation capacitance | $C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ | [4] | - | 58 | - | - | - | - | - | pF |
| **External components** | | | | | | | | | | | |
| $R_{EXT}$ | external resistance | $V_{CC}$ = 2.0 V | | 5 | - | - | - | - | - | - | kΩ |
| | | $V_{CC}$ > 3.0 V | | 1 | - | - | - | - | - | - | kΩ |
| $C_{EXT}$ | external capacitance | $V_{CC}$ = 2.0 V | [5] | - | - | - | - | - | - | - | pF |
| | | $V_{CC}$ > 3.0 V | [5] | - | - | - | - | - | - | - | pF |

[1] Typical values are measured at nominal supply voltage ($V_{CC}$ = 3.3 V and $V_{CC}$ = 5.0 V).

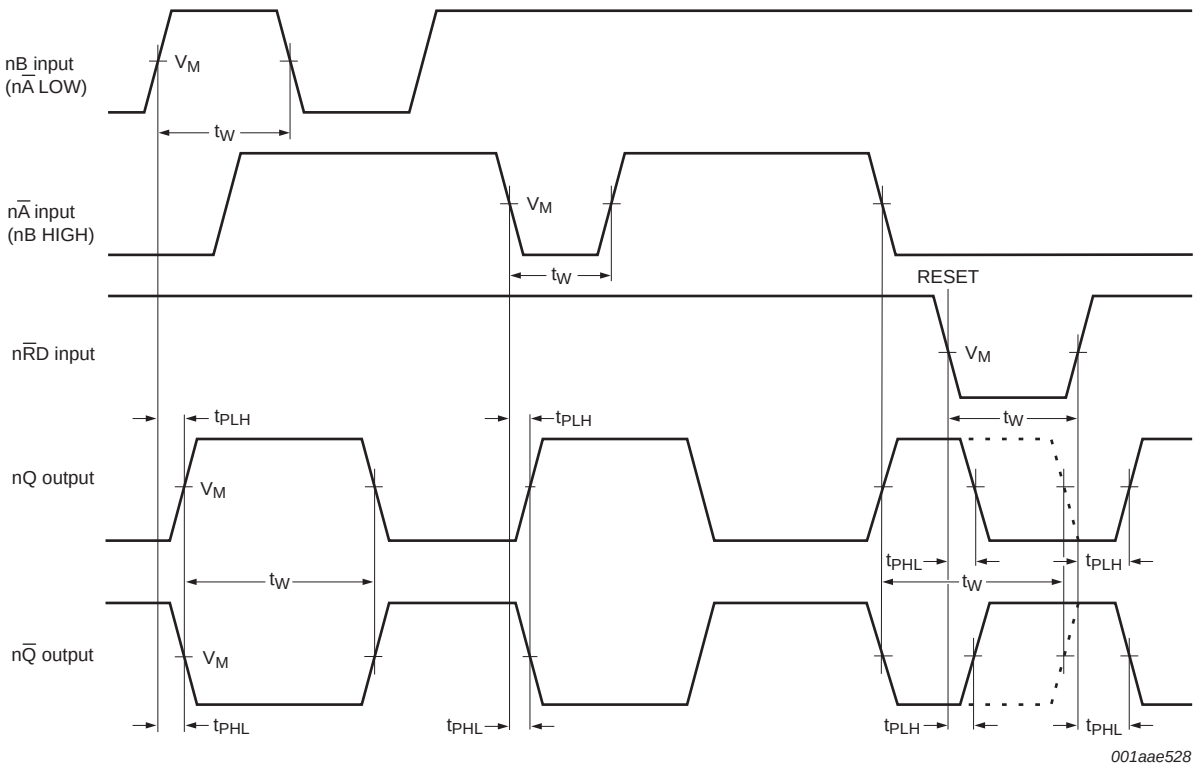
[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $C_{EXT}$ = 0 pF; $R_{EXT}$ = 5 kΩ.

[3] For $C_{EXT} \geq 10$ nF the typical value of the pulse width $t_W$ (μs) = $C_{EXT}$ (nF) × $R_{EXT}$ (kΩ).

[4] $C_{PD}$ is used to determine the dynamic power dissipation $P_D$ (μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V.

[5] $C_{EXT}$ has no limits.

## 11. Waveforms

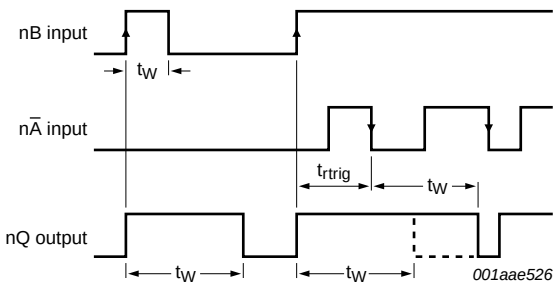



Measurement points are given in Table 8.

**Fig 7. Propagation delay input (nA, nB, nRD) to output (nQ, nQ)**

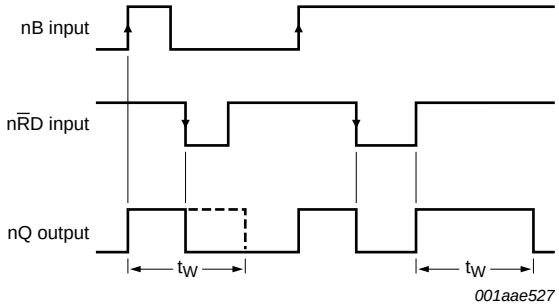
**Table 8. Measurement points**

| Type | Input | Output |
|---|---|---|
| | $V_M$ | $V_M$ |
| 74AHC123A | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74AHCT123A | 1.5 V | $0.5V_{CC}$ |




nRD = HIGH

**Fig 8. Output pulse control using retrigger pulse**




nA̅ = LOW

**Fig 9. Output pulse control using reset input nR̄D**

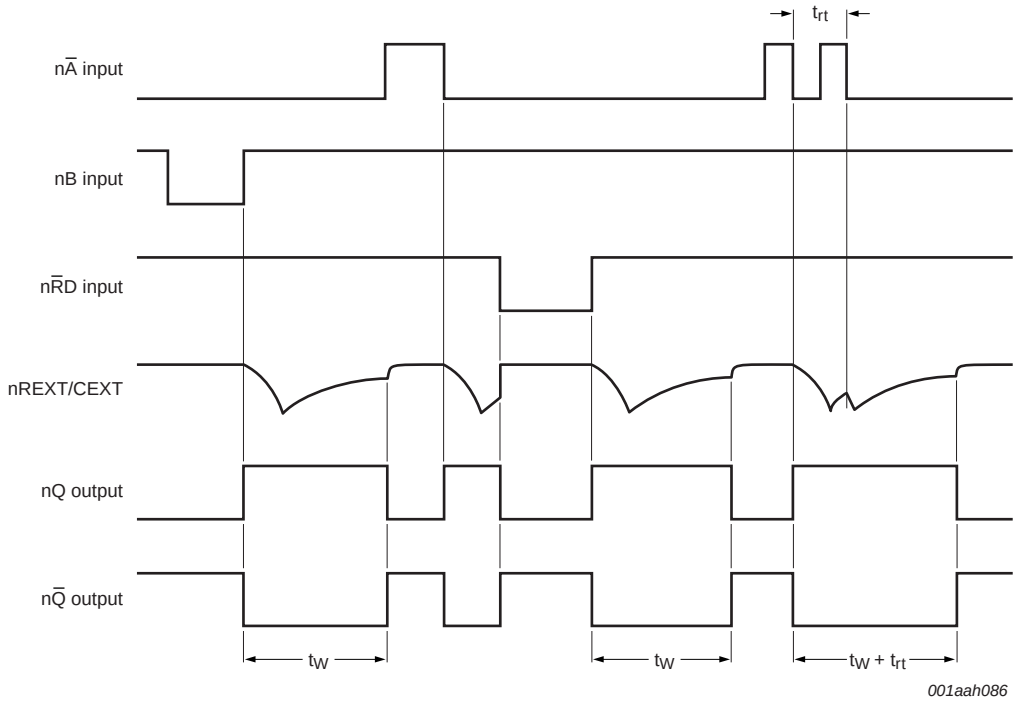



**Fig 10. Input and output timing**

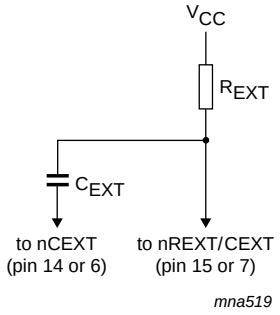
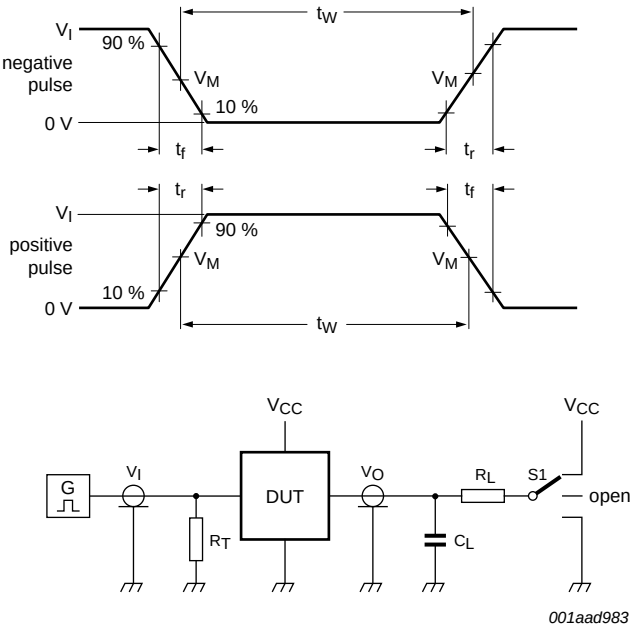



**Fig 11. Timing component connections**




Test data is given in Table 9.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator

$C_L$ = Load capacitance including jig and probe capacitance

$R_L$ = Load resistor

S1 = Test selection switch

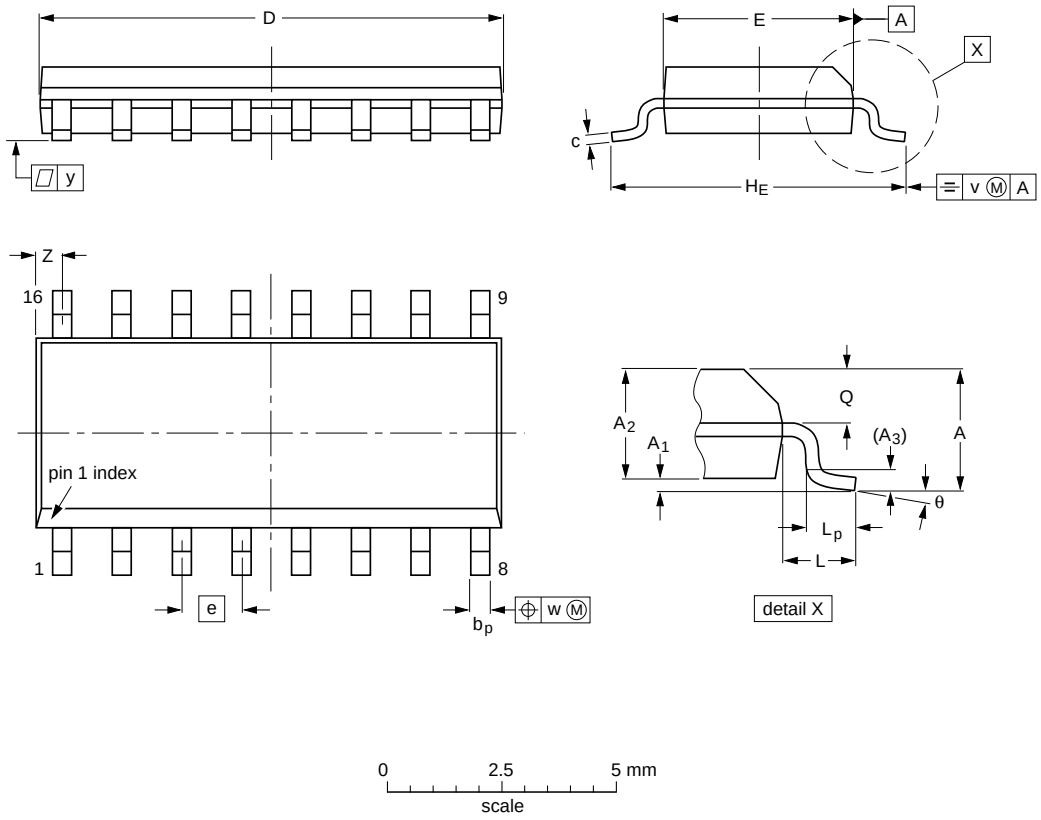
**Fig 12. Load circuitry for switching times**

**Table 9. Test data**

| Type | Input | | Load | | S1 position | | |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| 74AHC123A | $V_{CC}$ | 3.0 ns | 15 pF, 50 pF | 1 kΩ | open | GND | $V_{CC}$ |
| 74AHCT123A | 3.0 V | 3.0 ns | 15 pF, 50 pF | 1 kΩ | open | GND | $V_{CC}$ |

## 12. Package outline

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

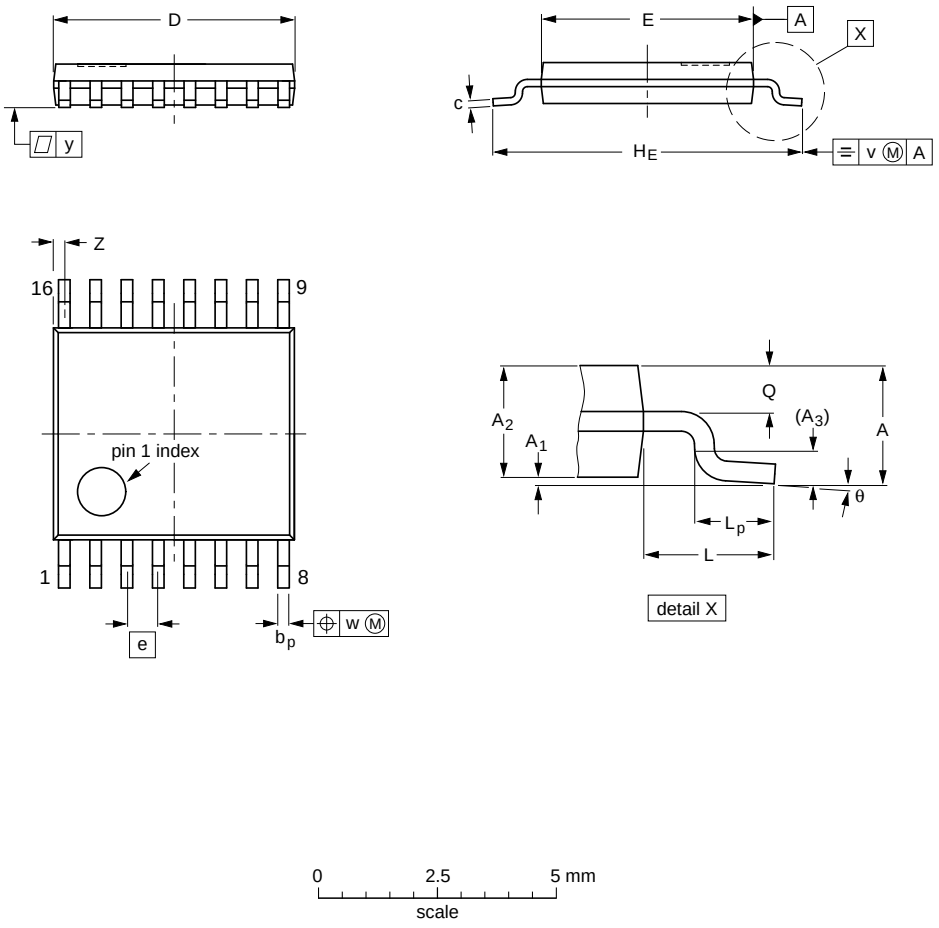
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 13. Package outline SOT109-1 (SO16)**

**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | $8^o$<br>$0^o$ |

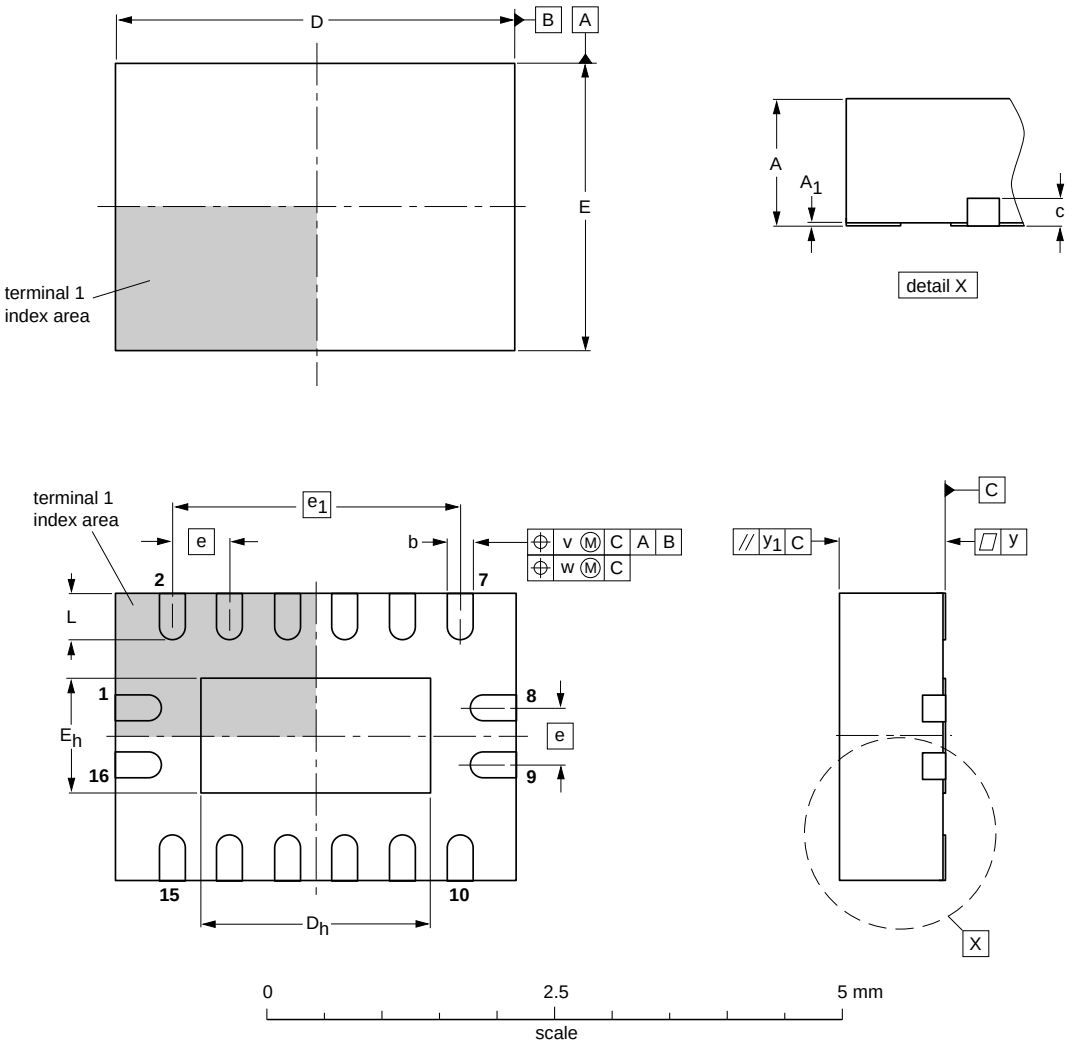
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 14. Package outline SOT403-1 (TSSOP16)**

**DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm** **SOT763-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | $A^{(1)}$ max. | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 3.6<br>3.4 | 2.15<br>1.85 | 2.6<br>2.4 | 1.15<br>0.85 | 0.5 | 2.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT763-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~<br>03-01-27 |

**Fig 15. Package outline SOT763-1 (DHVQFN16)**

## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged-Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74AHC_AHCT123A v.4 | 20111108 | Product data sheet | - | 74AHC_AHCT123A v.3 |
| Modifications: | • Legal pages updated. | | | |
| 74AHC_AHCT123A v.3 | 20110908 | Product data sheet | - | 74AHC_AHCT123A v.2 |
| 74AHC_AHCT123A v.2 | 20080118 | Product data sheet | - | 74AHC_AHCT123A v.1 |
| 74AHC_AHCT123A v.1 | 20000315 | Product specification | - | - |

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## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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