74LVC1G386

3-input EXCLUSIVE-OR gate

Rev. 4 — 9 May 2017 **Product data sheet**

1 General description

The 74LVC1G386 provides a 3-input EXCLUSIVE-OR function.

The input can be driven from either 3.3 or 5 V devices. This feature allows the use of these devices in a mixed 3.3 and 5 V environment.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall time.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2 Features and benefits

- Wide supply voltage range from 1.65 to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ±24 mA output drive (V_{CC} = 3.0 V)
- Latch-up performance exceeds 250 mA
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- ESD protection:
  - HBM EIA/JESD22-A114E exceeds 2 000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- SOT363 and SOT457 package
- Specified from -40 to +85 °C and -40 to +125 °C.

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G386GW	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
74LVC1G386GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4 Marking

Table 2. Marking

Type number	Marking code [1]
74LVC1G386GW	YH
74LVC1G386GV	YH

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5 Functional diagram

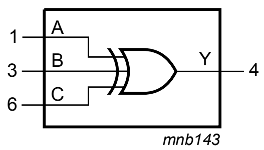

Figure 1. Logic symbol

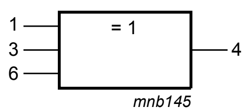

Figure 2. IEC logic symbol

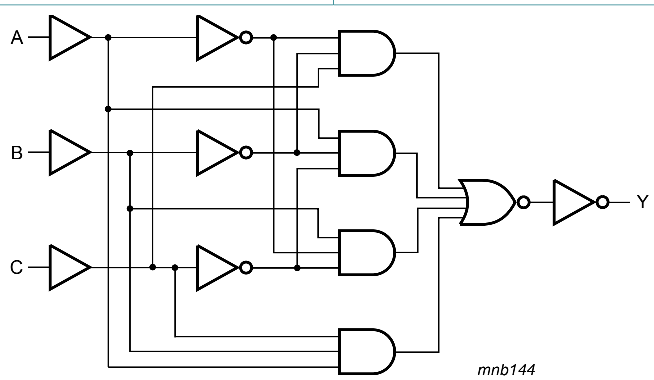

Figure 3. Logic diagram

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6 Pinning information

6.1 Pinning

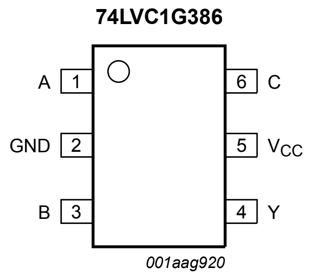

Figure 4. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
A	1	data input
GND	2	ground (0 V)
B	3	data input
Y	4	data output
V_{CC}	5	supply voltage
C	6	data input

7 Functional description

Table 4. Function table [1]

Input			Output
A	B	C	Y
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

[1] H = HIGH voltage level;
L = LOW voltage level

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8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	Active mode [1] [2]	-0.5	V_{CC} + 0.5	V
		Power-down mode [1] [2]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [3]	-	250	mW
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.
[3] For SC-74 and SC-88 packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V_O
		V_{CC} = 0 V; Power-down mode	0	-	5.5	V_O
T_{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

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10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -100 μA; V_{CC} = 1.65 V to 5.5 V	V_{CC} - 0.1	-	-	V
		I_O = -4 mA; V_{CC} = 1.65 V	1.2	-	-	V
		I_O = -8 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	2.2	-	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	2.3	-	-	V
		I_O = -32 mA; V_{CC} = 4.5 V	3.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	V
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND	-	±0.1	±1	μA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	±0.1	±2	μA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	0.1	4	μA
ΔI_{CC}	additional supply current	per pin; V_{CC} = 2.3 V to 5.5 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	5	500	μA
C_I	input capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC}	-	4	-	pF
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V

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Symbol	Parameter	Conditions	Min	Typy [1]	Max	Unit
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = -100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} - 0.1	-	-	V
		I_O = -4 mA; V_{CC} = 1.65 V	0.95	-	-	V
		I_O = -8 mA; V_{CC} = 2.3 V	1.7	-	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	1.9	-	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	2.0	-	-	V
		I_O = -32 mA; V_{CC} = 4.5 V	3.4	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.80	V
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND	-	-	±1	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	-	±2	µA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	-	4	µA
ΔI_{CC}	additional supply current	per pin; V_{CC} = 2.3 V to 5.5 V; $V_I = V_{CC}$ - 0.6 V; I_O = 0 A	-	-	500	µA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

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11 Dynamic characteristics

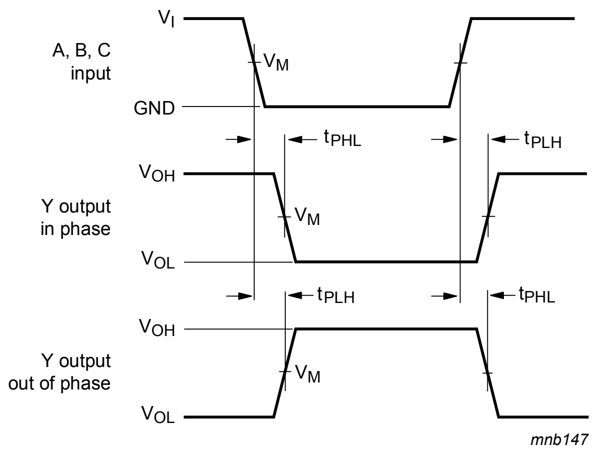
Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	A, B, C to Y; see Figure 5 [2]						
		V_{CC} = 1.65 V to 1.95 V	2.0	8.0	17.0	2.0	22.0	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	5.0	9.0	1.5	11.5	ns
		V_{CC} = 2.7 V	1.5	5.0	8.5	1.5	11.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	4.5	7.5	1.0	9.5	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	3.5	5.5	1.0	7.0	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3 V [3]	-	13	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1 Waveforms and test circuit



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 5. Input A, B, C to output Y propagation delays

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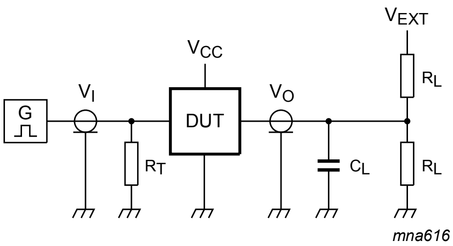
Table 9. Measurement points

V_{CC}	V_M	Input	
		V_I	$t_r = t_f$
1.65 V to 1.95 V	0.5 × V_{CC}	V_{CC}	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V_{CC}	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V_{CC}	V_{CC}	≤ 2.5 ns



Test data is given in Table 10.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

Figure 6. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load		V_{EXT}
V_{CC}	V_I	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	30 pF	1 kΩ	open
2.3 V to 2.7 V	V_{CC}	30 pF	500 Ω	open
2.7 V	2.7 V	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	50 pF	500 Ω	open

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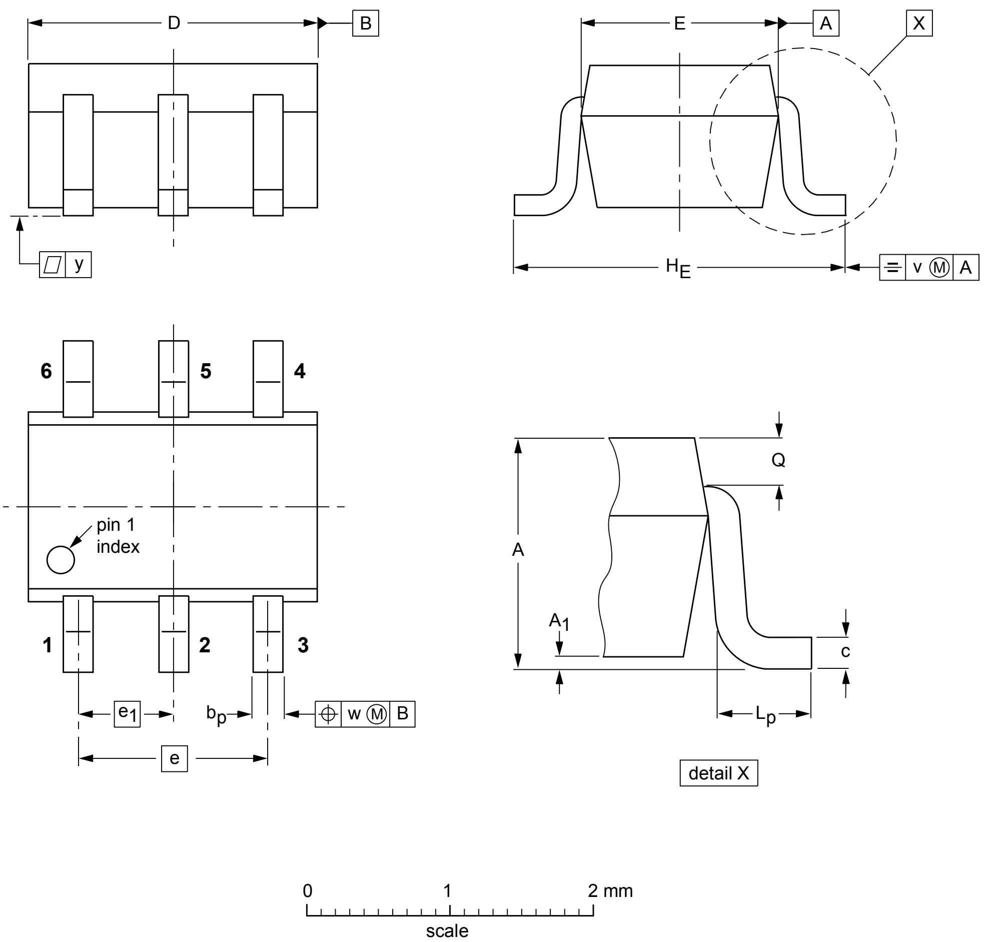
12 Package outline

Plastic surface-mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			~~04-11-08~~ 06-03-16

Figure 7. Package outline SOT363 (SC-88)

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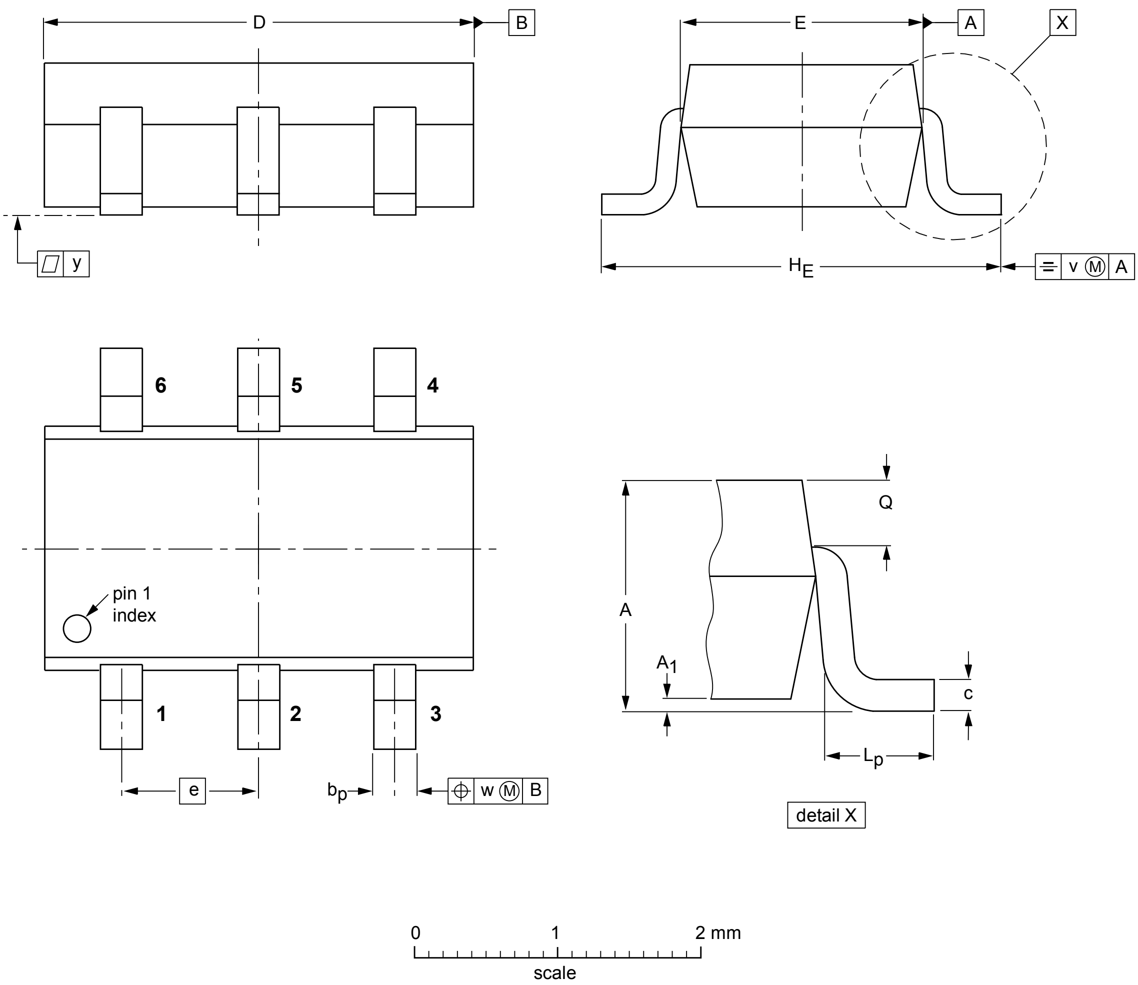
Plastic surface-mounted package (TSOP6); 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~05-11-07~~ 06-03-16

Figure 8. Package outline SOT457 (SC-74)

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13 Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G386 v.4	20170509	Product data sheet	-	74LVC1G386 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate			
74LVC1G386 v.3	20161207	Product data sheet	-	74LVC1G386 v.2
Modifications:	• Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC1G386 v.2	20121119	Product data sheet	-	74LVC1G386 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • In Section 10 "Static characteristics", changed conditions for input leakage and supply current.			
74LVC1G386 v.1	20031104	Product specification	-	

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15 Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

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