

74AHCU04-Q100

Hex unbuffered inverter

Rev. 2 — 7 December 2015

Product data sheet

1. General description

The 74AHCU04-Q100 is high-speed Si-gate CMOS device and is pin compatible with low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHCU04-Q100 is a general-purpose hex unbuffered inverter. Each of the six inverters is a single stage.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

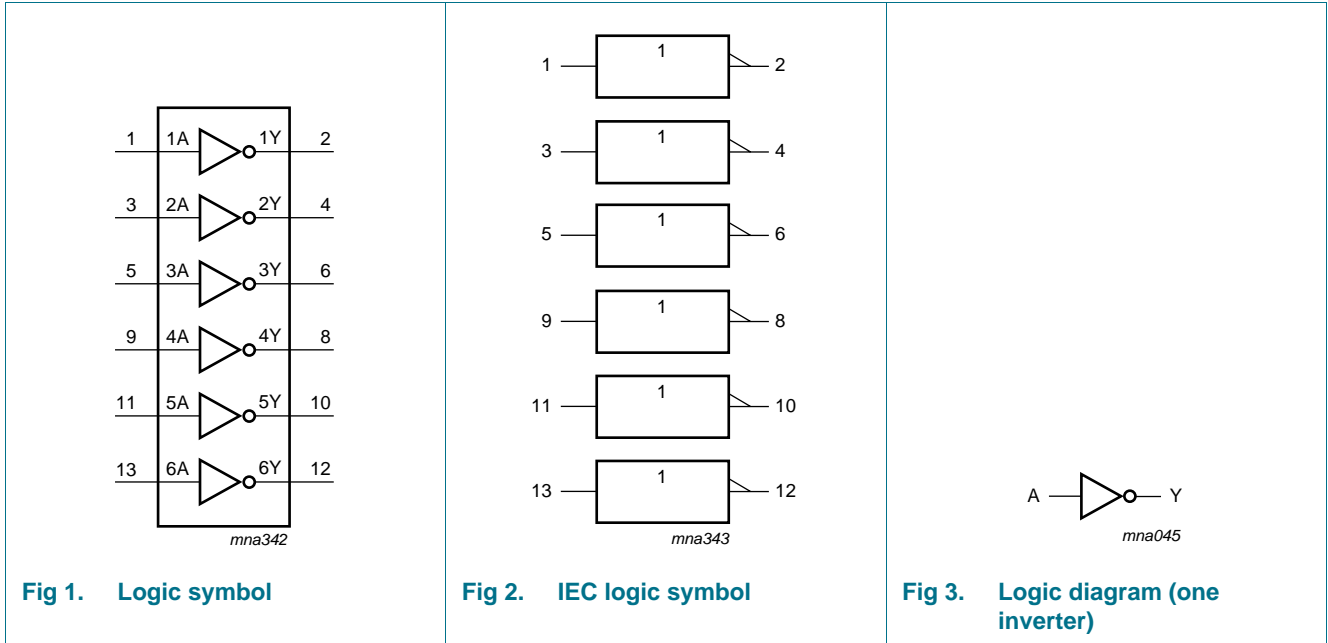
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Low power dissipation
- Balanced propagation delays
- Inputs accept voltages higher than V_{CC}
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- Multiple package options

3. Ordering information

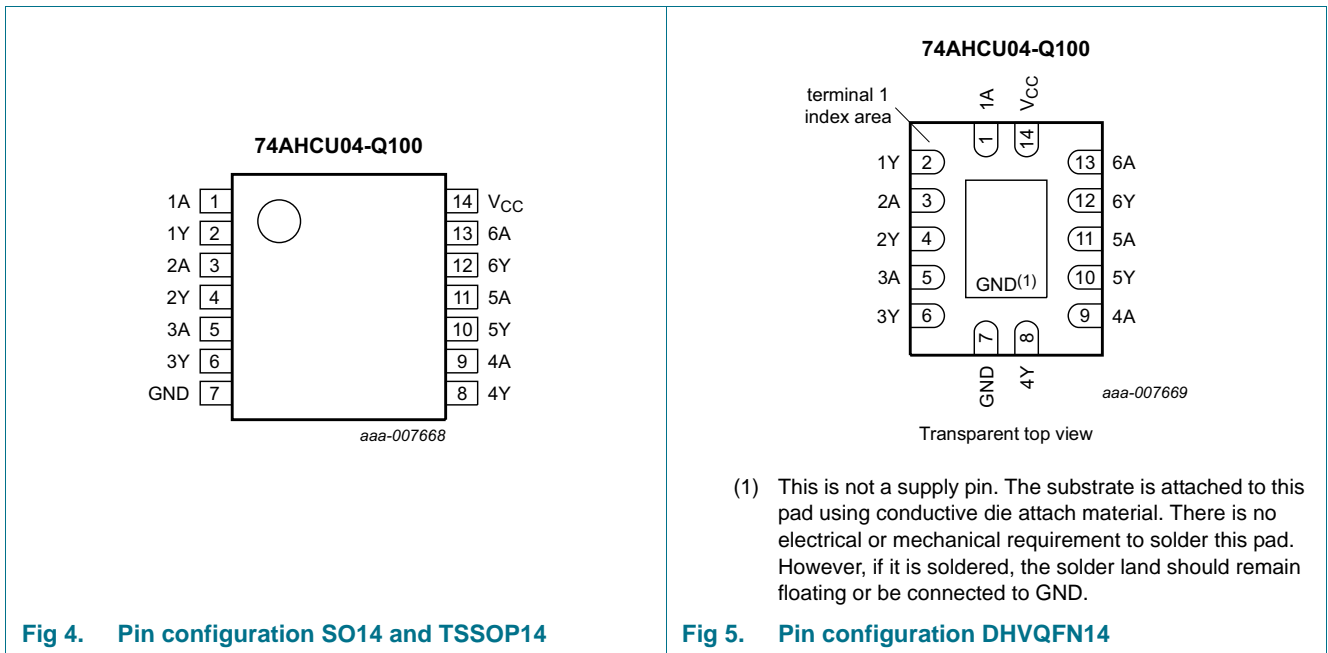
Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AHCU04D-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCU04PW-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCU04BQ-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1

4. Functional diagram



5. Pinning information



5.1 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
nA	nY
L	H
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V	-20	-	mA
V _I	input voltage		[1] -0.5	+7.0	V
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-	-	100	ns/V
		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0 \text{ V}$	1.7	-	-	1.7	-	1.7	-	V
		$V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.4	-	2.4	-	V
		$V_{CC} = 5.5 \text{ V}$	4.4	-	-	4.4	-	4.4	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0 \text{ V}$	-	-	0.3	-	0.3	-	0.3	V
		$V_{CC} = 3.0 \text{ V}$	-	-	0.6	-	0.6	-	0.6	V
		$V_{CC} = 5.5 \text{ V}$	-	-	1.1	-	1.1	-	1.1	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = -50 \mu\text{A}$; $V_{CC} = 2.0 \text{ V}$	1.8	2.0	-	1.8	-	1.8	-	V
		$I_O = -50 \mu\text{A}$; $V_{CC} = 3.0 \text{ V}$	2.7	3.0	-	2.7	-	2.7	-	V
		$I_O = -50 \mu\text{A}$; $V_{CC} = 4.5 \text{ V}$	4.0	4.5	-	4.0	-	4.0	-	V
		$I_O = -4.0 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.4	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 50 \mu\text{A}$; $V_{CC} = 2.0 \text{ V}$	-	0	0.2	-	0.2	-	0.2	V
		$I_O = 50 \mu\text{A}$; $V_{CC} = 3.0 \text{ V}$	-	0	0.3	-	0.3	-	0.3	V
		$I_O = 50 \mu\text{A}$; $V_{CC} = 4.5 \text{ V}$	-	0	0.5	-	0.5	-	0.5	V
		$I_O = 4.0 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
		$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μA
C_I	input capacitance		-	3	10	-	10	-	10	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics
GND = 0 V; For test circuit see Figure 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Figure 6 [1]								
		V _{CC} = 3.0 V to 3.6 V [2]								
		C _L = 15 pF	-	3.0	7.1	1.0	8.5	1.0	9.0	ns
		C _L = 50 pF	-	3.4	10.6	1.0	12.0	1.0	13.5	ns
		V _{CC} = 4.5 V to 5.5 V [3]								
		C _L = 15 pF	-	2.4	5.5	1.0	6.5	1.0	7.0	ns
		C _L = 50 pF	-	3.5	7.0	1.0	8.0	1.0	9.0	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} [4]	-	9.1	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [2] Typical values are measured at V_{CC} = 3.3 V.
- [3] Typical values are measured at V_{CC} = 5.0 V.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms

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$V_M = 0.5 \times V_{CC}; V_I = \text{GND to } V_{CC}.$

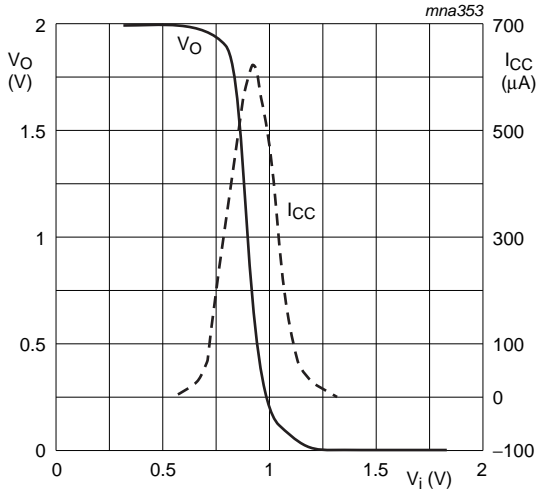
Fig 6. The input (nA) to output (nY) propagation delay times

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Test data is given in [Table 7](#).
 Definitions for test circuit:
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

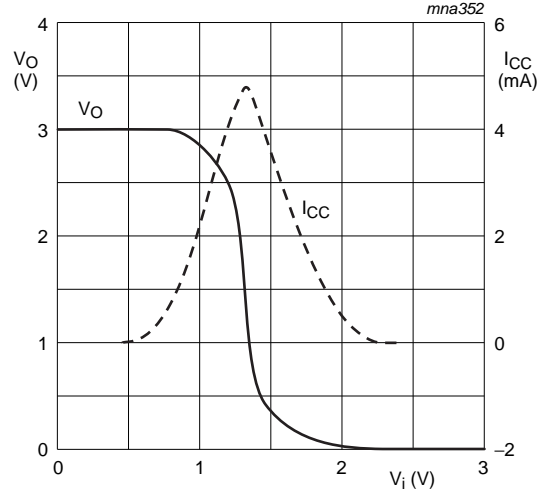
Fig 7. Test circuit for measuring switching times

12. Typical transfer characteristics



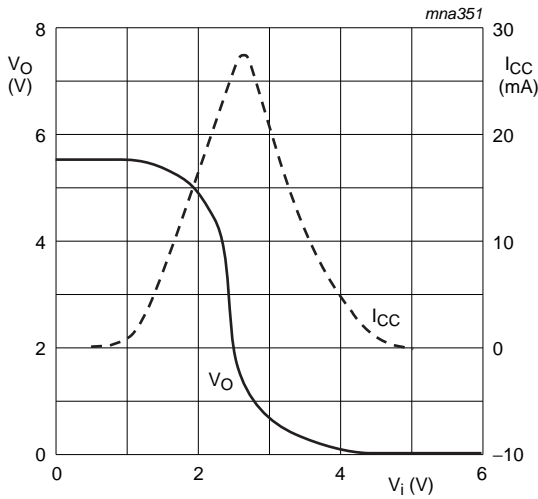
T_{amb} = 25 °C.

Fig 8. V_{CC} = 2.0 V; I_O = 0 A



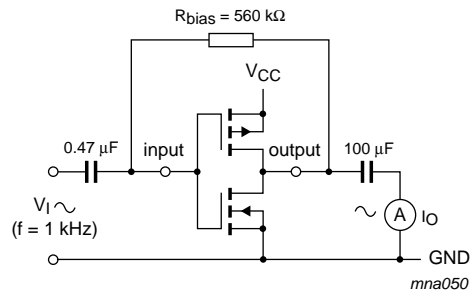
T_{amb} = 25 °C.

Fig 9. V_{CC} = 3.0 V; I_O = 0 A



T_{amb} = 25 °C.

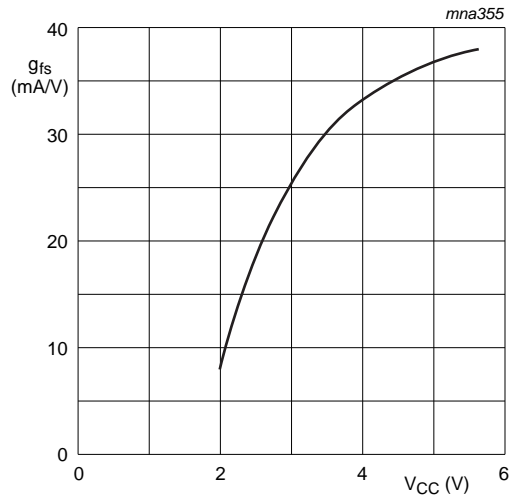
Fig 10. V_{CC} = 5.5 V; I_O = 0 A



$$g_{fs} = \frac{\Delta I_O}{\Delta V_I}$$

f_i = 1 kHz at V_O is constant

Fig 11. Test set-up for measuring forward transconductance



T_{amb} = 25 °C.

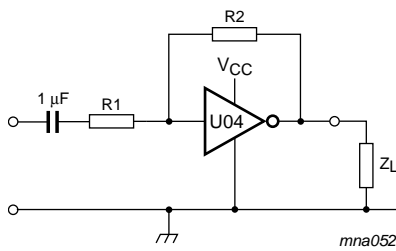
Fig 12. Typical forward transconductance as a function of the supply voltage

13. Application information

Some applications are:

- Linear amplifier (see [Figure 13](#))
- Crystal oscillator design (see [Figure 14](#))

Remark: All values given are typical unless otherwise specified.



Maximum V_{o(p-p)} = V_{CC} - 1.5 V centered at 0.5 × V_{CC}.

$$G_v = - \frac{G_{ol}}{1 + \frac{R1}{R2}(1 + G_{ol})}$$

G_{ol} = open loop gain

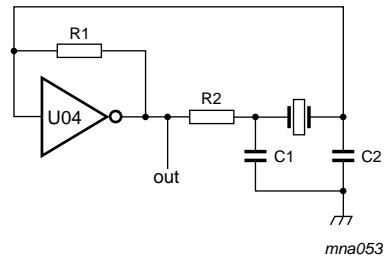
G_v = voltage gain

R1 ≥ 3 kΩ, R2 ≤ 1 MΩ

Z_L > 10 kΩ; G_{ol} = 12 (typical)

Typical unity gain bandwidth product is 5 MHz.

Fig 13. Used as a linear amplifier



C1 = 47 pF (typical)

C2 = 33 pF (typical)

R1 = 1 MΩ to 10 MΩ (typical)

R2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC}. I_{CC} is typically 5 mA at V_{CC} = 5 V and f_i = 10 MHz.

Fig 14. Crystal oscillator configuration

Table 8. External components for resonator (f < 1 MHz)

All values given are typical and must be used as an initial set-up.

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 M Ω	220 k Ω	56 pF	20 pF
16 kHz to 24.9 kHz	22 M Ω	220 k Ω	56 pF	10 pF
25 kHz to 54.9 kHz	22 M Ω	100 k Ω	56 pF	10 pF
55 kHz to 129.9 kHz	22 M Ω	100 k Ω	47 pF	5 pF
130 kHz to 199.9 kHz	22 M Ω	47 k Ω	47 pF	5 pF
200 kHz to 349.9 kHz	10 M Ω	47 k Ω	47 pF	5 pF
350 kHz to 600 kHz	10 M Ω	47 k Ω	47 pF	5 pF

Table 9. Optimum value for R2

Frequency	R2	Optimum for
3 kHz	2.0 k Ω	minimum required I _{CC}
	8.0 k Ω	minimum influence due to change in V _{CC}
6 kHz	1.0 k Ω	minimum required I _{CC}
	4.7 k Ω	minimum influence by V _{CC}
10 kHz	0.5 k Ω	minimum required I _{CC}
	2.0 k Ω	minimum influence by V _{CC}
14 kHz	0.5 k Ω	minimum required I _{CC}
	1.0 k Ω	minimum influence by V _{CC}
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF

14. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

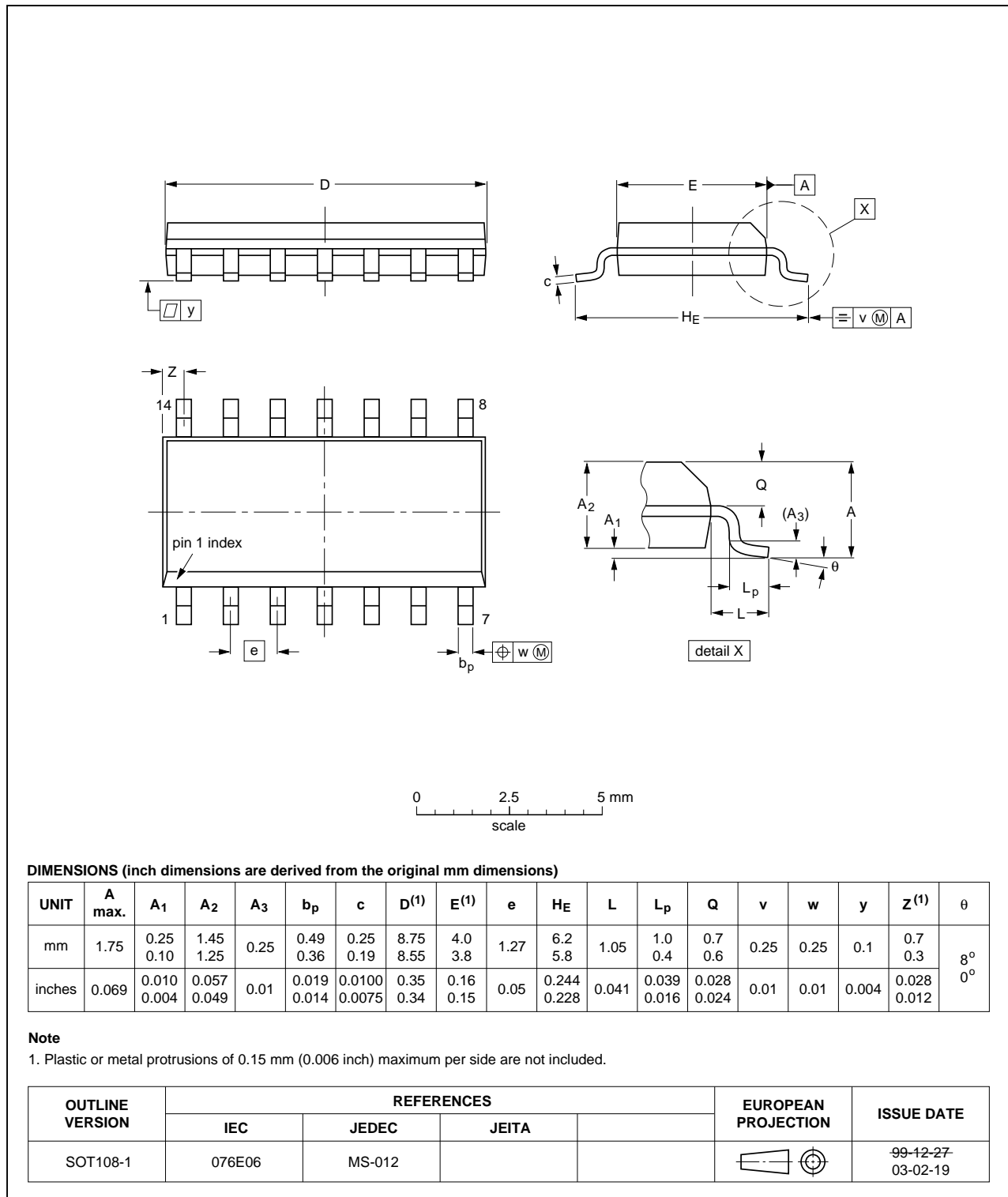


Fig 15. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

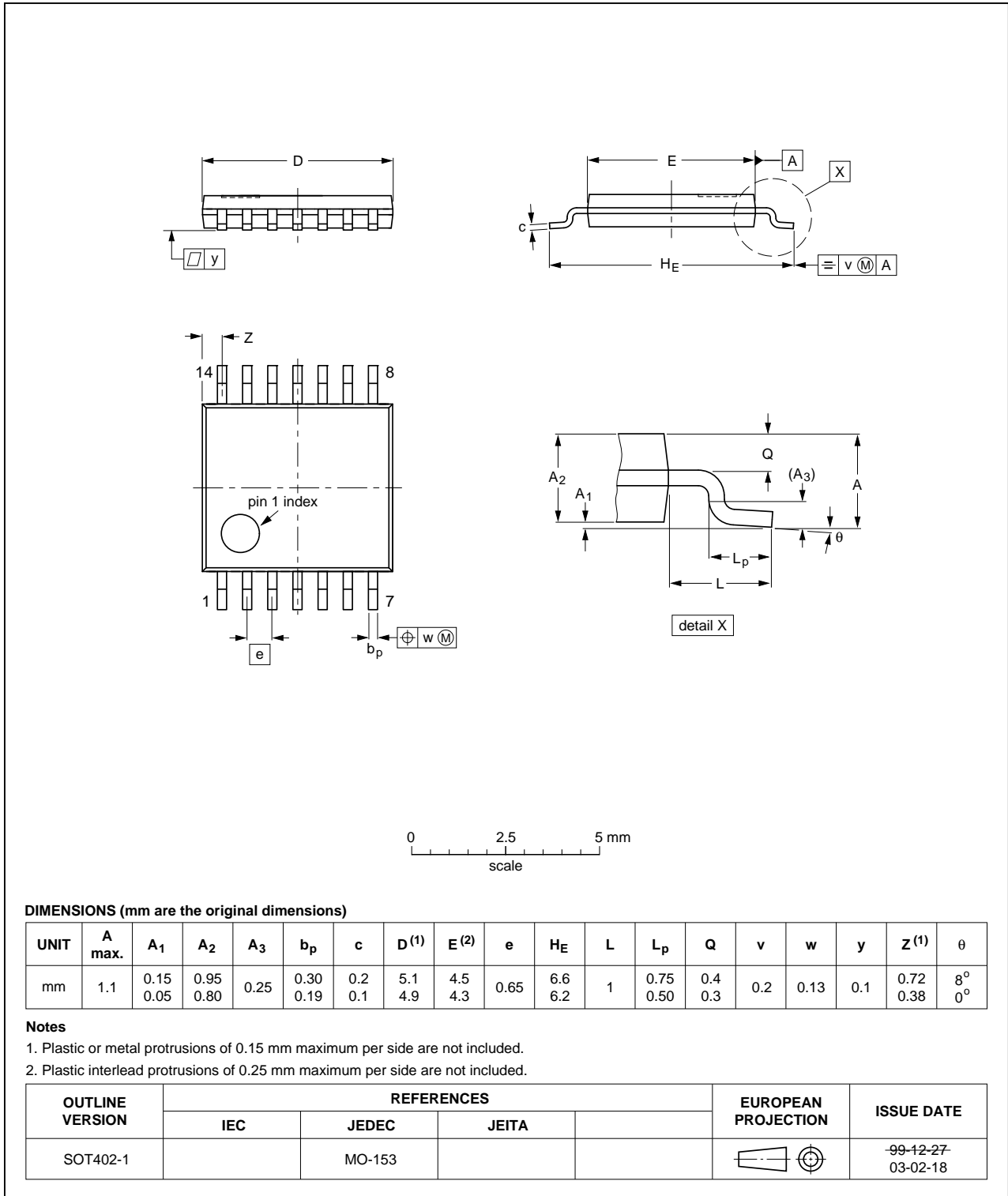


Fig 16. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

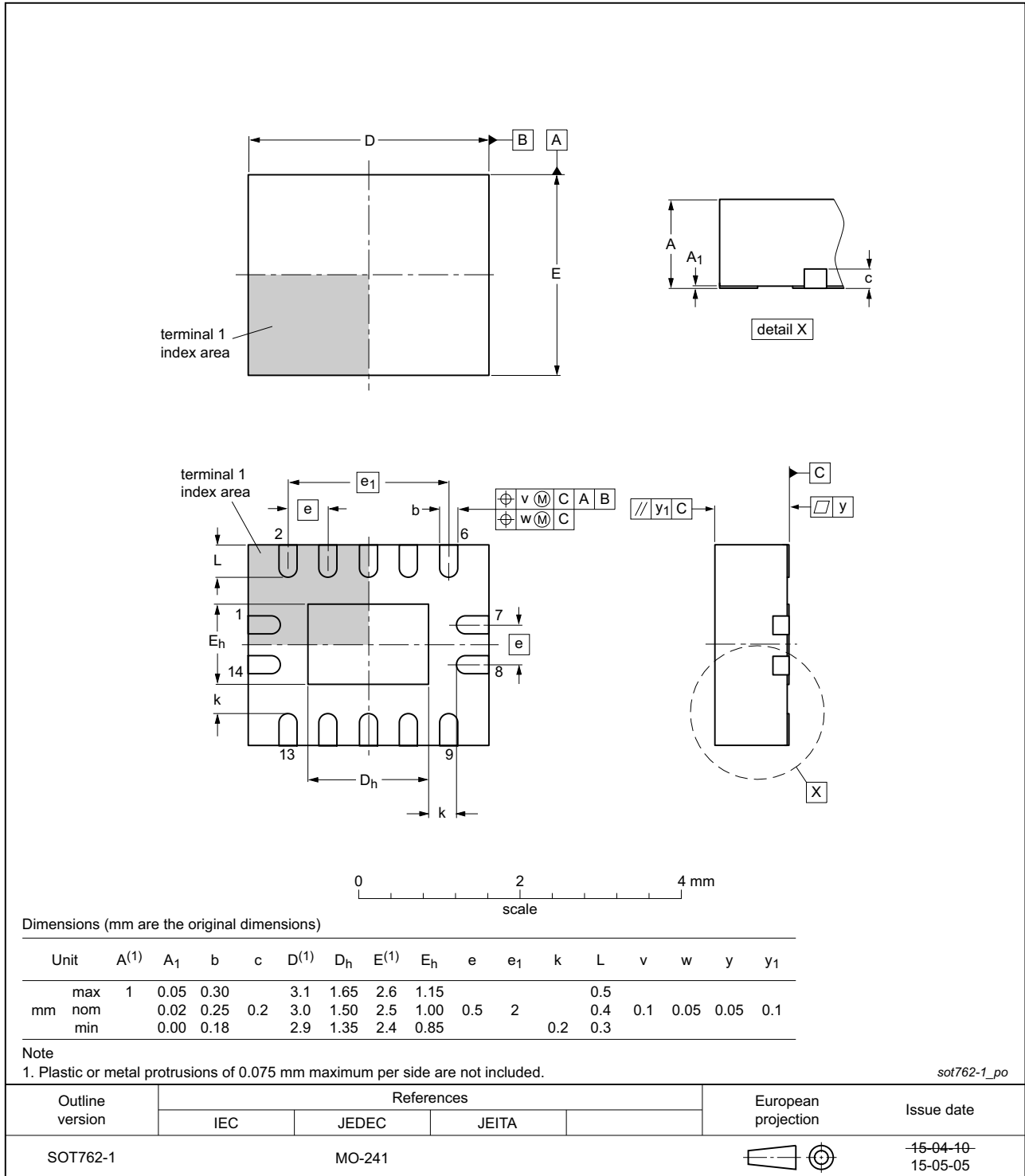


Fig 17. Package outline SOT762-1 (DHVQFN14)

15. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge Device Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHCU04_Q100 v.2	20151207	Product data sheet	-	74AHCU04_Q100 v.1
Modifications:	• General description corrected (added "-Q100" to product types (errata)).			
74AHCU04_Q100 v.1	20130605	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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