

# 74CBTLVD3244

8-bit level-shifting bus switch with 4-bit output enables

Rev. 3 — 5 April 2019

Product data sheet

## 1. General description

The 74CBTLVD3244 is a dual 4-pole, single-throw bus switch. The device features two output enable inputs ( $n\overline{OE}$ ) that each control four switch channels. The switches are disabled when the associated  $n\overline{OE}$  input is HIGH. Schmitt trigger action at control inputs makes the circuit tolerant of slower input rise and fall times. This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Supply voltage range from 3.0 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-B/JESD36 (3.0 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - CDM AEC-Q100-011 revision B exceeds 1000 V
- 5  $\Omega$  switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74CBTLVD3244PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74CBTLVD3244BQ	-40 °C to +125 °C	DHVQFN20	plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

### 4. Functional diagram

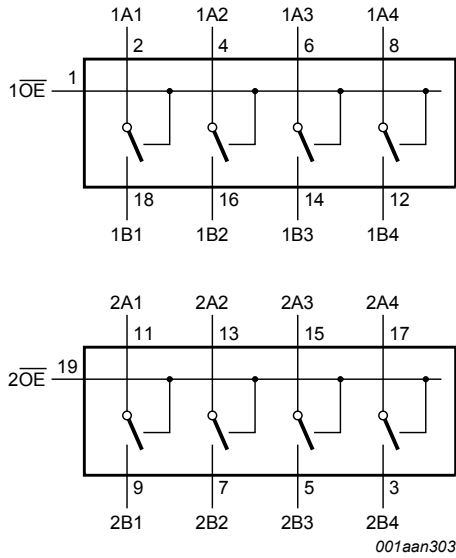


Fig. 1. Logic symbol

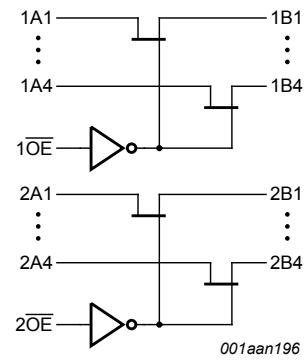


Fig. 2. Logic diagram

### 5. Pinning information

#### 5.1. Pinning

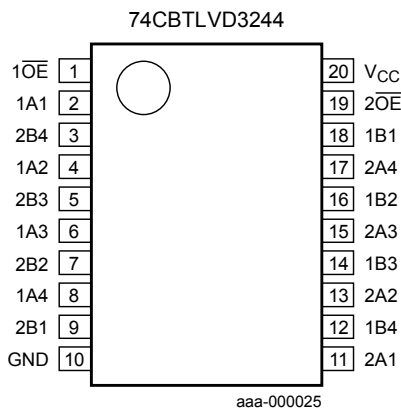
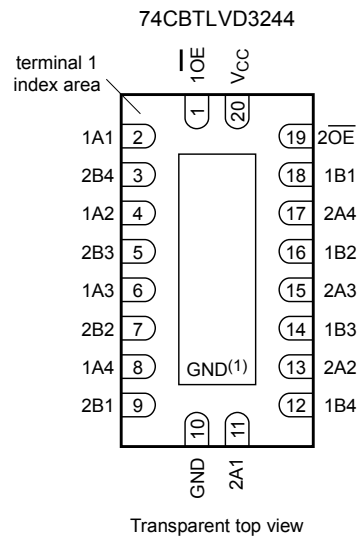


Fig. 3. Pin configuration SOT360-1 (TSSOP20)



(1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However if it is soldered the solder land should remain floating or be connected to GND.

Fig. 4. Pin configuration SOT764-1 (DHVQFN20)

## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active LOW)
1A1 to 1A4	2, 4, 6, 8	data input/output (A port)
2B1 to 2B4	9, 7, 5, 3	data input/output (B port)
GND	10	ground (0 V)
2A1 to 2A4	11, 13, 15, 17	data input/output (A port)
1B1 to 1B4	18, 16, 14, 12	data input/output (B port)
V <sub>CC</sub>	20	positive supply voltage

## 6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	Input/output
nOE	nAn, nBn
L	nAn = nBn
H	Z

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage	[1]	-0.5	+4.6	V
V <sub>SW</sub>	switch voltage	enable and disable mode [1]	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	input clamping current	V <sub>I/O</sub> < -0.5 V	-50	-	mA
I <sub>SK</sub>	switch clamping current	V <sub>I</sub> < -0.5 V	-50	-	mA
I <sub>SW</sub>	switch current	V <sub>SW</sub> = 0 V to V <sub>CC</sub>	-	±128	mA
I <sub>CC</sub>	supply current		-	+100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C [2]	-	500	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP20 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 5.5 mW/K.  
For DHVQFN20 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 4.5 mW/K.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		3.0	3.6	V
$V_I$	input voltage		0	3.6	V
$V_{SW}$	switch voltage	enable and disable mode	0	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [1]	0	200	ns/V

[1] Applies to control signal levels.

## 9. Static characteristics

Table 6. Static characteristics

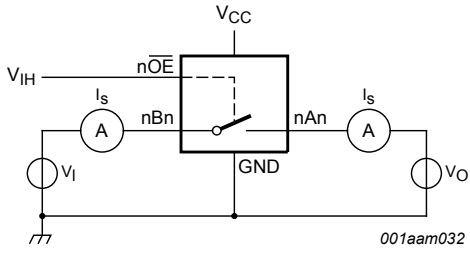
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			$T_{amb} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ [1]	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	0.9	-	0.9	V
$I_I$	input leakage current	pin $n\overline{OE}$ ; $V_I = \text{GND to }V_{CC}$ ; $V_{CC} = 3.6\text{ V}$	-	-	$\pm 1$	-	$\pm 20$	$\mu\text{A}$
$V_{pass}$	pass voltage	$V_I = V_{CC}$ ; see Fig. 7 to Fig. 11	-	-	-	-	-	V
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 3.6\text{ V}$ ; see Fig. 5	-	-	$\pm 1$	-	$\pm 20$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 3.6\text{ V}$ ; see Fig. 6	-	-	$\pm 1$	-	$\pm 20$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 0\text{ V to }3.6\text{ V}$ ; $V_{CC} = 0\text{ V}$	-	-	$\pm 10$	-	$\pm 50$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ ; $I_O = 0\text{ A}$ ; $V_{CC} = 3.6\text{ V}$ ; $V_{SW} = \text{GND or }V_{CC}$	-	-	20	-	50	$\mu\text{A}$
		$V_I = \text{GND}$ ; $I_O = 0\text{ A}$ ; $V_{CC} = 3.6\text{ V}$ ; $V_{SW} = \text{GND or }V_{CC}$	-	-	100	-	150	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	pin $n\overline{OE}$ ; $V_I = V_{CC} - 0.6\text{ V}$ ; $V_{SW} = \text{GND or }V_{CC}$ ; $V_{CC} = 3.6\text{ V}$ [2]	-	-	300	-	2000	$\mu\text{A}$
$C_I$	input capacitance	pin $n\overline{OE}$ ; $V_{CC} = 3.3\text{ V}$ ; $V_I = 0\text{ V to }3.3\text{ V}$	-	0.9	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance	$V_{CC} = 3.3\text{ V}$ ; $V_I = 0\text{ V to }3.3\text{ V}$	-	2.5	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	$V_{CC} = 3.3\text{ V}$ ; $V_I = 0\text{ V to }3.3\text{ V}$	-	9.0	-	-	-	pF

[1] All typical values are measured at  $T_{amb} = 25\text{ °C}$ .

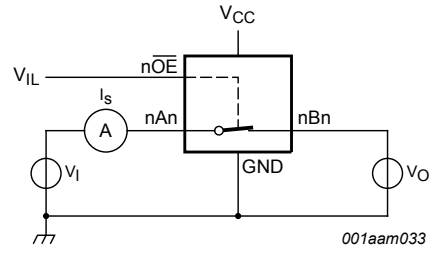
[2] One input at 3 V, other inputs at  $V_{CC}$  or GND.

9.1. Test circuits



$V_I = V_{CC}$  or  $GND$  and  $V_O = GND$  or  $V_{CC}$ .

Fig. 5. Test circuit for measuring OFF-state leakage current (one switch)



$V_I = V_{CC}$  or  $GND$  and  $V_O =$  open circuit.

Fig. 6. Test circuit for measuring ON-state leakage current (one switch)

9.2. Typical pass voltage graphs

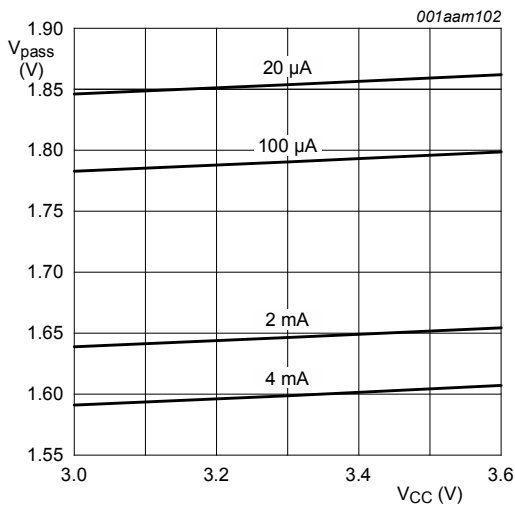


Fig. 7. Pass voltage versus supply voltage;  $T_{amb} = 125\text{ °C}$  (typical)

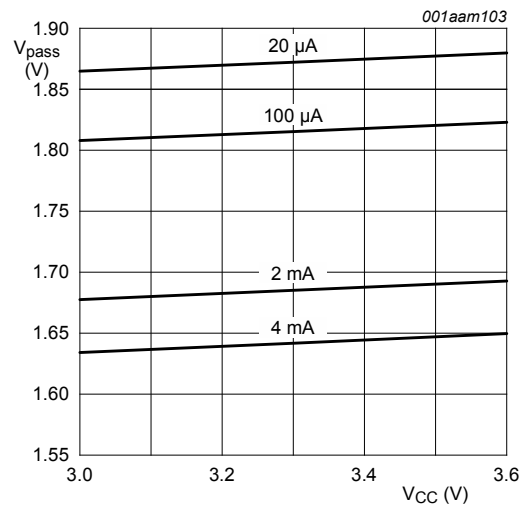


Fig. 8. Pass voltage versus supply voltage;  $T_{amb} = 85\text{ °C}$  (typical)

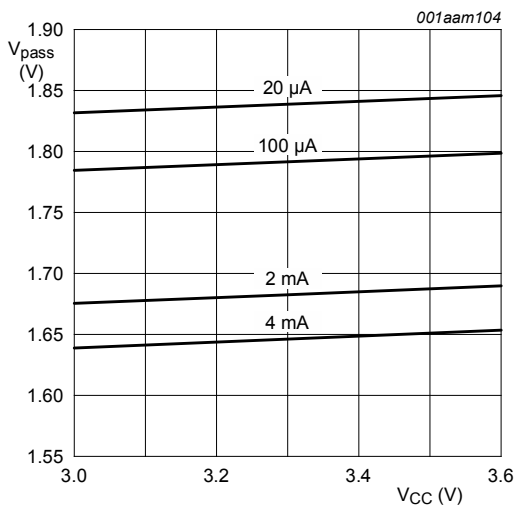


Fig. 9. Pass voltage versus supply voltage;  $T_{amb} = 25\text{ °C}$  (typical)

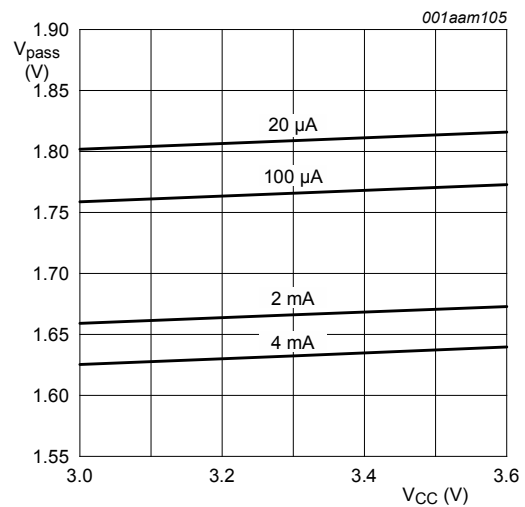


Fig. 10. Pass voltage versus supply voltage;  $T_{amb} = 0\text{ °C}$  (typical)

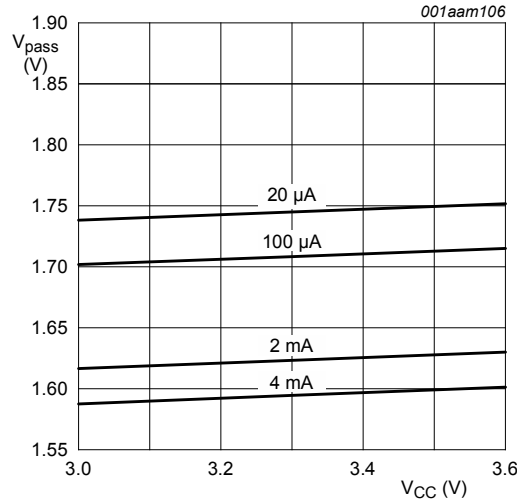


Fig. 11. Pass voltage versus supply voltage;  $T_{amb} = -40\text{ °C}$  (typical)

### 9.3. ON resistance

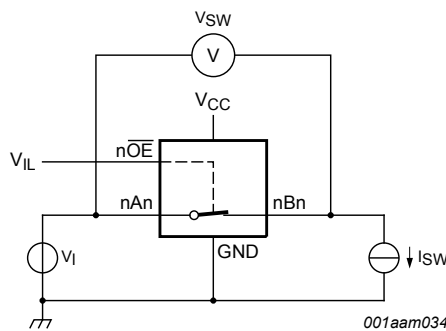
Table 7. Resistance  $R_{ON}$

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 12.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			$T_{amb} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ [1]	Max	Min	Max	
$R_{ON}$	ON resistance	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [2]						
		$I_{SW} = 64\text{ mA}; V_I = 0\text{ V}$	-	3.7	7.0	-	10.0	$\Omega$
		$I_{SW} = 24\text{ mA}; V_I = 0\text{ V}$	-	3.7	7.0	-	10.0	$\Omega$
		$I_{SW} = 15\text{ mA}; V_I = 1.2\text{ V}$	-	4.7	10.0	-	12.0	$\Omega$

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and nominal  $V_{CC}$ .

[2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



$$R_{ON} = V_{SW} / I_{SW}$$

Fig. 12. Test circuit for measuring ON resistance (one switch)

## 10. Dynamic characteristics

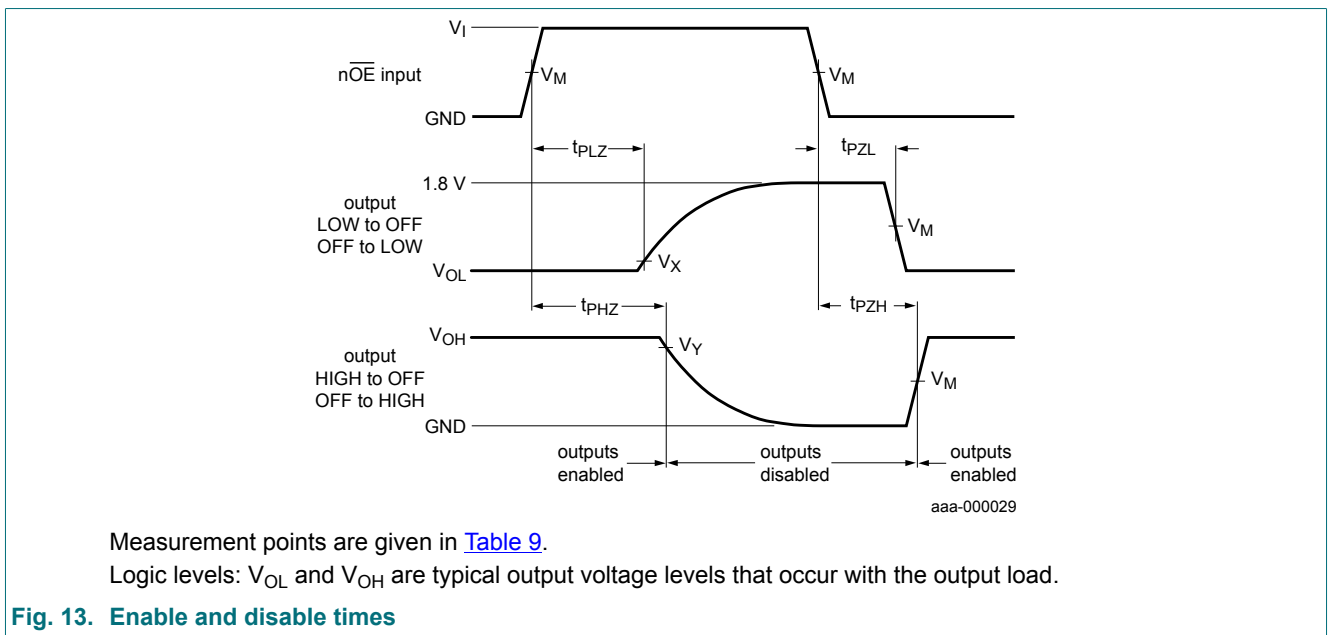
**Table 8. Dynamic characteristics**

$GND = 0\text{ V}$ ; for test circuit see [Fig. 15](#)

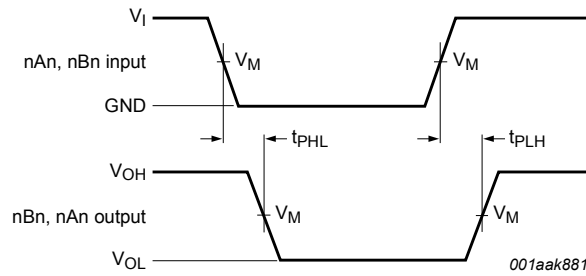
Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			$T_{amb} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ [1]	Max	Min	Max	
$t_{pd}$	propagation delay	nAn to nBn or nBn to nAn; $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ; see <a href="#">Fig. 14</a> [2][3]	-	-	0.11	-	0.22	ns
$t_{en}$	enable time	$\overline{nOE}$ to nAn or nBn; $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ; see <a href="#">Fig. 13</a> [4]	1.5	2.8	5.0	1.5	6.0	ns
$t_{dis}$	disable time	$\overline{nOE}$ to nAn or nBn; $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ; see <a href="#">Fig. 13</a> [5]	0.8	3.1	7.0	0.8	8.0	ns

- [1] All typical values are measured at  $T_{amb} = 25\text{ °C}$  and at nominal  $V_{CC}$ .
- [2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
- [3]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [4]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .
- [5]  $t_{dis}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .

### 10.1. Waveforms and test circuit



8-bit level-shifting bus switch with 4-bit output enables



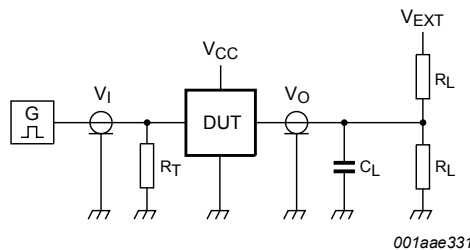
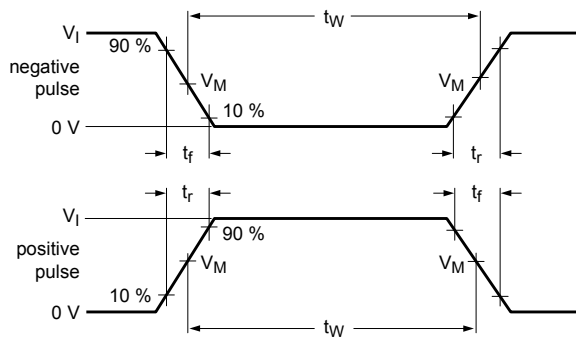
Measurement points are given in [Table 9](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 14. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times**

**Table 9. Measurement points**

Supply voltage	Input			Output		
$V_{CC}$	$V_M$	$V_I$	$t_r = t_f$	$V_M$	$V_X$	$V_Y$
3.0 V to 3.6 V	$0.5V_{CC}$	$V_{CC}$	$\leq 2.0$ ns	0.9 V	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V



Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 15. Test circuit for measuring switching times**

**Table 10. Test data**

Supply voltage	Load		$V_{EXT}$		
$V_{CC}$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
3.0 V to 3.6 V	30 pF	1 k $\Omega$	open	GND	3.6 V



10.2. Additional dynamic characteristics

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $V_I = GND$  or  $V_{CC}$  (unless otherwise specified);  $t_r = t_f \leq 2.5$  ns.

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			Unit
			Min	Typ [1]	Max	
f <sub>(-3dB)</sub>	-3 dB frequency response	V <sub>CC</sub> = 3.3 V; R <sub>L</sub> = 50 Ω; see Fig. 16 [2]	-	575	-	MHz

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 3.3 V.

[2] f<sub>i</sub> is biased at 0.5V<sub>CC</sub>.

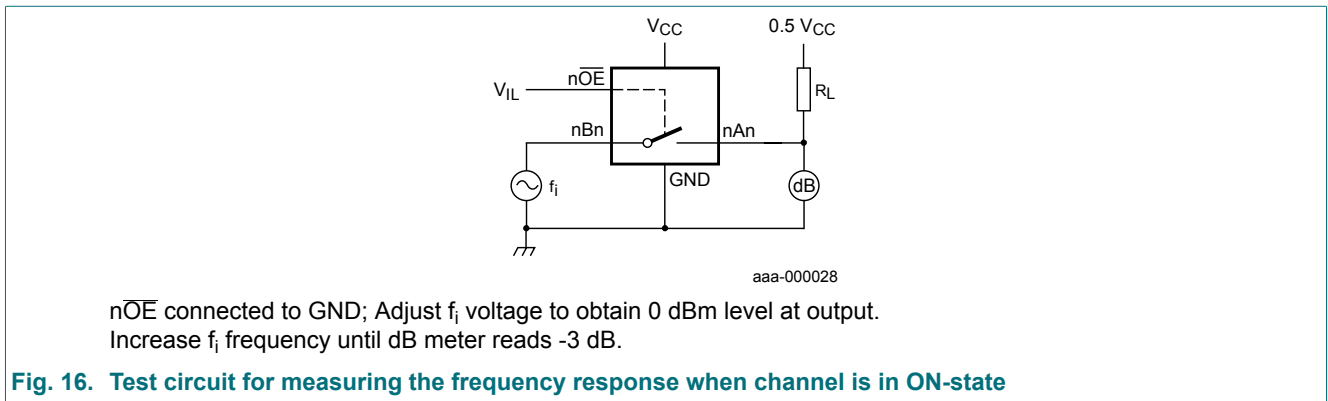


Fig. 16. Test circuit for measuring the frequency response when channel is in ON-state

### 11. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

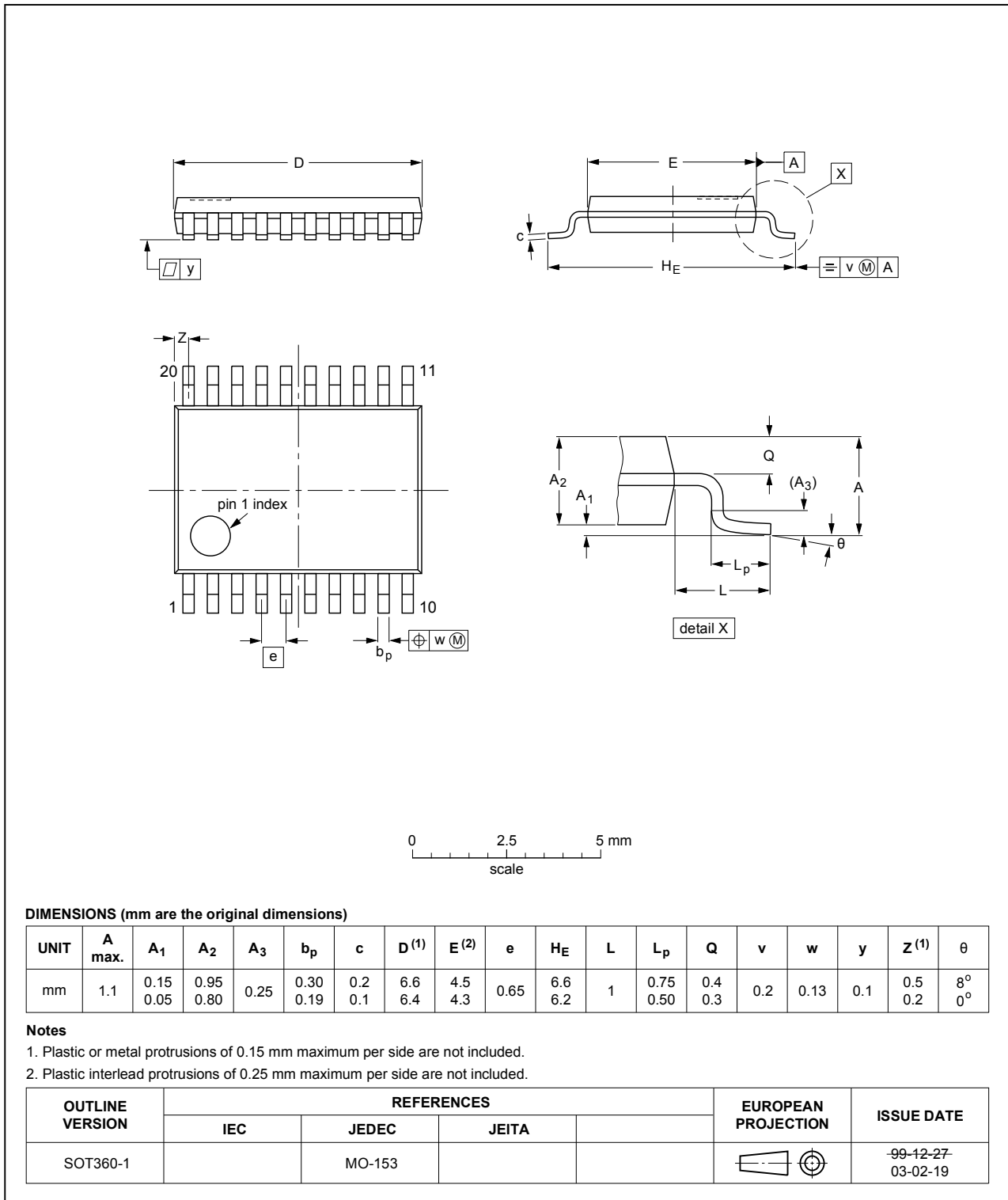


Fig. 17. Package outline SOT360-1 (TSSOP20)



## 12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

## 13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLVD3244 v.3	20190405	Product data sheet	-	74CBTLVD3244 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74CBTLVD3244DS (SSOP20/SOT724-1) removed.</li> <li>Package outline drawing <a href="#">SOT764-1</a> (DHSVFN20) updated.</li> <li>Typo corrected in <a href="#">Table 2</a>.</li> </ul>			
74CBTLVD3244 v.2	20111216	Product data sheet	-	74CBTLVD3244 v.1
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74CBTLVD3244 v.1	20110715	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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## Contents

<b>1. General description</b> .....	<b>1</b>
<b>2. Features and benefits</b> .....	<b>1</b>
<b>3. Ordering information</b> .....	<b>1</b>
<b>4. Functional diagram</b> .....	<b>2</b>
<b>5. Pinning information</b> .....	<b>2</b>
5.1. Pinning.....	2
5.2. Pin description.....	3
<b>6. Functional description</b> .....	<b>3</b>
<b>7. Limiting values</b> .....	<b>3</b>
<b>8. Recommended operating conditions</b> .....	<b>4</b>
<b>9. Static characteristics</b> .....	<b>4</b>
9.1. Test circuits.....	5
9.2. Typical pass voltage graphs.....	5
9.3. ON resistance.....	6
<b>10. Dynamic characteristics</b> .....	<b>7</b>
10.1. Waveforms and test circuit.....	7
10.2. Additional dynamic characteristics.....	9
<b>11. Package outline</b> .....	<b>10</b>
<b>12. Abbreviations</b> .....	<b>12</b>
<b>13. Revision history</b> .....	<b>12</b>
<b>14. Legal information</b> .....	<b>13</b>

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**Date of release: 5 April 2019**

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