MYD-CZU3EG Development Board

- > MYC-CZU3EG CPU Module as Controller Board
- Xilinx Zynq UltraScale+ ZU3EG MPSoC based on 1.2 GHz Quad Arm Cortex-A53 and 600MHz Dual Cortex-R5 Cores
- > 4GB DDR4 SDRAM (64bit, 2400MHz)
- > 4GB eMMC Flash, 128MB QSPI Flash
- > USB 3.0, Gigabit Ethernet, CAN, TF, DisplayPort (DP), PCIe interface, SATA interface, JTAG...
- > 2 x PMoD, 1 x FMC, 4 x SFP+ (only for EV MPSoCs), ARDUINO User Interface, HDMI, LCD
- > Optional 7-inch LCD Modules and USB Camera Module
- Ready-to-Run Linux 4.9.0



Figure 1-1 MYD-CZU3EG development board

The <u>MYD-CZU3EG development board</u> consists of the <u>MYC-CZU3EG CPU Module</u> and a specially designed base board to provide a complete and versatile platform for evaluating and prototyping based on Xilinx Zynq UltraScale+ MPSoC devices.

The <u>MYC-CZU3EG CPU Module</u> is an Arm SOM with integrated XCZU3EG-1SFVC784E MPSoC, 4GB DDR4, 4GB eMMC, and 128MB QSPI Flash, Ethernet PHY, USB PHY and Intel Power Module. It is mounted on the MYD-CZU3EG base board through two 0.5mm pitch 160-pin Razor Beam High-Speed Sockets.

The <u>MYD-CZU3EG</u> Zynq UltraScale+ ZU3EG MPSoC development board has extended a rich peripheral set and interfaces on the base board through connectors and headers including USB 3.0, Gigabit Ethernet, CAN, TF, DisplayPort (DP), PCIe interface, SATA interface, JTAG, HDMI, LCD interface, ARDUINO User Interface, PMoD, FMC, and four SFP+ interfaces (for EV MPSoCs only).

The <u>MYD-CZU3EG</u> is capable of running Linux OS and comes with necessary cable accessories as well as detailed documentations and software package. Typical applications are the Internet, cloud computing, Data center, Machine Vision, Military facilities, Flight navigation and other embedded applications.





Figure 1-3 MYC-CZU3EG CPU Module

Hardware Specification

Zynq[®] UltraScale+[™] MPSoC devices provide 64-bit processor scalability while combining real-time control with soft and hard engines for graphics, video, waveform, and packet processing. Built on a common real-time processor and programmable logic equipped platform, three distinct variants include dual application processor (CG) devices, quad application processor and GPU (EG) devices, and video codec (EV) devices.

	CG Devices	EG Devices	EV Devices
Application Processor	Dual-core ARM [®] Cortex [™] -A53 MPCore [™] up to 1.3GHz	Quad-core ARM Cortex-A53 MPCore up to 1.5GHz	Quad-core ARM Cortex-A53 MPCore up to 1.5GHz
Real-Time Processor	Dual-core ARM Cortex-R5 MPCore up to 533MHz	Dual-core ARM Cortex-R5 MPCore up to 600MHz	Dual-core ARM Cortex-R5 MPCore up to 600MHz
Graphics Processor		Mali™-400 MP2	Mali™-400 MP2
Video Codec			H.264 / H.265
Programmable Logic	103K–600K System Logic Cells	103K–1143K System Logic Cells	192K–504K System Logic Cells
Applications	 Sensor Processing & Fusion Motor Control Low-cost Ultrasound Traffic Engineering 	 Flight Navigation Missile & Munitions Military Construction Secure Solutions Networking Cloud Computing Security Data Center Machine Vision Medical Endoscopy 	 Situational Awareness Surveillance/Reconnaissance Smart Vision Image Manipulation Graphic Overlay Human Machine Interface Automotive ADAS Video Processing Interactive Display

Figure 1-4 Zynq UltraScale+ MPSoCs

The Zynq UltraScale+ family provides footprint compatibility to enable users to migrate designs from one device to another. Any two packages with the same footprint identifier code (last letter and number sequence) are footprint compatible. MYIR is using the **XCZU3EG-1SFVC784E** MPSoC for <u>MYD-CZU3EG</u> by default, the C784 package covers the widest footprint compatibilities that enable users to select devices among CG, EG and EV.

			Zynq® UltraScale+™																		
Disc		CG Devices			EG Devices									EV Devices							
Ркд	mm	ZU2CG ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EC	SZU17EG	ZU19EG	ZU4EV	ZU5EV	ZU7EV
A484	19																				
A625	21																				
C784	23		-										-		-		-		-	-0	
B900	31			-		-8				-0-	-		-						-	-8-	-0
C900	31				-		-				-			-	-	-0					
B1156	35				-		-			-		-8-	-	-0		-0					
C1156	35					-	-				-	-	-		-8-	1	-			_	-0
B1517	40														-		-	-			
F1517	40					-	-								-					_	
C1760	42.5														-						
D1760	42.5																-	-			
E1924	45									1							-				

Figure 1-5 Zynq $\ensuremath{\mathbb{R}}$ UltraScale+ $\ensuremath{^{\texttt{MPSoC}}}$ Device Migration Table

MYIR may also supply the <u>MYD-CZU3EG development boards</u> with XCZU2CG, XCZU3CG, XCZU4EV or XCZU5EV MPSoC as options. The main features for the MPSoC devices are summarized as below.

Device	XCZU2CG	XCZU3CG	XCZU3EG	XCZU4EV	XCZU5EV			
Logic cells (k)	103	154	154	192	256			
CLB Flip-Flops (K)	94	141	141	176	234			
CLB LUTs (K)	47 71		71	88	117			
Block RAM (Mb)	5.3 7.6		7.6	4.5	5.1			
UltraRAM (Mb)			-	13.5	18.0			
DSP Slices	240	360	360	728	1,248			
GTX transceivers	PS-GTR4x	x PS-GTR4x PS-GTR4x PS-G		PS-GTR4x (6Gb/s),	PS-GTR4x (6Gb/s),			
	(6Gb/s)	(6Gb/s)	(6Gb/s)	GTH4x (16.3Gb/s)	GTH4x (16.3Gb/s)			
Processor Units								
Application Processor Unit	Dual-core AF	RM®	Quad-core ARM® Cortex [™] -A53 MPCore [™] up to					
	Cortex [™] -A53	B MPCore™	1.5GHz					
	up to 1.3GHz							
Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB							
Real-Time Processor Unit	Dual-core ARM Cortex-R5 MPCore™ up to 600MHz							
Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core							
Graphics Processing Unit	Mali [™] -400 MP2 up to 667MHz							
Video Codec	-	-	- H.264 / H.265					
Memory L2 Cache	64KB							
External Memory, Connectivity, Integrated Block Functionality								
Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC							
Static Memory Interfaces	NAND, 2x Quad-SPI							
High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet							
General Connectivity	2 x USB 2.0, 2 x SD/SDIO, 2 x UART, 2 x CAN 2.0B, 2 x I2C, 2 x SPI, 4 x 32b GPIO							
Power Management	Full / Low / PL / Battery Power Domains							
Security	RSA, AES, and SHA							
AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor							

Table 1-1 MPSoC device selection guide

Mechanical Parameters

- ✓ Dimensions: 60.00mm x 52.00mm (CPU Module), 195.33mm x 123.95mm (base board)
- ✓ PCB Layers: 12-layer design (CPU Module), 6-layer design (base board)
- ✓ Power supply: 3.3V (CPU Module), 12V (base board)
- ✓ Working temp.: 0~70 Celsius (commercial grade)

The MYD-CZU3EG Controller Board (MYC-CZU3EG CPU Module)



Figure 1-6 <u>MYC-CZU3EG CPU Module</u> Top-view



Figure 1-7 <u>MYC-CZU3EG CPU Module</u> Bottom-view

MPSoC

- ✓ Xilinx Zynq UltraScale+ XCZU3EG-1SFVC784E (ZU3EG, 784 Pin Package) MPSoC
 - 1.2 GHz 64 bit Quad-core ARM® Cortex[™]-A53
 - 600MHz Dual-core ARM® Cortex[™]-R5 processor
 - 667MHz ARM Mali[™]-400MP2 Graphics Processor
 - 16nm FinFET+ FPGA fabric

Memory

- ✓ 4GB DDR4 SDRAM (64bit, 2400MHz)
- ✓ 4GB eMMC Flash
- ✓ 128MB QSPI Flash

Peripherals and Signals Routed to Pins

- MYC-CZU3EG Pinouts Description
- ✓ Gigabit Ethernet PHY
- ✓ USB PHY
- ✓ Intel Power Module
- ✓ Clock Generator
- ✓ Watchdog
- ✓ Four LEDs
 - One yellow LED for ERROR_STATUS indicator (indicate a secure lockdown state)
 - One yellow LED for ERROR_OUT indicator (Asserted for accidental power loss, hardware error)
 - One green LED for PS_Done indicator (indicate the pl configuration is done)
 - One green LED for PS_INIT indicator (indicate the ps is initialized after a power-on reset)

- Two 0.5mm pitch 160-pin Razor Beam High-Speed headers bring out
 - 4 PS GTR transceivers along with 2 GTR reference clock inputs
 - PS JTAG interface, USB 2.0 interface, Gigabit Ethernet interface and etc.
 - 4 PL GTH transceivers along with 1 GTH reference clock inputs (only for Zynq UltraScale+ EV Devices)
 - 156 user PL I/O pins

The MYD-CZU3EG Development Board Base Board (MYB-CZU3EG)



Figure 1-8 MYD-CZU3EG Development Board Base Board

PS Unit

- ✓ One USB 3.0 (Type-C interface)
- ✓ One USB to UART port
- ✓ One TF card slot
- ✓ One CAN interface
- ✓ One 10/100/1000Mbps Ethernet interface
- ✓ One PCIe interface
- ✓ One SATA interface
- ✓ One 2.54mm pitch 14-pin JTAG interface (PS, PL reused)
- \checkmark Buttons (one user button, one system reset button and one ps-programming button)
- ✓ One DisplayPort (DP)
- ✓ Battery backed RTC

PL Unit

- ✓ One Xilinx standard LPFMC interface
- ✓ One HDMI interface (signals reused with LCD/TSP interface)
- ✓ Four SFP+ transceiver interfaces (up to 10Gpbs, only for Zynq UltraScale+ EV Devices)
- ✓ Two-channel Pmod
- ✓ ARDUINO user interface
- ✓ LCD/TSP interface (24-bit RGB, supports resistive and capacitive touch screen panels)

- ✓ Three LEDs
- One blue LED for power indicator
- One red LED for FPGA programming indicator
- One green LED for user defined

Function Block Diagram



Figure 1-9 Function Block Diagram of MYD-CZU3EG

Dimension Chart







Software Features

The <u>MYD-CZU3EG Development Board</u> is preloaded with Linux 4.9.0. MYIR provides software package in product disk along with the goods delivery. The software package features as below:

Item	Features	itures Description I						
Cross compiler	gcc 5.2.1	gcc version 5.2.1 (Linaro GCC5.2)						
Boot program	BOOT.BIN	First boot program including FSBL, u-boot	Source code provided					
Linux Kernel	Linux 4.9.0	Customized kernel for MYD-CZU3EG Development Board	Source code provided					
	USB Host	USB2.0/USB3.0 Host driver	Source code provided					
	Ethernet	Gigabit Ethernet driver	Source code provided					
	MMC/SD/TF	MMC/SD/TF card driver	Source code provided					
	CAN	CAN driver	Source code provided					
	LCD Controller	LCD driver	Source code provided					
	DP Controller	DP Display driver	Source code provided					
	HDMI	HDMI (SII902X chip) driver	Source code provided					
	Button	Button driver	Source code provided					
Drivers	UART	UART driver	Source code provided					
	I2C	I2C driver	Source code provided					
	LED	LED driver	Source code provided					
	GPIO	GPIO driver	Source code provided					
	QSPI	QSPI Flash MT25QU512ABB driver	Source code provided					
	Resistive Touch	TSC2007 resistive touch screen driver	Source code provided					
	Capacitive Touch	FT5X0X capacitive touch screen driver	Source code provided					
	SATA	SATA HD driver	Source code provided					
	Watch dog	Watch dog driver	Source code provided					
File Crestory	Ramdisk	Ramdisk system image	File System					
riie System	Rootfs.tar	Buildroot, including QT	Source code provided					
Example	Including button, LED, CAN, RS232, Socket examples							

Table 1-2 Software Features of MYD-CZU3EG

Order Information

Item	Packing List					
MYD-CZU3EG Development Board (Part No.: MYD-CZU3EG-4E4D-1200-C)	 One MYD-CZU3EG Development Board (including the base board and CPU Module with installed active heatsink) One HDMI cable One 12V/5A Power adapter One 1.2m Micro USB2.0 cable One USB A 3.0 to Type-C cable Adapter One 16GB TF card One Product disk (including user manual, datasheet, base board schematic in PDF format and software packages) 					
MYC-CZU3EG CPU Module	MYC-CZU3EG CPU Module					
(Part No.: MYC-CZU3EG-4E4D-1200-C)	 One Product disk 					
MY-LCD70TP LCD Module (Part No.: MY-TFT070RV2)	7-inch LCD Module with resistive touch screen					
MY-LCD70TP-C LCD Module (Part No.: MY-TFT070CV2)	7-inch LCD Module with capacitive touch screen					
MY-CAM002U Camera Module (Part No.: MY-CAM002U)	USB Camera Module					



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