MYD-Y7Z010/007S Development Board

- *MYC-Y7Z010/007S CPU Module as Controller Board*
- *1.27mm pitch 180-pin Stamp Hole Expansion Interface for Board-to-Board Connections*
- *667MHz Xilinx XC7Z010 or XC7Z007S ARM Cortex-A9 Processor with Xilinx 7-series FPGA logic*
- *512MB DDR3 SDRAM (2 x 256MB, 32-bit)*
- *4GB eMMC Flash, 16MB QSPI Flash*
- *USB Host, 3 x Gigabit Ethernet ports, RS232, RS485, CAN, TF, JTAG, GPIO…*
- *Optional 4.3 or 7 inch LCD Module, WiFi Module, Camera Module and IO Extension Cape*
- *Ready-to-Run Linux 3.15.0*

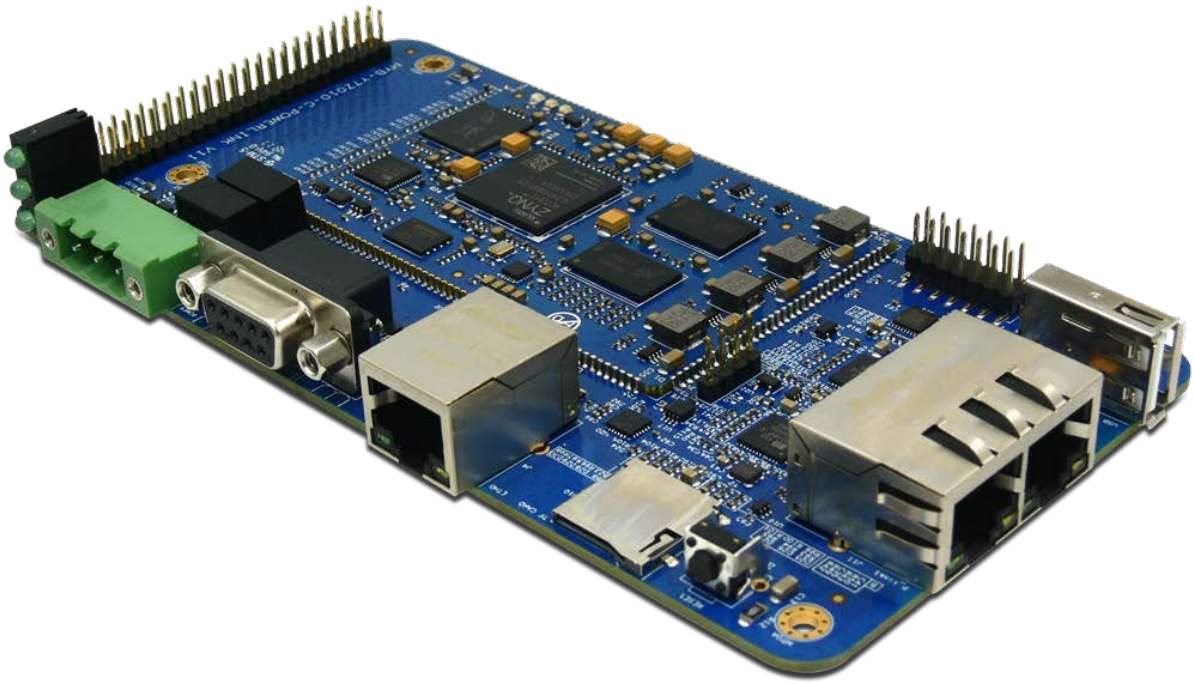

Figure 1-1 MYD-Y7Z010/007S Development Board

Description

The **MYD-Y7Z010/007S development board** is powered by **Xilinx XC7Z007S** (**Zynq-7007S**) or XC7Z010 (**Zynq-7010**) SoC device. It is a cost-effective and high-performance solution for industrial application such as Industrial Ethernet, machine vision, PLC/HMI and etc. The board is ready to run **Linux** and supports industrial operating temperature ranging from **-40 to +85 Celsius**.

The MYD-Y7Z010/007S development board employs the **MYC-Y7Z010/007S** as the controller board by populating the CPU Module on its base board through **1.27mm pitch 180-pin stamp-hole** (Castellated-Hole) interface, allowing users to take the advantages of numerous extended out signals. Core components on CPU Module including **Z-7010** or **Z-7007S** processor, **512MB DDR3 SDRAM**, **4GB eMMC**, **16MB QSPI Flash**, **Gigabit Ethernet PHY** and **external watchdog**. Additionally, the MYD-Y7Z010/007S development board takes full features of the Z-7010 or Z-7007S all programmable SoC to create a rich set of peripherals to the base board through headers and connectors including **RS232, RS485, USB Host, three Gigabit Ethernet ports, CAN, TF card slot, JTAG as well as one 2.54mm pitch 2 x 25-pin expansion header** to let more GPIOs available for further extension.

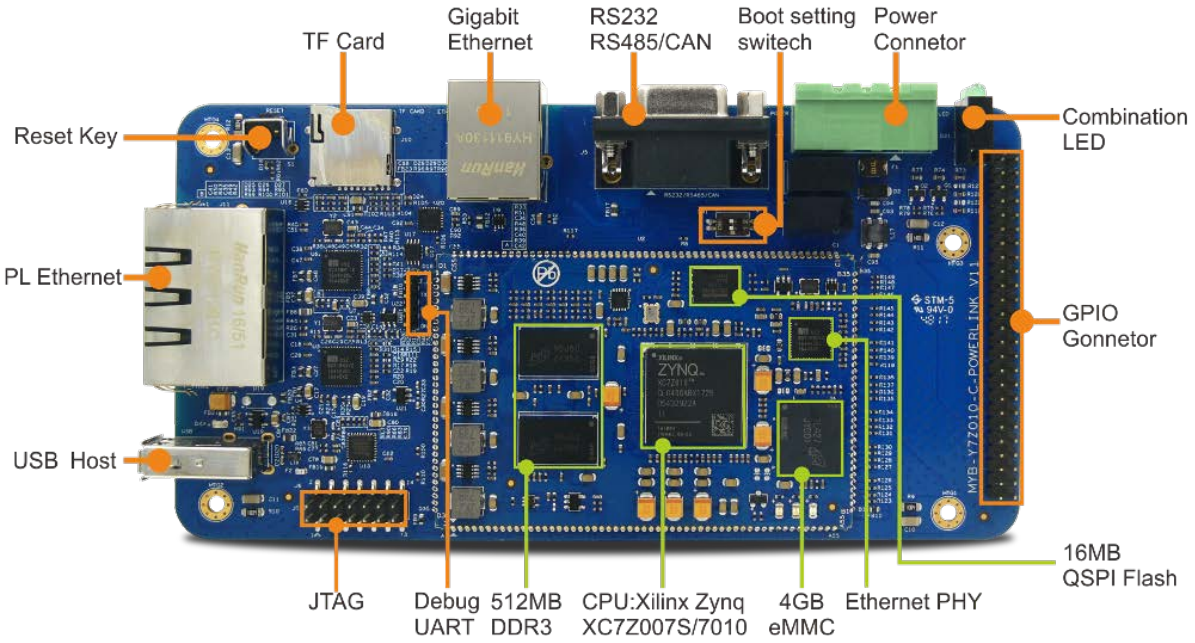

Figure 1-2 MYD-Y7Z010/007S Development Board

MYIR has designed an IO expansion board **MYD-Y7Z010/007S IO Cape** to connect to the **MYD-Y7Z010/007S development board** via the 2.54mm pitch 2 x 25-pin expansion header to expand and enhances its functionality with added peripherals and signals including HDMI, Camera, LCD and Pmods.

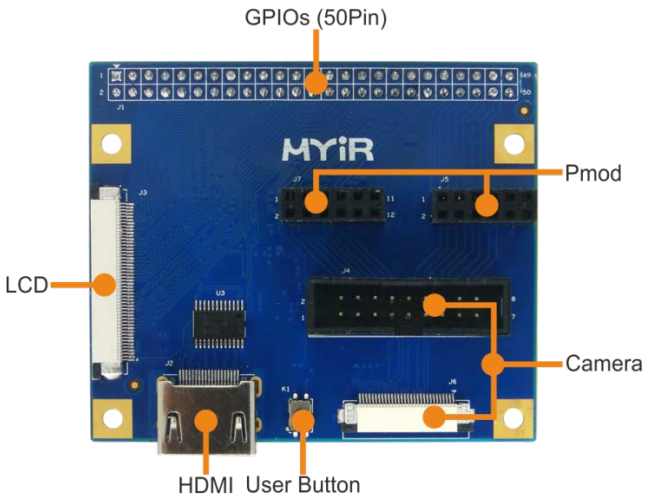

Figure 1-3 MYD-Y7Z010/007S IO Cape

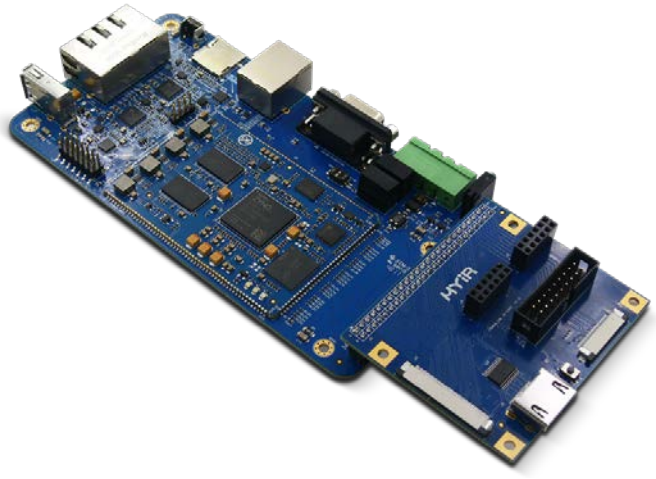

Figure 1-4 IO Cape Mounted on Development Board

The 4.3- and 7-inch LCD Modules as well as MY-CAM011B camera module from MYIR can be supported through the MYD-Y7Z010/007S IO Cape. Optional USB WiFi and Camera modules are also provided. With all these features, the MYD-Y7Z010/007S board is not only great for integration into custom design, but also can be used as a stand-alone development board for evaluating solutions based on Xilinx Zynq-7000.

Hardware Specification

The **Zynq®-7000 All Programmable SoC** (AP SoC) family integrates the software programmability of an ARM®-based processor with the hardware programmability of an FPGA, enabling key analytics and hardware acceleration while integrating CPU, DSP, ASSP, and mixed signal functionality on a single device. Consisting of single-core Zynq-7000S and dual-core Zynq-7000 devices, the Zynq-7000 family is the best price to performanceper-watt, fully scalable SoC platform for your unique application requirements.

Zynq-7000S

Zynq-7000S devices feature a single-core ARM Cortex™-A9 processor mated with 28nm Artix®-7 based programmable logic, representing the lowest cost entry point to the scalable Zynq-7000 platform. It includes Zynq Z-7007S, Z-7012S and Z-7014S which target smaller embedded designs. Available with 6.25Gb/s transceivers and outfitted with commonly used hardened peripherals, the Zynq-7000S delivers cost-optimized system integration ideal for industrial IoT applications such as motor control and embedded vision.

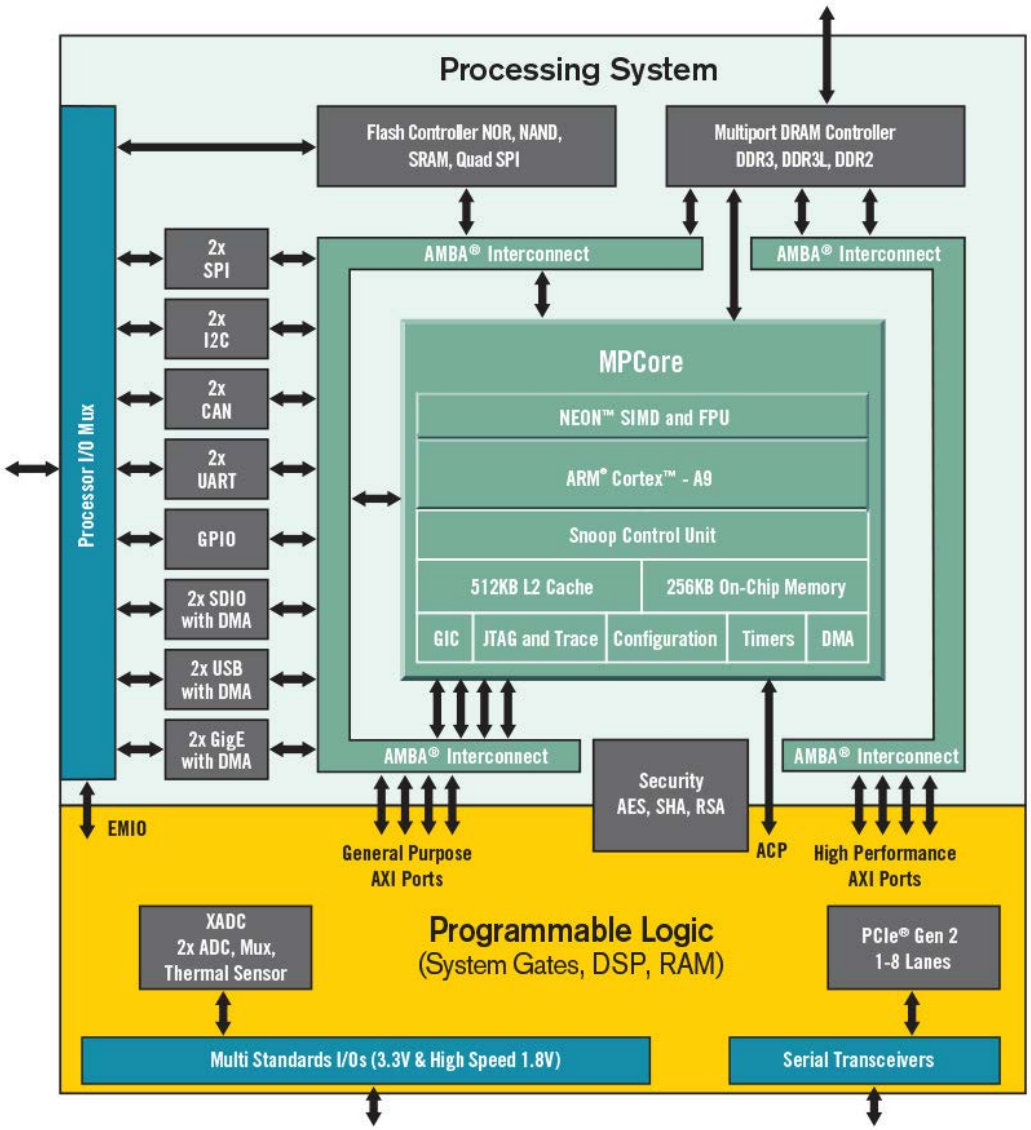

Figure 1-5 Zynq Z-7000S SoC Device Block Diagram

Zynq-7000

Zynq-7000 devices are equipped with dual-core ARM Cortex-A9 processors integrated with 28nm Artix-7 or Kintex®-7 based programmable logic for excellent performance-per-watt and maximum design flexibility. With up to 6.6M logic cells and offered with transceivers ranging from 6.25Gb/s to 12.5Gb/s, Zynq-7000 devices enable highly differentiated designs for a wide range of embedded applications including multi-camera drivers assistance systems and 4K2K Ultra-HDTV.

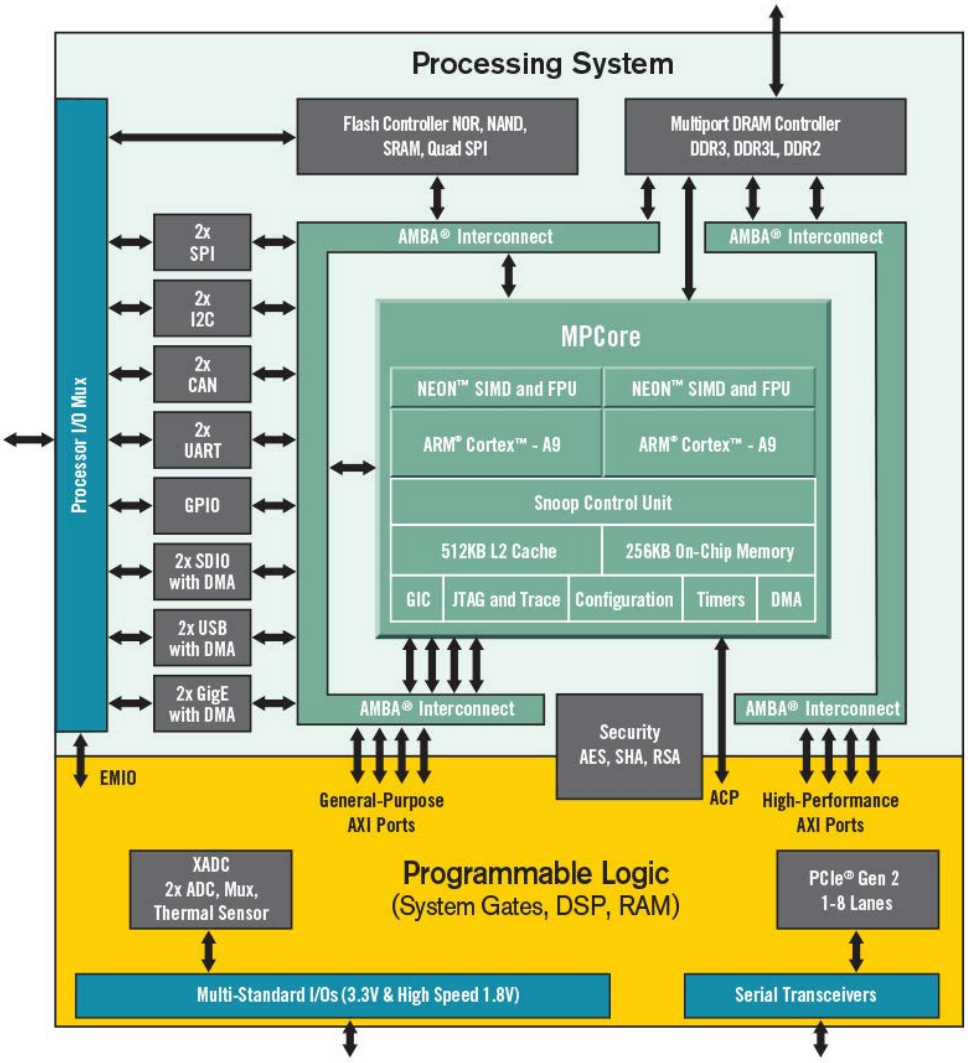

Figure 1-6 Zynq Z-7000 SoC Device Block Diagram

Zynq®-7000 All Programmable SoC Family

		Cost-Optimized Devices						Mid-Range Devices			
	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System (PS)	Processor Core	Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz			Dual-Core ARM Cortex-A9 MPCore Up to 866MHz			Dual-Core ARM Cortex-A9 MPCore Up to 1GHz[1]			
	Processor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor									
	L1 Cache	32KB Instruction, 32KB Data per processor									
	L2 Cache	512KB									
	On-Chip Memory	256KB									
	External Memory Support[2]	DDR3, DDR3L, DDR2, LPDDR2									
	External Static Memory Support[2]	2x Quad-SPI, NAND, NOR									
	DMA Channels	8 (4 dedicated to PL)									
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO									
	Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO									
	Security[3]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot									
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts									
Programmable Logic (PL)	7 Series PL Equivalent	Artix®-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Kintex®-7	Kintex-7	Kintex-7	Kintex-7
	Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM (# 36Kb Blocks)	1.8Mb (50)	2.5Mb (72)	3.8Mb (107)	2.1Mb (60)	3.3Mb (95)	4.9Mb (140)	9.3Mb (265)	17.6Mb (500)	19.2Mb (545)	26.5Mb (755)
	DSP Slices	66	120	170	80	160	220	400	900	900	2,020
	PCI Express®	—	Gen2 x4	—	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC[2]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security[3]	AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config									
	Speed Grades: Commercial	-1			-1			-1			-1
	Speed Grades: Extended	-2			-2,-3			-2,-3			-2
	Speed Grades: Industrial	-1, -2			-1, -2, -1L			-1, -2, -2L			-1, -2, -2L

Notes:
1. 1 GHz processor frequency is available only for -3 speed grades in Z-7030, Z-7035, and Z-7045 devices. See DS190, *Zynq-7000 All Programmable SoC Overview* for details.
2. Z-7007S and Z-7010 in CLG225 have restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual* for more details.
3. Security block is shared by the Processing System and the Programmable Logic.

Figure 1-7 Zynq Z-7000 and Z-7000S SoC Device Table

Mechanical Parameters

- ✓ Dimensions: 153mm x 80mm (base board), 75mm x 50mm (CPU Module)
- ✓ PCB Layers: 4-layer design (base board), 10-layer design (CPU Module)
- ✓ Power supply: 12V/2A
- ✓ Working temp.: -40~85 Celsius

The MYD-Y7Z010/007S Controller Board (MYC-Y7Z010/007S CPU Module)

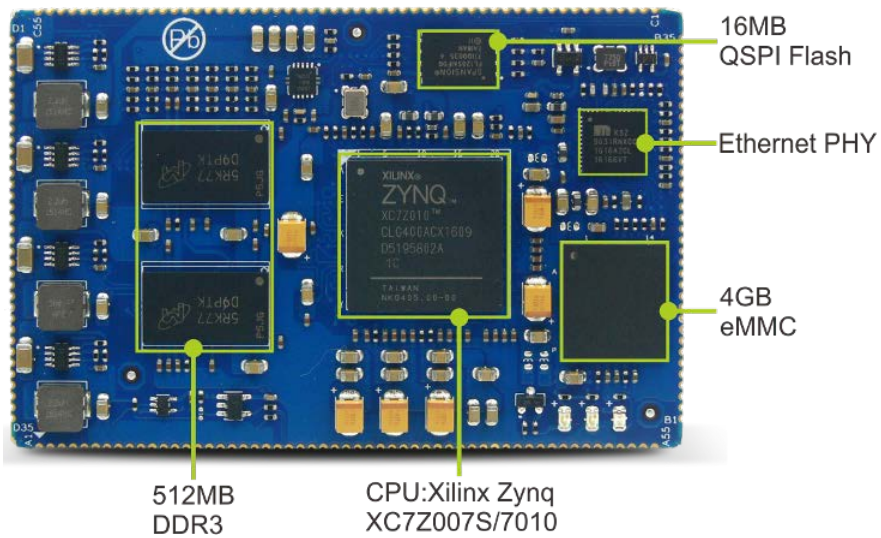

Figure 1-8 MYC-Y7Z010/007S CPU Module

SoC

✓ Xilinx XC7Z010-1CLG400I (Zynq-7010) or XC7Z007S-1CLG400I (Zynq-7007S)
ARM® Cortex™-A9 MPCore processor
- 667MHz dual-core processor (up to 866MHz, for XC7Z010)
- 667MHz single-core processor (up to 766MHz, for XC7Z007S)
- Integrated Artix-7 class FPGA subsystem
with 28K logic cells, 17,600 LUTs, 80 DSP slices (for XC7Z010)
with 23K logic cells, 14,400 LUTs, 66DSP slices (for XC7Z007S)
- NEON™ & Single / Double Precision Floating Point for each processor
- Supports a Variety of Static and Dynamic Memory Interfaces

Memory

✓ 512MB DDR3 SDRAM
✓ 4GB eMMC Flash
✓ 16MB QSPI Flash

Peripherals and Signals Routed to Pins

MYC-Y7Z010/007S Pinouts Description

✓ Gigabit Ethernet PHY
✓ External watchdog
✓ Three LEDs
- One red LED for power indicator
- One green LED for FPGA program done indicator
- One flashing green LED for system indicator
✓ 1.27mm 180-pin expansion connectors bring out below signals:
- One Gigabit Ethernet
- One USB OTG2.0 (need external USB PHY-USB3320)
- Two Serial ports
- Two I2C
- Two CAN BUS
- Two SPI
* Serial ports, I2C, CAN and SPI signals can be implemented through PL pins by Emio
- Two ADC (two independent differential ADC, 16-channel ADC brought out through PL pins)
- One SDIO

The MYD-Y7Z010/007S Base Board

PS Unit

✓ One USB Host
✓ One RS232 serial port (with isolation)
✓ One RS485 (with isolation)
✓ One TF card slot
✓ One CAN interface (with isolation)
✓ One 10/100/1000Mbps Ethernet interface
✓ One 2.54mm pitch 14-pin JTAG interface
✓ One Debug serial port (UART)

PL Unit

✓ One 2.54mm pitch 2 x 25-pin GPIO expansion headers
✓ Two 10/100/1000Mbps Ethernet interfaces
✓ Three user LEDs

Function Block Diagram

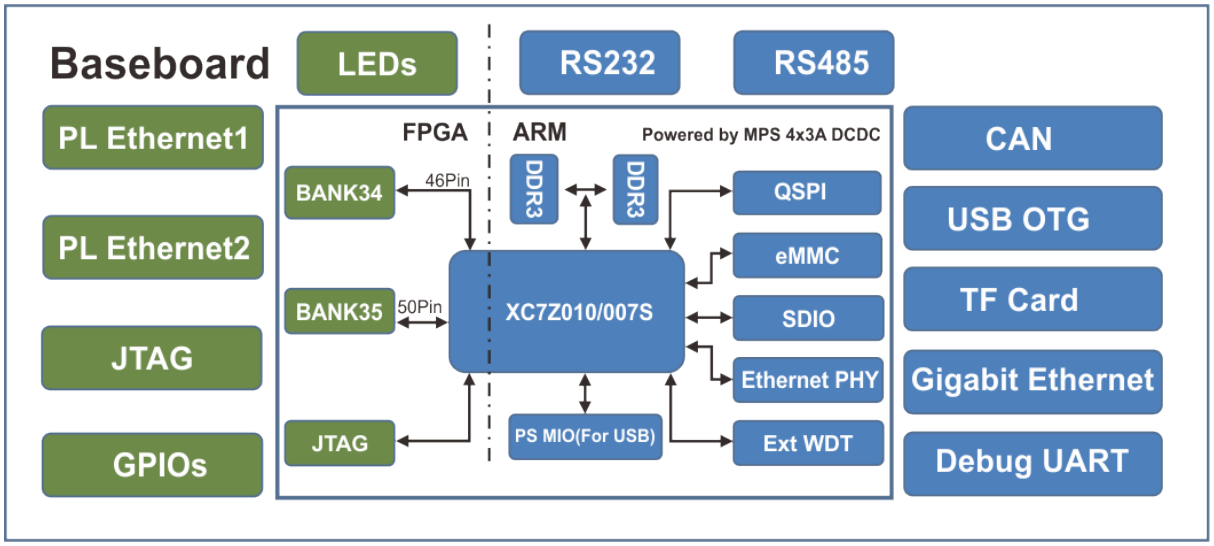

Figure 1-9 Function Block Diagram of MYD-Y7Z010/007S

Dimension Chart

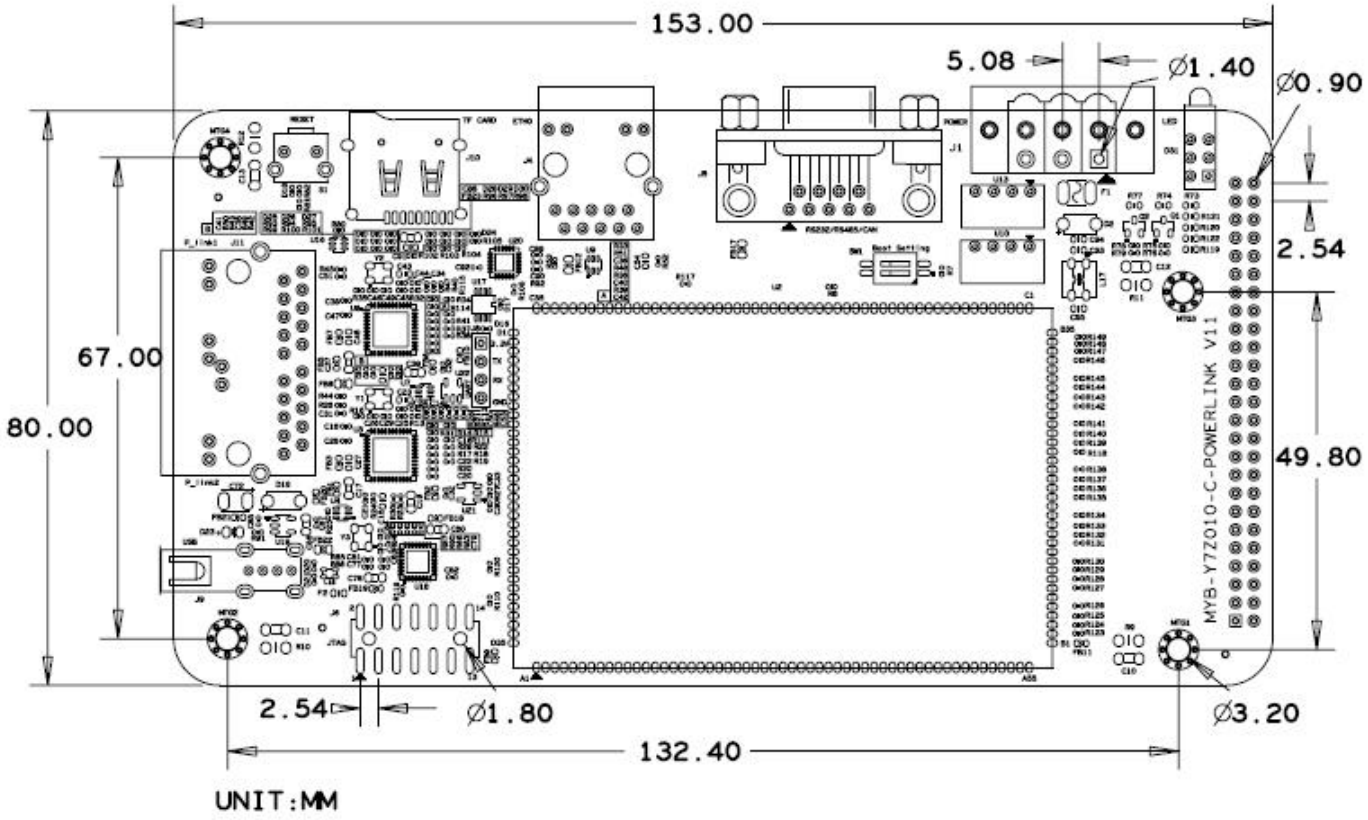

Figure 1-10 Dimension Chart of MYD-Y7Z010/007S

Software Features

Item	Features	Description	Remark
Cross compiler	gcc 4.6.1	gcc version 4.6.1 (SourceryCodeBench Lite 2011.09-50)	
Boot program	BOOT.BIN	First boot program including FSBL, bitstream	Source code provided
	u-boot	Secondary boot program	Source code provided
Linux Kernel	Linux 3.15.0	Customized kernel for MYD-Y7Z010/007S Development Board	Source code provided
Drivers	USB Host	USB Host driver	Source code provided
	Ethernet	Gigabit Ethernet driver	Source code provided
	MMC/SD/TF	MMC/SD/TF card driver	Source code provided
	CAN	CAN driver	Source code provided
	LCD Controller	LCD driver	Source code provided
	HDMI	HDMI (SII902X chip) driver	Source code provided
	Button	Button driver	Source code provided
	UART	UART driver	Source code provided
	LED	LED driver	Source code provided
	GPIO	GPIO driver	Source code provided
	QSPI	QSPI Flash W25Q128FW driver	Source code provided
	RTC	DS3231 RTC driver	Source code provided
	Resistive Touch	TSC2007 resistive touch screen driver	Source code provided
	Capacitive Touch	FT5X0X capacitive touch screen driver	Source code provided
	ADC	ADC driver	Source code provided
File System	Ramdisk	Ramdisk system image	
	Rootfs.tar	Tar file	

Table 1-1 Software Features of MYD-Y7Z010/007S

Order Information

<table>
<tr><th>Item</th><th>Part No.</th><th>Packing List</th></tr>
<tr><td>MYD-Y7Z010 Development Board</td><td>MYD-Y7Z010-4E512D-667-I</td><td rowspan="2">➢ One MYD-Y7Z010/007S Board (including the base board and CPU module)
➢ One 1.5m cross Ethernet cable
➢ One DB9 converting cable
➢ One power converting cable
➢ One 12V/1.25A Power adapter
➢ One Product Disk (including user manual, datasheet, base board schematic in PDF format and software packages)</td></tr>
<tr><td>MYD-Y7Z007S Development Board</td><td>MYD-Y7Z007S-4E512D-667-I</td></tr>
<tr><td>MYC-Y7Z010 CPU Module</td><td>MYC-Y7Z010-4E512D-667-I</td><td rowspan="10">Add-on Options:
➢ MYC-Y7Z010/007S CPU Module
➢ MY-LCD43TP LCD Module
➢ MY-LCD70TP LCD Module
➢ MY-LCD70TP-C LCD Module
➢ MY-CAM002U Camera Module
➢ MY-WF003U Camera Module
➢ MY-CAM011B Camera Module
➢ MYD-Y7Z010/007S IO CAPE</td></tr>
<tr><td>MYC-Y7Z007S CPU Module</td><td>MYC-Y7Z007S-4E512D-667-I</td></tr>
<tr><td>MY-WF003U WiFi Module</td><td>MY-WF003U</td></tr>
<tr><td>MY-CAM002U Camera Module</td><td>MY-CAM002U</td></tr>
<tr><td>MY-CAM011B Camera Module</td><td>MY-CAM011B</td></tr>
<tr><td>MY-LCD43TP 4.3-inch LCD Module with resistive touch screen</td><td>MY-TFT043RV2</td></tr>
<tr><td>MY-LCD70TP 7-inch LCD Module with resistive touch screen</td><td>MY-TFT070RV2</td></tr>
<tr><td>MY-LCD70TP-C 7-inch LCD Module with capacitive touch screen</td><td>MY-TFT070CV2</td></tr>
<tr><td>MYD-Y7Z010/007S IO CAPE</td><td>MY-CAPE003</td></tr>
<tr><td colspan="3">Remark: the MY-CAM011B Camera Module and LCD Modules are supported through IO CAPE.</td></tr>
</table>

MYiR™

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