

# **PSMN025-80YL**

N-channel 80 V, 25 mΩ logic level MOSFET in LFPAK56

14 April 2016 Product data sheet

## 1. General description

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product is designed and qualified for use in a wide range of power supply & motor control equipment.

#### 2. Features and benefits

- Advanced TrenchMOS provides low R<sub>DSon</sub> and low gate charge
- · Logic level gate operation
- Avalanche rated, 100% tested
- LFPAK provides maximum power density in a Power SO8 package

## 3. Applications

- Synchronous rectification in power supply equipment
- Chargers & adaptors with V<sub>out</sub> < 10 V</li>
- Fast charge & USB-PD applications
- Battery powered motor control
- LED lighting & TV backlight

#### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	80	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	-	37	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	95	W
Static characte	eristics						,
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C}; Fig. 11$		-	22.2	27	mΩ
Dynamic characteristics							
$Q_{GD}$	gate-drain charge	$I_D = 10 \text{ A}; V_{DS} = 64 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ °C}; \underline{\text{Fig. 13}}; \underline{\text{Fig. 14}}$		-	5.8	-	nC



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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D I
2	S	source		
3	S	source	[qj	G T T T
4	G	gate	<u>o o o o</u>	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

## 6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PSMN025-80YL	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669		

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN025-80YL	025L80

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	80	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	80	V
$V_{GS}$	gate-source voltage		-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>	-	95	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	-	37	Α
		V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>	-	26.5	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$ ; Fig. 3	-	150	Α
T <sub>stg</sub>	storage temperature		-55	175	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>j</sub>	junction temperature			-55	175	°C
Source-drain diode						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	37	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	150	Α
Avalanche ru	ggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 37 A; $V_{sup} \le 80$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[1][2]	-	45.4	mJ

- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.

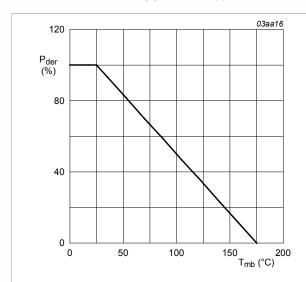


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

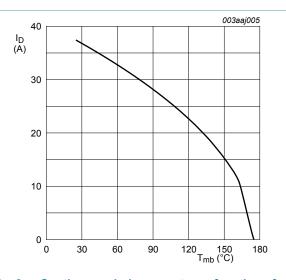


Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 5V$$

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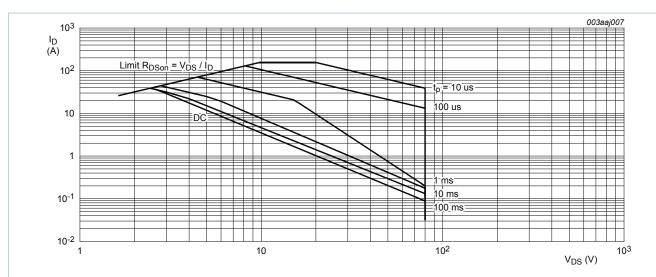
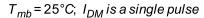


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



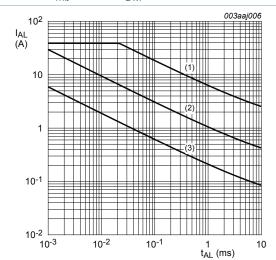


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1) 
$$T_{j(init)} = 25$$
°C; (2)  $T_{j(init)} = 150$ °C; (3) Repetitive Avalanche

#### 9. Thermal characteristics

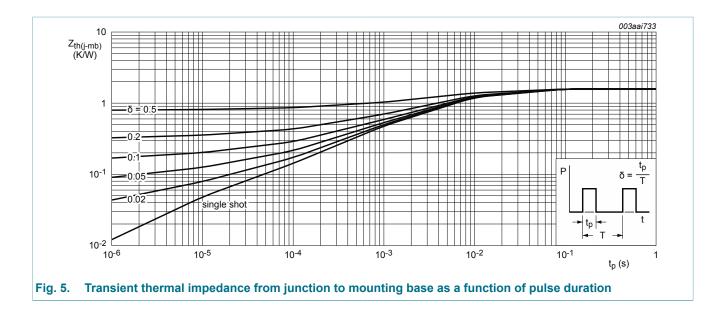
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 5	-	-	1.58	K/W

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## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		,			
V <sub>(BR)DSS</sub>	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	80	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	72	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}; Fig. 9;$ Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}; Fig. 9$	-	-	2.45	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; <u>Fig. 9</u>	0.5	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.1	1	μΑ
	V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μΑ	
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	22.2	27	mΩ
	resistance	$V_{GS}$ = 10 V; $I_D$ = 10 A; $T_j$ = 25 °C; Fig. 11	-	20.5	25	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 175 °C; Fig. 12; Fig. 11	-	-	67.8	mΩ
Dynamic ch	naracteristics		,			
Q <sub>G(tot)</sub>	total gate charge	$I_D$ = 10 A; $V_{DS}$ = 64 V; $V_{GS}$ = 5 V; $T_j$ = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	17.1	-	nC
		$I_D$ = 10 A; $V_{DS}$ = 64 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 13; Fig. 14	-	34.3	-	nC

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$Q_{GS}$	gate-source charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 64 V; V <sub>GS</sub> = 5 V;		-	5.2	-	nC
$Q_{GD}$	gate-drain charge	T <sub>j</sub> = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>		-	5.8	-	nC
C <sub>iss</sub>	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$		-	2032	2703	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 15</u>		-	147	176	pF
C <sub>rss</sub>	reverse transfer capacitance			-	75	103	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = 60 V; $R_{L}$ = 4.98 $\Omega$ ; $V_{GS}$ = 5 V; $R_{G(ext)}$ = 5 $\Omega$ ; $T_{j}$ = 25 °C		-	11.6	-	ns
t <sub>r</sub>	rise time			-	17.2	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	23.9	-	ns
t <sub>f</sub>	fall time			-	15.3	-	ns
Source-dra	ain diode				'		-1
$V_{SD}$	source-drain voltage	$I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$		-	0.81	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S$ = 10 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V;		-	23.8	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 25 V; T <sub>j</sub> = 25 °C		-	27	-	nC

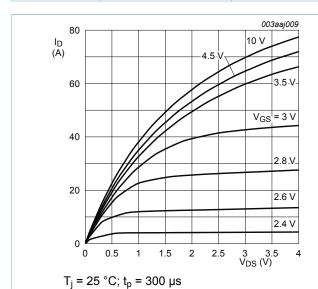


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

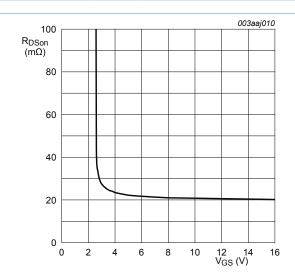


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values  $T_j = 25^{\circ}C; I_D = 10A$ 

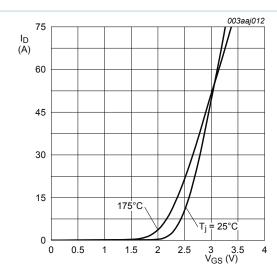


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$$V_{DS} = 10V$$

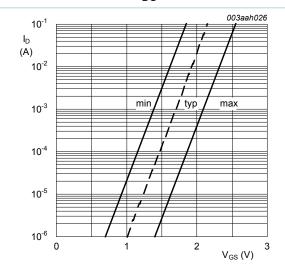


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^{\circ}C; \ V_{DS} = 5V$$

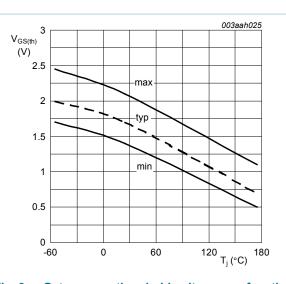
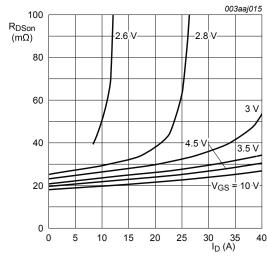


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D$$
 = 1 mA;  $V_{DS}$  =  $V_{GS}$ 



 $T_j = 25 \, ^{\circ}C; t_p = 300 \, \mu s$ 

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

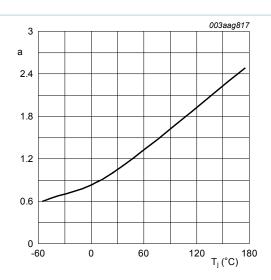


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25 °C)}}$$

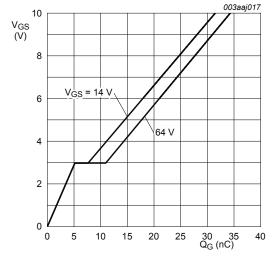


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}C; I_D = 10A$$

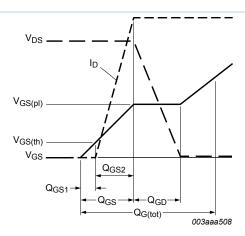


Fig. 13. Gate charge waveform definitions

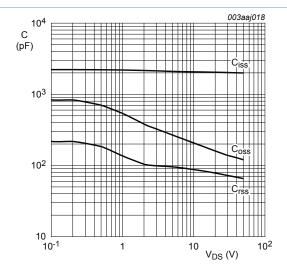


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V$$
;  $f = 1MHz$ 

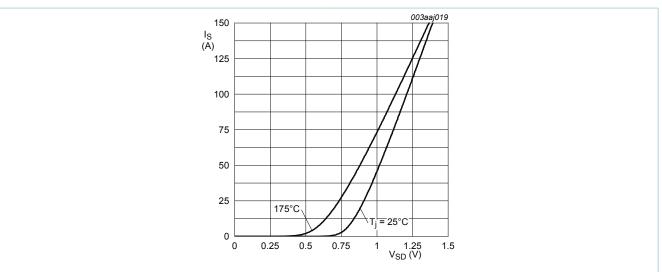


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values  $V_{\rm GS} = 0V$ 

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## 11. Package outline

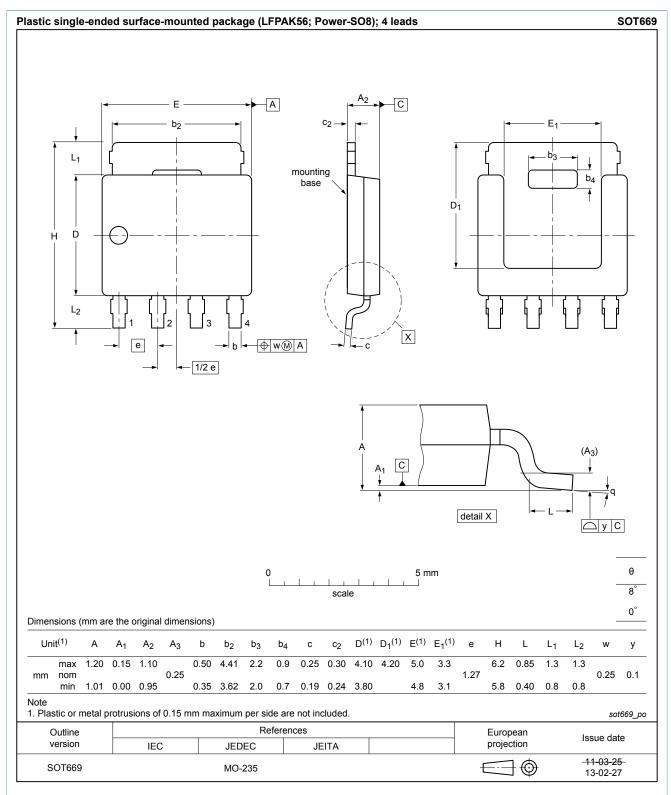


Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)

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Product [short] data sheet	Production	This document contains the product specification.

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