AN12589

VR5500, FS5502 product guidelines

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Document information

Information	Content
Keywords	VR5500, FS5502, power management, components, I2C, CRC, hardware
Abstract	This application note provides guidelines for integrating the VR5500/FS5502 power management family of devices into automotive electronic systems.

Revision history

Revision	Date	Description
1	20200204	Initial release

1 Introduction

This application note provides guidelines for integrating the VR5500/FS5502 system basis chip (SBC) family of devices into automotive electronic systems.

2 MCU mapping

The VR5500/FS5502 family covers a wide range of MCU core voltages from NXP and other MCU suppliers. It functions as standalone power management integrated circuit (PMIC) or in combination with an additional PMIC from NXP or other suppliers.

Table 1 summarizes several MCUs and PMICs compatible with the VR5500/FS5502 family of parts. This summary does not identify all possible working combinations of the VR5500/FS5502 with MCUs and PMICs from NXP or other vendors. If you plan to use the VR5500/FS5502 with an MCU not listed in Table 1, contact your local NXP representative to verify compatibility.

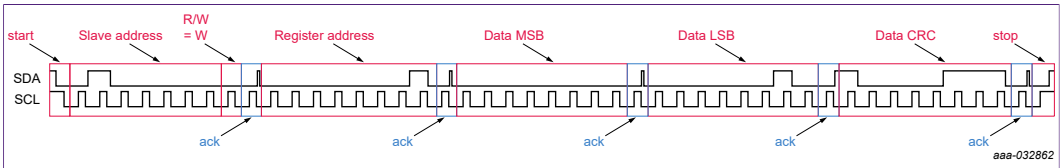
Table 1. MCU mapping

Device	MCU	Application
VR5500	SAF5x, SAF4x, iMX8	Infotainment, Telematix, Radio, V2X
FS5502	S32R274, S32R372	Radar

3 Communication with MCU

Refer to UM10204[13] for the complete I^2C bus specification.

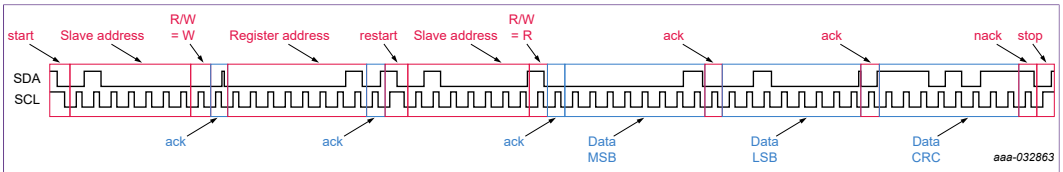
3.1 I^2C write frame



Red is master driving (MCU), blue is slave driving (VR5500/FS5502)

Figure 1. I^2C frame example with MAIN register M_MODE, address 0x01, write data 0x02

3.2 I^2C read frame



Red is master driving (MCU), blue is slave driving (VR5500/FS5502)

Figure 2. I^2C frame example with MAIN register M_MODE, address 0x01, read data

First perform an I^2C write access to configure the register address to read, then perform an I^2C read access to get data and CRC.

3.3 CRC implementation

I^2C communications are protected with an 8-bit CRC. This code example is a possible CRC implementation using a lookup table. Contact your local NXP representative for the complete VR5500 demo driver.

```
static uint8_t VR5500_CalcCRC(const uint8_t* data, uint8_t
 dataLen)
{
    uint8_t crc;      /* Result. */
    uint8_t tableIdx; /* Index to the CRC table. */
    uint8_t dataIdx;  /* Index to the data array (memory). */

    FS_ASSERT(data != NULL);
    FS_ASSERT(dataLen > 0);
    /* Set CRC seed value. */
    crc = VR5500_COM_CRC_INIT;
    for (dataIdx = dataLen - 1; dataIdx > 0; dataIdx--)
    {
       tableIdx = crc ^ data[dataIdx];
        crc = VR5500_CRC_TABLE[tableIdx];
    }
    return crc;
}
```

4 Debug mode

One time programming (OTP) or OTP emulation is possible only during customer engineering development.

With OTP, the device starts with the configuration at every power up. With OTP emulation, the configuration is lost if the power supply is removed.

4.1 Debug mode entry

The functional description *Debug mode* sections of data sheets VR5500 and FS5502 explain how the VR5500/FS5502 enters debug mode with the following sequence:

1. DBG pin = V_{DBG} and VSUP > V_{SUP_UVH}
2. WAKE1 or WAKE2 > $WAKE12_{VIH}$

V_{DBG} and VSUP come up at the same time as long as WAKE1 or WAKE2 come up last. There are 2 ways to achieve above sequence, either manually or automatically.

4.2 Manual debug mode entry

Manual debug mode entry is possible with the proposed circuitry in Figure 3.

The user generates the sequence 1-2-3 manually to enter debug mode

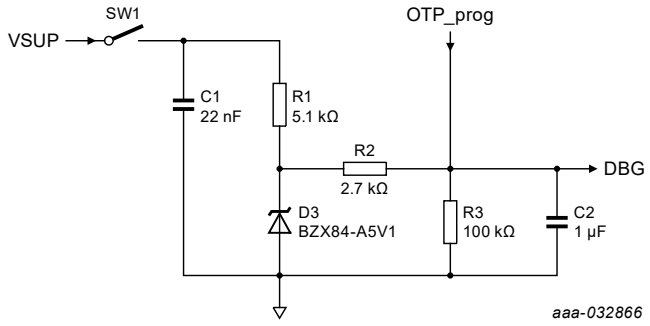


Figure 3. Manual debug mode entry circuitry

1. Close SW1
2. Apply VSUP
3. Apply WAKE1

The device starts and stops the state machines waiting for OTP or OTP emulation thru I^2C. OTP or OTP emulation can be done only with the Flex graphical user interface (FlexGUI)[11]. OTP requires that OTP_prog = 8 V upon FlexGUI request.

When OTP or OTP emulation is complete, open SW1 to enable the device to start with the power-up sequence in accordance with the OTP configuration.

4.3 Automatic debug mode entry

Automatic debug mode entry is possible with the proposed circuitry in Figure 4 attached to the WAKE1 (or WAKE2) pin. VSUP must be applied first, then WAKE input is applied.

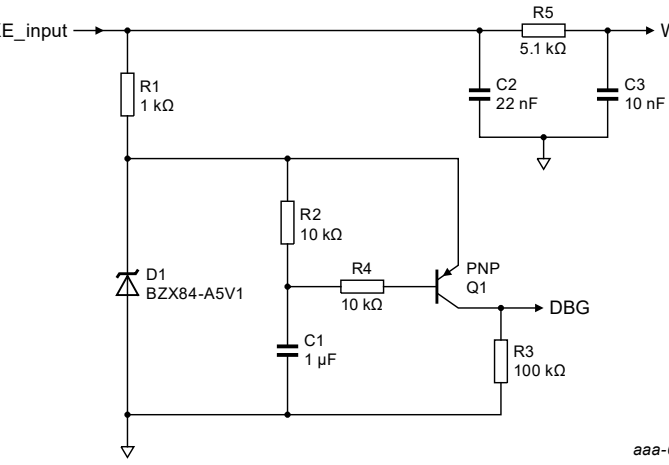


Figure 4. Automatic debug mode entry circuitry

This circuit is proposed for lab evaluation only. The pulse duration is affected by VSUP slew rate and does not work with very slow ramp up. NXP recommends applying VSUP voltage first, then WAKE_input voltage second. If VSUP is also supplying WAKE_input, a switch can be used to apply WAKE_input after VSUP. C1 needs time to discharge thru R2 + R1 between power down and power up cycle to generate a new pulse at DBG pin.

A pulse is automatically generated at the DBG pin to enter debug mode without OTP or OTP emulation but with the debug mode features listed in the Functional description *Debug mode* section of the product data sheet.

When R1 is populated, the device will automatically start in debug mode. When R1 is not populated, the device will start in normal mode.

To correctly detect the debug mode entry, a recommended pulse with duration greater than 7 ms is required when WAKE1 > $WAKE12_{VIH}$ is generated to have VBOS started and LBIST executed before the end of the pulse. The total pulse duration is estimated as $T_{PULSE} = -RC \times \ln(Q1\_V_{BE} / V_{D1})$ with R = R2 // R4, $Q1\_V_{BE}$ = 0.6 V and V_{D1} = 5.1 V.

In the circuitry of Figure 4, the RC value gives an estimated pulse duration of T_{PULSE} ~10.7 ms. The simulation in Figure 5 confirms a total T_{PULSE} ~10 ms, which is above the recommended 7 ms.

The external components values can be adjusted to optimize the pulse duration (longer or shorter) if needed.

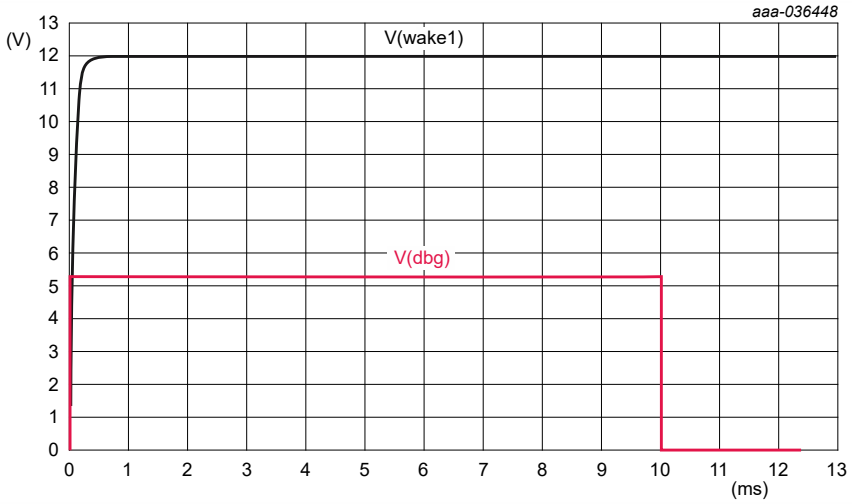


Figure 5. Automatic debug mode entry simulation

5 MCU programming

5.1 Production-level assembly line programming

After PCB assembly, the first time the MCU is powered up, the flash memory of the MCU is empty and needs to be programmed. To facilitate the programming, NXP recommends using the device debug mode applying the correct voltage at the DEBUG pin. Refer to the Functional description *Debug mode* section of the product data sheet.

When the programming is complete:

- If an MCU software reset is required, use a reset request with the RSTB_REQ bit in the FS_SAFE_IOs register to:
  - reset the MCU
  - execute the new software
  - leave the debug mode with DBG_EXIT bit in FS_STATES register
- In order to restart the MCU from a power-on reset and execute the software, send the device to standby with the GOTOSTBY bit in the M_MODE register using WAKE1 or WAKE2 at high level.

5.2 In-vehicle programming

When the programming is complete:

- If an MCU software reset is required, use a reset request with the RSTB_REQ bit in the FS_SAFE_IOs register to:
  - reset the MCU
  - execute the new software
  - leave the debug mode with DBG_EXIT bit in FS_STATES register
- In order to restart the MCU from a power-on reset and execute the software, send the device to standby with the GOTOSTBY bit in the M_MODE register using WAKE1 or WAKE2 at high level.

6 Application schematics

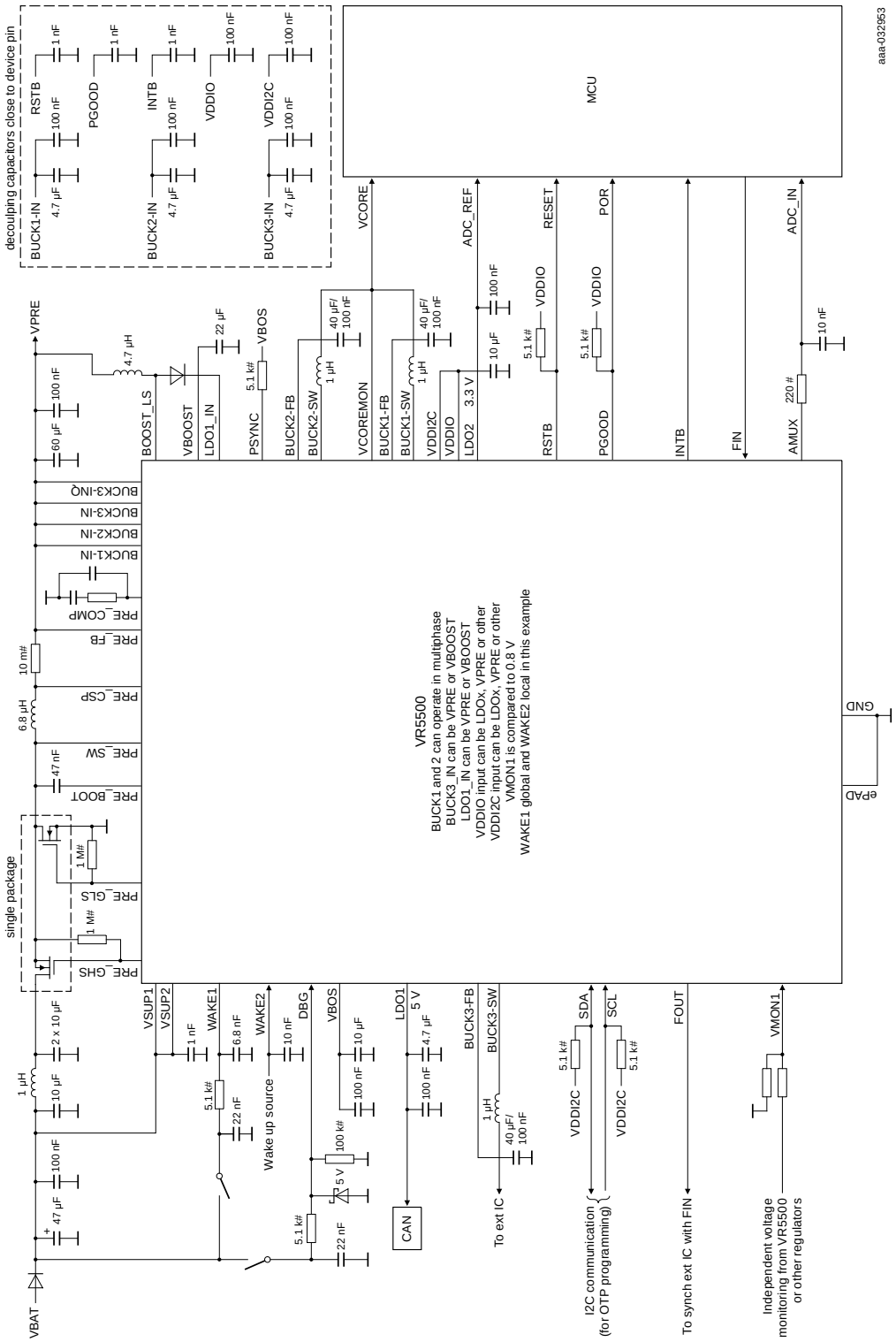


Figure 6. Application schematic - VR5500

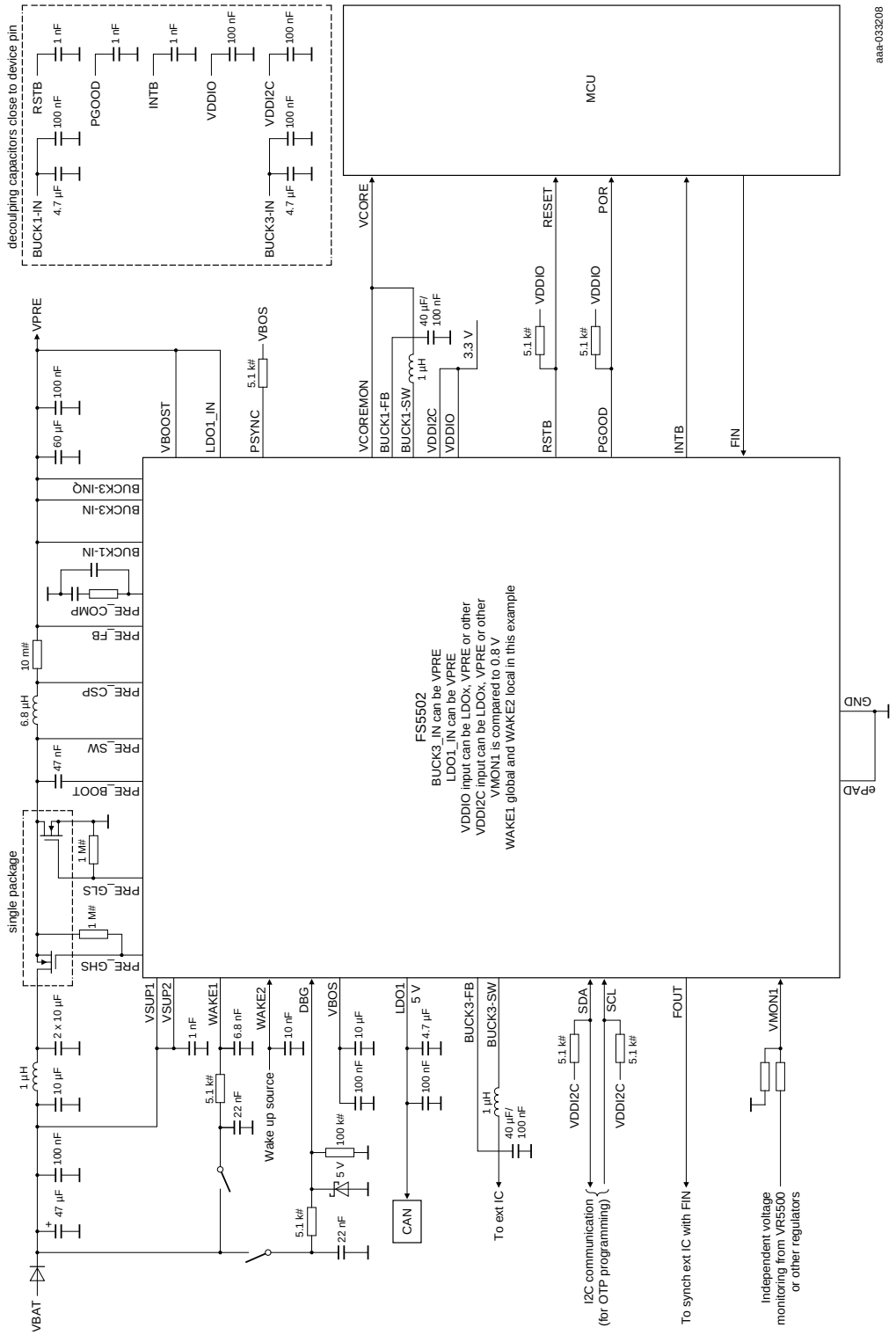


Figure 7. Application schematic - FS5502

6.1 VSUP components

- Reverse battery diode

  - Schottky with Low V_F
  - $I_F > I_{pre}$
  - V_R > 100 V to sustain ISO pulse 1
- Input Ctank capacitor
  - 47 µF or more
  - 50 V rating for 12 V automotive
  - 100 V rating for 24 V truck
- PI filter
  - $F_{RES} = 1 / [2\pi \times \sqrt{(LCpi1)}]$
  - Calculated for Fres < V_{PRE_SW} / 10
  - L = 1 µH
  - Cpi1 = 10 µF
  - 100 nF input decoupling capacitor for conducted emission
- VSUP decoupling capacitor
  - 1 nF decoupling capacitor close to the pin can help the conducted emission
  - 2.2 nF decoupling capacitor before the RBD can help the conducted emission

6.2 VPRE components

- MOSFETs
  - Logical level NMOS, gate drive comes from VBOS (5 V)
  - VDS > 40 V for 12 V automotive applications
  - VDS > 60 V for 24 V truck, bus applications
  - IDS > IPRE_LIM_max
  - At VPRE = 455 kHz:
    - Qg < 15 nC @Vgs = 5 V is recommended
    - At high current (> 6 A), each MOSFETs should be selected in single package to limit the heat exchange between HS and LS. Dual MOSFETs in the same package is OK for low and mid current. (< 6 A)
  - At VPRE = 2.22 MHz:
    - Qg < 7nC @Vgs = 5 V is recommended.
    - Each MOSFETs should be selected in single package to limit the heat exchange between HS and LS.
    - A Schottky diode in parallel to the LS helps to improve the efficiency.
  - Balance the power dissipation between conduction and switching
  - Refer to the *VPRE external MOSFETs* section of the product data sheet for recommended references.
- Inductor
  - Shielded 6.8 µH @ 455 kHz
  - Shielded 2.2 µH @ 2.22 MHz
  - ± 20 % tolerance is preferred but ± 30 % is allowed
  - ISAT > IPRE_LIM
- Output capacitor
  - Ceramic capacitors recommended
  - Typical 66 µF @ 455 kHz. Can be increased depending on load and transient
  - Typical 44 µF @ 2.22 MHz. Can be increased depending on load and transient
  - > 3 times VPRE voltage for the DC rating to minimize the DC biasing effect
- Bootstrap capacitor

- > 10 times the gate source capacitor of Q1, 47 nF used during the validation at NXP
- 16 V DC rating

- Rshunt
  - Between 10 and 20 mΩ
  - ± 1 % accuracy
  - Inductor DCR current sense can be used at high current to improve the efficiency. See Section 7.
- Compensation network connected at PRE_COMP pin
  - Refer to the *Compensation network and stability* section of the product data sheet to calculate these components.
  - Verify the stability with Simulation of Piecewise Linear Systems (SIMPLIS) using the VR5500_VPRE_Simplis_Model[6]

6.3 VBOOST components (VR5500 only)

- Diode
  - Schottky with low V_F
  - I_F > IBOOST_LIM
  - V_R > 10 V
- Inductor
  - Shielded 4.7 µH
  - ± 20 % tolerance is preferred but ± 30 % is allowed
  - ISAT > IBOOST_LIM
- Output capacitor
  - Ceramic capacitors recommended
  - Typical 44 µF. Can be increased depending on load and transient
  - > 3 times VBOOST voltage for the DC rating to minimize the DC biasing effect

6.4 LV_BUCK components

- Input capacitor
  - 4.7 µF // 100 nF recommended close to each BUCKx_IN pins
  - > 3 times VPRE voltage for the DC rating to minimize the DC biasing effect
- Inductor
  - Shielded 1 µH
  - ± 20 % tolerance is preferred but ± 30 % is allowed
  - ISAT > IBUCK_LIM
- Output capacitor
  - Ceramic capacitors recommended
  - Minimum 44 µF. Can be adjusted depending on load and transient
  - 100 nF decoupling capacitor can help the conducted emission
  - > 3 times BUCKx voltage for the DC rating to minimize the DC biasing effect

6.5 WAKE components

- WAKE global pin
  - 22 nF input capacitor to damp ESD Gun type of stress

- 5.1 K to limit the current, minimum 0805 size to avoid arching with high DV / DT like ESD GUN
- 10 nF decoupling capacitor close to the pin for immunity

• WAKE local pin
- 6.8 nF decoupling capacitor close to the pin for immunity

6.6 Output pins

• RSTB, PGOOD local pin
- 1 nF decoupling capacitor close to the pin for immunity

6.7 Automotive schematic used for BOM list

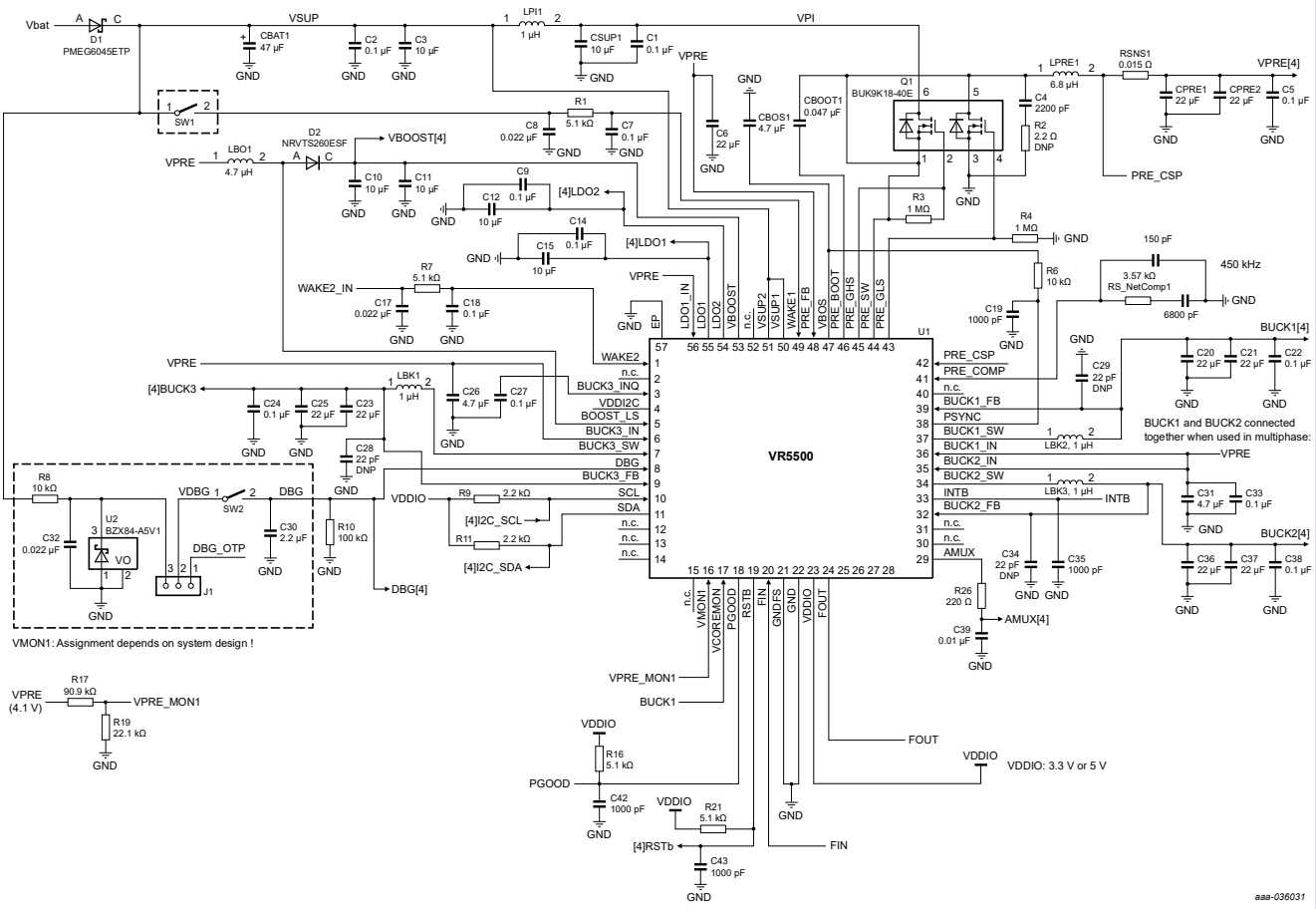


Figure 8. Automotive schematic used for VR5500 BOM list

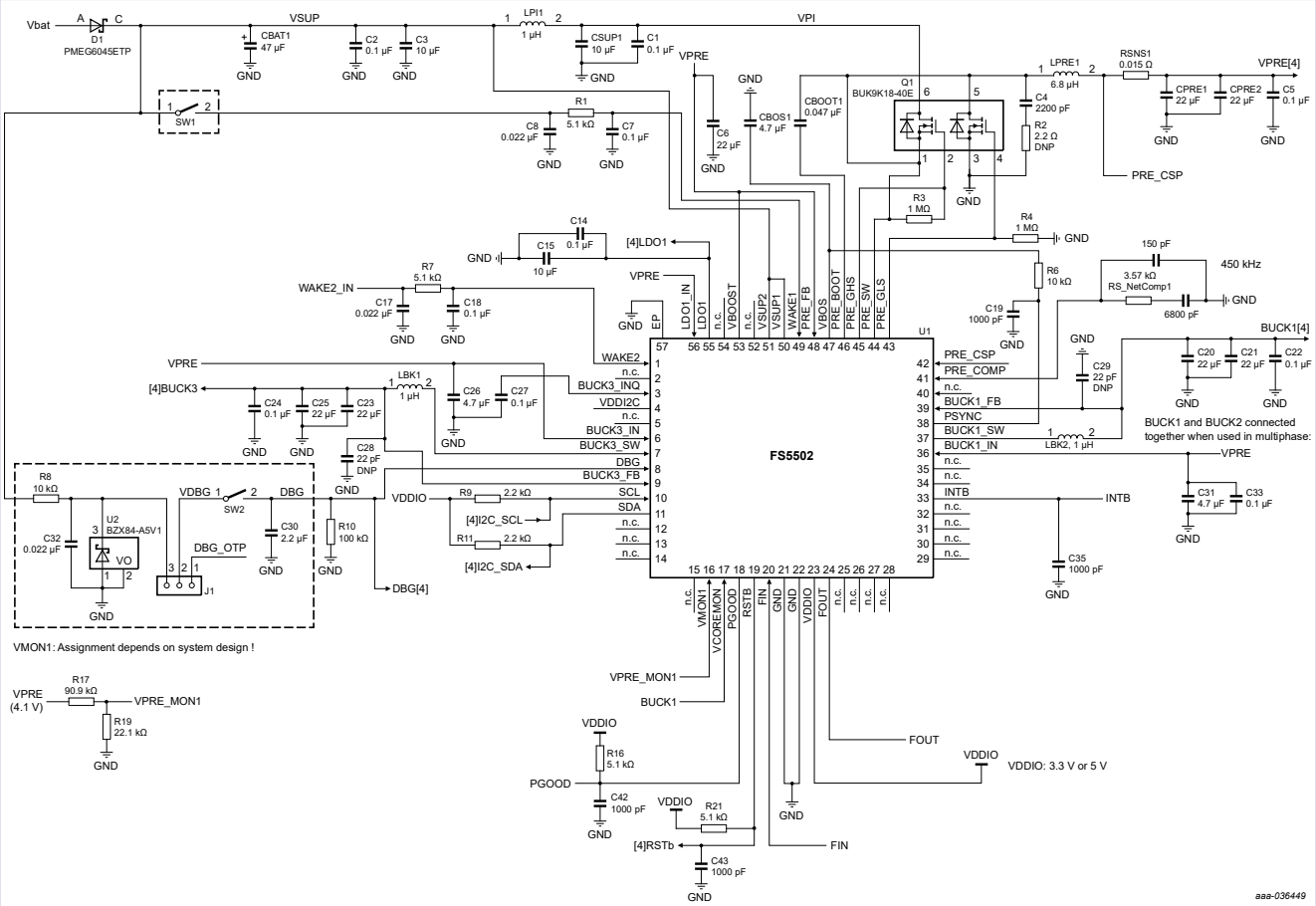


Figure 9. Automotive schematic used for FS5502 BOM list

6.8 Automotive BOM list

Table 2. Automotive BOM list

Part Reference	Value	Part Manufacturer[1]	Part Number[1]	Description
C1, C2, C5, C7, C9, C14, C18, C22, C24, C27, C33, C38	0.1 µF	TDK	CGA2B3X7R1H104K050BB	CAP CER 0.1 µF 50 V 10 % X7R AEC-Q200 0402
C3, CSUP1	10 µF	Murata	GCM32EC71H106KA03	CAP CER 10 µF 50 V 10 % X7S AEC-Q200 1210
C4	2200 pF	Murata	GCM155R72A222KA37D	CAP CER 2200 pF 100 V 10 % X7R AEC-Q200 0402
C6, C28, C29, C34	22 pF	AVX	04025A220FAT2A	CAP CER 22 pF 50 V 1 % C0G 0402
C8, C17, C40	0.022 µF	Murata	GCM155R71H223KA55D	CAP CER 0.022 µF 50 V 10 % X7R AEC-Q200 0402
C10, C11, C12, C15	10 µF	Murata	GCM21BC71C106ME36	CAP CER 10 µF 16 V 20 % X7S AEC-Q200 0805
C13	150 pF	Murata	GCM1555C1H151JA16D	CAP CER 150 pF 50 V 5 % C0G AEC-Q200 0402
C16	6800 pF	KEMET	C0402C682K5RAC_	CAP CER 6800 pF 50 V 10 % X7R 0402

Part Reference	Value	Part Manufacturer[1]	Part Number[1]	Description
C19, C35, C42, C43	1000 pF	Murata	GCM155R71H102KA37D	CAP CER 1000 pF 50 V 10 % X7R AEC-Q200 0402
C20, C21, C36, C37	22 µF	Murata	GCM31CR71A226KE02	CAP CER 22 µF 10 V 10 % X7R AEC-Q200 1206
C23, C25, CPRE1, CPRE2	22 µF	Murata	GCM32ER71C226ME19	CAP CER 22 µF 16 V 20 % X7R AEC-Q200 1210
C26, C31	4.7 µF	TDK	CGA4J3X7R1C475K125AB	CAP CER 4.7 µF 16 V 10 % X7R AEC-Q200 0805
C30	2.2 µF	TDK	CGA4J3X7R1C225K125AB	CAP CER 2.2 µF 16 V 10 % X7R AEC-Q200 0805
C32	0.022 µF	TDK	C2012X7R2A223K125AA	CAP CER 0.022 µF 100 V 10 % X7R 0805
C39	0.01 µF	Murata	GCM155R71H103KA55D	CAP CER 0.01 µF 50 V 10 % X7R AEC-Q200 0402
C41	0.01 µF	Murata	GCM155R71E103KA37D	CAP CER 0.01 µF 25 V 10 % X7R AEC-Q200 0402
CBAT1	47 µF	Panasonic	EEE1VA470WAP	CAP ALEL 47 µF 35 V 20 % -- AEC-Q200 SMT
CBOOT1	0.047 µF	TDK	CGA2B3X7R1H473K050BB	CAP CER 0.047 µF 50 V 10 % X7R AEC-Q200 0402
CBOS1	4.7 µF	Murata	GCM21BC71A475KA73	CAP CER 4.7 µF 10 V 10 % X7S AEC-Q200 0805
D1	PMEG6045ETP	Nexperia	PMEG6045ETPX	DIODE SCHOTTKY 60 V 4.5 A AEC-Q101 SOD128
D2	NRVTS260ESF	ON Semiconductor	NRVTS260ESFT1G	DIODE PWR SCH RECT 2 A 60 V AEC-Q101 SOD-123FL
LBK1, LBK2, LBK3	1 µH	TDK	TFM252012ALMA1R0MTAA	IND PWR 1.0 µH @ 1 MHz 4.7 A 20 % AEC-Q200 SMD
LBO1	4.7 µH	TDK	TFM252012ALMA4R7MTAA	IND PWR 4.7 µH @ 1 MHz 2.2 A 20 % AEC-Q200 SMD
LPI1	1 µH	TDK	SPM6545VT-1R0M-D	IND PWR 1.0 µH @ 100 KHz 22.9 A 20 % AUTO SMD
LPRE1	6.8 µH	TDK	SPM7054VT-6R8M-D	IND PWR 6.8 µH 10.9 A 20 % AUTO SMD
Q1	BUK9K18-40E	Nexperia	BUK9K18-40E, 115	TRAN NMOS PWR SW DUAL 19.5 mΩ 30 A 40 V AEC-Q101 LFPAK56D
R1, R7, R12, R14, R15, R16, R21	5.1 kΩ	Panasonic	ERA2AEB512X	RES MF 5.1 kΩ 1/16W 0.1 % 0402
R2	2.2 Ω	KOA Speer	RK73H1JTTD2R20F	RES MF 2.2 Ω 1/10 W 1 % 0603
R3, R4	1 MΩ	VISHAY	CRCW04021M00FKED	RES MF 1.0 MΩ 1/16 W 1 % AEC-Q200 0402
R5	3.57 kΩ	KOA Speer	RK73H1ETTP3571F	RES MF 3.57 kΩ 1/10 W 1 % AEC-Q200 0402
R6, R8, R13	10 kΩ	Yageo	RC0402FR-1310KL	RES MF 10 kΩ 1/16 W 1 % 0402
R9, R11	2.2 kΩ	Panasonic	ERJ-2RKF2201X	RES MF 2.2 kΩ 1/10 W 1 % AEC-Q200 0402
R10	100 kΩ	Panasonic	ERJ-2RKF1003X	RES MF 100 kΩ 1 % 1/10 W AEC-Q200 0402

Part Reference	Value	Part Manufacturer[1]	Part Number[1]	Description
R17	90.9 kΩ	KOA Speer	RK73H1ETTP9092F	RES MF 90.9 kΩ 1/10 W 1 % AEC-Q200 0402
R18	68.1 kΩ	KOA Speer	RK73H1ETTP6812F	RES MF 68.1 kΩ 1/16 W 1 % 0402
R19, R20, R23, R25	22.1 kΩ	Panasonic	ERJ-3EKF2212V	RES MF 22.1 kΩ 1/10 W 1 % AEC-Q200 0603
R22	41.2 kΩ	Vishay	CRCW040241K2FKED	RES MF 41.2 kΩ 1/16 W 1 % AEC-Q200 0402
R24	115 kΩ	KOA Speer	RK73H1ETTP1153F	RES MF 115 kΩ 1/10 W 1 % AEC-Q200 0402
RSNS1	0.015 Ω	Vishay	WSLP1206R0150FEA	RES MF 0.015 Ω 1 W 1 % AEC-Q200 1206
U2	BZX84-A5V1	Nexperia	BZX84-A5V1, 215	DIODE ZENER 5.1 V 250 MW AEC-Q101 SOT23

[1] NXP does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

7 VPRE using inductor DCR current sensing

For high current applications (I_{PRE} > 5 A), the power dissipation in the current sense resistor becomes non-negligible (> 0.25 W). In that case, the DCR current sense technique can be a good alternative, using the intrinsic DCR of the inductor to sense the current. However, the inductor DCR value is less accurate than a shunt resistor which impacts the current limitation. Higher resistance value means lower current limitation and less accuracy means wider current limitation range.

7.1 Low DCR value

When the inductor DCR is low (lower than 15 mΩ as a guideline only), the DCR current sense with a single capacitor C_{LH} is possible. In this case, the current limitation is linked to the inductor DCR value ($I_{LIM\_PRE} = V_{PRE\_LIM\_TH} / R_{DCR}$).

This DCR current sense implementation is visible in Figure 10 using the R_{LL} and C_{LH} components.

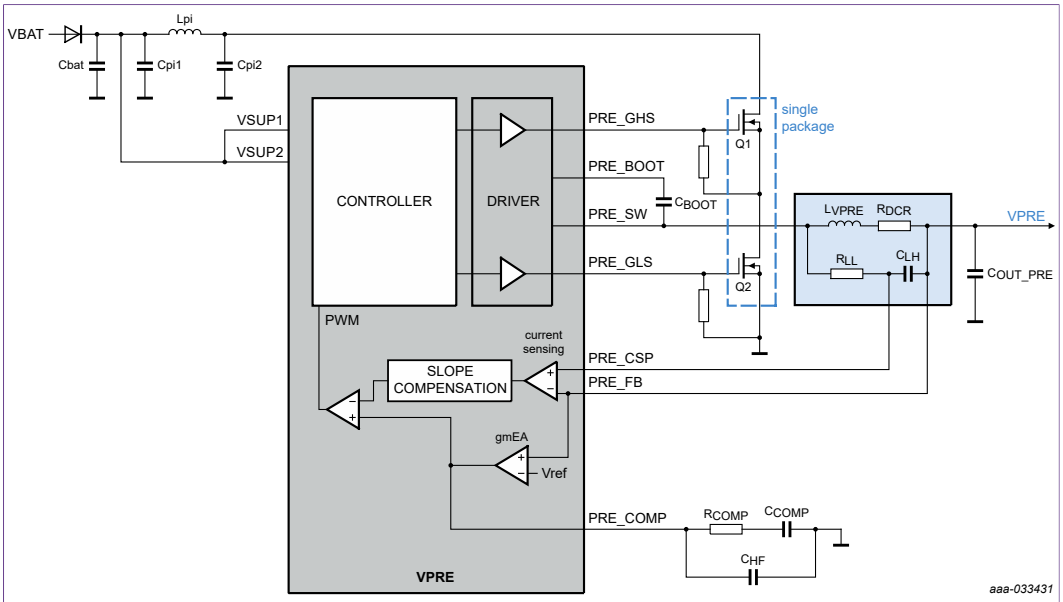


Figure 10. DCR current sense with a single capacitor

7.2 Components calculation

When R_{LL} and C_{LH} are selected in such a way that the RC time constant is equal to the ratio of inductance and its series resistance, the voltage across C_{LH} will be directly proportional to the inductor current.

$R_{LL} \times C_{LH} = L_{VPRE} / R_{DCR}$

Select R_{LL} = a resistor in the kΩ range or C_{LH} = a capacitor in the range of several hundred nF and calculate the other components.

Example for an inductor L = 6.8 µH and R_{DCR} = 10 mΩ:

- R_{LL} = 6.8 kΩ and C_{LH} = 100 nF
- I_{LIM_PRE} 12 A for $V_{PRE\_LIM\_TH}$ = 120 mV

7.3 Comparative results

V_{SUP} = 14 V, V_{PRE} = 4.1 V, Fsw = 455 kHz

L_{VPRE} = 6.8 µH, R_{DCR} = 10 mΩ, Cout = 66 µF

Rcomp = 3.57 kΩ, Ccomp = 6.8 nF, Chf = 150 pF

Figure 11 shows comparative results between the resistor current sensing with Rshunt = 10 mΩ and the inductor DCR current sensing with R_{DCR} = 10 mΩ, R_{LL} = 6.8 kΩ, C_{LH} = 100 nF.

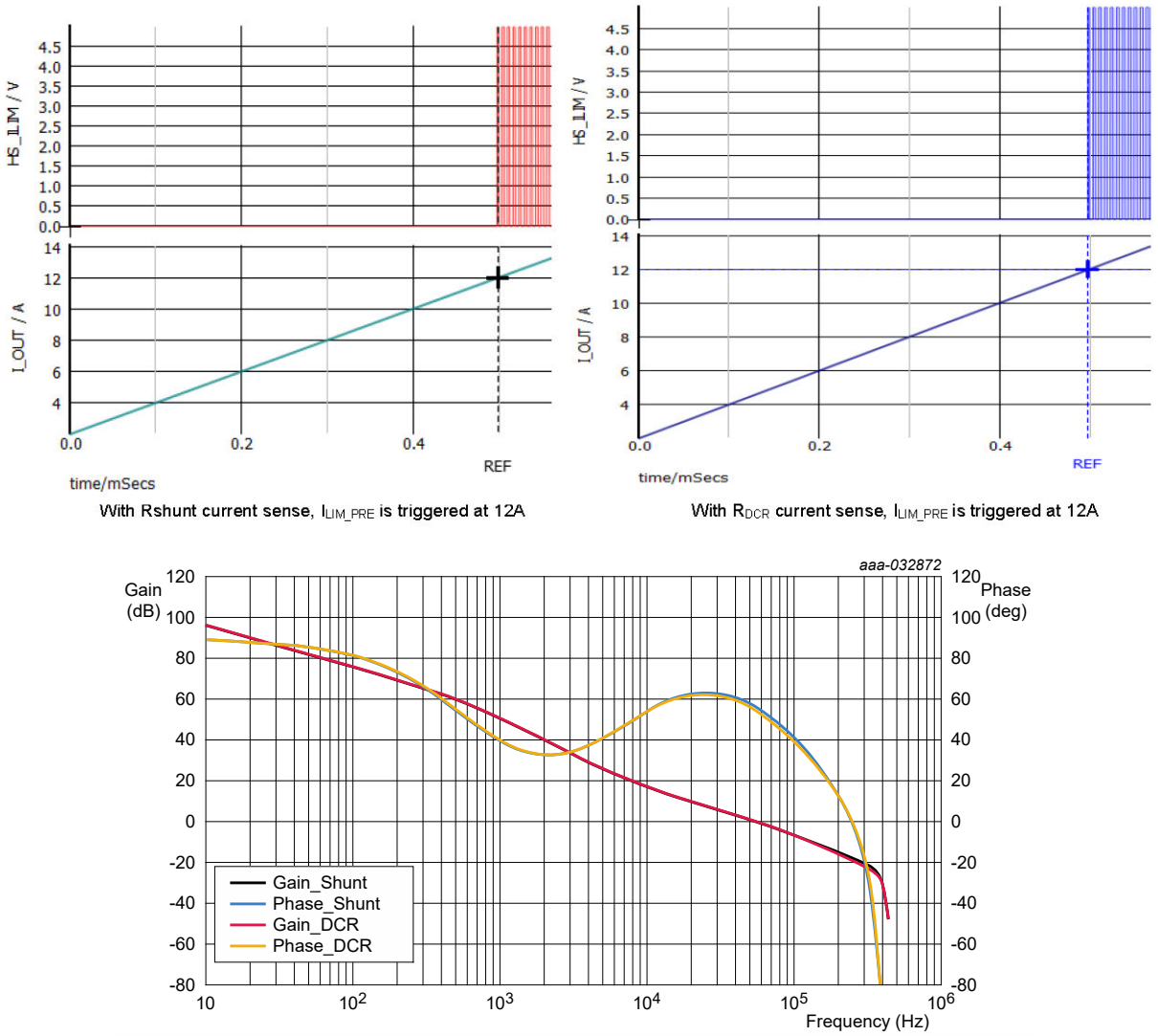


Figure 11. Resistor current sensing with Rshunt = 10 mΩ vs. inductor DCR current sensing with R_{DCR} = 10 mΩ, R_{LL} = 6.8 kΩ, C_{LH} = 100 nF

Table 3. Calculation summary

Current sense	Bandwidth	PM	GM	I_{LIM_PRE}
Rshunt	55 kHz	55 deg	17 dB	12 A
DCR	55 kHz	53 deg	18 dB	12 A

The results obtained with Rshunt current sense or inductor DCR current sense confirms similar performance.

7.4 High DCR value

When the inductor DCR is high (higher than 15 mΩ as a guideline only), the DCR current sense with a resistor divider (R_{LL} + R_{LH}) helps to maintain a high current limitation by feeding a ratio of the current to the differential amplifier.

In that case, the current limitation is linked to the voltage across R_{LH} resistor. The ratio between R_{LL} and R_{LH} to maintain the current limitation is considered in the components calculation.

This DCR current sense implementation is visible in the Figure 12 using R_{LL} + R_{LH} + C_{LH} components.

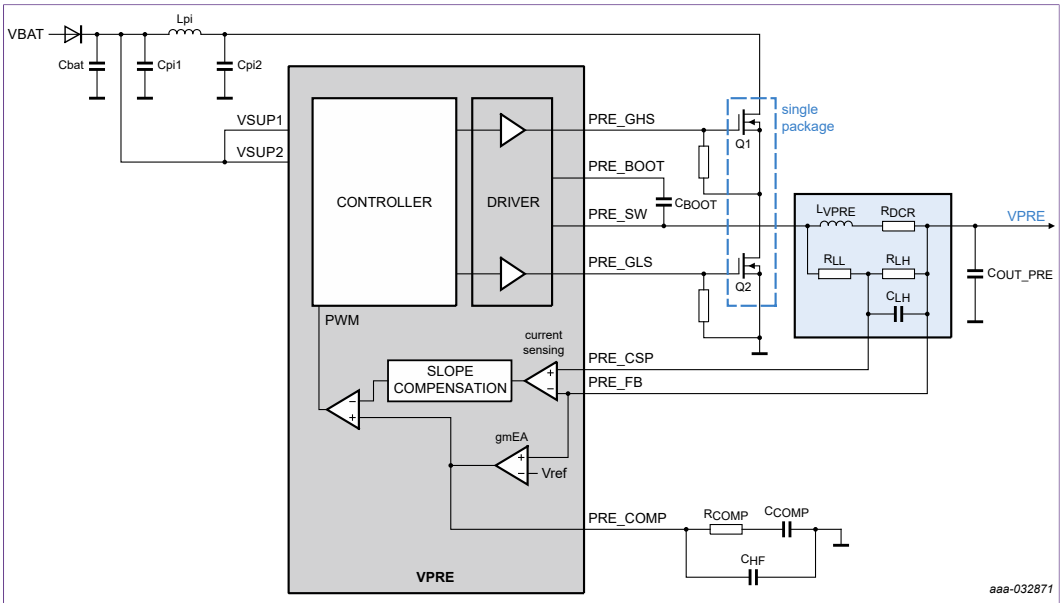


Figure 12. DCR current sense with a capacitor divider

7.5 Components calculation

When R_{LL} and C_{LH} are selected in such a way that the RC time constant is equal to the ratio of inductance and its series resistance, the voltage across C_{LH} will be directly proportional to the inductor current.

$R_{LL} \times C_{LH} = L_{VPRE} / R_{DCR}$

Select R_{LL} = a resistor in the kΩ range or C_{LH} = capacitor in the range of several hundred nF and calculate the other components.

Example for an inductor L = 6.8 µH and R_{DCR} = 20 mΩ

- I_{LIM_PRE} = 12 A for $V_{PRE\_LIM\_TH}$ = 120 mV
- C_{LH} is selected at 100 nF
- R_{LL} and R_{LH} are calculated.

Table 4. Calculation summary

Parameter	Value	Unit	Comments
L_{PRE}	6.8	µH	—
R_{DCR_REAL}	0.020	Ω	—
$V_{PRE\_LIM\_TH}$	0.12	V	ILIM (OTP)
I_{PRE_MAX}	12	A	—
R_{DCR_TARGET}	0.010	Ω	$V_{PRE\_LIM\_TH}$ / I_{PRE_MAX}

Parameter	Value	Unit	Comments
Ratio	2.0	°	R_{DCR_REAL} / R_{DCR_TARGET}
C_{LH}	100	nF	Selected
R_{LL}	—	kΩ	Lpre / R_{DCR_TARGET} / C_{LH}
R_{LH}	—	kΩ	—
V_L_{PRE}	0.3	V	R_{DCR_REAL} × I_{PRE_MAX}
V_R_{LH}	0.12	V	= $V_{PRE\_LIM\_TH}$ at I_{PRE_MAX}

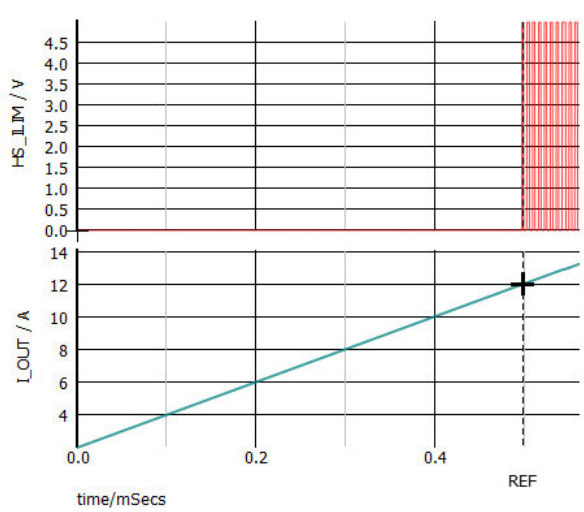
7.6 Comparative results

V_{SUP} = 14 V, V_{PRE} = 4.1 V, Fsw = 455 kHz

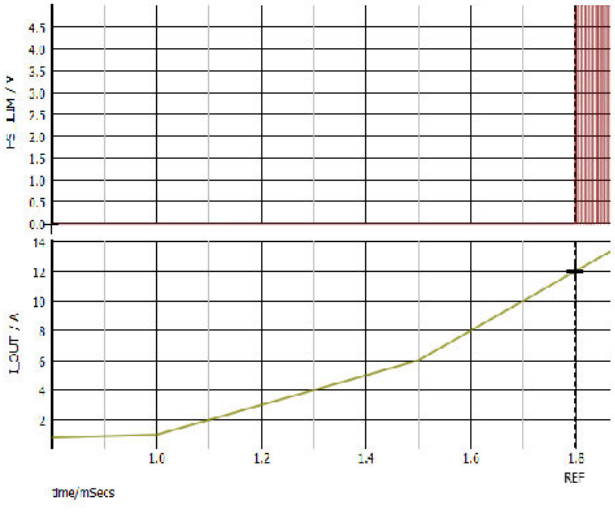
L_{VPRE} = 6.8 µH, R_{DCR} = 20 mΩ, Cout = 66 µF

Rcomp = 3.57 kΩ, Ccomp = 6.8 nF, Chf = 150 pF

Figure 13 shows comparative results between the resistor current sensing with Rshunt = 10 mΩ and the inductor DCR current sensing with R_{LL} = 6.8 kΩ, R_{LH} = 6.8KΩ, C_{LH} = 100 nF



With Rshunt current sense, I_{LIM_PRE} is triggered at 12A



With R_{DCR} current sense, I_{LIM_PRE} is triggered at 12A

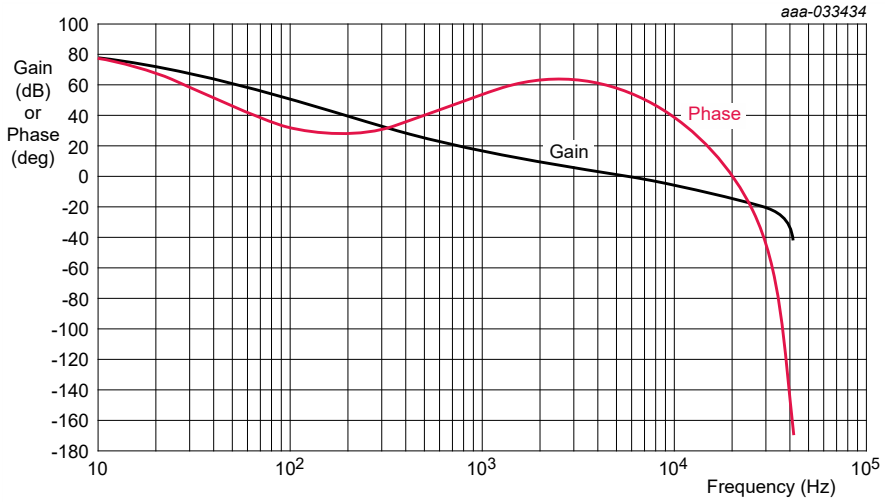


Figure 13. Resistor current sensing with Rshunt = 10 mΩ vs. inductor DCR current sensing with R_{LL} = 6.8 kΩ, R_{LH} = 6.8KΩ, C_{LH} = 100 nF

Table 5. Calculation summary

Current sense	Bandwidth	PM	GM	I_{LIM_PRE}
Rshunt	58 kHz	55 deg	14 dB	12 A
DCR	58 kHz	55 deg	14 dB	12 A

The results obtained with Rshunt current sense or inductor DCR current sense confirms similar performance.

8 How to use VR5500 and FS5502 without BUCK1

BUCK1 may not be required if VR5500[1] and FS5502[2] do not supply the MCU core or if the MCU core requires only 3.3 V or 5 V. Since BUCK1 cannot be disabled by OTP, follow this procedure to use VR5500, FS5502 without BUCK1:

1. BUCK1_IN connected to VPRE to keep VPRE_FB_OV protection otherwise BUCK1_IN can be left open.
2. BUCK1_SW and BUCK1_FB pins open.
3. BUCK1 in power up slot 7 by OTP to not start automatically.
4. VCOREMON pin open.
5. VCOREMON not assigned to PGOOD and ABIST1.
6. Permanent VCOREMON_UV will be reported. To be discarded since BUCK1 is not used.
7. Configure VCOREMON_UV_FS_IMPACT[1:0] = VCOREMON_OV_FS_IMPACT[1:0] = 00 during INIT_FS for no effect on RSTB by VCOREMON.

9 MCU with CORE_SENSE connection

In order to regulate the CORE voltage at the MCU silicon, some high-power MCUs have a sense connection for the CORE supply instead of through the input pin of the package. See Figure 14 for the recommended connection.

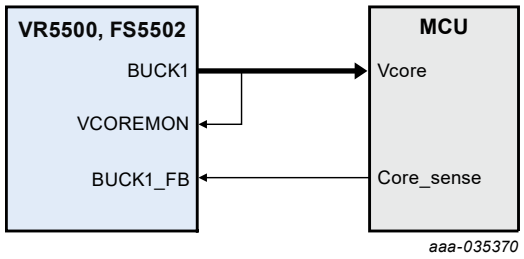


Figure 14. Recommended connection to regulate CORE voltage at MCU silicon

10 PGOOD and RSTB connections

10.1 VR5500/FS5502 connection to MCU

- VR5500/FS5502 PGOOD output connected to MCU PORB input for hardware reset
- PGOOD assertion is configured by OTP
- RSTB assertion is configured by I^2C during INIT_FS

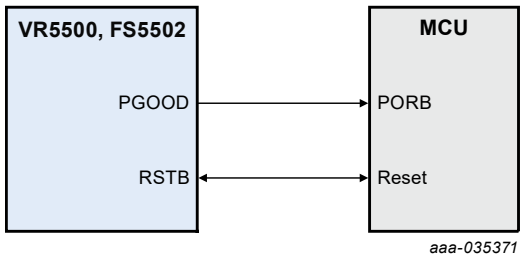


Figure 15. VR5500/FS5502 connection to MCU

11 ISO pulses

11.1 ISO-pulse description

For a description and images of test pulses, see Table 6.

Table 6. Pulse reference documents

Pulse	Reference documents[1]
Figure 5 — Test pulse 1, page 12. Figure 6 — Test pulse 2a, page 13 Figure 8 — Test pulse 3a, page 15 Figure 9 — Test pulse 3b, page 16	ISO 7637-2:2011(E)[16]
Figure 11: Cold start test pulse, page 29. 4a, 4b (former cranking pulses)	VW 80000: 2009-10[22]
Figure 9 — Test with centralized load dump suppression, (Test pulse 5b), page 12	ISO 16750-2:2012[18]
Figure 9 — Test with centralized load dump suppression, (Test pulse 5b1), page 13	ISO 16750-2:2010(E)[17]

[1] See Section 15 for a list of documents referenced in this application note.

11.1.1 12 V automotive system

- **Pulse 1:** Ua = 14 V, Us = –150 V, Ri = 10 Ω, Td = 2 ms, Tr = 1 µs, T 1 = 0.5 s, T2 = 200 ms, T3 < 100 µs, 500 pulses
- **Pulse 2a:** Ua = 14 V, Us = 112 V, Ri = 2 Ω, Td = 50 µs, Tr = 1 µs, T1 = 0.2 s, 500 pulses
- **Pulse 3a:** Ua = 14 V, Us = –220 V, Ri = 50 Ω, Td = 150 ns, Tr = 5 ns, T1 = 100 µs, T4 = 10 ms, T5 = 90 ms, 1 Hr
- **Pulse 3b:** Ua = 14 V, Us = 150 V, Ri = 50 Ω, Td = 150 ns, Tr = 5 ns, T1 = 100 µs, T4 = 10 ms, T5 = 90 ms, 1 Hr
- **Pulse 4a:** Ub = 11V, Ut = Us = 4.5V, Ua = 6.5V, Ur = 2V, Tf = 1ms, T4 = T5 = 0, T6 = 19ms, T7 = 50ms, T8 = 10s, Tr = 100 ms, F = 2Hz, 10 cycles at interval 2 s
- **Pulse 4b:** Ub = 11V, Ut = 3.2V, Us = 5.0 V, Ua = 6.0 V, Ur = 2 V, Tf = 1 ms, T4 = 19 ms, T5 = 1 ms, T6 = 329 ms, T7 = 50 ms, T8 = 10 s, Tr = 100 ms, F = 2Hz, 10 cycles at interval 2 s
- **Pulse 5b:** Ua = 14V, Us = 35 V, Ri = 1 Ω, Td = 400 ms, Tr = 5 ms, 10 pulses at interval of 1 min

11.1.2 24 V truck system

- **Pulse 1:** Ua = 28 V, Us = –600 V, Ri = 50 Ω, Td = 1 ms, Tr = 3 µs, T1 = 0.5s, T2 = 200 ms, T3 < 100 µs, 500 pulses
- **Pulse 2a:** Ua = 28 V, Us = 112 V, Ri = 2 Ω, Td = 50 µs, Tr = 1 µs, T1 = 0.2 s, 500 pulses
- **Pulse 3a:** Ua = 28 V, Us = –300 V, Ri = 50 Ω, Td = 150 ns, Tr = 5 ns, T1 = 100 µs, T4 = 10 ms, T5 = 90 ms, 1 Hr
- **Pulse 3b:** Ua = 28 V, Us = 300 V, Ri = 50 Ω, Td = 150 ns, Tr = 5 ns, T1 = 100 µs, T4 = 10 ms, T5 = 90 ms, 1 Hr
- **Pulse 5b:** Ua = 28 V, Us = 58 V, Ri = 2 Ω, Td = 350 ms, Tr = 5 ms, 10 pulses at interval of 1 min
- **Pulse 5b1:** Ua = 28 V, Us = 65 V, Ri = 2 Ω, Td = 350 ms, Tr = 5 ms, 10 pulses at interval of 1 min

11.2 Product setup and failing criteria for ISO pulses

All the ISO test pulses are applied to VBAT, at 25 °C, with all regulators loaded according to Table 7.

Table 7. Regulators setting

Output	Vout (V)	Iout (A)
VPRE	4.1	3.3
Buck1	1.25	1.25
Buck2	1.8	1.2
Buck3	2.3	1
Boost	5.74	Loaded by LDO
LDO1	1.8	0.1
LDO2	3.3	0.1

Class A: RSTB remains released during the stress

Class C: RSTB is asserted during the stress but released after the stress

11.3 ISO pulse results

Table 8. ISO pulse results

System Voltage	Pulse	Duration	Result
12 V	Pulse 1	500 pulses	**Class C**[1]
24 V	Pulse 1	500 pulses	**Class A**
12 V	Pulse 2a	500 pulses	**Class A**
24 V	Pulse 2a	500 pulses	**Class A**
12 V	Pulse 3a	1 hour	**Class A**
24 V	Pulse 3a	1 hour	**Class A**
12 V	Pulse 3b	1 hour	**Class A**
24 V	Pulse 3b	1 hour	**Class A**
12 V	Pulse 5b	10 pulses	**Class A**
24 V	Pulse 5b	10 pulses	**Class A**
24 V	Pulse 5b1	10 pulses	**Class A**[2]
12 V	LV 124[22] E-11 (4a)	1 pulses	**Class A**
12 V	LV 124[22] E-11 (4b)	1 pulses	**Class A**

[1] Negative pulse 1 generates a device reset after each pulse, inducing RSTB assertion.
[2] External TVS protection required in front of VSUP1/2 pins. MMSZ56T1G TVS reference was used in combination with VPRE MOSFET SQJB80EP-T1 (80 V capable).

12 Non-ISO pulses

12.1 Non-ISO pulse description

For a description and images of test pulses described and documented in various ISO documents, see Table 9.

Table 9. Pulse reference documents

Pulse	Reference documents[1]
Figure 6: Test pulse E-07 Slow decrease and increase of the supply voltage, page 20	VW 80000: 2009-10[22]
Figure 7: Test pulse E-08 Slow decrease, quick increase of the supply voltage, page 22	VW 80000: 2009-10[22]
Figure 9: Test pulses E-10 Short interruptions, page 27	VW 80000: 2009-10[22]

[1] See Section 15 for a list of documents referenced in this application note.

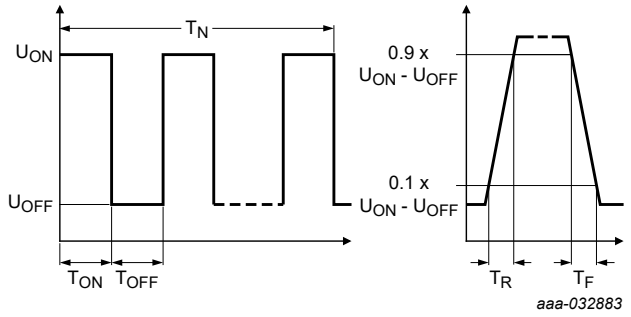


Figure 16. Battery voltage dropout

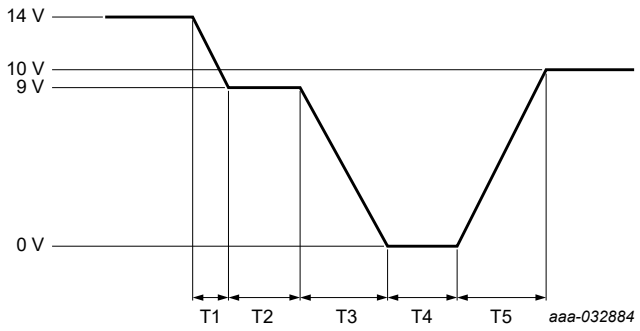


Figure 17. Battery brownout/recovery

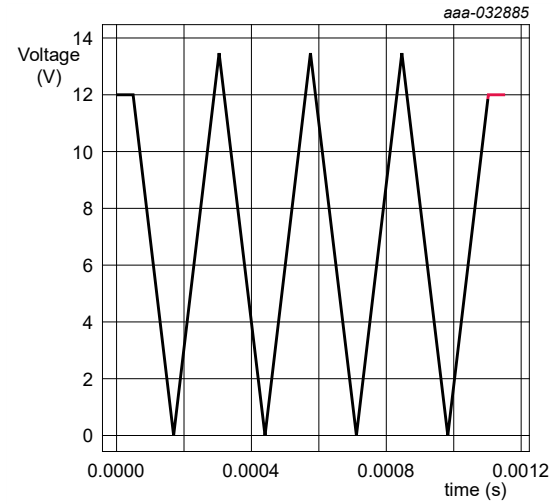


Figure 18. Triangular pulse 1

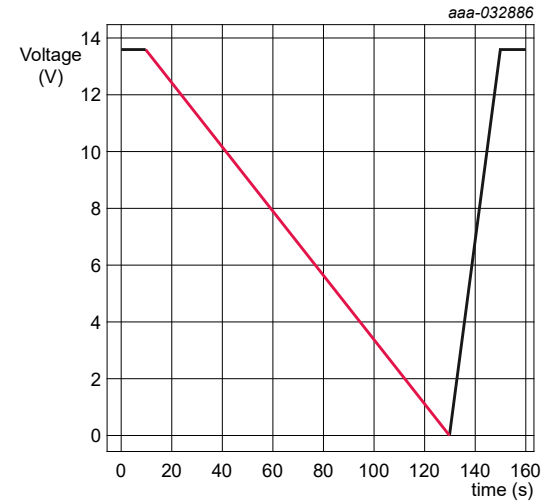


Figure 19. Triangular pulse 2

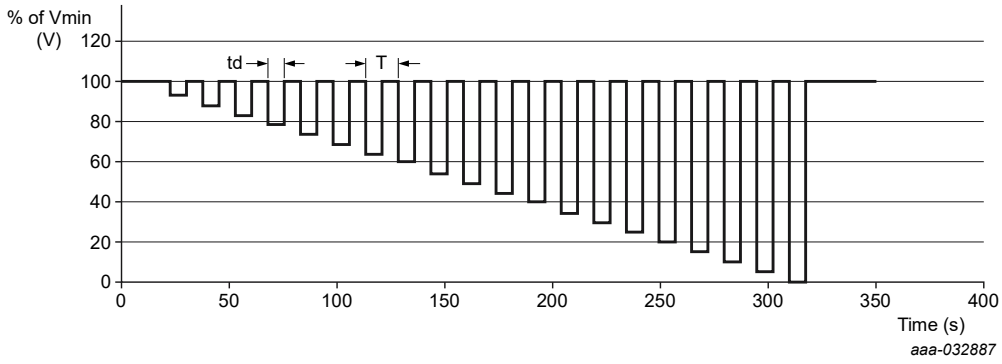


Figure 20. Re-init pulse

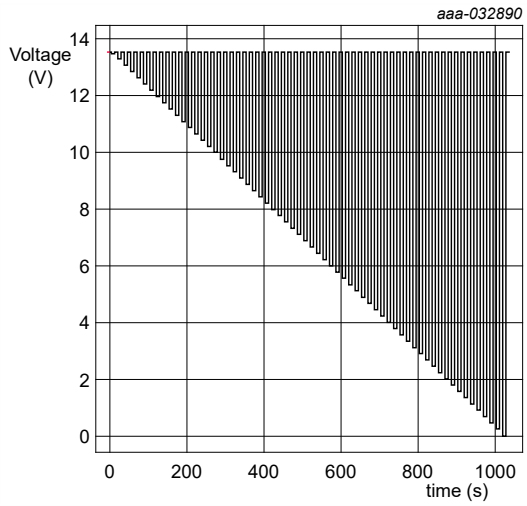


Figure 21. LV124[22] E-09

12.2 Product setup and failing criteria for non-ISO pulses

All the non ISO test pulses are applied at VBAT. They are executed in temperature (at Ta = – 40 °C, Ta = + 25 °C and Ta = + 125 °C), with VPRE at 455 kHz and 2.2 MHz, without load and with loads according to Table 10.

Table 10. Regulators setting

Output	Vout (V)	Iout (A)
VPRE	4.1	3.3
Buck1	1.25	1.25
Buck2	1.8	1.2
Buck3	2.3	1
Boost	5.74	Loaded by LDO
LDO1	1.8	0.1
LDO2	3.3	0.1

Class A: RSTB remains released during the stress

Class C: RSTB is asserted during the stress but released after the stress

12.3 Non-ISO pulse results

Table 11. Non-ISO pulse results

Pulse type	Pulse description	No. of pulses	Results
Truck jump start	VBAT = 48 V during 15 min	1	Class A
Battery Voltage Dropout VBAT = UON = 13.5 V, UOFF = 0 V, tr/tf ≤ 1 µs, Ri = 0.01 Ω	t_{ON} = 0.9 ms, t_{OFF} = 0.1 ms	4000	Class A
	t_{ON} = 9 ms, t_{OFF} = 1 ms	10	Class C
	t_{ON} = 9 ms, t_{OFF} = 6 ms	10	Class C
	t_{ON} = 200 ms, t_{OFF} = 10 ms	10	Class C
	t_{ON} = 200 ms, t_{OFF} = 100 ms	10	Class C
Battery Brownout/Recovery VBAT = 13.5 V	T1 = 1 s, T2 = 10 s, T3 = 28800 s, T4 = 10 s, T5 = 7200 s	1	Class C
Triangular Pulse 1 VBAT_start = 12 V, VBAT_stop = 0 V, VBAT_max = 13.5 V	Slope = 0.1 V / µs	3	Class A
	Slope = 1 V / s	3	Class C
	Slope = 1 V / min	3	Class C
Triangular Pulse 2 VBAT_start = 12 V, VBAT_stop = 0 V	Fall time from 2 min to 30 min by step of 2 min	1	Class C
	Fall time from 1 h to 7 h by step of 2 h	1	Class C
	Rise time from 2 min to 30 min by step of 2 min	1	Class C
	Rise time from 1 h to 7 h by step of 2 h	1	Class C
Re-init pulse VBAT = 13.5 V	tr/tf = 1 ms, td = 5 s, T = 10 s, 20 steps by 5 %	1	Class C
LV124[22] **E-07** UBmax = VBATmax = 12 V, UBmin = VBATmin = xV	Slope 0.5 V / min	1	Class C
LV124[22] **E-08** UBmax = VBATmax = 12 V, UBmin = VBATmin = xV	Slope = 0.5 V/min Holding at 0 V = 1 min Tr < 0.5 s	1	Class C
LV124[22] **E-09** VBAT_start = 13.5 V, VBAT_stop = 0 V,	Frequency = 0.06 Hz duty cycle = 0.5	1	Class C
LV124[22] **E-10** VBAT = 11 V, T2 = 10s	T1 > 10 µs to 100 µs with interval of 10 µs T1 = 100 µs to 1 ms with interval of 100 µs	1	Class A
	T1 = 1 ms to 10 ms with interval of 1 ms T1 = 10 ms to 100 ms with interval of 10 ms T1 = 100 ms to 2 s with interval of 100 ms	1	Class C

Results depend on the use case condition. Table 11 does not include all the possible, custom non-ISO test pulses applied to VR5500/FS5502. Only one third of the most common tests are listed. Contact your local NXP representative if custom pulses are needed for your application.

13 EMC performance

13.1 PCB components placement

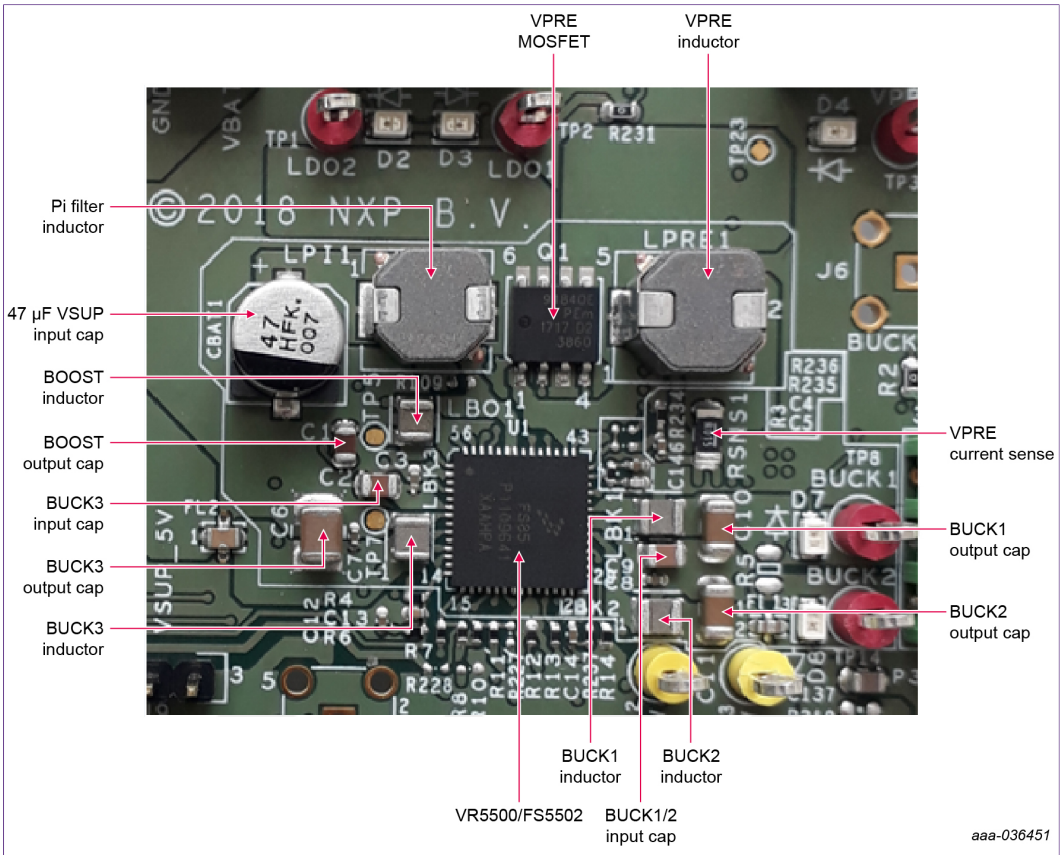


Figure 22. PCB component placement

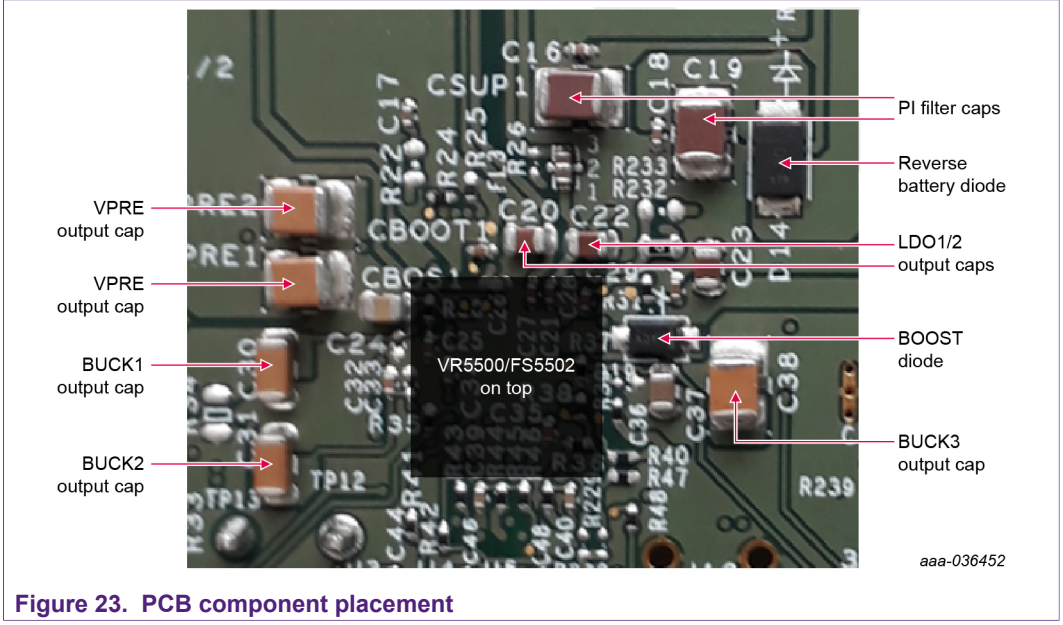


Figure 23. PCB component placement

13.2 Layout guidelines

- Design uses 6 PCB layers:
  - L1 : Top layer used as DC/DC power plane
  - L2 : System ground
  - L3 : Power Island / Signal
  - L4 : System Ground
  - L5 : Signal
  - L6 : DC/DC local power plane
- If a high current loop is going through multiple PCB layers, multiple vias are recommended to limit the parasitic (R and L) in the high current path.
- When a signal is going thru multiple PCB layers, ground vias around the layer interconnection are recommended to contain the electrical field
- Avoid low level signals below SMPS power components
- To avoid noise injection, connect components with high-impedance signals close to the device pin
- SMPS current loop as small as possible with wide tracks
- SMPS feedback lines shall be shielded
- BUCK1/2/3 feedbacks shall be connected close to the load
- When BUCK1/2 are used in multiphase, BUCK1 and BUCK2 layout shall be as symmetrical as possible
- VPRE feedback is also used for Current Sense Negative. so VPRE feedback shall be connected to Rshunt and not to the load.

Refer to the *Layout and PCB guidelines* section of the product data sheet for additional information.

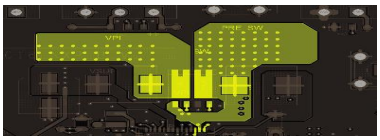
13.3 Thermal management

13.3.1 Package with exposed pad

The VR5500/FS5502 package is a QFN 56-pin package with an exposed pad for enhanced thermal dissipation. Details of the PCB footprint design are available in the section titled *PCB footprint design* of AN1902[14].

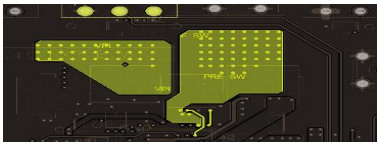
13.3.2 VPRE MOSFET power dissipation

- To minimize the power dissipation in VPRE external MOSFETs, a minimum PCB copper area can be used for this purpose. The application note, AN10874[15] provides useful information.
- On NXP EVB design, 70 µm copper layer thickness for top and bottom layers are used to improve the dissipation. The power dissipation in the MOSFETs is optimized by the copper areas on Layers 1 (Figure 24), 3 (Figure 25) and 6 (Figure 26).



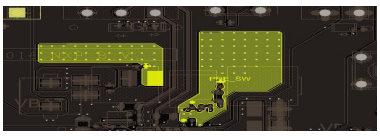
aaa-032894

Figure 24. Layer 1



aaa-032895

Figure 25. Layer 3



aaa-032896

Figure 26. Layer 6

13.4 Product setup

All EMC tests are performed at 25 °C, with all regulators configured and loaded according to the *EMC compliance* section of the product data sheet.

13.5 Conducted Emission (CE)

Compliance to IEC 61967-4:[19]

- Global pins: VBAT (Vsup1 and Vsup2), 150 Ω method, 12-M level
- Local pins: VPRE, VBOOST, BUCK1/2/3, LDO1/2, 150 Ω method, 10-K level

The main parameters for the emission measurements are described in Table 12 according to the IEC specification.

Table 12. Emission measurements main parameters

Frequency range	Resolution bandwidth RBW	Step size
150 kHz to 30 MHz	9 kHz	4.5 kHz
30 MHz to 1 GHz	120 kHz	60 kHz

VBAT results are obtained with spread spectrum enabled and the external components discussed in Section 6. For spread spectrum information, refer to the *Spread spectrum* section of the product data sheet.

VPRE results are obtained after ferrite Murata BLM31PG601SH1 + 100 nF to GND.

VBOOST results are obtained after ferrite Murata BLM31PG601SH1 + 47 nF to GND.

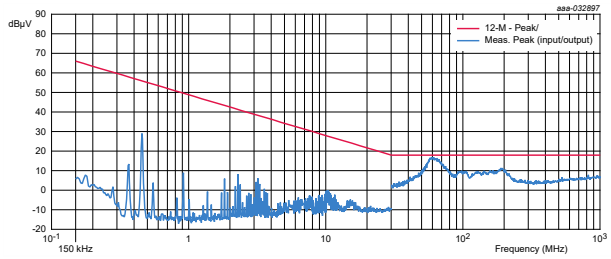


Figure 27. VBAT with VPRE = 455 kHz

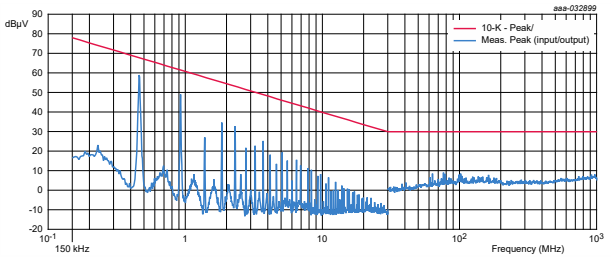


Figure 28. VPRE @ 455 kHz

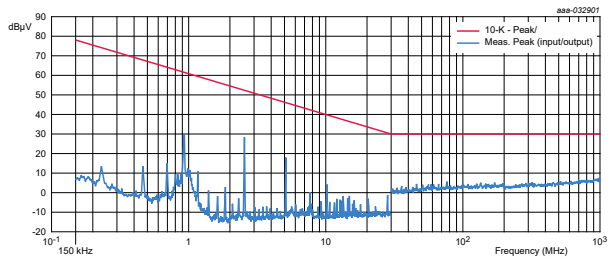


Figure 29. VBOOST @ 2.22 MHz

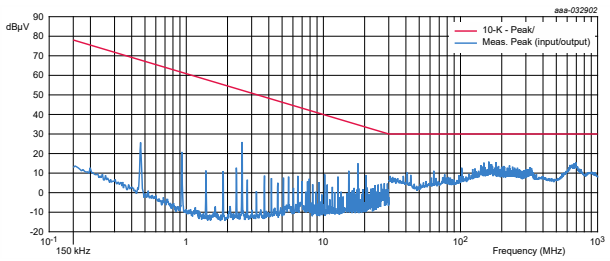


Figure 30. LDO1/2

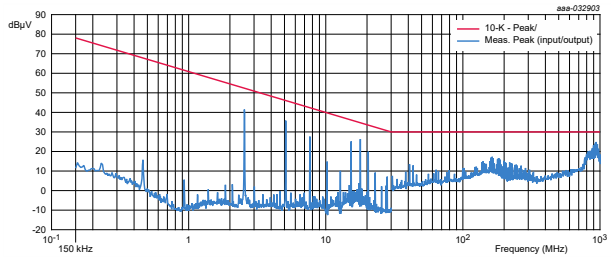


Figure 31. BUCK1/2 @ 2.22 MHz

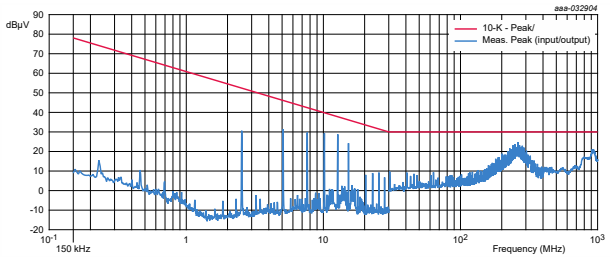


Figure 32. BUCK3 @ 2.22 MHz

13.6 Direct Power Injection (DPI)

Compliance to IEC 62132-4.[20]

- Global pins (supplies): VBAT (Vsup1 and Vsup2), 36 dBm, Class A
- Global pins (non-supplies): WAKE1, WAKE2, 30 dBm, Class A
- Local pins (supplies): VPRE @455 kHz, BUCK1/2/3 @ 2.22 MHz, LDO1/2, 12 dBm, Class A
- Local pins (non-supplies): RSTB, PGOOD, VDDIO, VDDI2C, VBOS, 12 dBm, Class A

Class A: no state change on RSTB, PGOOD state and all regulators in spec

Table 13. DPI results

Pin	Classification	Level	Result
VBAT (Vsup1, Vsup2)	Global	36 dBm	**PASS**
WAKE1 and WAKE2	Global	30 dBm	**PASS**
WAKE2	Local	12 dBm	**PASS**
VPRE	Local	12 dBm	**PASS**
BUCK1, BUCK2	Local	12 dBm	**PASS**
LDO1, LDO2	Local	12 dBm	**PASS**
BUCK3, VDDIO	Local	12 dBm	**PASS**
VDDI2C	Local	12 dBm	**PASS**
VBOS	Local	12 dBm	**PASS**
RSTB	Local	12 dBm	**PASS**
PGOOD	Local	12 dBm	**PASS**

13.7 Radiated Emission (RE)

Compliance with FMC1278[21] RE 310 Level 2 Requirement in Normal mode

Table 14. Limits in dB µV/m, level 2

Frequency (MHz)	G1 0.53 - 1.7	NA1 45 - 48	G2 65 - 88	JA1 75 - 91	G3 89 - 109	G4 140 - 176	G5 172 - 242
Limit A, PK	20	20	20	20	20	20	20
Limit A, AV	12	12	12	12	12	12	12
Limit B, QP	30	24	24	24	24	24	24

Frequency (MHz)	G6a 310 - 320	EU3 380 - 430	G6b 429 - 439	G7a 868 - 870	G67b 902 - 904	EU4 1598 - 1604
Limit A, PK	20	20	25	30	30	—
Limit A, AV	14	14	19	24	24	4
Limit B, QP	30	30	30	—	—	—

Frequency (MHz)	G8 1567 - 1574	G8 1574 - 1576	G8 1576 - 1583
Limit A, AV	44 – 20664 × log(f/1567)	4	4 + 20782 × log(f/1576)

13.7.1 RE setup

- VBAT = 13.5 V, Room temperature (23 °C)
- LISN is used only on Battery +
- Battery ground is connected on the ground plane.
- Ground to DUT is done with a wire.

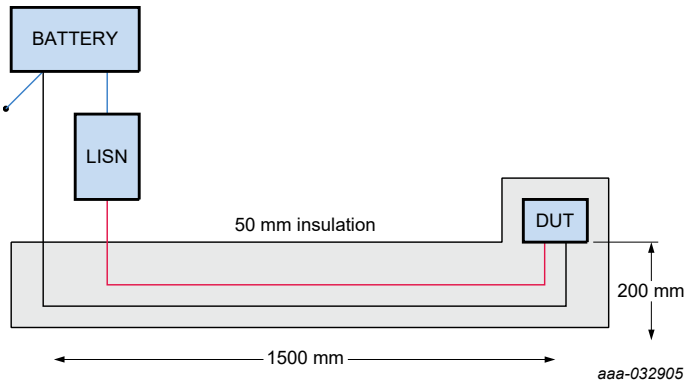


Figure 33. Radiated emission setup diagram

Table 15. Radiated emission test settings

Setting	Range
Frequency Range	0.15 - 1605 MHz
Bandwidth acc. to CISPR 25	1 / 9 / 120 kHz
Frequency Step Δf	0.25 / 2.25 / 30 kHz (FFT)

Setting	Range
Measuring time	200 ms / QP: 1000 ms
Detector	Peak (PK) / Average (AV) / Quasi-Peak (QP)

13.7.2 RE results

aaa-032906

Figure 34. Radiated emission test setup: board shielded, spread spectrum enabled, VPRE @ 455 kHz, SRLS = 11, SRHS = 00

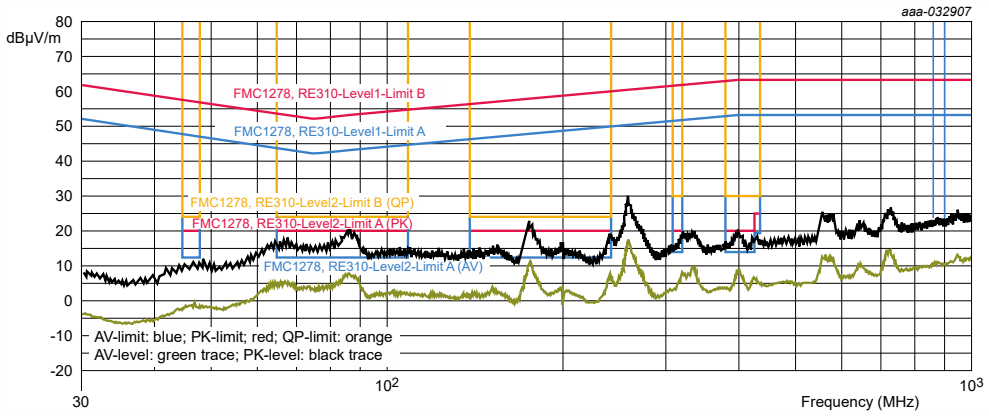


Figure 35. Radiated emission results: compliant for 12 kHz PK/AV BW limits

Table 16. Settings for radiated emission results: compliant for 12 kHz PK/AV BW limits

Setting	Value
f	30 - 1000 MHz
Δf	30 kHz (FFT)
Det.	PK / AV
BW	120 kHz
T	200 ms
Antenna	Horizontal

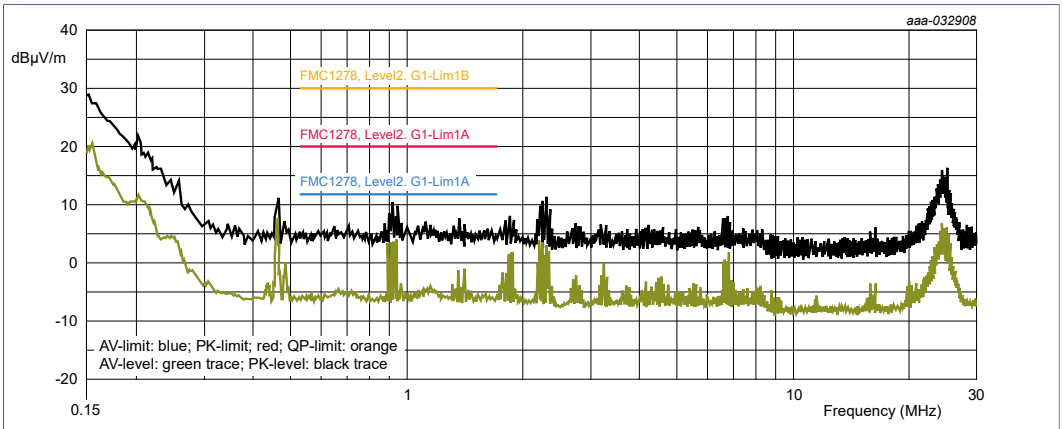


Figure 36. Radiated emission results: compliant for 9 kHz PK/AV BW limits

Table 17. Settings for radiated emission results: compliant for 9 kHz PK/AV BW limits

Setting	Value
f	0.15 - 30 MHz
Δf	2.25 kHz (FFT)
Det.	PK / AV
BW	9 kHz
T	200 ms
Antenna	Vertical

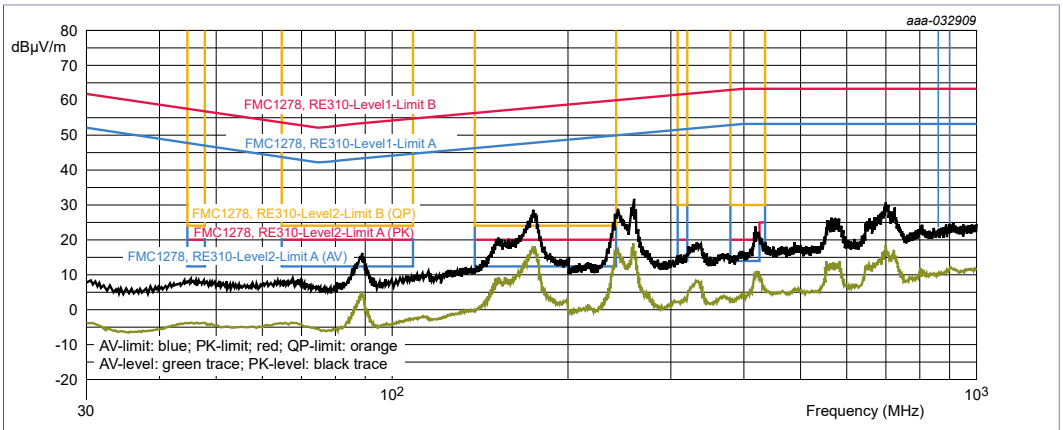


Figure 37. Radiated emission results: compliant for 12 kHz PK/AV BW limits

Table 18. Settings for radiated emission results: compliant for 12 kHz PK/AV BW limits

Setting	Value
f	30 - 1000 MHz
Δf	30 KHz (FFT)
Det.	PK / AV
BW	120 kHz
T	200 ms
Antenna	Vertical

13.8 Bulk Current Injection (BCI)

- Injection level per FMC1278[21] RI 112 Level 2 Requirement in Normal mode, RSTB released and no assertion
- Injection level per FMC1278[21] RI 112 Level 2 Requirement in Normal mode, RSTB asserted and no release
- No wake up when injecting FMC1278[21] RI 112 Level 2 Requirement in standby mode

13.8.1 BCI setup

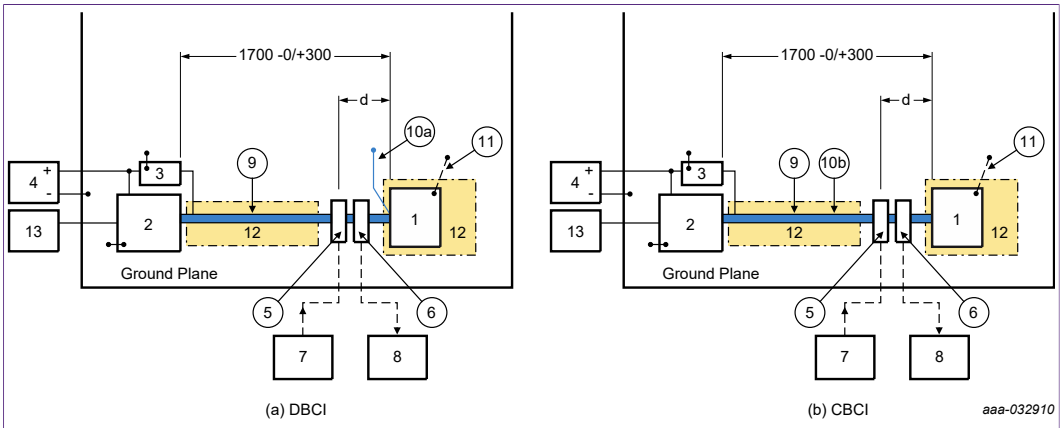


Figure 38. Bulk current injection setup

Table 19. BCI setup

Key	
1. DUT	8. Current monitoring equipment
2. Load simulator	9. DUT wire harness
3. Artificial network	10a. DUT power return removed from wire harness and connected directly to sheet metal. Wire length is 200 mm ± 50 mm.
4. Power supply	10b. DUT power return included in DUT wire harness
5. Injection probe	11. DUT case ground (refer to section 12.2, *Generic Test Setup* of FMC1278[21])
6. Monitor probe (requires prior approval by FMC EMC approval to use).	12. dielectric support ($\varepsilon_r \leq 1.4$)
7. RF generation equipment	13. Support/monitoring equipment

13.8.2 BCI results

Table 20. BCI test results

BCI test	Mode	Result
CBCI 150 mm	Normal	**PASS**
CBCI 450 mm	Normal	**PASS**
CBCI 750 mm	Normal	**PASS**

BCI test	Mode	Result
DBCI 150 mm	Normal	**PASS**
DBCI 450 mm	Normal	**PASS**
CBCI 150 mm	Standby	**PASS**
CBCI 450 mm	Standby	**PASS**
CBCI 750 mm	Standby	**PASS**
DBCI 150 mm	Standby	**PASS**
DBCI 450 mm	Standby	**PASS**

14 Interface customer module with NXP GUI by I²C

During engineering development only, it is possible to emulate or program an OTP configuration in VR5500/FS5502 device on customer module using a KL25z freedom interface. This board is providing USB to I²C interface. The hardware connection between the freedom board and the customer board is detailed in Figure 39.

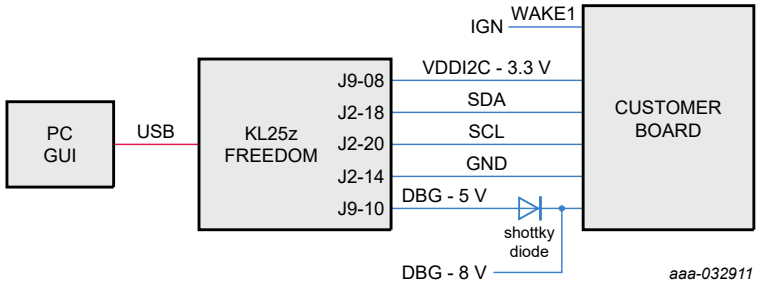


Figure 39. I²C interface with KL25z freedom board

- Ignition connected to WAKE1 to start the device
- DBG = 5 V used for emulation mode
- DBG = 8 V used for OTP burning (external power supply)
- GUI revision:
  - 0.5.4 with VR5500-b0-i2c-config-freedom-v1.0.3-ctm.flgi configuration file
  - or 0.7.4 or above selecting VR5500_with_KL25z_board_interface kit at startup
- KL25z firmware: NXP_FlexGUI_Firmware_v0.2.1.s19
- Default I²C address configured: 0x20 for the Main and 0x21 for the Fail-safe. If different, to be configured in the GUI before starting communication

OTP Emulation:

- Apply DBG voltage (5 V) and Vsup.
- Apply Wake 1.
- Load OTP script with the GUI.
- Release DBG voltage (back to GND with on board pull down).

OTP Burning:

- Apply DBG voltage (5 V) and Vsup.
- Apply Wake 1.
- Load OTP script with the GUI.

- Burn the OTP with the GUI.
- The GUI opens a pop-up to follow.
- The user is asked to apply DBG = 7.95 V at DBG - 8 V input. See Figure 39.

15 References

[1] **VR5500** — High voltage PMIC with multiple SMPS and LDO product data sheet
http://www.docstore.nxp.com
VR5500 product information web page https://www.nxp.com/VR5500

[2] **FS5502** — High voltage PMIC with multiple SMPS and LDO objective data sheet
http://www.docstore.nxp.com
FS5502 product information web page https://www.nxp.com/FS5502

[3] **VR5500_PDTCALC** — VPRE compensation network calculation and power dissipation tool (Excel file)
https://www.nxp.com/downloads/en/calculators/VR5500-PDTCALC.xlsx

[4] **VR5500_OTP_Config.xlsm** — OTP programming configuration (Excel file)
https://www.nxp.com/webapp/Download?colCode=VR5500-OTP&appType=moderatedWithoutFAE

[5] **FS5502_OTP_Config.xlsm** — OTP programming configuration (Excel file)
https://www.nxp.com/downloads/en/snippets-boot-code-headers-monitors/FS5502-OTP.xlsm

[6] **VR5500_VPRE_Simplis_Model**[1] — Simplis model for stability and transient simulations

[7] **Schematic**[1] — Reference schematic in Cadence and PDF formats

[8] **Layout**[1] — Reference layout in Cadence format

[9] **KITFVR5500AEEVM** — VR5500 24 V/36 V SBC evaluation board (EVB)
http://www.nxp.com/KITVR5500AEEVM

[10] **KITVR55-FSSKTEVM** — VR5500 SBC programming board
http://www.nxp.com/KITVR55-FSSKTEVM

[11] **FlexGUI** — Software Tool for Evaluation of Reference Design Kits
https://www.nxp.com/design/:FLEXGUI-SW

[12] **SW drivers rev 1.1** — SDK software drivers
https://www.nxp.com/design/:FS8500-FS8400-SW-DRIVER
Note: *VR5500/FS5502 and FS8400/FS8500 are part of the same product family. SDK software drivers, rev 1.1 for FS8400/FS8500 are applicable for VR5500/FS5502.*

[13] **UM10204** — I^2C-bus specification and user manual
https://www.nxp.com/docs/en/user-guide/UM10204.pdf

[14] **AN1902**— Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages application note
https://www.nxp.com/files/analog/doc/app_note/AN1902.pdf

[15] **AN10874** — LFPAK MOSFET thermal design guide application note
https://assets.nexperia.com/documents/application-note/AN10874.pdf

[16] **ISO 7637-2:2011(E)** — *Road Vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only*, International Standards Organization.

[17] **ISO 16750-2:2010(E)** — *Road vehicles – Environmental conditions and testing for electrical and electronic equipment – Part 2: Electrical loads*, International Standards Organization.

[18] **ISO 16750-2:2012(E)** — *Road vehicles – Environmental conditions and testing for electrical and electronic equipment – Part 2: Electrical loads*, International Standards Organization.

[19] **IEC 61967-4:2002** — *Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 4: Measurement of conducted emissions, 1 ohm/150 ohm direct coupling method*, International Electrotechnical Commission.

[20] **IEC 62132-4:2006** — *Integrated circuits – Measurement of electromagnetic immunity 150 kHz to 1 GHz – Part 4: Direct RF power injection method*, International Electrotechnical Commission.

[21] **FMC1278:2016** — *General Specification, Electrical/Electronic – Electromagnetic Compatibility Specification For Electrical/Electronic Components and Subsystems*, Ford Motor Company.

[22] **VW 80000: 2009-10**, Volkswagen AG implementation of LV 124, v 1.3 — *Electric and Electronic Components in Motor Vehicles up to 3.5 t – General Component Requirements, Test Conditions and Tests*

[1] Contact your NXP sales representative.

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