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PF7100 design guidelines

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Document information

Information	Content
Keywords	PMIC, PF7100, i.MX 8, S32
Abstract	This application note provides a comprehensive list of design guidelines used for the hardware development of PF7100 device.

Revision history

Rev	Date	Description
1.0	20200615	• Initial version

1 Overview

The PF7100 family of devices feature a power management integrated circuit (PMIC) designed for high performance i.MX 8 processors. It features high-efficiency buck converters and linear regulators for powering the processor, memory and miscellaneous peripherals.

The PF7100 PMIC family comprises three devices, to address different market needs:

- PF7100 automotive ASIL B device provides a full feature PMIC with five switching regulators and two LDOs, integrates functional safety mechanism to comply with the ISO 26262 standard, and provides a powerful and flexible solution for ASIL B(D) automotive modules.
- PF7100 automotive QM device provides the same switching and LDO regulator resources as ASIL B device, but without the functional safety overhead to provide an economic platform for systems not required to meet the ASIL B qualification.
- PF7100 industrial version device provides all the same switching and LDO regulator resources as automotive ASIL B device. It addresses industrial market applications.

Built-in one-time programmable (OTP) memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after power-up offering flexibility for different system states.

The PF7100 devices are available in HVQFN48 package with dimple wettable flank. Refer to PF7100 data sheet for more information.

2 Package pinout

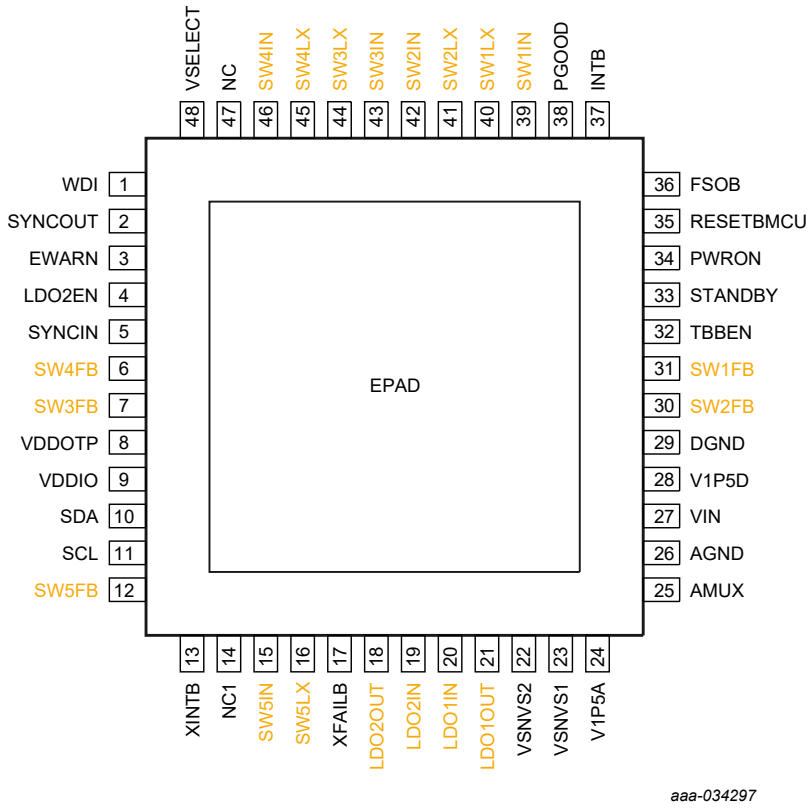

Figure 1. Pin configuration PF7100

3 PMIC control schematic design

3.1 I/O interfacing diagram

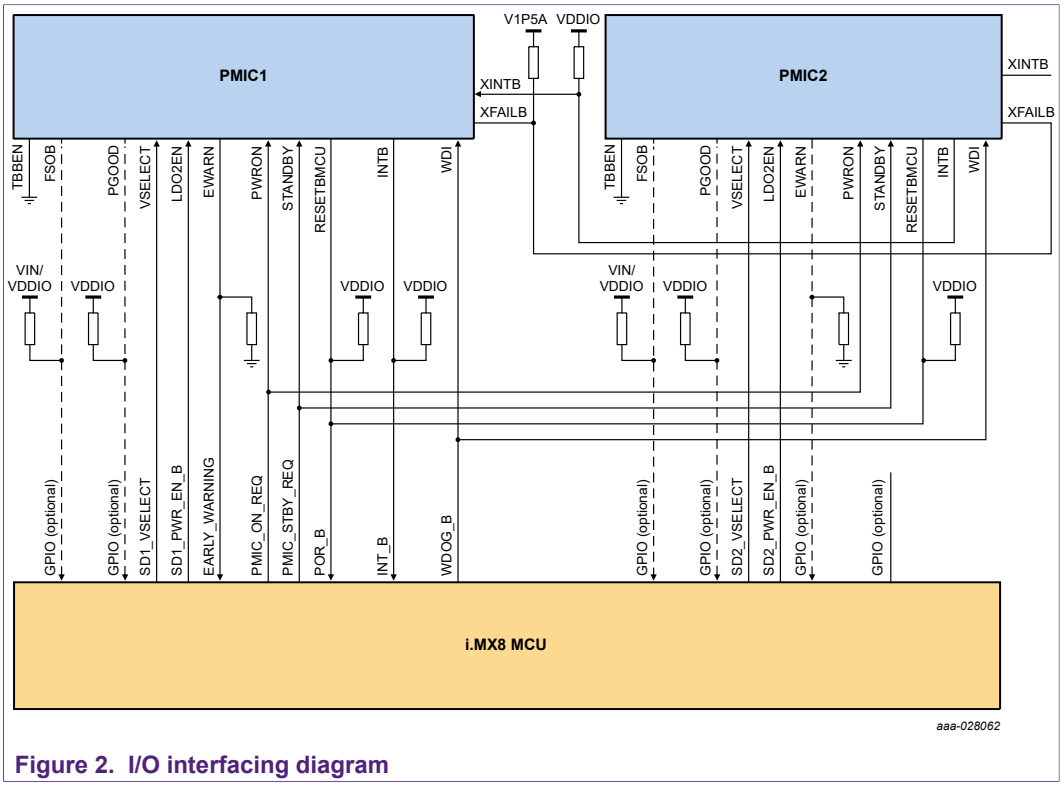

Figure 2. I/O interfacing diagram

Pin #	Symbol	Pin description	Type	i.MX8 application connection
MCU interface I/Os				
34	PWRON	PWRON input	I	Autostart mode: 100 kΩ pull up to VIN or VSNVS SCU control mode: connected to MCU PMIC_ON_REQ
33	STANDBY	STANDBY input	I	Connected to MCU PMIC_STBY_REQ
1	WDI	Watchdog Input from MCU	I	Connected to MCU WDOG_B
35	RESETBMCU	RESETBMCU open drain output	O	Connected to MCU I/O (POR_B) with 100 kΩ pull up to VDDIO
37	INTB	INTB open drain output	O	Connected to MCU INT_B with a 100 kΩ pull up to VDDIO
3	EWARN	Early warning to MCU	O	Connected to MCU EARLY_WARNING with a 100 kΩ pull down to ground
General function I/Os				
4	LDO2EN	LDO2 Enable pin	I	Connect to MCU I/O
48	VSELECT	LDO2 voltage select input	I	Connected to MCU SDx_VSELECT
38	PGOOD	PGOOD open drain output	O	Connect to MCU I/O with 100 kΩ pull up to VDDIO
5	SYNCIN	External clock input pin for synchronization	I	Connect to external clock signal
2	SYNCOUT	Clock out pin for external part synchronization	O	Pin for master clock generation
25	AMUX	Analog multiplexer output	O	Connect to MCU analog to digital converter
36	FSOB	Safety output pin	O	Connected to safety output monitoring I/O on MCU with a 100 kΩ pull up to VDDIO Optional system interface pin with a 470 kΩ pull up to VIN
11	SCL	I^2C synchronous clock	I	2.2 kΩ pull up to VDDIO

Pin #	Symbol	Pin description	Type	i.MX8 application connection
10	SDA	I^2C data line	I/O	2.2 kΩ pull up to VDDIO
PMIC interface I/Os				
13	XINTB	External interrupt input	I	Connected to companion PMIC INTB pin with a 100 kΩ pull up to VDDIO
17	XFAILB	External fail detection and PMIC synchronization pin	I/O	Connect to companion PMIC XFAILB with a 100 kΩ pull up to its own V1P5A
32	TBBEN	Try before buy enable pin	I	GND
PMIC core supplies				
9	VDDIO	System I/O supply	I/O	Bypass with a 0.1 µF capacitor
23	VSNVS1	VSNVS1 regulator output	I	Connected to SNVS domain in MCU with a 2.2 µF capacitor
22	VSNVS2	VSNVS2 regulator output	O	Second connection to SNVS domain in MCU with a 2.2 µF capacitor Used as general purpose always in power supply
24	V1P5A	Internal 1.5 V analog supply decoupling pin	O	Bypass with 1.0 µF capacitor
28	V1P5D	Internal 1.5 V digital supply decoupling pin	O	Bypass with 1.0 µF capacitor

3.2 PMIC control signals

The PF7100 automotive devices are targeted for a range of automotive applications, including Infotainment, telematics. For this reason, the devices have been defined to comply with the AEQ-100 automotive standard. In order to fulfill the automotive standards at system level, it is encouraged to use automotive grade components.

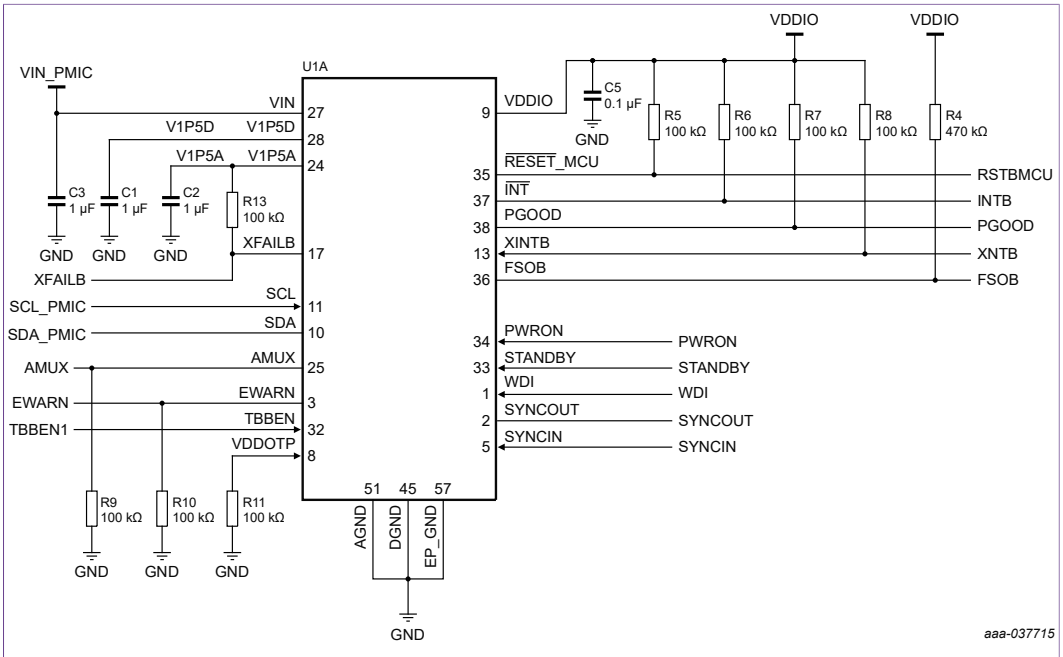

Figure 3. PMIC control signals

3.3 Special use case configurations

One of the main features of the PF7100 PMIC device is the flexibility to configure the default configuration of the system as well as provide full control of the PMIC during the system-on state via the I^2C communication bus.

The default configuration (OTP) can be defined and programmed in several ways:

- For high volume opportunities, NXP offers full device customization, including default OTP programing and custom part marking.
- For lower volume opportunities, NXP works with distributors to enable them to provide in-house programming of the PF7100 PMIC device for their customers.
- On-board device programming is available for customers that require in-house programming out of their production line.

For customers opting for on-board OTP configuration, a special configuration is required to allow proper access to the PMIC configuration signals without interfering or damaging any components from the main system. Figure 4 shows the recommended configuration compatible with NXP programming tools.

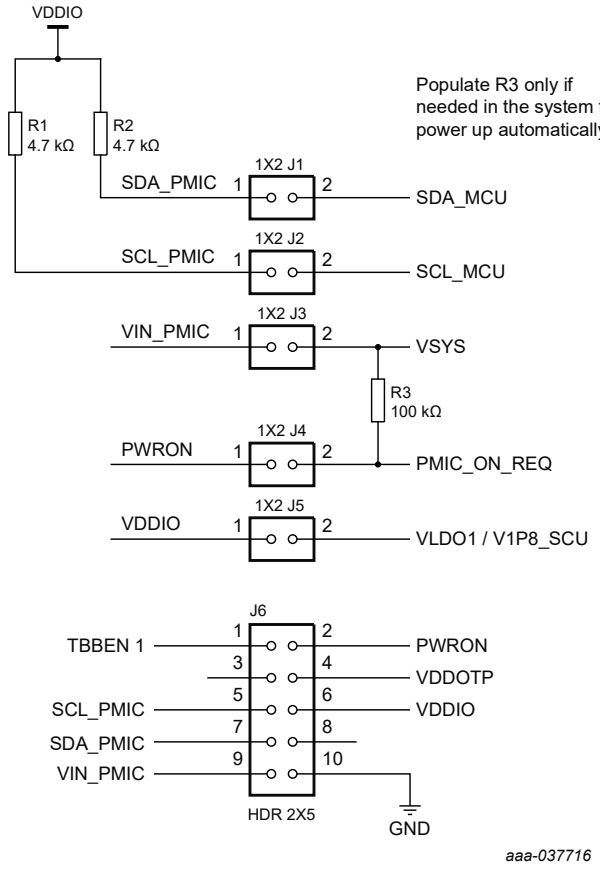

Figure 4. Programming interface

Note: *Programming interface connector pinout shown in Figure 4 is compatible with the KITPF7100FRDMPGM programming tool.*

Note: *Configuration signal may require isolation from the main system in order to allow proper communication with the PMIC during OTP programming procedure. Such isolation may be achieved via two row pin headers, 0 Ω resistor arrays or a dip switch array.*

Note: *PMIC_ON_REQ pull up may be moved to the SNVS_SCU_V1P8 domain on i.MX8 processor or not connected when the PMIC_ON_REQ is a push pull driver.*

3.4 Unused pin termination

When a specific feature is not required on the system, certain rules should be followed to properly terminate the unused pins on the system. Likewise, some software/OTP configuration may be required to ensure proper operation of the PMIC. Table 1 provides all considerations for unused pin termination.

Table 1. Unused functional pin termination

Pin #	Symbol	Termination if not used	Software/OTP considerations
47	NC	1. NC 2. GND	
32	TBBEN	GND	
48	VSELECT	GND	OTP_VSELECTEN = 0
1	WDI	GND	OTP_WDI_INV = 0
3	EWARN	100 kΩ pulled down to GND	
35	RESETBMCU	100 kΩ pulled up to VDDIO	
34	PWRON	N/A	
33	STANDBY	GND	OTP_STBY_INV = 0
37	INTB	100 kΩ pulled up to VDDIO	All interrupt mask = 1
36	FSOB	100 kΩ pulled up to VDDIO/VIN	OTP_ASS_FSOB = 0 OTP_FSOB configuration bits = 0
13	XINTB	1. NC 2. 100 kΩ pulled up to VDDIO	
38	PGOOD	1. NC 2. 100 kΩ pulled up to VDDIO	1. All OTP_SWx_PG_EN bits = 0 and OTP_LDOx_PG_EN bits = 0
4	LDO2EN	GND	OTP_LDO2EN = 0
17	XFAILB	1. 100 kΩ pulled up to V1P5A 2. GND	OTP_XFAIL_EN = 0
23	VSNVS1	2.2 µF	OTP_VSNVS1 = 00
22	VSNVS2	2.2 µF	OTP_VSNVS2 = 00
5	SYNCIN	GND	OTP_SYNCIN_EN = 0
2	SYNCOUT	1. NC 2. 100 kΩ pulled down to GND	OTP_SYNCOUT_EN = 0
25	AMUX	1. NC 2. 100 kΩ pulled down to GND	AMUX_EN = 0

4 Power supplies schematic design

LDO regulators schematic require only the input capacitance and output capacitance as shown in Figure 5.

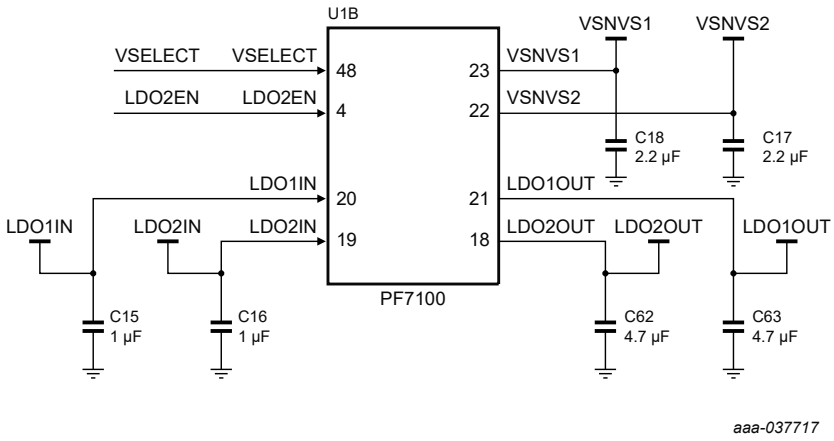

Figure 5. PMIC LDO regulators

Input/output capacitors must be rated at least twice the value of the input in the pin. For input capacitors, it is recommended to use at least a 10 V or 16 V rating and for output capacitors at least 6.3 V to 10 V rating to minimize capacitance variation overvoltage.

Switching regulators require the following components:

- 4.7 µF input capacitor rated at least 10 V or 16 V.
- 1.0 µH inductor with saturation current higher than the current limit selected for the application. DCR < 40 mΩ is recommended to improve efficiency performance of the regulator.
- 2 x 22 µF output capacitor rated at least 6.3 V. Multiple capacitors are required to improve total ESR of the output capacitor.
- Both input and output may add a small 0.1 µF capacitor for decoupling high frequency noise on the pins, however the noise reduction impact with these capacitors is minimal and they may be excluded if desired.

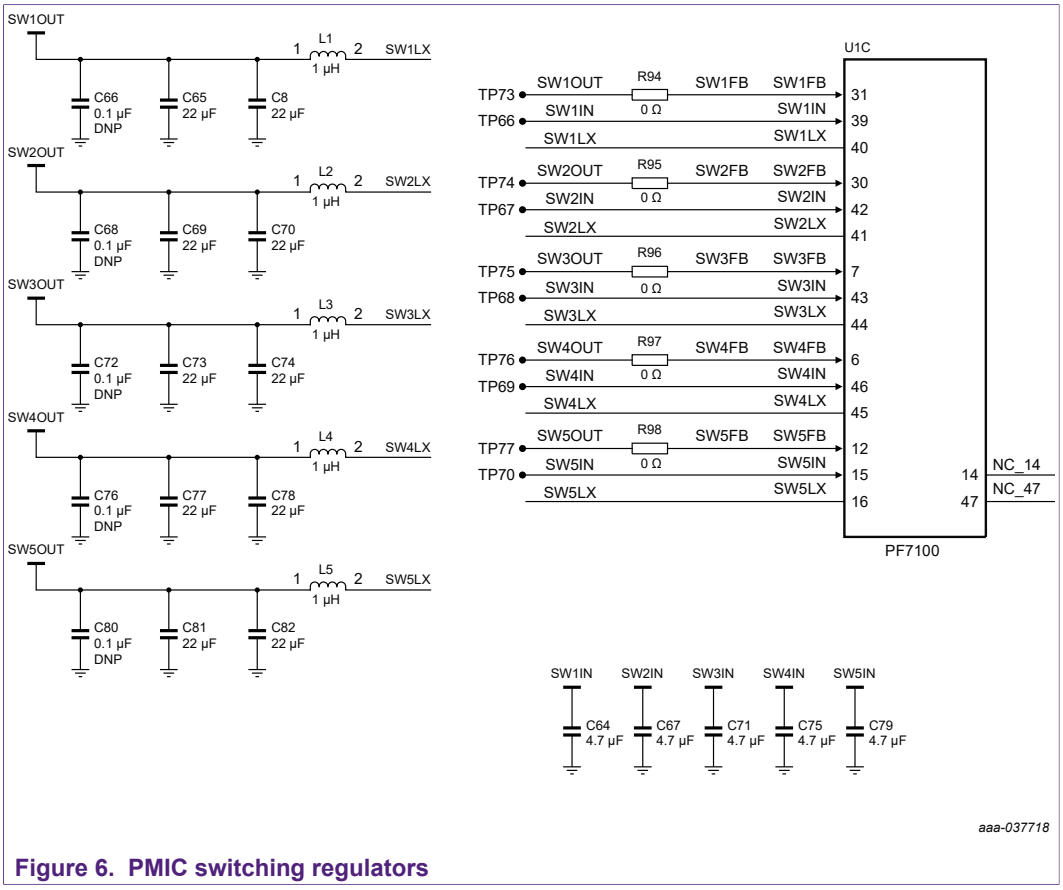

Figure 6. PMIC switching regulators

4.1 Terminating unused regulator pins

For unused LDO regulators, the OTP_LDOx_SEQ must be set as 0x00 in OTP and the LDOs cannot be enabled by software when PMIC is On. The pins can be terminated as indicated below:

- LDOxIN = GND
- LDOxOUT = GND

For unused switching regulators, the OTP_SWx_SEQ must be set as 0x00 in OTP and the regulators cannot be enabled by software when PMIC is On. The pins can be terminated as shown in Table 2.

Table 2. Switching regulator termination

No connects allowed (preferred)	Physical termination required
SWxIN = VIN	SWxIN = GND
SWxLX = not connected	SWxLX = GND
SWxFB = GND	SWxFB = GND

5 PCB layout recommendations

5.1 General layout recommendations

1. The PF7100 PMIC device pinout is defined in such a way that it can be laid-out in as little as four layers, however, at least six layers are recommended to provide proper shielding and grounding to minimize ground loops and ensure proper operation.
   - High current signals
   - GND
   - Signal
   - Signal
   - GND
   - High current signal
2. Allocate TOP layer for main component placement and output power routing of the switching regulators and LDOs; place a dynamic copper plane to ground on the unused area.
3. Allocate bottom layer for input power routing; place a dynamic copper plane to ground on the unused area.
4. Use internal layers sandwiched between two GND planes for the SIGNAL routing.
5. It is desirable to keep all components related to the power stage as close to the PMIC as possible, specially decoupling input and output capacitors.

5.2 General routing requirements

1. Some recommended rules to keep in mind for manufacturability:
   - Via in pads require a 4.5 mil minimum annular ring. Pad must be 9.0 mils larger than the hole
   - Maximum copper thickness for lines less than 5.0 mils wide is 0.6 oz copper
   - Minimum allowed spacing between line and hole pad is 3.5 mils
   - Minimum allowed spacing between line and line is 3.0 mils
2. Care must be taken with SWxFB pins traces. These signals are susceptible to noise and must be routed far away from power, clock, or high-power signals, like the ones on the SWxIN, SWx, SWxLX pins.
3. Run feedback traces of the regulators in the inner layers to keep them shielded from the power and noise nodes.
4. Avoid coupling V1P5D, V1P5A traces with any high current, high-speed switching nodes (i.e. SWxLX nodes).
5. Make sure all components related to a specific block are referenced to the corresponding ground. Use through vias to connect signals to the closest ground plane to minimize the ground loop.

5.3 Switching regulators layout recommendations

1. Per design, the switching regulators in PF7100 PMIC device, are designed to operate with only one input bulk capacitor. Depending on the strategy and the specific PCB layout design rules, the input capacitor can be placed on the top layer as close as possible to the input pin, or placed on the bottom layer underneath the PMIC, using enough vias to connect to the Input pin and to the expose path.

2. A high frequency filter input capacitor (CIN_hf), can be added to help filter out high frequency noise at the regulator input. This capacitor should be in the range of 100 nF and should be placed right next to or under the IC, closest to the IC pins.
3. Make the LX nodes as wide and short as possible to minimize the trace inductance and improve the output efficiency.
4. Make high-current traces as symmetrical as possible for dual or quad phase regulators.

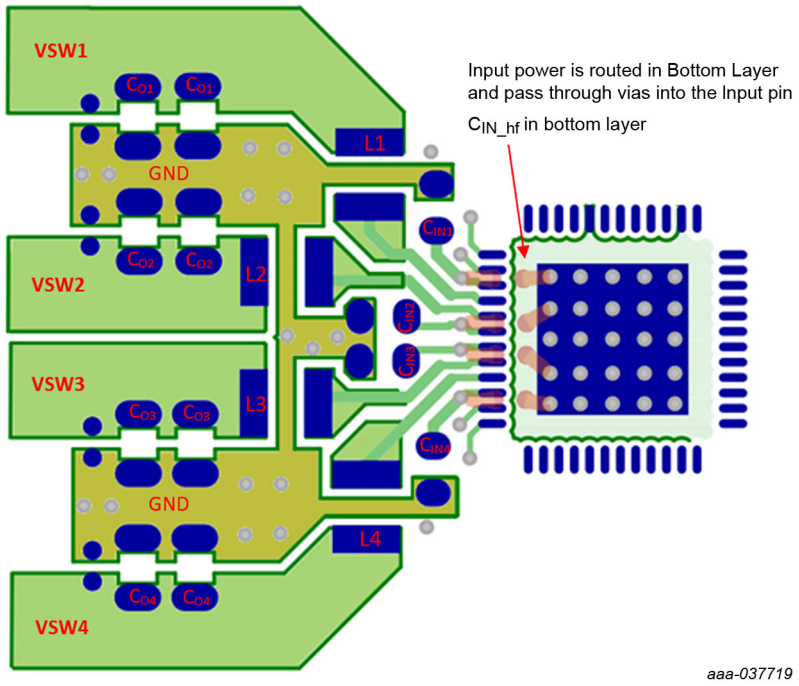

Figure 7. Switching regulators placement and routing examples

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