LPC55S2x/LPC552x

Errata sheet LPC55S2x/LPC552x

Rev. 1.2 — October 22, 2019 Errata sheet

Document information

Info	Content
Keywords	LPC55S28JBD100, LPC55S26JBD100, LPC55S28JEV98 LPC55S26JEV98, LPC55S28JBD64, LPC55S26JBD64, LPC5528JBD100, LPC5526JBD100, LPC5528JEV98, LPC5526JEV98, LPC5528JBD64, LPC5526JBD64
Abstract	LPC55S2x/LPC552x errata

Revision history

Rev	Date	Description
1.2	20191021	Enhances product identification and adds USB.1 and USB.2 errata.
1.1	20190923	Describes ROM failure to enter ISP mode when an image is corrupted with flash pages in an erased or unprogrammed state.
1.0	20190719	Initial version.

Contact information

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1. Product identification

The LPC55S2x/LPC552x VFBGA98 package has the following top-side marking:

- First line: LPC55S2x/LPC552x
- Second line: JEV98
- Third line: xxxxxxxx
- Fourth line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 1B

The LPC55S2x/LPC552x HLQFP100 package has the following top-side marking:

- First line: LPC55S2x/LPC552x
- Second line: xxxxxxxx
- Third line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 1B

The LPC55S2x/LPC552x HTQFP64 package has the following top-side marking:

- First line: LPC55S2x/LPC552x
- Second line: JBD64
- Third line: xxxx
- Fourth line: xxxx
- Fifth line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 1B

2. Errata overview

Table 1. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
ADC.1	Async interrupts with resume not supported.	1B	Section 3.1
ROM.1	ROM fails to enter ISP mode when image is corrupted with flash pages in an erased or unprogrammed state.	0A, 1B	Section 3.2
USB.1	USB HS host fails when connecting to an LS device (mouse).	1B	Section 3.3
USB.2	Automatic USB rate adjustment not functional when using multiple hubs.	1B	Section 3.4

Table 2. AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
n/a	n/a	n/a	n/a

Table 3. Errata notes

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3. Functional problems detail

3.1 ADC.1: Async interrupts with resume not supported

Introduction

The ADC controller is available on all LPC55S2x/LPC552x devices. Trigger detect with up to 16 trigger sources is supported with priority level configuration. A software or hardware trigger option is provided for each.

Problem

The following problems are all related to the restart after interrupt feature:

- Low priority trigger executes twice when resumed.
- Trigger can't restart when it is configured to do so.
- Incorrect trigger resumed after exception.

Work-around

There is no work-around.

The async interrupts with resume is not supported on device revisions 0A and 1B.

3.2 ROM.1: ROM fails to enter ISP mode when image is corrupted with flash pages in an erased or unprogrammed state

Introduction

On the LPC55S2x/LPC552x, if the image is corrupted with flash pages in an erased or unprogrammed state, the ROM may fail to automatically enter ISP mode.

Problem

When secure boot is enabled in CMPA, and the flash memory contains an erased or unprogrammed memory page inside the memory region specified by the image size field in the image header, the device does not automatically enter into ISP mode using the fallback mechanism, as in the case of a failed boot for an invalid image. This problem occurs when the application image is only partially written or erased but a valid image header is still present in memory.

Work-around

Perform a mass-erase to remove the incomplete and corrupted image using one of the following methods:

- Execute the erase command using Debug Mailbox. The device will enter directly into ISP mode after exiting the mailbox.
- Enter into ISP mode using the Debug Mailbox command and use the flash-erase command.
- Reset the device and enter into ISP mode using the ISP pin. Use the flash-erase command to erase the corrupted (incomplete) image.

On device revision 1B, this issue only affects devices with bootloader property T1.1.0. This issue does not occur on device revision 1B with bootloader property T1.1.4. The bootloader property can be read using the GetProperty ROM command. Please see the user manual for further details.

3.3 USB.1: HS host fails when connecting with the LS device (mouse)

Introduction

The USB1 high-speed controller is available on select LPC55S2x/LPC552x devices and provides a plug-and-play connection of peripheral devices to a host with three different data speeds:

- high-speed with a data rate of 480Mbps.
- full-speed with a data rate of 12 Mbps.
- low-speed with a data rate of 1.5 Mbps.

Many portable devices can benefit from the ability to communicate with each other over the USB interface without intervention of a host PC.

Problem

USB HS host fails when connecting with an LS device (mouse).

Work-around

To support Full-Speed and Low-Speed applications, it is recommended to use the USB0 Full-Speed port and the USB1 High-speed port for Device or Host. In addition, should an application require support of Low-Speed USB devices with a USB High-Speed Host, this can be accomplished by inserting a USB Hub between the USB1 High-speed port and external USB devices.

3.4 USB. 2: Automatic USB rate adjustment is not functional when using multiple hubs

Introduction:

Full-speed and low-speed signaling uses bit stuffing throughout the packet without exception. If the receiver sees seven consecutive ones anywhere in the packet, then a bit stuffing error has occurred, and the packet should be ignored.

The time interval just before an End of Packet (EOP) is a special case. The last data bit before the EOP can become stretched by hub switching skews. This is known as dribble and can lead to a situation where dribble introduces a sixth bit that does not require a bit stuff. Therefore, the receiver must accept a packet where there are up to six full bit times at the port with no transitions prior to the EOP.

Problem:

The LPC55S2x/LPC552x devices use the start of an EOP for frequency measurements. This is not functional when going through multiple hubs that introduce a dribble bit because of hub switching skews. For this reason, the start of the EOP cannot be used for frequency measurements for automatic USB rate adjustment (by setting USBCLKADJ in the FRO192M_CTRL register). The problem does not occur when a single hub is used.

Work-around:

Use the FRO calibration library provided in technical note TN00063. This library allows the application to have a crystal-less USB device operation in full-speed mode.

4. AC/DC deviations detail

No known errata.

5. Errata notes detail

No known errata.

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