AN12365

NTAG 5 - How to use energy harvesting Rev. 1.1 — 4 March 2020

530411

Application note COMPANY PUBLIC

Document information

Information	Content
Keywords	NTAG 5 switch, NTAG 5 link, NTAG 5 boost, energy harvesting, circuit, schematics, reference application
Abstract	Guidelines for designing applications using NTAG 5 energy harvesting capabilities.



Revision history

Re	₽V	Date	Description
v .1	1.1	20200304	General update
v.1	1.0	20200109	Initial version

1 Abbreviations

Acronym	Description
NFC	Near Field Communication
EH	Energy Harvesting
ALM	Active Load Modulation
VCD	Vicinity Coupling Device
VICC	Vicinity Integrated Circuit Card

2 Introduction

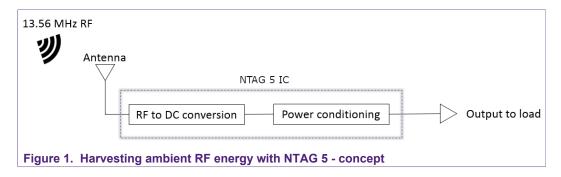
This document describes "energy harvesting" capabilities of NTAG 5 family ICs. NTAG 5 phrase in this document refers to all three IC variants: NTAG 5 switch, NTAG 5 link, NTAG 5 boost. To reduce complexity, NTAG 5 abbreviation is used through whole document for all three IC variants.

The NTAG 5 provides the capability to harvest energy from the RF field. This feature can be used to supply external circuits or devices (e.g., microcontrollers, sensors) with enough energy to operate.

NTAG 5 is the first IC with configurable regulated power output.

This document focuses on showing how much energy the NTAG 5 can deliver and under which conditions, how to design a circuitry to optimize energy harvesting capabilities.

It shall be considered that **ALM** (Active Load Modulation) functionality and **energy harvesting** are **not available at the same time**.



In the case energy harvesting is used to power NTAG 5 (when V_{CC} is not supplied externally), all harvested excess power (power not required to supply NTAG 5) is available to supply external circuits.

NTAG 5 consists of configurable current detection block. It allows triggering energy harvesting only when enough energy is retrieved from RF to provide expected current level.

2.1 Target applications

- Fully sealed devices
- Sensor Tags, Sensor tags with NTAG 5 in I²C master mode (w/o MCU), reference [<u>Application note</u>]
- Maintenance of broken systems, in case of general power outage, reference [Application note]
- Especially for devices where power is an issue

2.2 Influencing factors on energy harvesting

Main factors influence the power NTAG 5 is able to harvest are the following:

 Antenna size: Larger is the NTAG 5 antenna higher is the level of energy collected by NTAG 5 from RF.

- Antenna turn count: Lower is the number of turns higher is the level of energy collected by NTAG 5 from RF.
- Antenna matching: In case of highly coupled systems (reader and NTAG 5 antennas size are the same, with small or even zero distance in between) the reader can be detuned from the tag. This can reduce amount of energy collected by NTAG 5.
- Field strength: Stronger is the field emitted by the RF reader higher is the level of energy collected by NTAG 5. Field strength dropping while distance between reader antenna and NTAG 5 antenna increase.

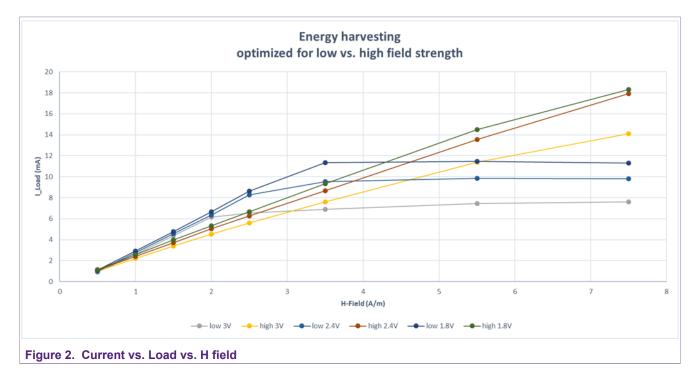
<u>Note</u>: In general, under the load V_{OUT} voltage drops if too much current is taken out of the NTAG 5 or if field strength gets weaker. In this condition (DISABLE_ POWER_CHECK = 0b and field strength too weak to deliver configured output) NTAG 5 <u>only</u> responds to INVENTORY command and READ/WRITE CONFIGURATION to access session registers on NFC interface side.

For stable I^2C communication, the V_{CC} should not drop below recommended minimum V_{CC} (Electrical characteristics in [Datasheet]).

2.3 Modes of operation

There are two (2) modes which can be set for energy harvesting operation, with bits EH_MODE:

- Energy harvesting optimized for low field strength (default) if expected VCDs have lower NFC field strength (e.g. NFC mobiles)
- Energy harvesting optimized for high field strength if expected VCDs be able to output more strong field (e.g. specially designed VCDs)



3 Recommendations

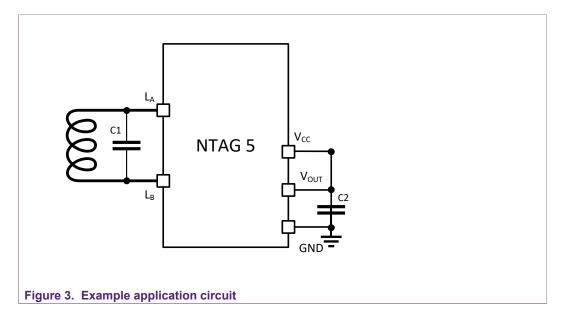
To optimize energy harvesting as whole, following topics shall be considered: on system level and on components surrounding IC.

3.1 System level

- Minimize the current needed to be harvested. Energy supplied via EH, needs to be supplied by the reader, therefore reduces the read range of the NTAG 5.
- On MCU systems, clock down the MCU and also use the deep sleep modes to minimize the current consumption.
- The power requirements connected to the energy harvesting pin should be kept at minimum as needed by the external system. The larger the requirements are, the harder it is for the reader to wake up and supply the NTAG 5.
- Use optimum Vtx level on VCD

3.2 Application level

The external capacitor (C below) value must be chosen to prevent voltage drop below 100 mV during VCD modulation pauses.



Voltage drop during VCD pauses (miller modulation type) can be calculated following below formula, where V_{drop} is the voltage drop during VCD modulation pauses in volts, I_L is the load current in amps and t_{pause} is the modulation pause duration in seconds:

$$V_{drop} = \frac{I_L \times t_{pause}}{C} \tag{1}$$

Additionally, the external capacitor value impacts the V_{OUT} ramp-up time according below formula, where t_{ramp} is the V_{OUT} ramp-up time in seconds and I_{field} is the configured output current in amps (refers to EH_VOUT_I_SEL):

All information provided in this document is subject to legal disclaimers.	© NXP B.V. 2020. All rights reserved.
Rev. 1.1 — 4 March 2020	
530411	6 / 23
	Rev. 1.1 — 4 March 2020

(2)

$$t_{ramp} = \frac{V_{out} \times C}{I_{field} \cdot I_L}$$

• V_{OUT} can also be used as an "NFC field detector" alternative (among ED pin¹)

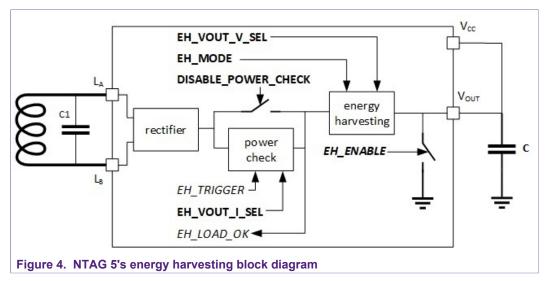
- In case NTAG 5's V_{OUT} (harvested energy) also supplies I²C bus, then V_{CC} must be connected to V_{OUT}, and pull-up resistors are required on the SCL and SDA lines. These pull-up resistors must be sized appropriately to limit the sink current when the lines are pulled low. Resistors value depends on the devices connected on the bus, recommendation is to start with value 4.7 kOhms and adjust it down if necessary.
- In case NTAG 5's V_{OUT} (harvested energy) also supplies ED pin (Event Detect pin [<u>Application note</u>]) in Pass-through mode [<u>Application note</u>], then the pull-up resistor on the Event Detect line must be sized appropriately to limit the sink current when pulled low by NTAG 5.

¹ When using ED pin functionality, NTAG 5 does not need to be VCC supplied.

3.3 Energy harvesting block operation

NTAG 5 offers a <u>current detection</u> mechanism which can be enabled or disabled through DISABLE_POWER_CHECK. Current detection mechanism will be operating (if enabled) ONLY when RF field is available.

<u>Note</u>: If the current detection is enabled and there is not enough field strength available to enable V_{OUT} , EEPROM access is disabled. NTAG 5 is then answering ONLY to INVENTORY command and READ/WRITE CONFIGURATION to access session registers on NFC interface.



4 How to configure NTAG 5 for energy harvesting

Mode of energy harvesting feature can be configured by either of following bytes:

- EH_CONFIG_REG in session register (Block address from NFC:A7h, from I²C:10A7h, Byte0) >> Current session
- EH_CONFIG in configuration memory (Block address from NFC:3Dh, from I²C:103Dh, Byte0) >> Start-up behavior

As soon as energy harvesting is used, V_{OUT} and V_{CC} must be connected. Otherwise no EEPROM access is possible from NFC side and status registers reflect invalid information.

Detailed description of those parameters can be found in NTAG 5 [Datasheet].

The two different possible methods of enabling EH are described in next chapters:

- 1. Enabling EH by session registers (Recommended method) [Section 4.1]
- 2. EH enabled during boot [Section 4.2]

4.1 Enabling EH by session registers - the recommended method

This first method is the recommended one because it provides more reliable NFC communication (less time slot in which NFC communication cannot be fully achieved). However it requires dedicated scenario from the VCD side, therefore requiring specific application running on VCD.

Prerequisites:

- in EH_CONFIG (3Dh from NFC / 103Dh from I^2C):
 - Energy harvesting at startup must be disabled, setting bit EH_ENABLE to 0b, since it will on the fly be enable through session register
 - EH_VOUT_V_SEL and EH_VOUT_I_SEL must be set according to the requirement
 DISABLE POWER CHECK has no effect, as EH ENABLE is set to 0b
- In CONFIG (37h from NFC / 1037h from I²C) desired energy harvesting mode must be chosen (optimized for low or high field strength - see <u>Section 2.3</u>)

Procedure:

- VCD triggers current detection by by writing to EH_CONFIG_REG session register (A7h) → EH_TRIGGER (Bit3) set to 1b
- 2. VCD polls EH_CONFIG_REG (A7h) until the available field strength is sufficient → EH_LOAD_OK (Bit7) equal to 1b
- 3. VCD enables the energy harvesting by writing to EH_CONFIG_REG session register (A7h) → EH_ENABLE (Bit0) set to 1b and EH_TRIGGER (Bit3) set to 1b
- VCD polls STATUS1_REG (A0h) until VCC ramps up → VCC_BOOT_OK (Bit7) equal to 1b

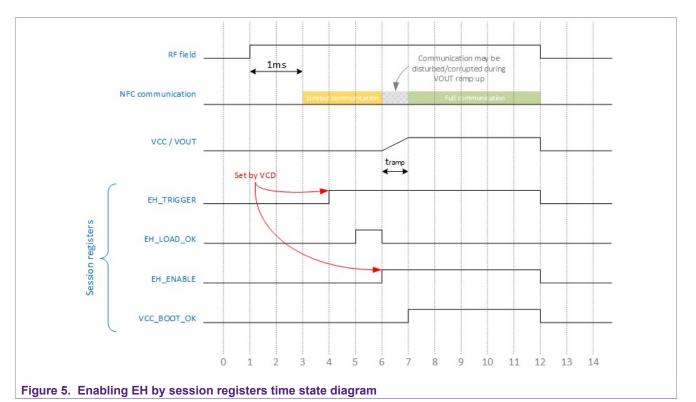
<u>Note:</u> If VCD directly enables EH (step 3) without checking if field strength is sufficient (step 1 and 2), risk is NTAG 5 may reset because of voltage drop (if not enough energy). EH will be disabled (since only valid for current NFC session).

<u>Note:</u> If EH_ARBITER_MODE_EN (CONFIG_1 register 37h from NFC / 1037h from I^2C) is set to 0 the ARBITER_MODE is selected via CONFIG_1_REG session register (A1h from NFC) since related setting from CONFIG_1 configuration register is ineffective.

AN12365

Limitations:

- Until V_{OUT} gets generated and V_{CC} ramps up, the communication to memory is not possible. Only INVENTORY command and access to session registers are possible from NFC interface.
- Any NFC communication during V_{OUT} ramp up may be disturbed/corrupted.



rs dy for NFC activation from VCD
session register: EH_TRIGGER = 1b
EH_LOAD_OK status signal in session registers
session register EH_ENABLE = 1b and EH_TRIGGER = 1b s. V _{CC} boot to be restarted if V _{CC} toggles between time 6 and 7
ully functional
strength drops or Load current increases, the V_{OUT} will drop, consequently also V_{CC} drops low 1.62 V, the system reset will be triggered and NTAG 5 will reboot
bears leading to V_{OUT} drop then NTAG 5 shutdown

Note: Writing to Session Registers to enable energy harvesting, will be treated as a "Write alike" command which means V_{CC} ramp can go up to 20 ms max. If V_{CC} supply does not come up until 20 ms, then the VCD needs to take a corrective action.

4.2 Energy harvesting enabled during boot

This second method is the only one which can be considered if there is no control to the VCD application.

Prerequisites

- in EH_CONFIG (3Dh from NFC / 103Dh from I²C):
 - Energy harvesting at startup must be enabled, setting bit EH_ENABLE to 1b
 - EH_VOUT_V_SEL and EH_VOUT_I_SEL must be set according to the requirement
 - DISABLE_POWER_CHECK can be configured to use current detection monitor or not

Procedure:

 Depending on DISABLE_POWER_CHECK setting, energy harvesting will be directly enabled after boot or only when field strength becomes stronger enough to generate the required load

Limitations:

- Until V_{OUT} gets generated and V_{CC} ramps up, the communication to EEPROM is not possible. Only INVENTORY command and access to registers are possible from NFC interface.
- Any NFC communication during V_{OUT} ramp up may be disturbed/corrupted.

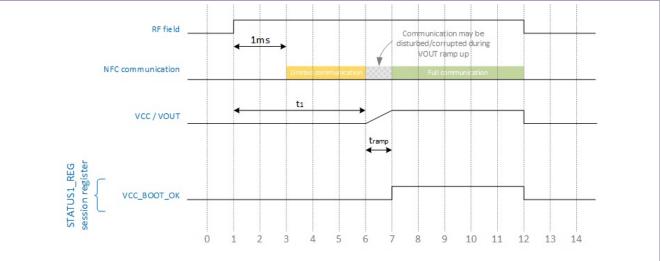


Figure 6. EH enabled by Configuration Bytes timing state diagram

Timestamp	Description
1	RF field appears
3	NTAG 5 is ready for NFC activation from VCD
3-6	VCD can activate NTAG 5 but cannot access memory (only access to registers is granted)
6	$V_{\rm CC}$ boot starts. $V_{\rm CC}$ boot to be restarted if $V_{\rm CC}$ toggles between time 6 and 7
7	NFC and I ² C fully functional
7-12	If the RF field strength drops or Load current increases, the V_{OUT} will drop, consequently also V_{CC} drops If V_{CC} goes below 1.62 V, the system reset will be triggered and NTAG 5 will reboot

NXP Semiconductors

AN12365

NTAG 5 - How to use energy harvesting

Timestamp	Description
12	RF field disappears leading to V_{OUT} drop then NTAG 5 shutdown
	The EH sequence will be retriggered after every boot.
	Time between RF field appears and V_{CC} boot starts (timestamp 1 to timestamp 6) when EH is enabled at boot, indicated as t ₁ on above diagram, is about 1.52 ms.
	To check, if the NTAG 5 is powered and if EH is enabled or not, session register can be checked:
	 STATUS0_REG (A0h from NFC / 10A0h from I²C), bit VCC_SUPPLY_OK EH_CONFIG (A7h from NFC / 10A7h from I²C), bit EH_ENABLE

5 Antenna design guidelines

Optimal energy transfer can be achieved by considering the following recommendations:

- 1. larger antenna size with lesser turns
- 2. antenna size close to a reader's antenna size (but not exact same size to avoid decoupling effect at low or zero distance)

To achieve most optimum configuration for RF performance (read range) and energy harvesting power yield, it is recommended to use a parallel capacitor for tuning and to lower antenna's inductance.

<u>Example</u>: For an antenna having total 1 μ H inductance, parallel 82 pF tuning can be used.

More details on "How to design antenna for NTAG 5" can be found in [Application note].

6 Example measurements

6.1 Reference setup

The reference setup used for the measurement is the NTAG 5 demo board referenced as OM23510ARD featuring a 3 turns 54 mm x 27 mm antenna.



Figure 7. OM23510ARD NTAG 5 demo board

Following measurements are done using different devices, acting as Vicinity readers, to provide wide range of NTAG 5 energy harvesting capabilities.

Note: Minimum load allowing to run energy harvesting depends on the V_{OUT} configuration:

- for V_{OUT} configured to 3.0 V \rightarrow minimum load is 430 Ω
- for V_{OUT} configured to 2.4 V \rightarrow minimum load is 260 Ω
- for V_{OUT} configured to 1.8 V \rightarrow minimum load is 160 Ω

6.1.1 CLRC663 plus demo board

Measurement with CLRC663 plus are performed using CLEV6630B demo board.

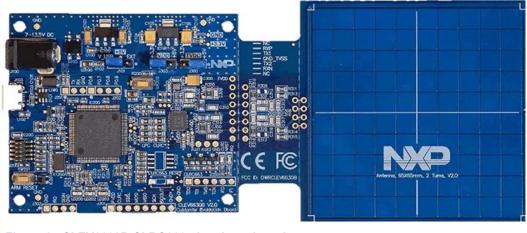
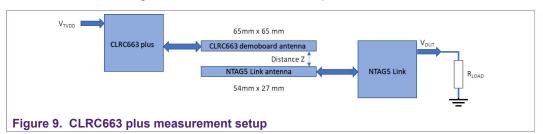


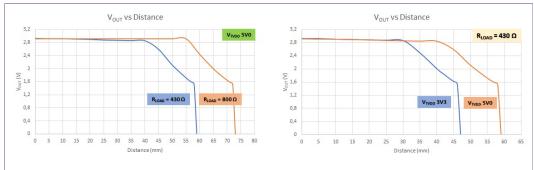
Figure 8. CLEV6630B CLRC663 plus demo board



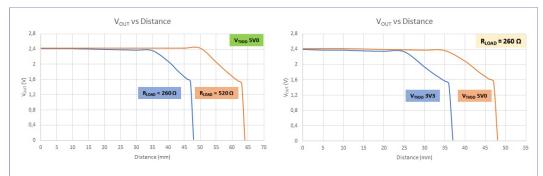
See in below block diagram of the measurement setup.

Below are measurement results for different values of R_{load} and V_{TVDD} , and different V_{OUT} configurations (EH_VOUT_V_SEL parameter).

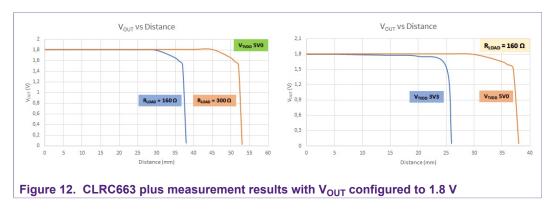
Note: Measurements with CLRC663 plus are done with NTAG 5 set in energy harvesting mode optimized for high field strength (EH_MODE parameter).











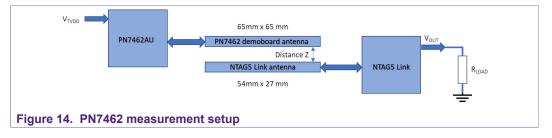
AN12365 Application note COMPANY PUBLIC © NXP B.V. 2020. All rights reserved.

6.1.2 PN7462 demo board

Measurement with PN7462 is performed using PNEV7462C demo board.

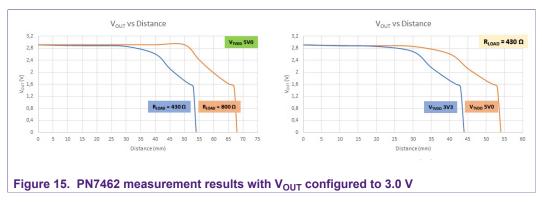


See in below block diagram of the measurement setup.



Below are measurement results for different values of R_{load} and V_{TVDD} , and different V_{OUT} configurations (EH_VOUT_V_SEL parameter).

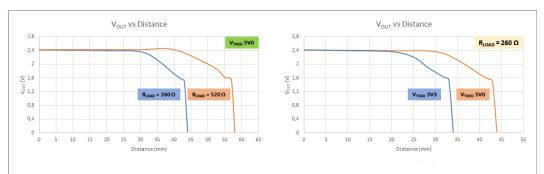
Note: Measurements with PN7462 are done with NTAG 5 set in energy harvesting mode optimized for high field strength (EH_MODE parameter).



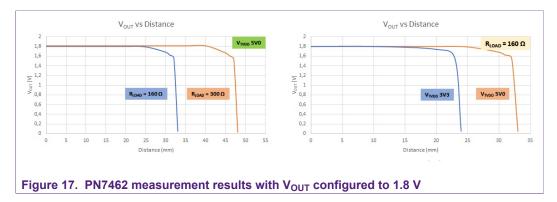
NXP Semiconductors

AN12365

NTAG 5 - How to use energy harvesting







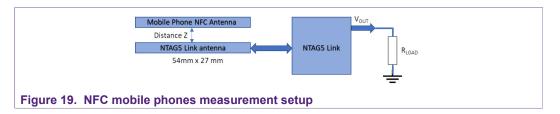
6.1.3 NFC mobile phones

Measurement with mobile phones is performed using NFC mobile phones Google Pixel 3, Huawei P20 Pro and Apple iPhone 11.



See in below block diagram of the measurement setup.

AN12365 Application note COMPANY PUBLIC



Below are measurement results for different values of R_{load} and different V_{OUT} configurations (EH_VOUT_V_SEL parameter).

Note: Measurements with NFC mobile phones are done with NTAG 5 set in energy harvesting mode optimized for low field strength (EH_MODE parameter).



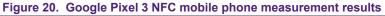




Figure 21. Huawei P20 Pro NFC mobile phone measurement results



Figure 22. Apple iPhone 11 NFC mobile phone measurement results

6.2 Boot sequence example timings

Below is a diagram of a boot sequence example when EH is enabled by configuration registers (see <u>Section 4.2</u>).

It shows timing of RF field ON event and V_{OUT} signal ramp-up, until the start of a PWM (GPIO_PAD1 configured as PWM output).

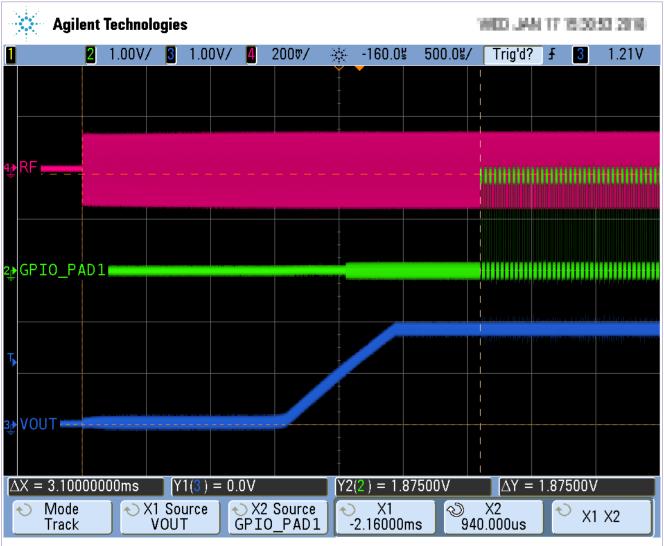


Figure 23. Enable EH by Config. bytes (Boot up behavior) - time/state diagram scope trace

7 References

- [1] NTP5210 NTAG 5 switch, NFC Forum-compliant PWM and GPIO bridge, doc.no. 5477xx <u>https://www.nxp.com/docs/en/data-sheet/NTP5210.pdf</u>
- [2] NTA5332 NTAG 5 boost, NFC Forum-compliant l²C bridge for tiny devices, doc.no. 5475xx
 - https://www.nxp.com/docs/en/data-sheet/NTA5332.pdf
- [3] AN11203 NTAG 5 Use of PWM, GPIO and Event detection, doc.no. 5302xx https://www.nxp.com/docs/en/application-note/AN11203.pdf
- [4] AN12364 NTAG 5 Bidirectional data exchange, doc.no. 5303xx https://www.nxp.com/docs/en/application-note/AN12364.pdf
- [5] AN12368 NTAG 5 Link I²C Master mode, doc.no. 5306xx https://www.nxp.com/docs/en/application-note/AN12368.pdf
- [6] AN12339 Antenna Design Guide for NTAG 5 https://www.nxp.com/docs/en/application-note/AN12339.pdf

AN12365

NTAG 5 - How to use energy harvesting

8 Legal information

8.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

8.2 Disclaimers

Limited warranty and liability - Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a

default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — While NXP Semiconductors has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP Semiconductors accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

8.3 Licenses

Purchase of NXP ICs with NFC technology

Purchase of an NXP Semiconductors IC that complies with one of the Near Field Communication (NFC) standards ISO/IEC 18092 and ISO/ IEC 21481 does not convey an implied license under any patent right infringed by implementation of any of those standards. Purchase of NXP Semiconductors IC does not include a license to any NXP patent (or other IP right) covering combinations of those products with other products, whether hardware or software.

8.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NTAG — is a trademark of NXP B.V.

Tables

AN12365

NTAG 5 - How to use energy harvesting

Figures

Fig. 1.	Harvesting ambient RF energy with NTAG 5
	- concept
Fig. 2.	Current vs. Load vs. H field5
Fig. 3.	Example application circuit6
Fig. 4.	NTAG 5's energy harvesting block diagram7
Fig. 5.	Enabling EH by session registers time state
	diagram9
Fig. 6.	EH enabled by Configuration Bytes timing
	state diagram 10
Fig. 7.	OM23510ARD NTAG 5 demo board13
Fig. 8.	CLEV6630B CLRC663 plus demo board 13
Fig. 9.	CLRC663 plus measurement setup 14
Fig. 10.	CLRC663 plus measurement results with
	VOUT configured to 3.0 V14
Fig. 11.	CLRC663 plus measurement results with
	VOUT configured to 2.4 V14
Fig. 12.	CLRC663 plus measurement results with
	VOUT configured to 1.8 V14

Fig. 13.	PNEV7462C PN7462 demo board	15
Fig. 14.	PN7462 measurement setup	15
Fig. 15.	PN7462 measurement results with VOUT	
	configured to 3.0 V	15
Fig. 16.	PN7462 measurement results with VOUT	
	configured to 2.4 V	16
Fig. 17.	PN7462 measurement results with VOUT	
	configured to 1.8 V	16
Fig. 18.	NFC Mobile phones	. 16
Fig. 19.	NFC mobile phones measurement setup	17
Fig. 20.	Google Pixel 3 NFC mobile phone	
	measurement results	17
Fig. 21.	Huawei P20 Pro NFC mobile phone	
	measurement results	17
Fig. 22.	Apple iPhone 11 NFC mobile phone	
	measurement results	17
Fig. 23.	Enable EH by Config. bytes (Boot up	
	behavior) - time/state diagram scope trace	. 18

NXP Semiconductors

AN12365

NTAG 5 - How to use energy harvesting

Contents

1	Abbreviations	3
2	Introduction	4
2.1	Target applications	4
2.2	Influencing factors on energy harvesting	4
2.3	Modes of operation	
3	Recommendations	6
3.1	System level	6
3.2	Application level	6
3.3	Energy harvesting block operation	7
4	How to configure NTAG 5 for energy	
	harvesting	8
4.1	Enabling EH by session registers - the	
	recommended method	8
4.2	Energy harvesting enabled during boot	10
5	Antenna design guidelines	. 12
6	Example measurements	13
6.1	Reference setup	. 13
6.1.1	CLRC663 plus demo board	13
6.1.2	PN7462 demo board	. 15
6.1.3	NFC mobile phones	16
6.2	Boot sequence example timings	18
7	References	19
8	Legal information	20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2020.

All rights reserved.

For more information, please visit: http://www.nxp.com For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 March 2020 Document identifier: AN12365 Document number: 530411