UD408G5S1AF

256Mx32 8Gb DDR4 SDRAM

Features

- Density
  - 8Gbits
- Organization
  - 32M words × 32 bits × 8 banks
- Package
  - 144-ball FCBGA (11.5mm × 15.5mm)
  - Lead-free/RoHS
- Power Supply
  - VDD = VDDQ = 1.14V – 1.26V
  - VPP = 2.375V – 2.75V
- Data Rate：
  - 3200Mbps/2933Mbps/2666Mbps/2400Mbps/ 2133Mbps/1866Mbps/1600Mbps
- Internal Banks
  - 8 banks (4 banks × 2 bank groups)
- Interface: Pseudo Open Drain (POD)
- Burst Length (BL): 8 and 4 with Burst Chop (BC)
- CAS Latency (CL): 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24
- CAS Write Latency (CWL): 9, 10, 11, 12, 14, 16, 18, 20
- On-Die Termination (ODT): nom. values of RZQ/7, RZQ/5 (RZQ = 240Ω)
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh Cycles
  - Average refresh period

    7.8 µs at 0℃ ≦ T_C ≦ +85℃

    3.9 µs at +85℃ < T_C ≦ +95℃
- Operating Case Temperature Range
  - Commercial: T_C = 0℃ to +95℃
  - Industrial: T_C = -40℃ to +95℃
- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS_t and DQS_c) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center- aligned with data for WRITEs
- Differential clock inputs (CK_t and CK_c)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data Mask (DM) for write data
- Write Cyclic Redundancy Code (CRC) for DQ error detect and inform it to controller during high-speed operation
- Data Bus Inversion (DBI)

  Improve the power consumption and signal integrity of the memory interface
- Programmable preamble is supported both of 1tCK and 2tCK mode
- Command Address (CA) Parity for command/address signal error detect and inform it to controller
- VREFDQ training

  VREFDQ generate inside DRAM and further train per DRAM
- Per DRAM Addressability (PDA)

  Each DRAM can be set a different mode register value individually and has individual adjustment.
- Fine granularity refresh

  2x, 4x mode for smaller tRFC
- Maximum power saving mode for the lowest power consumption with no internal refresh activity
- Programmable Partial Array Self-Refresh (PASR)
- RESET_n pin for power-up sequence and reset function

Table 1: Key Timing Parameters

Speed code	Data rate (MT/s)	CL-nRCD-nRP	Cycle time (ns)	tRCD (ns)	tRP (ns)
-24D0	2400	17-17-17	0.833	14.16	14.16
-26F0	2666	19-19-19	0.75	14.25	14.25
-29H0	2933	21-21-21	0.682	14.32	14.32
-32J0	3200	22-22-22	0.625	13.75	13.75

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Order Part Number Information

U D4 08G 5 S 1 A F I – 32J0

UltraMemory Inc.

Product Family
D4：DDR4 SDRAM

Density
08G：8Gbits

Organization
5：x32

Rank
S：Single Rank

Power Supply, interface
1：1.20V, SSTL_12

Die Revision
A：Version A

Package
F：FCBGA

Temperature
C：Commercial Temp. (T_C = 0℃ to +95 ℃)
I：Industrial Temp. (T_C = -40℃ to +95 ℃)

Speed Grade
32J0：DDR4-3200 CL22-22-22
29H0：DDR4-2933 CL21-21-21
26F0：DDR4-2666 CL19-19-19
24D0：DDR4-2400 CL17-17-17

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Content

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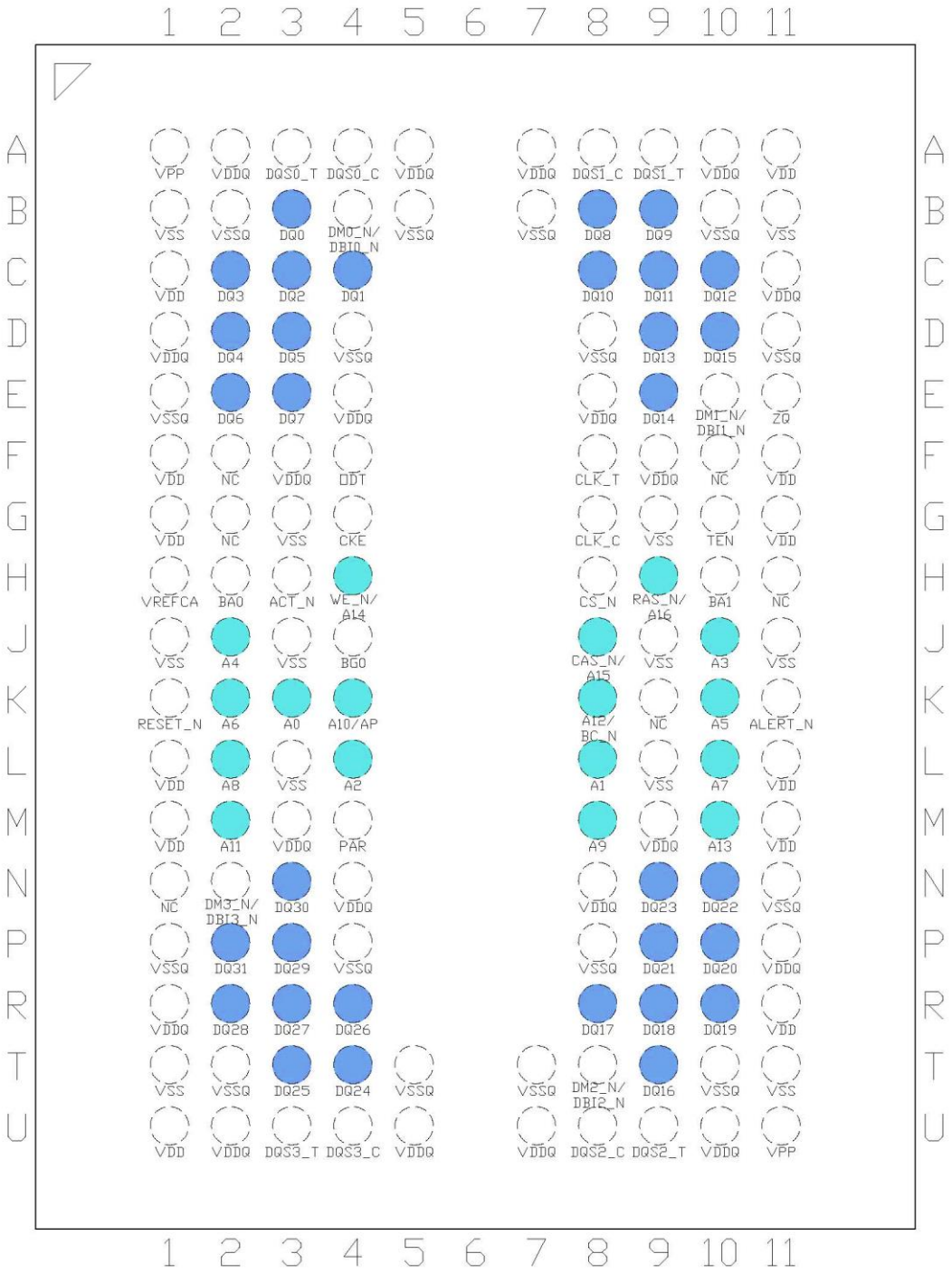
1. Ball Assignment

144-ball FCBGA (x32 configuration)



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(Top view)

Table 2: Ball Out Description

Ball name	Function	Ball name	Function
A0 to A13*2	Address inputs A10/AP: Auto precharge A12/BC_n: Burst chop	ODT*2	ODT control
BA0, BA1*2	Bank select	RESET_n*2	Active low asynchronous reset
BG0*2	Bank group input	PAR	Command and address parity
DQ0 to DQ31	Data input/output	ALERT_n	Alert
DQS0_t to DQS3_t DQS0_c to DQS3_c	Differential data strobe	VDD	Supply voltage for internal circuit
CS_n*2	Chip select	VSS	Ground for internal circuit
RAS_n/A16*2 CAS_n/A15*2 WE_n/A14*2	Command input	VDDQ	Supply voltage for DQ circuit
ACT_n*2	Activation command input	VSSQ	Ground for DQ circuit
CKE*2	Clock enable	VREFCA	Reference voltage for CA
CK_t, CK_c	Differential clock input	ZQ	Reference pin for ZQ calibration
DM0_n to DM3_n	Write data mask	NC*1	No connection
DBI0_n to DBI3_n	Data bus inversion	TEN	Connectivity test mode enable

Note:
1. Not internally connected with die.
2. Input only pins (address, command, CKE, ODT and RESET_n) do not supply termination.

2. Input / Output Function Description

Table 3: Input / Output function description

Symbol	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE	Input	**Clock enable:** CKE HIGH activates, and CKE LOW deactivates, the internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operations (all banks idle), or Active Power-Down (row active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
ODT	Input	**On die termination:** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS[3:0]_t, DQS[3:0]_c, DM[3:0]_n/DBI[3:0]_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	**Activation command input:** ACT_n defines an ACTIVATE command being entered along with CS_n. The input into WE_n/A14 will be considered as Row Address A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	**Command inputs:** WE_n/A14 (along with CS_n) define the command being entered. This pin has multi-function. For example, for activation with ACT_n LOW, this is Addressing like A14 but for non-activation command with ACT_n HIGH, this is Command pin for READ, WRITE and other command defined in command truth table
DM[3:0]_n/DBI[3:0]_n	Input/Output	**Input data mask and data bus inversion:** DM[3:0]_n is an input mask signal for write data. Input data is masked when DM[3:0]_n is sampled LOW coincident with that input data during a Write access. DM[3:0]_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. DBI[3:0]_n is an input/output identifying whether to store/output the true or inverted data. If DBI[3:0]_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI[3:0]_n is HIGH.
BG0	Input	**Bank group inputs:** BG0 defines to which bank group an ACTIVE, READ, WRITE or PRECHARGE command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
A0-A16	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.The address inputs also provide the op-code during Mode Register Set commands.
A10/AP	Input	**Auto-precharge:** A10 is sampled during READ and WRITE commands to determine whether auto-precharge should be performed to the accessed bank after a READ or WRITE operation. (HIGH: auto-precharge; LOW: no auto-precharge). A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop; LOW: burst chopped). See the Command Truth Table for details.
RESET_n	Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
DQ	Input/Output	**Data input / output:** Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS[3:0]_t, DQS[3:0]_c	Input/Output	**Data strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS[3:0]_t is paired with differential signal DQS[3:0]_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
PAR	Input	**Command and address parity input:** DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n,CAS_n/A15,WE_n/ A14,BG0-BG1,BA0-BA1,A15-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	**Alert:** It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.

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Symbol	Type	Description
TEN	Input	**Connectivity test mode enable:** Required on x16/x32 devices with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		**No connect:** No internal electrical connection is present.
VDDQ	Supply	**DQ power supply:** 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	**Power supply:** 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	**DRAM activating power supply:** 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration
Note: Input only pins (BG0, BA0-BA1, A0-A15, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.		

Table 4: 8Gb Addressing Table

Configuration		256 Mb x32
Bank Address	# of Bank Groups	2
	BG Address	BG0
	Bank Address in a BG	BA0~BA1
Row Address		A0~A14
Column Address		A0~A9
Page size		2KB

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3. Electrical Conditions

3.1 Absolute Maximum Ratings

Table 5: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	-0.3 to +1.5	V	1, 3
Power supply voltage for output	VDDQ	-0.3 to +1.5	V	1, 3
DRAM activation power supply	VPP	-0.3 to +3.0	V	4
Input voltage	VIN	-0.3 to +1.5	V	1
Output voltage	VOUT	-0.3 to +1.5	V	1
Reference voltage	VREFCA	-0.3 to 0.6 x VDD	V	3
Storage temperature	Tstg	-55 to +100	°C	1, 2

Note:
1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be no greater than 0.6 × VDDQ, When VDD and VDDQ are less than 500mV; VREFCA may be equal to or less than 300mV.
4. VPP must be equal or greater than VDD/VDDQ at all times.

3.2 Operating Temperature Condition

Table 6: Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	T_C	0 to +95	°C	1

Note:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM.

3.3 Recommended DC Operating Conditions

Table 7: Recommended DC Operating Conditions (TC = 0 °C to +95 °C)

Parameter	Symbol	min	typ	max	Unit	Notes
Supply voltage	VDD	1.14	1.2	1.26	V	1, 2, 3
Supply voltage for DQ	VDDQ	1.14	1.2	1.26	V	1, 2, 3
DRAM activating power supply	VPP	2.375	2.5	2.75	V	3
Ground	VSS	0	0	0	V	
Ground for DQ	VSSQ	0	0	0	V	

Notes:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

3.4 IDD and IDDQ Specification Parameters and Test conditions

3.4.1 IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined.
The figure Measurement Setup and Test Load for IDD and IDDQ Measurements shows the setup and test load for IDD,

IPP and IDDQ measurements.

- IDD currents are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Note: IDDQ values cannot be directly used to calculate I/O power of the DDR4 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in correlation from simulated channel I/O power to actual channel I/O power supported by IDDQ measurement.

For IDD, IPP and IDDQ measurements, the following definitions apply:
- L and 0: VIN ≤ VIL(AC) max
- H and 1: VIN ≥ VIH(AC) min
- MID-LEVEL: defined as inputs are VREFCA = VDD / 2
- Timings used for IDD, IPP and IDDQ measurement-loop patterns are provided in Table 6.
- Basic IDD, IPP and IDDQ measurement conditions are described in Table 7.
  Note: The IDD, IPP and IDDQ measurement-loop patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Detailed IDD, IPP and IDDQ measurement-loop patterns are described in IDD0 Measurement-Loop Pattern table through IDD7 Measurement-Loop Pattern table.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting.
  RON = RZQ/7 (34Ωin MR1);
  Qoff = 0B (Output buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40Ωin MR1);
  RTT_WR = RZQ/2 (120Ωin MR2);
  RTT_PARK = Disable;
  TDQS_t feature disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear-down mode disabled in MR3;
  Read/Write DBI disabled in MR5;
  DM_n disabled in MR5
- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} : = {H, L, L, L, L} ; apply BG/BA changes when directed.
- Define /D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} : = {H, H, H, H, H}; apply BG/BA changes when directed.

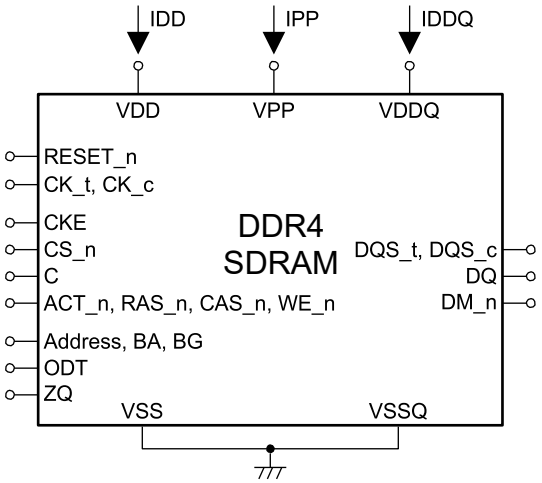

Figure 1: Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

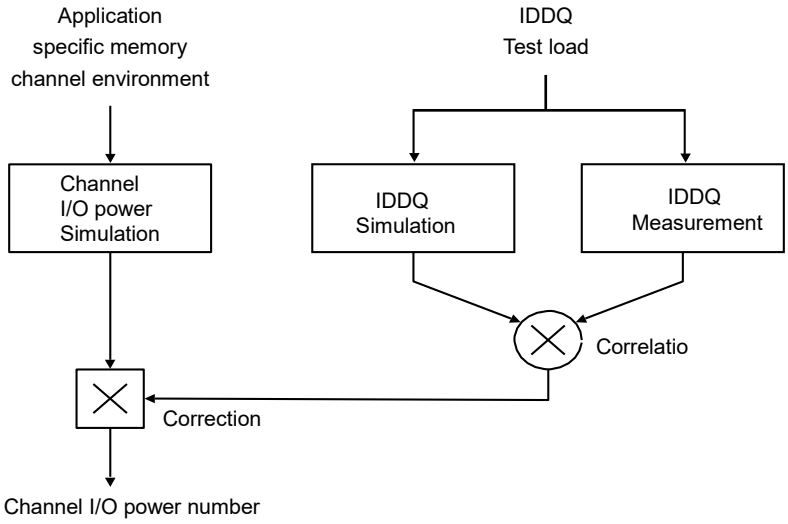

Figure 2: Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement

3.4.2 Timings Used for IDD, IPP and IDDQ Measurement-Loop Patterns

Table 8: Timings Used for IDD, IPP and IDDQ Measurement-LoopPatterns

Symbol	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	21-21-21	22-22-22	
tCK	1.25	1.071	0.938	0.833	0.750	0.682	0.625	ns
CL	11	13	15	17	19	21	22	nCK
CWL	11	12	14	16	18	20	20	nCK
nRCD	11	13	15	17	19	21	22	nCK
nRC	39	45	51	56	62	69	74	nCK
nRAS	28	32	36	39	42	48	52	nCK
nRP	11	13	15	17	19	21	22	nCK
nFAW	28	28	32	36	40	44	48	nCK
nRRDS	5	5	6	7	8	8	9	nCK
nRRDL	6	6	7	8	9	9	11	nCK
tCCD_S	4	4	4	4	4	4	4	nCK
tCCD_L	5	5	6	6	7	8	8	nCK
tWTR_S	2	3	3	3	4	4	4	nCK
tWTR_L	6	7	8	9	10	11	12	nCK
nRFC 8Gb	280	327	374	421	467	514	560	nCK

3.4.3 Basic IDD and IDDQ Measurement Conditions

Table 9: Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** CKE: H; External clock: on; tCK, nRC, nRAS, CL: see Table 8; BL: 8*1; AL: 0; CS_n: H between ACT and PRE; Command, address, bank group address, bank address inputs: partially toggling according to Table 10; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: cycling with one bank active at a time: 0,0,1,1,2, 2, ... (see Table 10); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; Pattern details: see Table 10
IDD0A	**Operating One Bank Active-Precharge Current (AL=CL-1)** AL = CL-1, Other conditions: see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current** Same condition with IDD0
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 8; BL: 8*1; AL: 0; CS_n: H between ACT, RD and PRE; Command, address, bank group address, bank address inputs, data I/O: partially toggling according to Table 11; DM_n: stable at 1; Bank activity: cycling with one bank active at a time: 0,0,1,1,2, 2, ... (see Table 11); Output buffer and RTT: enabled in MR*2; ODT Signal: stable at 0; Pattern details: see Table 11
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** AL=CL-1, Other conditions: see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPP Current** Same condition with IDD1
IDD2N	**Precharge Standby Current (AL=0)** CKE: H; External clock: on; tCK, CL: see Table 8; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to Table 12; data I/O: VDDQ; DM_n: stable at 1; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 12
IDD2NA	**Precharge Standby Current (AL=CL-1)** Same condition with IDD2N
IPP2N	**Precharge Standby IPP Current** AL = CL-1, Other conditions: see IDD2N
IDD2NT	**Precharge Standby ODT Current** CKE: H; External clock: on; tCK, CL: see Table 8; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to Table 13; data I/O: VSSQ; DM_n: stable at 1; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: toggling according to Table 13; pattern details: see Table 13
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled*3
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled*3,*5
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled*3
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled*3
IDD2P	**Precharge Power-Down Current** CKE: Low; External clock: on; tCK, CL: see Table 8; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; data I/O: VDDQ; DM_n: stable at 1; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
IPP2P	**Precharge Power-Down IPP Current** Same condition with IDD2P
IDD2Q	**Precharge Quiet Standby Current** CKE: H; External clock: On; tCK, CL: see Table 8; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: stable at 0; data I/O: VDDQ; DM_n: stable at 1;bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
IDD3N	**Active Standby Current** CKE: H; External clock: on; tCK, CL: see Table 12; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to Table 10; data I/O: VDDQ; DM_n: stable at 1; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 12
IDD3NA	**Active Standby Current (AL=CL-1)** Same condition with IDD3N

Symbol	Description
IPP3N	**Active Standby IPP Current** AL = CL-1, Other conditions: see IDD3N
IDD3P	**Active Power-Down Current** CKE: L; External clock: on; tCK, CL: see Table 8; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; data I/O: VDDQ; DM_n:stable at 1; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
IPP3P	**Active Power-Down IPP Current** Same condition with IDD3P
IDD4R	**Operating Burst Read Current** CKE: H; External clock: on; tCK, CL: see Table 8; BL: 8*1; AL: 0; CS_n: H between RD; Command, address, Bank group address, Bank address Inputs: partially toggling according to Table 14; data I/O: seamless read data burst with different data between one burst and the next one according to Table 14; DM_n: stable at 1;Bank activity: all Banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 14); output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 14
IDD4RA	**Operating Burst Read Current (AL=CL-1)** AL = CL-1, Other conditions: see IDD4R
IDD4RB	**Operating Burst Read Current with Read DBI** Read DBI enabled*3, Other conditions: see IDD4R
IPP4R	**Operating Burst Read IPP Current** Same condition with IDD4R
IDD4W	**Operating Burst Write Current** CKE: H; External clock: on; tCK, CL: see Table 8; BL: 8*1; AL: 0; CS_n: H between WR; command, address, bank group address, bank address inputs: partially toggling according to Table 15; data I/O: seamless write data burst with different data between one burst and the next one according to Table 15; DM_n: stable at 1; bank activity: all banks open, WR commands cycling through banks: 0,0,1,1,2, 2, ... (see Table 15); output buffer and RTT: enabled in MR*2; ODT signal: stable at H; pattern details: see Table 15
IDD4WA	**Operating Burst Write Current (AL=CL-1)** AL = CL-1, Other conditions: see IDD4W
IDD4WB	**Operating Burst Write Current with Write DBI** Write DBI enabled*3, Other conditions: see IDD4W
IDD4WC	**Operating Burst Write Current with Write CRC** Write CRC enabled*3, Other conditions: see IDD4W
IDD4W_par	**Operating Burst Write Current with CA Parity** CA Parity enabled*3, Other conditions: see IDD4W
IPP4W	**Operating Burst Write IPP Current** Same condition with IDD4W
IDD5B	**Burst Refresh Current (1X REF)** CKE: H; External clock: on; tCK, CL, nRFC: see Table 8; BL: 8*1; AL: 0; CS_n: H between REF; Command, address, bank group address, bank address Inputs: partially toggling according to Table 17; data I/O: VDDQ; DM_n: stable at 1; bank activity: REF command every nRFC (Table 17); output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 17
IPP5B	**Burst Refresh IPP Current (1X REF)** Same condition with IDD5B
IDD5F2	**Burst Refresh Current (2X REF)** tRFC=tRFC_x2, Other conditions: see IDD5B
IPP5F2	**Burst Refresh Write IPP Current (2X REF)** Same condition with IDD5F2
IDD5F4	**Burst Refresh Current (4X REF)** tRFC=tRFC_x4, Other conditions: see IDD5B
IPP5F4	**Burst Refresh Write IPP Current (4X REF)** Same condition with IDD5F4
IDD6N	**Self Refresh Current: Normal Temperature Range** T_C: 0 to 85^{O}C; LP ASR: Normal*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Table 8; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** Same condition with IDD6N

Symbol	Description
IDD6E	**Self-Refresh Current: Extended Temperature Range** T_C: 0 to 95°C; LP ASR: Extended*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Table 8; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: Extended temperature self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** Same condition with IDD6E
IDD6R	**Self-Refresh Current: Reduced Temperature Range** T_C: 0 to 45°C; LP ASR: Reduced*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Table 8; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: Reduced temperature self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range** Same condition with IDD6R
IDD6A	**Auto Self Refresh Current** T_C: 0 to 95°C; LP ASR: Auto*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Table 8; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: auto self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
IPP6A	**Auto Self Refresh IPP Current** Same condition with IDD6A
IDD7	**Operating Bank Interleave Read Current** CKE: H; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Table 8; BL: 8*1 ; AL: CL-1; CS_n: H between ACT and RDA; Command, address, bank group address, bank address Inputs: partially toggling according to Table 18; data I/O: read data bursts with different data between one burst and the next one according to Table 18; DM_n: stable at 1; bank activity: two times interleaved cycling through banks (0, 1, …7) with different addressing, see Table 18; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 18
IPP7	**Operating Bank Interleave Read IPP Current** Same condition with IDD7
IDD8	**Maximum Power Down Current** TBD
IPP8	**Maximum Power Down IPP Current** Same condition with IDD8

Notes:
1. Burst Length: BL8 fixed by MRS: MR0 bits A[1,0] = [0,0].

2. MR: Mode Register Output buffer enable:
   set MR1 bit A12 = 0: Qoff = output buffer enabled
   and MR1 bits A[2, 1] = [0,0]: output driver impedance control = RZQ/7 RTT_Nom enable:
   set MR1 bits A[10:8] = [0,1,1]: RTT_Nom = RZQ/6
   RTT_WR enable:
   set MR2 bits A[11:9] = [0,0,1]: RTT_WR = RZQ/2
   RTT_PARK disable:
   set MR5 bits A[8:6] = [0,0,0]

3. CAL enabled:
   set MR4 bits A[8:6] = [0,0,1]: 1600MT/s;
   [0,1,0]: 1866MT/s, 2133MT/s;
   [0,1,1]: 2400MT/s
   Gear down mode enabled:
   set MR3 bit A3 = 1: 1/4 Rate DLL disabled:
   set MR1 bit A0 = 0 CA parity enabled:
   set MR5 bits A[2:0] = [0,0,1]: 1600MT/s,1866MT/s, 2133MT/s
   [0,1,0]: 2400MT/s
   Read DBI enabled:
   set MR5 bit A12 = 1 Write DBI enabled:
   set MR5 bit A11 = 1
4. Low Power Array Self-Refresh (LP ASR)
   set MR2 bits A[7:6] = [0,0]: Normal
   [0,1]: Reduced temperature range
   [1,0]: Extended temperature range
   [1,1]: Auto self-refresh

Table 10: IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][2]	BG0	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use BG0 = 1, BA[1:0] = 1 instead																
		2	2*nRC	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 2 instead																
		3	3*nRC	repeat Sub-Loop 0, use BG0 = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 1 instead																
		5	5*nRC	repeat Sub-Loop 0, use BG0 = 1, BA[1:0] = 2 instead																
		6	6*nRC	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 3 instead																
		7	7*nRC	repeat Sub-Loop 0, use BG0 = 1, BA[1:0] = 0 instead																

Note:
1. DQS_t, DQS_c are VDDQ.
2. C[2:0] are used only for 3DS device
3. DQ signals are VDDQ.

Table 11: IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][2]	BG0	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3, 4	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
			nRCD -AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																
			1*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			1*nRC + nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																
		2	2*nRC	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 2 instead																
		3	3*nRC	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 1 instead																
		5	5*nRC	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 2 instead																
		6	6*nRC	repeat Sub-Loop 0, use BG0= 0, BA[1:0] = 3 instead																
		8	7*nRC	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 0 instead																

Note:
1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. C[2:0] are used only for 3DS device
3. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

Table 12: IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2N_par, IPP2, IDD3N, IDD3NA, and IDD3P Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][2]	BG0	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	0
			3	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	0
		1	4-7	repeat Sub-Loop 0, use BG0 = 1, BA[1:0] = 1 instead																
		2	8-11	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 0, use BG0 = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 0, use BG0 = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 0, use BG0 = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, use BG0 = 2, BA[1:0] = 0 instead																
		9	36-39	repeat Sub-Loop 0, use BG0 = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, use BG0 = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 0, use BG0 = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, use BG0 = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 0, use BG0 = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, use BG0 = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 0, use BG0 = 3, BA[1:0] = 0 instead																

Note:
1. DQS_t, DQS_c are VDDQ.
2. C[2:0] are used only for 3DS device
3. DQ signals are VDDQ.

Table 13: IDD2NT and IDDQ2NT Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][2]	BG0	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			3	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and BG0 = 1, BA[1:0] = 1 instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and BG0 = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BG0 = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BG0 = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and BG0 = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and BG0 = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BG0 = 1, BA[1:0] = 0 instead																

Note:
1. DQS_t, DQS_c are VDDQ.
2. C[2:0] are used only for 3DS device
3. DQ signals are VDDQ.

Table 14: IDD4R, IDD4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][2]	BG0	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		1	4	RD	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 0 instead																

Note:
1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. C[2:0] are used only for 3DS device
3. Burst Sequence driven on each DQ signal by Read Command.

Table 15: IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][2]	BG0	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 0 instead																

Note:
1. DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2. C[2:0] are used only for 3DS device
3. Burst Sequence driven on each DQ signal by Write Command.

Table 16: IDD4WC Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][2]	BG0	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC
			1,2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
		1	5	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC
			6,7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			8,9	D#, D#	1	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
		2	10-14	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 2 instead																
		3	15-19	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 3 instead																
		4	20-24	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 1 instead																
		5	25-29	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 2 instead																
		6	30-34	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 3 instead																
		7	35-39	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 0 instead																

Note:
1. DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2. C[2:0] are used only for 3DS device
3. Burst Sequence driven on each DQ signal by Write Command.

Table 17: IDD5B Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][2]	BG0	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	REF	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	-
		1	1	D	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	-
			3	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			4	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			5-8	repeat pattern 1...4, use BG0 = 1, BA[1:0] = 1 instead																
			9-12	repeat pattern 1...4, use BG0 = 0, BA[1:0] = 2 instead																
			13-16	repeat pattern 1...4, use BG0 = 1, BA[1:0] = 3 instead																
			17-20	repeat pattern 1...4, use BG0 = 0, BA[1:0] = 1 instead																
			21-24	repeat pattern 1...4, use BG0 = 1, BA[1:0] = 2 instead																
			25-28	repeat pattern 1...4, use BG0 = 0, BA[1:0] = 3 instead																
			29-32	repeat pattern 1...4, use BG0 = 1, BA[1:0] = 0 instead																
		2	65 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																

Note:
1. DQS_t, DQS_c are VDDQ.
2. C[2:0] are used only for 3DS device.
3. DQ signals are VDDQ.

Table 18: IDD7 Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][2]	BG0	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	RDA	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			...	repeat pattern 2...3 until nRRD - 1, if nRCD > 4. Truncate if necessary																
		1	nRRD	ACT	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	-
			nRRD + 1	RDA	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRCD > 4. Truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 2 instead																
		3	3*nRRD	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 3 instead																
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 1 instead																
		6	nFAW + nRRD	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 2 instead																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use BG0 = 0, BA[1:0] = 3 instead																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use BG0 = 1, BA[1:0] = 0 instead																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																

Note:
1. DQS_t, DQS_c are VDDQ.
2. C[2:0] are used only for 3DS device.
3. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

4. Electrical Specifications

4.1 IDD Specifications

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

Table 19: IDD and IDDQ Specification

Symbol	2133	2400	2666	2933	3200	Unit
I_{DD0}	115	125	130	135	140	mA
I_{DD0A}	115	125	130	135	140	mA
I_{DD1}	160	170	175	185	185	mA
I_{DD1A}	160	170	175	185	185	mA
I_{DD2N}	70	75	80	85	90	mA
I_{DD2NA}	70	75	80	85	90	mA
I_{DD2NT}	105	115	125	135	140	mA
I_{DD2NL}	80	85	90	95	100	mA
I_{DD2NG}	70	75	80	85	90	mA
I_{DD2ND}	50	50	50	50	50	mA
I_{DD2N_par}	75	85	90	95	100	mA
I_{DD2P}	40	40	45	45	50	mA
I_{DD2Q}	70	75	80	85	85	mA
I_{DD3N}	100	110	115	120	120	mA
I_{DD3NA}	100	110	115	120	120	mA
I_{DD3P}	75	75	80	80	80	mA
I_{DD4R}	330	365	405	445	510	mA
I_{DD4RA}	330	365	405	445	510	mA
I_{DD4RB}	320	355	390	425	455	mA
I_{DD4W}	340	375	410	450	455	mA
I_{DD4WA}	340	375	410	450	455	mA
I_{DD4WB}	310	345	375	410	415	mA
I_{DD4WC}	310	340	370	405	430	mA
I_{DD4W_par}	310	350	385	420	430	mA
I_{DD5B}	300	305	310	315	320	mA
I_{DD5F2}	225	230	235	240	245	mA
I_{DD5F4}	200	205	210	215	215	mA
I_{DD7}	430	450	465	480	520	mA
I_{DD8}	20	20	20	20	20	mA

Table 20: IPP Specification

Symbol	2133	2400	2666	2933	3200	Unit
I_{PP0}	8	8	8	8	8	mA
I_{PP1}	8	8	8	8	8	mA
I_{PP2N}	2	2	2	2	2	mA
I_{PP2P}	2	2	2	2	2	mA
I_{PP3N}	2	2	2	2	2	mA
I_{PP3P}	2	2	2	2	2	mA
I_{PP4R}	2	2	2	2	2	mA
I_{PP4W}	2	2	2	2	2	mA
I_{PP5B}	30	30	30	30	30	mA
I_{PP5F2}	30	30	30	30	30	mA
I_{PP5F4}	25	25	25	25	25	mA
I_{PP7}	35	35	35	35	35	mA
I_{PP8}	2	2	2	2	2	mA

Table 21: IDD6 Specification

Symbol	Temperature Range	Value		Unit	NOTE
		IDD (max.)	IPP (max.)		
IDD6N	0 - 85℃	53	4	mA	1
IDD6E	0 - 95℃	65	6	mA	2
IDD6R	0 – 45℃	46	3	mA	3
IDD6A	0 - 85℃	58	6	mA	4

Note:
1. Applicable for MR2 settings A6 = 0 and A7 = 0.
2. Applicable for MR2 settings A6 = 0 and A7 = 1. IDD6E is only specified for devices which support the extended temperature range feature.
3. Applicable for MR2 settings A6 = 1 and A7 = 0. IDD6R is only specified for devices which support the reduced temperature range feature.
4. Applicable for MR2 settings A6 = 1 and A7 = 1. IDD6A is only specified for devices which support the auto self-refresh feature.

4.2 Input / Output Capacitance

Table 22: Silicon pad I/O Capacitance

Symbol	Parameter	DDR4 1600/1866/2133		DDR4 2400/2666/2933/3200		Unit	NOTE
		min	max	min	max		
C_{IO}	Input/output capacitance	0.55	1.4	0.55	1.15	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	pF	1,3,4
C_{I}	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	0.5	2.3	0.5	2.3	pF	1,3,12
CTEN	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,3,13

Note:
1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure TBD.
2. DQ, DM[3:0]_n, DQS[3:0]_t, DQS[3:0]_c. Although the DM pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CLK_t, CLK_c
5. Absolute value of CIO(DQS[3:0]_t)-CIO(DQS[3:0]_c)
6. CI applies to ODT, CS_n, CKE, A0-A15, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7. CDI CTRL applies to ODT, CS_n and CKE
8. CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_t)+CI(CLK_c))
9. CDI_ADD_ CMD applies to, A0-A15, BA0-BA1, BG0-BG1,RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_t)+CI(CLK_c))
11. CDIO = CIO(DQ,DM)-0.5*(CIO(DQS[3:0]_t)+CIO(DQS[3:0]_c))
12. Maximum external load capacitance on ZQ pin: TBD pF.
13. TEN pin is DRAM internally pulled low through a weak pull-down resistor to VSS.

Table 23: DRAM package electrical specifications

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933/3200		Unit	NOTE
		min	max		
Z_{IO}	Input/output Zpkg	45	85	Ω	1
T_{dIO}	Input/output Pkg Delay	14	45	ps	1
L_{io}	Input/Output Lpkg	-	3.4	nH	1,2
C_{io}	Input/Output Cpkg	-	0.82	pF	1,3
$Z_{IO\ DQS}$	DQS_t, DQS_c Zpkg	45	85	Ω	1
$Td_{IO\ DQS}$	DQS_t, DQS_c Pkg Delay	14	45	ps	1
$L_{io\ DQS}$	DQS Lpkg	-	3.4	nH	1,2
$C_{io\ DQS}$	DQS Cpkg	-	0.82	pF	1,3
$DZ_{DIO\ DQS}$	Delta Zpkg DQSU_t, DQSU_c	-	10	Ω	-
	Delta Zpkg DQSL_t, DQSL_c	-	10	Ω	
$D_{TdDIO\ DQS}$	Delta Delay DQSU_t, DQSU_c	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	ps	
$Z_{I\ CTRL}$	Input- CTRL pins Zpkg	50	90	Ω	1
$T_{dI\_\ CTRL}$	Input- CTRL pins Pkg Delay	14	42	ps	1
Li CTRL	Input CTRL Lpkg	-	3.4	nH	1,2
Ci CTRL	Input CTRL Cpkg	-	0.7	pF	1,3
$Z_{IADD\ CMD}$	Input- CMD ADD pins Zpkg	50	90	Ω	1
$Td_{IADD\_\ CMD}$	Input- CMD ADD pins Pkg Delay	14	52	ps	1
Li ADD CMD	Input CMD ADD Lpkg	-	3.9	nH	1,2
Ci ADD CMD	Input CMD ADD Cpkg	-	0.86	pF	1,3
Z_{CK}	CLK_t & CLK_c Zpkg	50	90	Ω	1
Td_{CK}	CLK_t & CLK_c Pkg Delay	14	42	ps	1
Li CLK	Input CLK Lpkg	-	3.4	nH	1,2
Ci CLK	Input CLK Cpkg	-	0.7	pF	1,3
DZ_{DCK}	Delta Zpkg CLK_t & CLK_c	-	10	Ω	-
D_{TdCK}	Delta Delay CLK_t & CLK_c	-	5	ps	-
Z_{OZQ}	ZQ Zpkg	40	100	Ω	
$Td_{O\ ZQ}$	ZQ Delay	20	90	ps	
$Z_{O\ ALERT}$	ALERT Zpkg	40	100	Ω	
$Td_{O\ ALERT}$	ALERT Delay	20	55	ps	

Note:
1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown
2. It is assumed that Lpkg can be approximated as Lpkg = Zo*Td
3. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo

4.3 Speed Bin Table

Table 24: DDR4-1600 Speed Bins

Speed Bin				DDR4-1600		Unit	NOTE
CL-nRCD-nRP				11-11-11			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.75[14] (13.50)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	12
ACT to internal read or write delay time			tRCD	13.75 (13.50)[5,12]	-	ns	12
PRE command period			tRP	13.75 (13.50)[5,12]	-	ns	12
ACT to PRE command period			tRAS	35	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	48.75 (48.50)[5,12]	-	ns	12
	Normal	Read DBI					
CWL =9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5	1.6	ns	1,2,3,4,11,14
				(Optional)[5,12]			
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,11
CWL =9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings				9,11,12		nCK	13,14
Supported CL Settings with read DBI				11,13,14		nCK	13
Supported CWL Settings				9,11		nCK	

Table 25: DDR4-1866 Speed Bins

Speed Bin				DDR4-1866		Unit	NOTE
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.92[14] (13.50)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	12
ACT to internal read or write delay time			tRCD	13.92 (13.50)[5,12]	-	ns	12
PRE command period			tRP	13.92 (13.50)[5,12]	-	ns	12
ACT to PRE command period			tRAS	34	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	47.92 (47.50)[5,12]	-	ns	12
	Normal	Read DBI					
CWL =9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5	1.6	ns	1,2,3,4,11,14
				(Optional)[5,12]			
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,11
CWL =9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
				(Optional)[5,12]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL =10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings				9,11,12,13,14		nCK	13,14
Supported CL Settings with read DBI				11,13,14 ,15,16		nCK	13
Supported CWL Settings				9,10,11,12		nCK	

Table 26: DDR4-2133 Speed Bins

Speed Bin				DDR4-2133		Unit	NOTE
CL-nRCD-nRP				15-15-15			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.06[14] (13.50)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) +3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.06 (13.50)[5,12]	-	ns	12
PRE command period			tRP	14.06 (13.50)[5,12]	-	ns	12
ACT to PRE command period			tRAS	33	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	47.06 (46.50)[5,12]	-	ns	12
	Normal	Read DBI					
CWL =9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5	1.6	ns	1,2,3,4,11,14
				(Optional)[5,12]			
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,11
CWL =9,11	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,7
				(Optional)[5,12]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL =10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
				(Optional)[5,12]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL =11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.938	<1.071	ns	1,2,3
Supported CL Settings				9,11,12,13,14,15,16		nCK	13,14
Supported CL Settings with read DBI				11,13,14,15,16,18,19		nCK	
Supported CWL Settings				9,10,11,12,14		nCK	

Table 27: DDR4-2400 Speed Bin

Speed Bin				DDR4-2400		Unit	NOTE
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.16 (13.75)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) +3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.16 (13.75)[5,12]	-	ns	12
PRE command period			tRP	14.16 (13.75)[5,12]	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.16 (45.75)[5,12]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18		nCK	13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21		nCK	
Supported CWL Settings				9,10,11,12,14,16		nCK	

Table 28: DDR4-2666 Speed Bin

Speed Bin				DDR4-2666		Unit	NOTE
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.25[12] (13.75)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) +3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.25 (13.75)[5,12]	-	ns	12
PRE command period			tRP	14.25 (13.75)[5,12]	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.25 (45.75)[5,12]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
				(Optional)[5,10]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,9
				(Optional)[5,10]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
				(Optional)[5,10]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.750	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.750	<0.833	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20		nCK	13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23		nCK	
Supported CWL Settings				9,10,11,12,14,16,18		nCK	

Table 29: DDR4-2933 Speed Bin

Speed Bin				DDR4-2933		Unit	NOTE
CL-nRCD-nRP				21-21-21			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.32[12] (13.75)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 4nCK	tAA(max) +4nCK	ns	12
ACT to internal read or write delay time			tRCD	14.32 (13.75)[5,12]	-	ns	12
PRE command period			tRP	14.32 (13.75)[5,12]	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.32 (45.75)[5,12]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,13
				(Optional)[5,10]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,15
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,15
				(Optional)[5,10]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,15
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,15
				(Optional)[5,10]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,15
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,15
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,15
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,15
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,15
	CL = 19	CL = 22	tCK(AVG)	0.750	<0.833	ns	1,2,3,4,15
	CL = 20	CL = 23	tCK(AVG)	0.750	<0.833	ns	1,2,3,15
CWL = 16,20	CL = 19	CL = 23	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 21	CL = 24	tCK(AVG)	0.682	<0.750	ns	1,2,3,4
	CL = 22	CL = 24	tCK(AVG)	0.682	<0.750	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20,21,22		nCK	13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23,24		nCK	13
Supported CWL Settings				9,10,11,12,14,15,16,18,20		nCK	

Table 30: DDR4-3200 Speed Bin

Speed Bin				DDR4-3200		Unit	NOTE
CL-nRCD-nRP				22-22-22			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.75	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 4nCK	tAA(max) +4nCK	ns	12
ACT to internal read or write delay time			tRCD	13.75	-	ns	12
PRE command period			tRP	13.75	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	45.75	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,10
				(Optional)[5,10]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,10
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,10
				(Optional)[5,10]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,10
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,10
				(Optional)[5,10]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,10
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,10
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,10
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 19	CL = 22	tCK(AVG)	0.750	<0.833	ns	1,2,3,4,10
	CL = 20	CL = 23	tCK(AVG)	0.750	<0.833	ns	1,2,3,10
CWL = 16,20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 21	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 22	CL = 24	tCK(AVG)	0.625	<0.682	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20,21,22		nCK	13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23,24		nCK	
Supported CWL Settings				9, 10, 11, 12, 14, 16, 18, 20		nCK	

Speed Bin Table Notes

Absolute Specification
- VDDQ = VDD = 1.26V – 1.14V
- VPP = 2.375V – 2.75V

The values defined with above-mentioned table are DLL ON case.
DDR4- 1600, 1866, 2133, 2400, 2666, 2933 and 3200 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
11. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
12. Parameter apply from tCK(avg)min to tCH(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
13. CL number in parentheses, it means that these numbers are optional.
14. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
15. Any DDR4-2933 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

英尚国际有限公司
Http://www.sramsun.com
E-mail: sales@sramsun.com
Tel:0755-6665 8299

5. Electrical Characteristics & AC Timing

5.1 Reference Load for AC Timing and Output Slew Rate

Figure 3 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.
It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

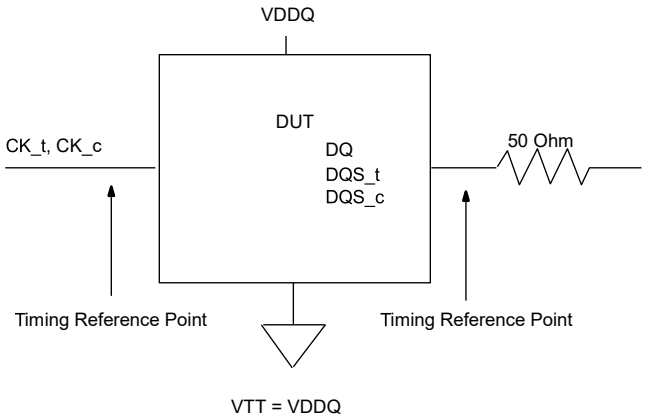

Figure 3: Reference Load for AC Timing and Output Slew Rate

5.2 tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

Table 31: tREFI by device density

Parameter	Symbol		8Gbit	Unit
Average periodic refresh interval	tREFI	0℃ < T_{CASE} ≦ 85℃	7.8	µs
		85℃ < T_{CASE} ≦ 95℃	3.9	µs

5.3 Timing Parameters by Speed Grade

Table 32: Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2133

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.938	<1.071	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_ tot	tCK(avg)max + tJIT(per)max_ tot	tCK(avg)min + tJIT(per)min_ tot	tCK(avg)max + tJIT(per)max_ tot	tCK(avg)min + tJIT(per)min_ tot	tCK(avg)max + tJIT(per)max_ tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	ps	25
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_to- tal	125		107		94		ps	25
Cycle to Cycle Period Jitter determin- istic	tJIT(cc)_dj	63		54		47		ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	100		86		75		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	ps	
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	ps	
Cumulative error across 16 cycles	tERR(16per)	-180	180	-155	155	-135	135	ps	
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	ps	
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	^{t}ERR(nper)min = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total min) ^{t}ERR(nper)max = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total max)						ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	ps	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	ps	
Command and Address Timing									
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(5nCK, 6.250ns)	-	Max(5nCK, 5.355ns)	-	Max(5nCK, 5.355ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 6ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 7.5ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 35ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-		1,2, 34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		1,34
Internal READ Command to PRE- CHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (4nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write trans- action to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (4nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns	2, 29, 34
delay from start of internal write trans- action to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max (4nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-		50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recov- ery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	-	
Auto precharge write recovery + pre- charge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))						nCK	
CS_n to Command Address Latency									
CS_n to Command Address Latency	tCAL	3	-	4	-	4	-	nCK	
DRAM Data Timing									
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	tCK(avg) /2	13,18, 39,49
DQ output hold time from DQS_t,DQS_c	tQH	TBD	-	TBD	-	TBD	-	tCK(avg) /2	13,17,18 ,39,49
DQS_t, DQS_c differential READ Preamble(1 clock preamble)	tRPRE	0.9	TBD	0.9	TBD	0.9	TBD	tCK	
DQS_t, DQS_c differential READ Preamble(2 clock preamble)	tRPRE	NA	NA	NA	NA	NA	NA	tCK	
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	TBD	0.33	TBD	0.33	TBD	tCK	
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK	21

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Http://www.sramsun.com
E-mail: sales@sramsun.com
Tel:0755-6665 8299

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	TBD	0.33	TBD	0.33	TBD	tCK	43
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK	-225	225	-195	195	-180	180	ps	37,38,39
MPSM Timing									
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		tCKSRX(min)		tCKSRX(min)			
Exit MPSM to commands not requir- ing a locked DLL	tXMP	TBD		TBD		TBD			
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)			
CS setup time to CKE	tMPX_S	TBD	-	TBD	-	TBD	-		
CS hold time to CKE	tMPX_H	TBD	-	TBD	-	TBD	-		
Calibration Timing									
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-		
Exit Self Refresh to commands re- quiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self re- fresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-		
Minimum CKE low width for Self re- fresh entry to exit timing with CA Par- ity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-		

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Http://www.sramsun.com
E-mail: sales@sramsun.com
Tel:0755-6665 8299

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKS-RE_PAR	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-		
Power Down Timing									
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to com- mands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-		
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	nCK	
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing									
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)		max(16nCK, 10ns)		max(16nCK, 10ns)			
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD			
ODT Timing									
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing									
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write level- ing mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/ DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling output error	tWLOE							ns	
CA Parity Timing									
Commands not guaranteed to be ex- ecuted during this time	tPAR_UN-KNOWN	-	PL	-	PL	-	PL		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	nCK	
Parity Latency	PL	4		4		4		nCK	
1CRC Error Reporting									
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	nCK	
tREFI									
tRFC1 (min)	8Gb	350	-	350	-	350	-	ns	34
tRFC2 (min)	8Gb	260	-	260	-	260	-	ns	34
tRFC4 (min)	8Gb	160	-	160	-	160	-	ns	34

Table 33: Timing Parameters by Speed Bin for DDR4-2400 to DDR4-3200

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	0.833	<0.937	0.75	<0.833	0.682	<0.750	0.625	<0.682	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-42	42	-38	38	-34	34	-32	32	ps	25
Clock Period Jitter- deterministic	JIT(per)_dj	-21	21	-19	19	-17	17	-16	16	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-33	33	-30	30	-27	27	-25	25	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	83	-	75	-	68	-	62	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	67	-	60	-	55	-	50	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-61	61	-55	55	-50	50	-46	46	ps	
Cumulative error across 3 cycles	tERR(3per)	-73	73	-66	66	-60	60	-55	55	ps	
Cumulative error across 4 cycles	tERR(4per)	-81	81	-73	73	-66	66	-61	61	ps	
Cumulative error across 5 cycles	tERR(5per)	-87	87	-78	78	-71	71	-65	65	ps	
Cumulative error across 6 cycles	tERR(6per)	-92	92	-83	83	-75	75	-69	69	ps	
Cumulative error across 7 cycles	tERR(7per)	-97	97	-87	87	-79	79	-73	73	ps	
Cumulative error across 8 cycles	tERR(8per)	-101	101	-91	91	-83	83	-76	76	ps	
Cumulative error across 9 cycles	tERR(9per)	-104	104	-94	94	-85	85	-78	78	ps	
Cumulative error across 10 cycles	tERR(10per)	-107	107	-96	96	-88	88	-80	80	ps	
Cumulative error across 11 cycles	tERR(11per)	-110	110	-99	99	-90	90	-83	83	ps	
Cumulative error across 12 cycles	tERR(12per)	-112	112	-101	101	-92	92	-84	84	ps	
Cumulative error across 13 cycles	tERR(13per)	-114	114	-103	-103	-93	93	-86	86	ps	
Cumulative error across 14 cycles	tERR(14per)	-116	116	-104	104	-95	95	-87	87	ps	
Cumulative error across 15 cycles	tERR(15per)	-118	118	-106	106	-97	97	-89	89	ps	
Cumulative error across 16 cycles	tERR(16per)	-120	120	-108	108	-98	98	-90	90	ps	
Cumulative error across 17 cycles	tERR(17per)	-122	122	-110	110	-100	100	-92	92	ps	
Cumulative error across 18 cycles	tERR(18per)	-124	124	-112	112	-101	101	-93	93	ps	
Cumulative error across n = 13, 14 . ... 49, 50 cycles	tERR(nper)	$t_{ERR(nper)min} = ((1 + 0.68ln(n)) * t_{JIT(per)\_total\ min})$ $t_{ERR(nper)max} = ((1 + 0.68ln(n)) * t_{JIT(per)\_total\ max})$								ps	

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) /Vil(ac) levels	tIS(base)	62	-	55	-	48	-	40	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	162	-	145	-	138	-	130	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	87	-	80	-	73	-	65	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	162	-	145	-	138	-	130	-	ps	
Control and Address Input pulse width for each input	tIPW	410	-	385	-	365	-	350	-	ps	
Command and Address Timing											
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(5nCK, 5ns)	-	Max(5nCK, 5ns)	-	Max(5nCK, 5ns)	-	Max (5nCK, 5ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	Max(2nCK, 2.5ns)	-	Max(2nCK, 2.5ns)	-	Max(2nCK, 2.5ns)	-	Max(2nCK, 2.5ns)	-	ns	1,2, 34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	ns	1,34
Internal READ Command to PRE- CHARGE Command delay	tRTP	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	ns	34
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank groups with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns	2, 29, 34

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Http://www.sramsun.com
E-mail: sales@sramsun.com
Tel:0755-6665 8299

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	768	-	854	-	940	-	1024	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	Max(24nCK, 15ns)	-	Max(24nCK, 15ns)	-	Max(24nCK, 15ns)	-	Max(24nCK, 15ns)	-	nCK	50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	33
Multi-Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	nCK	
Auto precharge write recovery + pre- charge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))								nCK	
Data setup time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,47
Data hold time from first DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	UI	46,47
CS_n to Command Address Latency											
CS_n to Command Address Latency	tCAL	max(3nCK, 3.748ns)	-	max(3nCK, 3.748ns)	-	max(3nCK, 3.748ns)	-	max(3nCK, 3.748ns)	-	nCK	
Mode Resister Set command cycle time in CAL mode	tMRD_CAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	nCK	
Mode Resister Set update delay in CAL mode	tMOD_CAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	nCK	
DRAM Data Timing											
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.17	-	0.18	-	0.19	-	0.22	tCK(avg) /2	13,18, 39,49
DQ output hold time from DQS_t,DQS_c	tQH	0.74	-	0.74	-	0.74		0.74	-	tCK(avg) /2	13,17, 18,39,4 9
Data Valid Window per device per UI :(tQH-tDQSQ) of each UI on a given DRAM	tDVWd	0.64	-	0.64	-	0.64		0.64	-	UI	17,18, 39,49
Data Valid Window per pin per UI :(tQH-tDQSQ) of each UI on a given DRAM	tDVWp	0.72	-	0.72	-	0.72		0.72	-	UI	17,18, 39,49
DQ low impedance time from CK_t,CK_c	tLZ(DQ)	-330	175	-310	170	-280	165	-250	160	ps	39
DQ high impedance time from CK_t,CK_c	tHZ(DQ)	-	175	-	170	-	165	-	160	ps	39
Data Strobe Timing											
DQS_t, DQS_c differential READ Preamble (1 clock preamble)	tRPRE	0.9	Note44	0.9	Note44	0.9	Note44	0.9	Note44	tCK	39,40
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	tRPRE2	1.8	Note44	1.8	Note44	1.8	Note44	1.8	Note44	tCK	39,41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	Note45	0.33	Note45	0.33	Note45	0.33	Note45	tCK	39

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	tWPRE2	1.8	-	1.8	-	1.8	-	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-330	175	-310	170	-280	165	-250	160	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	175	-	170	-	165	-	160	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	-0.50	0.5	-0.50	0.5	-0.50	0.5	-0.50	0.5	tCK	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-			0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c with DLL On mode	tDQSCK	-175	175	-170	170	-165	165	-160	160	ps	37,38, 39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI	-	290	-	270	-	265	-	260	ps	37,38, 39
MPSM Timing											
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	nCK	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	nCK	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	nCK	
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-	nCK	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	nCK	
CS setup time to CKE	tMPX_S	tISmin+tIHmin	-	tISmin+tIHmin	-	tISmin+tIHmin	-	tISmin+tIHmin	-	ns	

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Http://www.sramsun.com
E-mail: sales@sramsun.com
Tel:0755-6665 8299

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CS_n High hold time to CKE rising edge	tMPX_HH	tXP(min)	-	tXP(min)	-	tXP(min)	-	tXP(min)	-	ns	
CS_n Low hold time to CKE rising edge	tMPX_LH	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	ns	
Calibration Timing											
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing											
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min) +10ns	-	tRFC(min) +10ns	-	tRFC(min) +10ns	-	tRFC(min) +10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT (min)	tRFC4(min) +10ns	-	tRFC4(min) +10ns	-	tRFC4(min) +10ns	-	tRFC4(min) +10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min) +10ns	-	tRFC4(min) +10ns	-	tRFC4(min) +10ns	-	tRFC4(min) +10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) +1nCK	-	tCKE(min) +1nCK	-	tCKE(min) +1nCK	-	tCKE(min) +1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min) +1nCK+PL	-	tCKE(min) +1nCK+PL	-	tCKE(min) +1nCK+PL	-	tCKE(min) +1nCK+PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max (5nCK,10ns)	-	max (5nCK,10 ns)	-	max (5nCK,10ns)	-	max (5nCK,10 ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max (5nCK,10ns)	-	Max (5nCK,10 ns)	-	Max (5nCK,10 ns)	-	max (5nCK,10 ns)	-	nCK	
Power Down Timing											
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	nCK	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK	

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Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	2	-	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+ 1	-	WL+4+WR+ 1	-	WL+4+WR+ 1	-	WL+4+WR+ 1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP BC4DEN	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP BC4DEN	WL+2+WR+ 1	-	WL+2+WR+ 1	-	WL+2+WR+ 1	-	WL+2+WR+ 1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	nCK	
PDA Timing											
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD	-	tMOD	-	tMOD	-	tMOD	-	nCK	
ODT Timing											
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.28	0.72	0.28	0.72	tCK(avg)	
Write Leveling Timing											
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/ DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	

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Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
crossing											
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns	
CA Parity Timing											
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	72	144	80	160	88	176	96	192	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	64	-	71	-	78	-	85	nCK	
Parity Latency	PL	5	-	5	-	6	-	6	-	nCK	
CRC Error Reporting											
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	nCK	
Geardown timing											
Exit RESET from CKE HIGH to a valid MRS geardown	tXPR_GEAR	-		tXPR		tXPR		tXPR		nCK	
CKE High Assert to Gear Down Enable time	tXS_GEAR	-		tXS		tXS		tXS		nCK	
MRS command to Sync pulse time	tSYNC_GEAR	-		tMOD + 4CK		tMOD + 4CK		tMOD + 4CK		nCK	27
Sync pulse to First valid command	tCMD_GEAR	-		tMOD		tMOD		tMOD		nCK	27
Geardown setup time	tGEAR_setup	-	-	2	-	2	-	2	-	nCK	
Geardown hold time	tGEAR_hold	-	-	2	-	2	-	2	-	nCK	
tREFI											
tRFC1 (min)	8Gb	350	-	350	-	350	-	350	-	ns	34
tRFC2 (min)	8Gb	260	-	260	-	260	-	260	-	ns	34
tRFC4 (min)	8Gb	160	-	160	-	160	-	160	-	ns	34

Note:
1. Start of internal write transaction is defined as follows:
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TCASE.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.

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14. The deterministic component of the total timing. Measurement method TBD.
15. DQ to DQ static offset relative to strobe per group. Measurement method TBD.
16. This parameter will be characterized and guaranteed by design.
17 When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock.(output deratings are relative to the SDRAM input clock). Example TBD.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI.
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables shown in section 10.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg).min/2
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM.
39. Value is only valid for RONNOM = 34 ohms.
40. 1tCK toggle mode with setting MR4:A11 to 0.
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666/2933/3200 speed grade.
42. 1tCK mode with setting MR4:A12 to 0.
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point.
46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High.
47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ.
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

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6. DDR4 Function Matrix

DDR4 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

Table 34: Function Matrix (By ORG. V: Supported, Blank: Not supported)

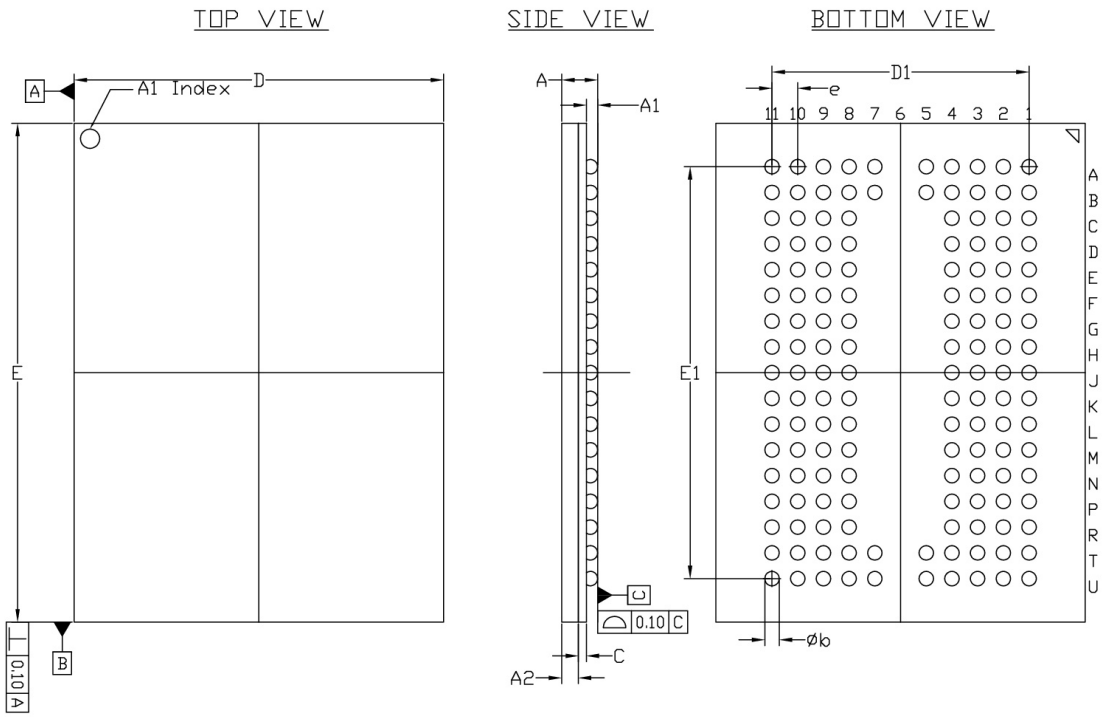
Functions	X32	NOTE
Write Leveling	V	
Temperature controlled Refresh	V	
Low Power Auto Self Refresh	V	
Fine Granularity Refresh	V	
Multi Purpose Register	V	
Data Mask	V	
Data Bus Inversion	V	
TDQS		
ZQ calibration	V	
DQ Vref Training	V	
Per DRAM Addressability	V	
Mode Register Readout	V	
CAL	V	
WRITE CRC	V	
CA Parity	V	
Control Gear Down Mode	V	
Programmable Preamble	V	
Maximum Power Down Mode		
Boundary Scan Mode	V	
Additive Latency		

Table 35: Function Matrix (By Speed. V: Supported, Blank: Not supported)

Functions	DLL Off mode		DLL On mode		NOTE
	equal or slower than 250Mbps	1600/1866/2133 Mbps	2400 Mbps	2666/2933/3200 Mbps	
Write Leveling	V	V	V	V	
Temperature controlled Refresh	V	V	V	V	
Low Power Auto Self Refresh	V	V	V	V	
Fine Granularity Refresh	V	V	V	V	
Multi Purpose Register	V	V	V	V	
Data Mask	V	V	V	V	
Data Bus Inversion	V	V	V	V	
TDQS		V	V	V	
ZQ calibration	V	V	V	V	
DQ Vref Training	V	V	V	V	
Per DRAM Addressability		V	V	V	
Mode Register Readout	V	V	V	V	
CAL		V	V	V	
WRITE CRC		V	V	V	
CA Parity		V	V	V	
Control Gear Down Mode				V	
Programmable Preamble (= 2tCK)			V	V	
Maximum Power Down Mode		V	V	V	
Boundary Scan Mode	V	V	V	V	

7. Package Diagram

144 Ball Fine Pitch Ball Grid Array Outline



PKG outline

REF.	Dimension in mm		
	Min	Nom	Max
A	1.000	1.100	1.200
A1	0.300	0.350	0.400
A2	0.510	0.530	0.550
øb	0.400	0.450	0.500
C	0.190	0.220	0.250
D	11.400	11.500	11.600
D1	8.000 BSC		
E	15.400	15.500	15.600
E1	12.800 BSC		
e	0.800 BSC		

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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[Product usage]
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3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL2, H2S, NH3, SO2, and NOx.
4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
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