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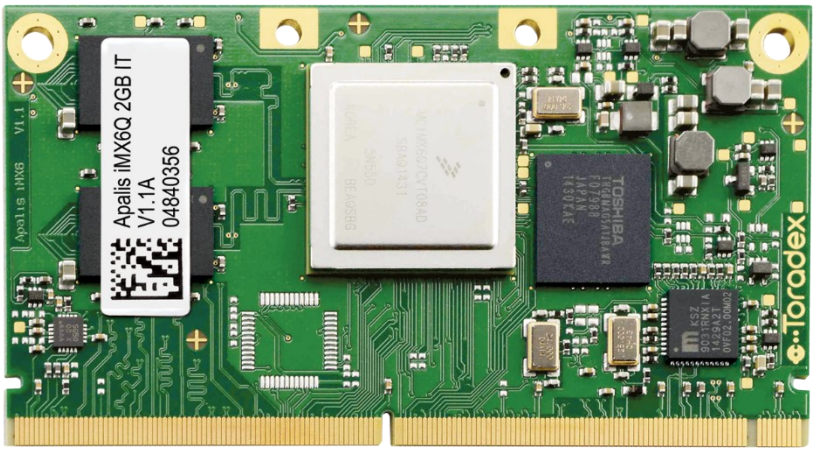
Apalis iMX6

Datasheet



Revision History

Date	Doc. Rev.	Apalis iMX6 Version	Changes
10-Feb-2014	Rev. 0.9	V1.0	Initial Release: Preliminary version
21-Feb-2014	Rev. 0.91	V1.0	Apalis iMX6Q 2GB IT and Apalis iMX6D 512MB added Minor changes
18-Mar-2014	Rev. 0.92	V1.0	Correction in eMMC Flash size (section 1.3.2)
02-July-2014	Rev. 0.93	V1.1	Add information about GPIO16 when using IEEE 1588 Correction of UART RX/TX lines for PCB V1.1 Clarification for Colour mapping in Table 5-12 Clarifications in digital audio section 5.15
11-Nov-2014	Rev. 0.94	V1.1	Updated hyperlinks in the section 5.15.1
17-Nov-2014	Rev. 0.95	V1.1	Section 8.7 renamed and updated Additional information to RTC added (section 5.8.1 and 8.3)
15-April-2015	Rev. 0.96	V1.1	Section 1.3.3, Interfaces Updated number of available GPIOs Section 5.25, Media Local Bus (MLB150) Corrected Table 5-73 name
22-Oct-2015	Rev. 0.97	V1.1	Correction of iMX6Q 2GB IT RAM size (from 1GB to 2GB) Add Figure 18
17-Dec-2015	Rev. 0.98	V1.1	Correction of iMX6Q 2GB IT eMMC NAND size (from 4GB to 8GB) Added note after the function list table. Minor correction in the LVDS section. Minor corrections in recovery mode section: Recovery mode can only be entered during initial power-up (cold boot)
30-Dec-2015	Rev. 1.0	V1.1	Corrected iMX 6 ball name from CSI0_HSYNC to CSI0_MCLK for Apalis iMX6 pin 197 Corrected iMX6Q 2GB IT eMMC NAND size (from 8GB to 4GB)
12-Feb-2015	Rev. 1.1	V1.1	Add RESET_MOCI# circuit description (Figure 5) Change to generic SoC part numbers (section 1.3.1) Corrected part number of Ethernet PHY (section 1.5.2) Add SPI master/slave signal direction table (section 5.10) Correction of junction temperature of non-IT version (Table 8-4) Update document according to merge of Freescale with NXP
15-Jun-2015	Rev. 1.2	V1.1	Section 5.10: correct maximum SPI clock frequency Section 8.3: add typical power consumption of iMX6Q
12-Jan-2017	Rev. 1.3	V1.1	Add new Apalis iMX6D 1GB IT Add information about available heatsinks (section 8.6) External Links updated Minor changes
08-Oct-2018	Rev. 1.4	V1.1	Section 1.3.2: adding flash memory endurance remark Section 3.2: rename DAP1_RESET to DAP1_RESET# Section 5.5.1: correct colour configuration table Section 5.14: correct SGTL500 pin number for AAP1_HP_L Section 5.15.1: Correct I2S Slave pins Section 5.15.2: Correct AC'97 pins Section 7: add link to errata page Update missing internal document links
16-May-2019	Rev. 1.5	V1.1	Section 5.13: correct SD1 signal pins
30-Sep-2020	Rev. 1.6	V1.1	Section 8.5.1: update MXM3 connector

Contents

1. Introduction

1.1 Hardware

The Apalis iMX6 is a computer module based on the NXP®/Freescale i.MX 6 embedded System-on-Chip (SoC). The SoC features a scalable multicore ARM Cortex™ A9 processor with one to four cores, depending on the version. The CPU frequency peaks at 1.2GHz. The module delivers high CPU and graphical performance with minimum power consumption.

The Apalis iMX6 incorporates DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling which enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature to achieve the best performance with the lowest power consumption. The module is also available in industrial temperature range (-40°C to 85°C) variants.

The module targets a wide range of applications, including: Digital Signage, Medical Devices, Navigation, Industrial Automation, HMIs, Avionics, Entertainment system, POS, Data Acquisition, Thin Clients, Robotics, Gaming and much more

It offers a wide range of interfaces from simple GPIOs, industry standard I2C, SPI, CAN, and UART buses through to high speed USB 2.0 interfaces and high speed PCI Express, SATA, and gigabit Ethernet. The HDMI and dual channel LVDS interfaces make it very easy to connect large, full HD resolution displays.

The Apalis iMX6 module encapsulates the complexity associated with modern day electronic design, such as high speed impedance controlled layouts with high component density utilising blind and buried via technology. This allows the customer to create a carrier board which implements the application specific electronics generally being much less complicated. The Apalis iMX6 module takes this one step further and implements an interface pin out which allows direct connection of real world I/O ports without needing to cross traces or traverse layers, referred to as Direct Breakout™. This becomes increasingly important for customers as more interfaces move toward high speed, serial technologies that use impedance controlled differential pairs, as it allows them to easily route such interfaces to common connectors in a simple, robust fashion.

1.2 Software

The Apalis iMX6 comes with a core runtime licence for Windows Embedded Compact 2013. Windows Embedded Compact 7 and Embedded Linux images are also available.

Toradex works with partners in case you require another Operating System. For more information, contact our support.

1.3 Main Features

1.3.1 CPU

	iMX6Q 1GB	iMX6Q 2GB IT	iMX6D 512MB	iMX6D 1GB IT
NXP SoC	MCIMX6Q5EYM10Ax	MCIMX6Q7CVT08Ax	MCIMX6D5EYM10Ax	MCIMX6D7CVT08Ax
CPU Cores	4	4	2	2
L1 Instruction Cache (each core)	32KByte	32KByte	32KByte	32KByte
L1 Data Cache (each core)	32KByte	32KByte	32KByte	32KByte
L2 Cache (shared by cores)	1MByte	1MByte	1MByte	1MByte
NEON MPE	✓	✓	✓	✓
Maximum CPU frequency	996MHz	792MHz	996MHz	792MHz
ARM TrustZone	✓	✓	✓	✓
Advanced High Assurance Boot	✓	✓	✓	✓
Cryptographic Acceleration and Assurance Module	✓	✓	✓	✓
Secure Real-Time Clock	✓	✓	✓	✓
Secure JTAG Controller	✓	✓	✓	✓

1.3.2 Memory

	iMX6Q 1GB	iMX6Q 2GB IT	iMX6D 512MB	iMX6D 1GB IT
DDR3 RAM Size	1GByte	2GByte	512MByte	1GByte
DDR3 RAM Speed	1066MT/s	1066MT/s	1066MT/s	1066MT/s
DDR3 RAM Memory Width	64bit	64bit	64bit	64bit
eMMC NAND Flash (8bit)*	4GByte	4GByte	4GByte	4GByte

*eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear levelling in the eMMC controller makes sure the cells are getting worn out evenly. More information can be found here http://developer.toradex.com/knowledge-base/flash-memory and here https://en.wikipedia.org/wiki/Flash_memory#Write_endurance.

1.3.3 Interfaces

	iMX6Q 1GB	iMX6Q 2GB IT	iMX6D 512MB	iMX6D 1GB IT
LCD RGB (24bit, 225 Mpixel/s)	1	1	1	1
LVDS (2x single channel 85 Mpxiel/s or 1x dual channel 165 Mpixel/s)	1	1	1	1
HDMI 1.4a (266Mpixel/s)	1	1	1	1
VGA Analogue Video	1	1	1	1
MIPI DSI	1x 2 Data Lanes*	1x 2 Data Lanes*	1x 2 Data Lanes*	1x 2 Data Lanes*
Resistive Touch Screen	4 Wire	4 Wire	4 Wire	4 Wire
Analogue Audio Headphone out	1 (Stereo)	1 (Stereo)	1 (Stereo)	1 (Stereo)
Analogue Audio Line in	1 (Stereo)	1 (Stereo)	1 (Stereo)	1 (Stereo)
Analogue Audio Mic in	1 (Mono)	1 (Mono)	1 (Mono)	1 (Mono)
AC97/I2S/SSI	1+2*	1+2*	1+2*	1+2*
ESAI	1*	1*	1*	1*

	iMX6Q 1GB	iMX6Q 2GB IT	iMX6D 512MB	iMX6D 1GB IT
S/PDIF	1 in / 1 out	1 in / 1 out	1 in / 1 out	1 in / 1 out
Parallel Camera Interface	1+1*	1+1*	1+1*	1+1*
MIPI CSI-2	1x 4 Data Lanes*	1x 4 Data Lanes*	1x 4 Data Lanes*	1x 4 Data Lanes*
I2C	3	3	3	3
SPI	2+1*	2+1*	2+1*	2+1*
UART	4+1*	4+1*	4+1*	4+1*
SD/SDIO/MMC	2+1*	2+1*	2+1*	2+1*
GPIO	135*	135*	135*	135*
USB 2.0 OTG (host/device)	1	1	1	1
USB 2.0 host	3+1*	3+1*	3+1*	3+1*
PCIe (Gen 2.0)	1 Lane	1 Lane	1 Lane	1 Lane
Serial ATA II (3Gbit/s)	1	1	1	1
10/100/1000 MBit/s Ethernet	1 (IEEE 1588)	1 (IEEE 1588)	1 (IEEE 1588)	1 (IEEE 1588)
PWM	4	4	4	4
Analogue Inputs	4	4	4	4
CAN	2	2	2	2
MLB	2*		2*	
8bit NAND Interface	1*	1*	1*	1*

*These interfaces are available on pins that are not defined as standard interfaces in the Apalis architecture. The pins are either located in the type specific area or are alternate functions of other pins. There are restrictions on using different interfaces simultaneously, please check the available alternate functions to understand any constraints. For more information, please check the list of type specific interfaces in section 1.4 and the description of the associated interface in section 5

1.3.4 Graphics Processing Unit

	iMX6Q 1GB	iMX6Q 2GB IT	iMX6D 512MB	iMX6D 1GB IT
Independent Image Processing Units	2	2	2	2
OpenGL® ES 2.0 (88M triangles/s, 1.066G pixel/s)	✓	✓	✓	✓
Number of OpenGL® Shaders	4	4	4	4
Dedicated OpenVG 1.1 accelerator	✓	✓	✓	✓
OpenVG 1.1	✓	✓	✓	✓
Windows Direct3D	✓	✓	✓	✓
OpenCL EP	✓	✓	✓	✓
16x Line Anti-aliasing	✓	✓	✓	✓
8K x 8K texture and 8K x 8K rendering target	✓	✓	✓	✓
Ultra-threaded, unified vertex and fragment shaders	✓	✓	✓	✓

1.3.5 HD Video Decode

- ✓ MPEG-2 (Main, High Profile) – 1080p30, 720p60, (50Mbps)
- ✓ MPEG4/XviD (Simple, Advanced Simple Profile) – 1080p30 (40Mbps)
- ✓ H.263 (P0/P3) – 16CIF(1408x1152) 30fps (20Mbps)
- ✓ H.264 (Constrained Baseline, Baseline, Main, High Profile) – 1080p30, 720p60, (50Mbps)
- ✓ H.264-MVC (Baseline, Main, High Profile) – 720p60
- ✓ VC1 (Simple, Main, Advanced Profile) – 1080p30 (45Mbps)
- ✓ RV (8/9/10) – 1080p30 (40Mbps)
- ✓ DivX (3/4/5/6) – 1080p30 (40Mbps)
- ✓ On2 VP6/VP8 – 720p30 (20Mbps)
- ✓ AVS Jizhun – 1080p30 (40Mbps)
- ✓ MJPEG (Baseline) – 8192x8192 (120MPixel/s)

1.3.6 HD Video Encode

- ✓ MPEG4 (Simple Profile) – 720p30 (12Mbps)
- ✓ H.263 (P0/P3) – 4CIF(704x576) 30fps (8Mbps)
- ✓ H.264 (Constrained Baseline, Baseline Profile) – 1080p30, (14Mbps)
- ✓ MJPEG (Baseline) – 8192x8192 (160MPixel/s)

1.3.7 Supported Operating Systems

- ✓ Windows Embedded Compact 7
- ✓ Windows Embedded Compact 2013
- ✓ Embedded Linux
- ✓ Contact Toradex for Android
- ✓ Other operating systems are available through Toradex partners

1.4 Interface Overview

The table in Figure 1 shows the interfaces that are supported on the Apalis® iMX6 module, and whether an interface is provided on standard or type specific pins. The USB interface is an example of an interface that makes use of standard and type specific pins – four USB ports are provided as part of the standard interface pin out while an additional port is type specific.

Some interfaces are available as alternate function of a pin. This function can only be used if the primary function of the pin is not used. Check section 4.4 for a list of all alternate functions of the MXM3 pins.

Feature	Apalis®™ iMX6	Standard	Type Specific	Alternate Function
4 Wire Resistive Touch	1	1		
Analogue Inputs	4	4		
Analogue Audio (Line in/out, Mic in)	1	1		
CAN	2	2		
CSI (Quad Lane)	1		1	
DSI (Dual Lane)	1		1	
Dual Channel LVDS Display (2x Single or 1x Dual)	1	1		
Gigabit Ethernet	1	1		
GPIO	134	8	11	115
AC97/I2S/SSI	2	1		1
ESAI	1			1
HDMI (TDMS)	1	1		
I2C	3	3		
Parallel Camera	2	1		1
Parallel LCD	1	1		
PCI-Express (lane count)	1	1		
PWM	4	4		
SATA	1	1		
SD/SDIO/MMC	3	2		1
S/PDIF In	1	1		
S/PDIF Out	1	1		
SPI	3	2		1
UART	5	4		1
USB 2.0 OTG (host/device)	1	1		
USB 2.0 host	4	3	1	
VGA	1	1		
MLB	2*		1*	1*
8bit NAND interface	1			1

Figure 1: Apalis® iMX6 Module Interfaces

*These interfaces are not available on all versions of the Apalis iMX6 module. Please see section 1.3.3 for more information

1.5 Reference Documents

1.5.1 NXP/Freescale i.MX 6

You will find the details about i.MX 6 SoC in the Datasheet and Reference Manual provided by NXP.
www.nxp.com

1.5.2 Ethernet Transceiver

Apalis iMX6 uses the Micrel KSZ9031RNX Gigabit Ethernet Transceiver (PHY).
www.microchip.com

1.5.3 Audio Codec

Apalis iMX6 uses the NXP SGTL5000 Audio Codec.
www.nxp.com

1.5.4 Touch Screen Controller / ADC

Apalis iMX6 uses the STMicroelectronics STMPE811 Touchscreen Controller.
www.st.com

1.5.5 Apalis Carrier Board Design Guide

This document provides additional information about the Apalis form factor. A custom carrier board should follow the Apalis Carrier Board Design Guide in order to make the board compatible within the Apalis module family. Please study this document in detail prior to starting your carrier board design.
http://docs.toradex.com/101123-apalis-arm-carrier-board-design-guide.pdf

1.5.6 Layout Design Guide

This document contains information about high speed layout design and additional information that helps to get the carrier board layout the first time right.
http://docs.toradex.com/102492-layout-design-guide.pdf

1.5.7 Toradex Developer Centre

You can find a lot of additional information in the Toradex Developer Centre, which is updated with the latest product support information on a regular basis.

Please note that the Developer Centre is common for all Toradex products. You should always check to ensure if information is valid or relevant for the Apalis iMX6.
http://www.developer.toradex.com

1.5.8 Apalis Evaluation Board Schematics

We provide the completed schematics plus the Altium project file which includes library symbols and IPC-7351 compliant footprints for the Apalis Evaluation Board free of charge. This is a great help when designing your own Carrier Board.
http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

2. Architecture Overview

2.1 Block Diagram

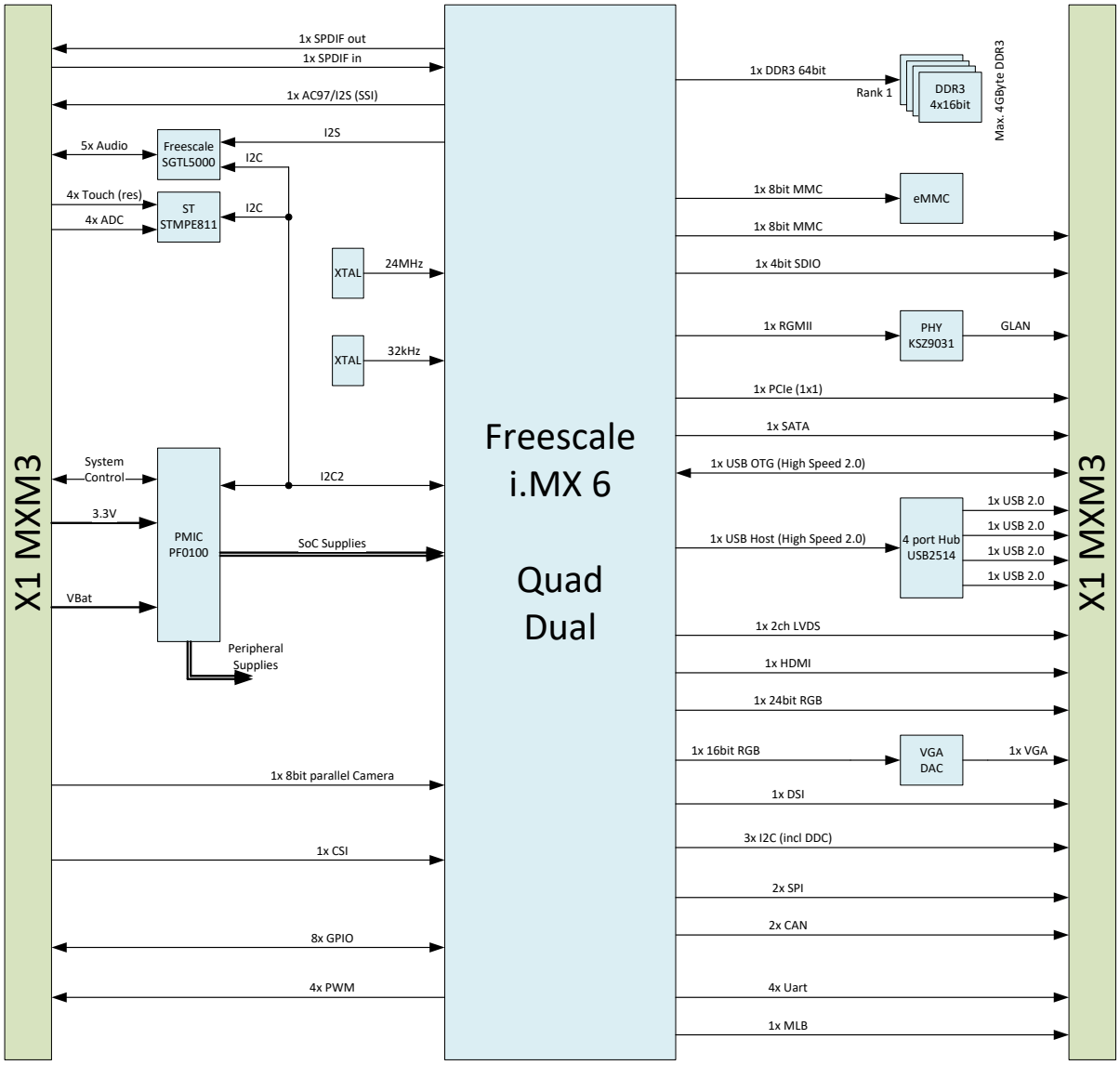


Figure 2 Apalis iMX6 Block Diagram

3. Apalis iMX6 Connectors

3.1 Pin Numbering

The diagrams in figures Figure 3 and Figure 4 show the pin numbering schema on both sides of the module. The schema deviates from the unrelated MXM3 standard pin numbering schema.
Pins on the top side of the module have an even number and pins on the bottom side have an odd number.

The pin number increases linearly as a multiple of the pitch – that is, pins which are not assembled in the connector (between pins 18 and 23) are also accounted for in the numbering (pins 19 through 22 do not exist). Similarly, pins which do not exist due to the connector notch are also accounted for (pins 166 through 172).

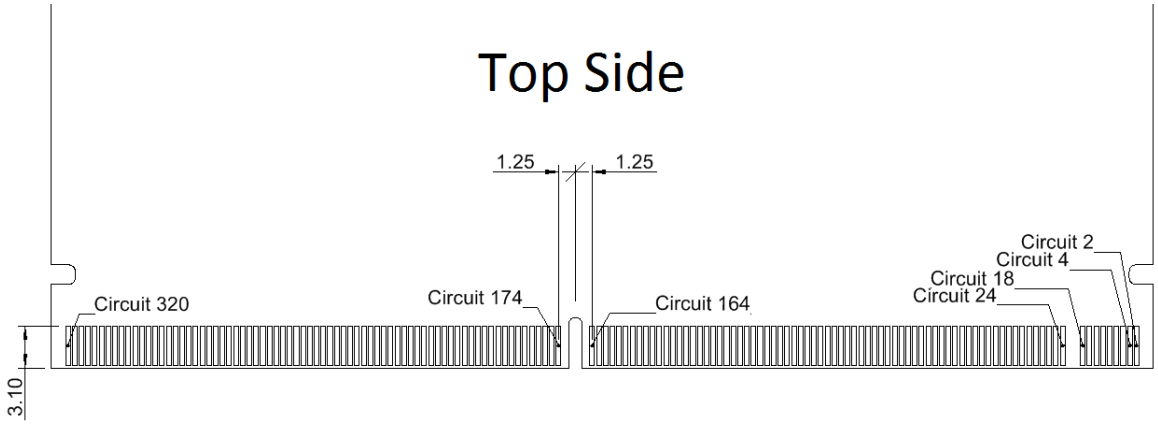


Figure 3: Pin numbering schema on the top side of the module

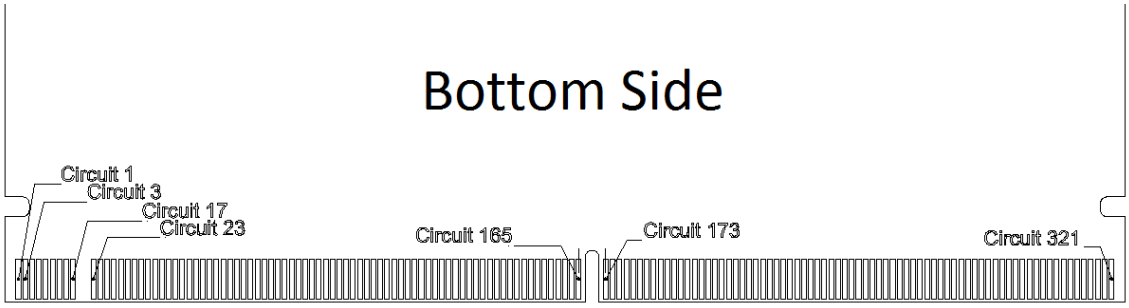


Figure 4: Pin numbering schema on the bottom side of the module

3.2 Assignment

The following table describes the MXM3 connector pin out. Some pins are shaded dark grey as type specific interfaces. These pins might be not compatible with other modules in the Apalis family. Please be aware that you might lose compatibility with other Apalis modules on your carrier board if you make use of these interfaces. It should be noted that type specific interfaces will be kept common across modules that share such interfaces where possible. For example, if both module A and module B have three additional PCI-Express lanes which are available in the same configurations as a type specific interface, then they shall be assigned to the same pins in the type specific area of the connector. Hence, both module A and module B shall share compatibility between these parts of the type specific interface.

- X1: Pin number on the MXM3 module edge connector (X1).
- Apalis Signal Name: The name of the signal according to the Apalis form factor definition. This name corresponds to the default usage of the pin. Most of the pins also have alternate function, but in order to be compatible with other Apalis modules, only the default function should be used and the carrier board should be implemented according to the Apalis Carrier Board Design Guide.
- iMX6 Ball Name: The name of the pin of the i.MX 6 chip.

Table 3-1 X1 Connector

X1	Apalis Signal Name	iMX6 Ball Name	Notes	X1	Apalis Signal Name	iMX6 Ball Name	Notes
1	GPIO1	NAND_DATA04		2	PWM1	GPIO09	
3	GPIO2	NAND_DATA05		4	PWM2	GPIO01	
5	GPIO3	NAND_DATA06		6	PWM3	SD4_DATA1	
7	GPIO4	NAND_DATA07		8	PWM4	SD4_DATA2	
9	GND			10	VCC		
11	GPIO5	NAND_READY		12	CAN1_RX	GPIO08	
13	GPIO6	NAND_WP_B		14	CAN1_TX	GPIO07	
15	GPIO7	GPIO02		16	CAN2_RX	KEY_ROW4	
17	GPIO8	GPIO06		18	CAN2_TX	KEY_COL4	
23	GND			24	POWER_ENABLE_MOCI		PWR Management
25	SATA1_RX+	SATA_PHY_RX_P		26	RESET_MOCI#		PWR Management
27	SATA1_RX-	SATA_PHY_RX_N		28	RESET_MICO#		PWR Management
29	GND			30	VCC		
31	SATA1_TX-	SATA_PHY_TX_N		32	ETH1_MDI2+		KSZ9031 Pin 7
33	SATA1_TX+	SATA_PHY_TX_P		34	ETH1_MDI2-		KSZ9031 Pin 8
35	SATA1_ACT#	EIM_AD15		36	VCC		
37	WAKE1_MICO	GPIO04		38	ETH1_MDI3+		KSZ9031 Pin 10
39	GND			40	ETH1_MDI3-		KSZ9031 Pin 11
41	PCIE1_RX-	PCIE_RX_N		42	ETH1_ACT		KSZ9031 Pin17 (level shifted)
43	PCIE1_RX+	PCIE_RX_P		44	ETH1_LINK		KSZ9031 Pin15 (level shifted)
45	GND			46	ETH1_CTREF		NC
47	PCIE1_TX-	PCIE_TX_N		48	ETH1_MDI0-		KSZ9031 Pin 3
49	PCIE1_TX+	PCIE_TX_P		50	ETH1_MDI0+		KSZ9031 Pin 2
51	GND			52	VCC		
53	PCIE1_CLK-	CLK1_N		54	ETH1_MDI1-		KSZ9031 Pin6
55	PCIE1_CLK+	CLK1_P		56	ETH1_MDI1+		KSZ9031 Pin5
57	GND			58	VCC		

X1	Apalis Signal Name	iMX6 Ball Name	Notes
59	TS_DIFF1-	MLB_CLK_N	Type specific
61	TS_DIFF1+	MLB_CLK_P	Type specific
63	TS_1	BOOT_MODE0	Type specific
65	TS_DIFF2-	MLB_DATA_N	Type specific
67	TS_DIFF2+	MLB_DATA_P	Type specific
69	GND		
71	TS_DIFF3-	MLB_SIG_N	Type specific
73	TS_DIFF3+	MLB_SIG_P	Type specific
75	GND		
77	TS_DIFF4-	CSI0_DATA_EN	Type specific
79	TS_DIFF4+	NAND_CS0_B	Type specific
81	GND		
83	TS_DIFF5-	NAND_CLE	Type specific
85	TS_DIFF5+	SD4_CLK	Type specific
87	TS_2	BOOT_MODE1	Type specific
89	TS_DIFF6-	NAND_CS3_B	Type specific
91	TS_DIFF6+	NAND_ALE	Type specific
93	GND		
95	TS_DIFF7-	SD4_DATA0	Type specific
97	TS_DIFF7+		Type specific
99	TS_3	SD4_CMD	Type specific
101	TS_DIFF8-		Type specific
103	TS_DIFF8+	TAMPER	Type specific
105	GND		
107	TS_DIFF9-		USB2514 (8) USBDN4_DM
109	TS_DIFF9+		USB2514 (9) USBDN4_DP
111	GND		
113	TS_DIFF10-	DSI_DATA1_N	Type specific
115	TS_DIFF10+	DSI_DATA1_P	Type specific
117	GND		
119	TS_DIFF11-	DSI_DATA0_N	Type specific
121	TS_DIFF11+	DSI_DATA0_P	Type specific
123	TS_4	SD4_DATA3	Type Specific
125	TS_DIFF12-	DSI_CLK0_N	Type specific
127	TS_DIFF12+	DSI_CLK0_P	Type specific
129	GND		

X1	Apalis Signal Name	iMX6 Ball Name	Notes
60	USBO1_VBUS	USB_OTG_VBUS	
62	USBO1_SSRX+	nc	NC
64	USBO1_SSRX-	nc	NC
66	VCC		
68	USBO1_SSTX+	nc	NC
70	USBO1_SSTX-	nc	NC
72	USBO1_ID	ENET_RX_ER	
74	USBO1_D+	USB_OTG_DP	
76	USBO1_D-	USB_OTG_DN	
78	VCC		
80	USBH2_D+		USB2514 (2) USBDN1_DP
82	USBH2_D-		USB2514 (1) USBDN1_DM
84	USBH_EN	GPIO00	
86	USBH3_D+		USB2514 (4) USBDN2_DP
88	USBH3_D-		USB2514 (3) USBDN2_DM
90	VCC		
92	USBH4_SSRX-	nc	NC
94	USBH4_SSRX+	nc	NC
96	USBH_OC#	GPIO03	
98	USBH4_D+		USB2514 (7) USBDN3_DP
100	USBH4_D-		USB2514 (6) USBDN3_DM
102	VCC		
104	USBH4_SSTX-	nc	NC
106	USBH4_SSTX+	nc	NC
108	VCC		
110	UART1_DTR	EIM_DATA24	
112	UART1_TXD	CSI0_DATA11	
114	UART1_RTS	EIM_DATA20	
116	UART1_CTS	EIM_DATA19	
118	UART1_RXD	CSI0_DATA10	
120	UART1_DSR	EIM_DATA25	
122	UART1_RI	EIM_EB3	
124	UART1_DCD	EIM_DATA23	
126	UART2_TXD	SD4_DATA4	
128	UART2_RTS	SD4_DATA5	
130	UART2_CTS	SD4_DATA6	

X1	Apalis Signal Name	iMX6 Ball Name	Notes
131	TS_DIFF13-	CLK2_N	Type specific
133	TS_DIFF13+	CLK2_P	Type specific
135	TS_5	EIM_DATA29	Type Specific
137	TS_DIFF14-	CSI_DATA3_N	Type specific
139	TS_DIFF14+	CSI_DATA3_P	Type specific
141	GND		
143	TS_DIFF15-	CSI_DATA2_N	Type specific
145	TS_DIFF15+	CSI_DATA2_P	Type specific
147	GND		
149	TS_DIFF16-	CSI_DATA1_N	Type specific
151	TS_DIFF16+	CSI_DATA1_P	Type specific
153	GND		
155	TS_DIFF17-	CSI_DATA0_N	Type specific
157	TS_DIFF17+	CSI_DATA0_P	Type specific
159	TS_6	EIM_WAIT	Type Specific
161	TS_DIFF18-	CSI_CLK0_N	Type specific
163	TS_DIFF18+	CSI_CLK0_P	Type specific
165	GND		
173	CAM1_D7	CSI0_DATA19	
175	CAM1_D6	CSI0_DATA18	
177	CAM1_D5	CSI0_DATA17	
179	CAM1_D4	CSI0_DATA16	
181	CAM1_D3	CSI0_DATA15	
183	CAM1_D2	CSI0_DATA14	
185	CAM1_D1	CSI0_DATA13	
187	CAM1_D0	CSI0_DATA12	
189	GND		
191	CAM1_PCLK	CSI0_PIXCLK	
193	CAM1_MCLK	NAND_CS2_B	
195	CAM1_VSYNC	CSI0_VSYNC	
197	CAM1_HSYNC	CSI0_MCLK	
199	GND		
201	I2C3_SDA (CAM)	EIM_DATA18	

X1	Apalis Signal Name	iMX6 Ball Name	Notes
132	UART2_RXD	SD4_DATA7	
134	UART3_TXD	KEY_ROW0	
136	UART3_RXD	KEY_COL0	
138	UART4_TXD	KEY_ROW1	
140	UART4_RXD	KEY_COL1	
142	GND		
144	MMC1_D2	SD1_DATA2	
146	MMC1_D3	SD1_DATA3	
148	MMC1_D4	NAND_DATA00	
150	MMC1_CMD	SD1_CMD	
152	MMC1_D5	NAND_DATA01	
154	MMC1_CLK	SD1_CLK	
156	MMC1_D6	NAND_DATA02	
158	MMC1_D7	NAND_DATA03	
160	MMC1_D0	SD1_DATA0	
162	MMC1_D1	SD1_DATA1	
164	MMC1_CD#	DI0_PIN04	
174	VCC_BACKUP		
176	SD1_D2	SD2_DATA2	
178	SD1_D3	SD2_DATA3	
180	SD1_CMD	SD2_CMD	
182	GND		
184	SD1_CLK	SD2_CLK	
186	SD1_D0	SD2_DATA0	
188	SD1_D1	SD2_DATA1	
190	SD1_CD#	NAND_CS1_B	
192	GND		
194	DAP1_MCLK	GPIO19	
196	DAP1_D_OUT	DISP0_DATA17	
198	DAP1_RESET#	EIM_LBA	
200	DAP1_BIT_CLK	DISP0_DATA16	
202	DAP1_D_IN	DISP0_DATA19	

X1	Apalis Signal Name	iMX6 Ball Name	Notes
203	I2C3_SCL (CAM)	EIM_DATA17	
205	I2C2_SDA (DDC)	EIM_DATA16	
207	I2C2_SCL (DDC)	EIM_EB2	
209	I2C1_SDA	CSI0_DATA08	
211	I2C1_SCL	CSI0_DATA09	
213	GND		
215	SPDIF1_OUT	GPIO17	
217	SPDIF1_IN	GPIO16	
219	GND		
221	SPI1_CLK	CSI0_DATA04	
223	SPI1_MISO	CSI0_DATA06	
225	SPI1_MOSI	CSI0_DATA05	
227	SPI1_CS	CSI0_DATA07	
229	SPI2_MISO	EIM_OE	
231	SPI2_MOSI	EIM_CS1	
233	SPI2_CS	EIM_RW	
235	SPI2_CLK	EIM_CS0	
237	GND		
239	BKL1_PWM	EIM_AD14	
241	GND		
243	LCD1_PCLK	EIM_ADDR16	
245	LCD1_VSYNC	EIM_AD12	
247	LCD1_HSYNC	EIM_AD11	
249	LCD1_DE	EIM_AD10	
251	LCD1_R0	EIM_ADDR21	
253	LCD1_R1	EIM_ADDR22	
255	LCD1_R2	EIM_ADDR23	
257	LCD1_R3	EIM_ADDR24	
259	LCD1_R4	EIM_DATA31	
261	LCD1_R5	EIM_DATA30	
263	LCD1_R6	EIM_DATA26	
265	LCD1_R7	EIM_DATA27	
267	GND		
269	LCD1_G0	EIM_AD01	
271	LCD1_G1	EIM_AD00	
273	LCD1_G2	EIM_EB1	

X1	Apalis Signal Name	iMX6 Ball Name	Notes
204	DAP1_SYNC	DISP0_DATA18	
206	GND		
208	VGA1_R		VGA DAC
210	VGA1_G		VGA DAC
212	VGA1_B		VGA DAC
214	VGA1_HSYNC	DI0_PIN02	
216	VGA1_VSYNC	DI0_PIN03	
218	GND		
220	HDMI1_CEC	KEY_ROW2	
222	HDMI1_TXD2+	HDMI_TX_DATA2_P	
224	HDMI1_TXD2-	HDMI_TX_DATA2_N	
226	GND		
228	HDMI1_TXD1+	HDMI_TX_DATA1_P	
230	HDMI1_TXD1-	HDMI_TX_DATA1_N	
232	HDMI1_HPD	HDMI_TX_HPD	Level shifted
234	HDMI1_TXD0+	HDMI_TX_DATA0_P	
236	HDMI1_TXD0-	HDMI_TX_DATA0_N	
238	GND		
240	HDMI1_TXC+	HDMI_TX_CLK_P	
242	HDMI1_TXC-	HDMI_TX_CLK_N	
244	GND		
246	LVDS1_A_CLK-	LVDS0_CLK_N	
248	LVDS1_A_CLK+	LVDS0_CLK_P	
250	GND		
252	LVDS1_A_TX0-	LVDS0_DATA0_N	
254	LVDS1_A_TX0+	LVDS0_DATA0_P	
256	GND		
258	LVDS1_A_TX1-	LVDS0_DATA1_N	
260	LVDS1_A_TX1+	LVDS0_DATA1_P	
262	USBO1_OC#	EIM_DATA21	
264	LVDS1_A_TX2-	LVDS0_DATA2_N	
266	LVDS1_A_TX2+	LVDS0_DATA2_P	
268	GND		
270	LVDS1_A_TX3-	LVDS0_DATA3_N	
272	LVDS1_A_TX3+	LVDS0_DATA3_P	
274	USBO1_EN	EIM_DATA22	

X1	Apalis Signal Name	iMX6 Ball Name	Notes
275	LCD1_G3	EIM_EB0	
277	LCD1_G4	EIM_ADDR17	
279	LCD1_G5	EIM_ADDR18	
281	LCD1_G6	EIM_ADDR19	
283	LCD1_G7	EIM_ADDR20	
285	GND		
287	LCD1_B0	EIM_AD09	
289	LCD1_B1	EIM_AD08	
291	LCD1_B2	EIM_AD07	
293	LCD1_B3	EIM_AD06	
295	LCD1_B4	EIM_AD05	
297	LCD1_B5	EIM_AD04	
299	LCD1_B6	EIM_AD03	
301	LCD1_B7	EIM_AD02	
303	AGND		
305	AN1_ADC0		STMPE811 Pin 8
307	AN1_ADC1		STMPE811 Pin 9
309	AN1_ADC2		STMPE811 Pin 11
311	AN1_TSWIP_ADC 3		STMPE811 Pin 12
313	AGND		
315	AN1_TSPX		STMPE811 Pin 13
317	AN1_TSMX		STMPE811 Pin 16
319	AN1_TSPY		STMPE811 Pin 15
321	AN1_TSMY		STMPE811 Pin 1

X1	Apalis Signal Name	iMX6 Ball Name	Notes
276	LVDS1_B_CLK-	LVDS1_CLK_N	
278	LVDS1_B_CLK+	LVDS1_CLK_P	
280	GND		
282	LVDS1_B_TX0-	LVDS1_DATA0_N	
284	LVDS1_B_TX0+	LVDS1_DATA0_P	
286	BKL1_ON	EIM_AD13	
288	LVDS1_B_TX1-	LVDS1_DATA1_N	
290	LVDS1_B_TX1+	LVDS1_DATA1_P	
292	GND		
294	LVDS1_B_TX2-	LVDS1_DATA2_N	
296	LVDS1_B_TX2+	LVDS1_DATA2_P	
298	GND		
300	LVDS1_B_TX3-	LVDS1_DATA3_N	
302	LVDS1_B_TX3+	LVDS1_DATA3_P	
304	AGND		
306	AAP1_MICIN		SGTL5000 Pin 10
308	AGND		
310	AAP1_LIN_L		SGTL5000 Pin 9
312	AAP1_LIN_R		SGTL5000 Pin 8
314	AVCC		
316	AAP1_HP_L		SGTL5000 Pin 4
318	AAP1_HP_R		SGTL5000 Pin 1
320	AVCC		

4. I/O Pins

4.1 Function Multiplexing

The NXP®/Freescale i.MX6 SoC I/O pins can be configured in any of up to eight alternate functions. Most of the pins can also be used as “normal” GPIOs (General Purpose I/O, sometimes also referred to as Digital I/O). For example, the i.MX6 signal pin on the MXM3 finger pin 118 has the primary function UART1_TX_DATA (Apalis standard function UART1_RXD), but can also provide the following alternate functions: GPIO5_IO28 (GPIO), IPU1_CSI0_DATA10 (serial camera input), AUD3_RXC (digital audio interface), or ECSPI2_MISO (SPI interface).

The default setting for this pin is the primary function uart1.UART1_TX_DATA. It is strongly recommended to, whenever possible, use a pin for a function which is compatible with all Apalis modules. This guarantees the best compatibility with the standard software and with the other modules in the Apalis family.

Most of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behaviour.

In the table in chapter 4.4 you will find a list of all pins which have alternate functions. There you can find which alternate functions are available for each individual pin.

4.2 Pin Control

The alternate function of each pin can be changed independently. Every pin has a Pad Mux Register in which the following settings can be set (some settings might not be available on certain pins). The Register is called IOMUXC_SW_MUX_CTL_PAD_x where x is the name of the i.MX6 pin. More information about the available register settings can be found in the i.MX6 Reference Manual.

Table 4-1 Pad Mux Registor

Bit	Field	Description	Remarks
31-5	Reserved		
4	SION	0 Software Input On Field disabled 1 Software Input On Field enabled	Force the selected mux mode input path
3	Reserved		
2-0	MUX_MODE	000 Select mux mode: ALT0 mux port 001 Select mux mode: ALT1 mux port 010 Select mux mode: ALT2 mux port 011 Select mux mode: ALT3 mux port 100 Select mux mode: ALT4 mux port 101 Select mux mode: ALT5 mux port (GPIO) 110 Select mux mode: ALT6 mux port 111 Select mux mode: ALT7 mux port:	Check chapter 4.4 for the available alternate function of the pin

The pins have an additional register which allows configuration of pull up/down resistors, drive strength and other settings. The register is called IOMUXC_SW_PAD_CTL_PAD_x where x is the name of the i.MX6 pin. Some settings might not be available on certain pins. More information about the available register settings can be found in the i.MX6 Reference Manual.

Table 4-2 Pad Control Registor

Bit	Field	Description	Remarks
31-17	Reserved		
16	HYS	0 CMOS input 1 Schmitt trigger input	
15-14	PUS	00 100 kOhm Pull Down 01 47 kOhm Pull Up 10 100 kOhm Pull Up 11 22 kOhm Pull Up	
13	PUE	0 Keeper enable 1 Pull enable	Selection between keeper and pull up/down function
12	PKE	0 Pull/Keeper Disabled 1 Pull/Keeper Enabled	Enable keeper or pull up/down function
11	ODE	0 Output is CMOS 1 Output is open drain	
10-8	Reserved		
7-6	SPEED	00 Reserved 01 Low (50 MHz) 10 Medium (100 MHz) 11 High (200 MHz)	
5-3	DSE	000 output driver disabled (Hi Z) 001 240 Ohm 010 120 Ohm 011 80 Ohm 100 60 Ohm 101 48 Ohm 110 40 Ohm 111 34 Ohm	If possible decrease the drive strength by increasing the resistance in order to reduce EMC problems
2-1	Reserved		
0	SRE	0 Slow Slew Rate 1 Fast Slew Rate	Use slow slew rate if possible for reducing EMC problems

Input functions that are available at more than one physical pin require an additional input multiplexer. This multiplexer is configured by a register called IOMUXC_x _SELECT_INPUT where x is the name of the input function. More information about this register can be found in the NXP reference manual.

4.3 Pin Reset Status

After a reset, the pins can be in different modes. Most of them are configured as GPIO input with a 100k pull up resistor enabled. Please check the table in chapter 4.4 for the default alternate function after releasing the reset. For pins that are by default not configured as GPIO, please check the NXP reference manual for the corresponding default configuration state (input/output, enabled pull up resistors, etc.). As soon as the bootloader is executing, it is possible to reconfigure the pins and their states.

4.4 Functions List

Below is a list of all the i.MX6 pins which are available on the MXM3 connector. It shows the alternate functions that are available for each pin. The GPIO functionality is always defined as the ALT5 function. The alternate functions used to provide the primary interfaces to ensure best compatibility with other Apalis modules are highlighted.

Function Short Forms

AUD:	Synchronous Serial Interface for Audio (I2S and AC97)
CCM:	Clock Control Module
CE-ATA:	Consumer Electronics-Advanced Technology Attachment, specification for attaching mass storage drives over the MMC-interface
CSI:	Camera Sensor Interface
ECSPI:	Enhanced Configurable Serial Peripheral Interface Bus
EIM:	External Interface Module (External Memory Bus)
eMMC:	*Embedded MultiMediaCard, device down memory chip that uses the MMC interface*
ESAI:	Enhanced Serial Audio Interface
FLEXCAN:	Flexible Controller Area Network
GPIO:	General Purpose Input Output
HDMI:	High Definition Multimedia Interface
I2C:	Inter Integrated Circuit
IPU:	Image Processing Units
MIPI/CSI:	Mobile Industry Processor Interface / Camera Serial Interface
MMC:	MultiMediaCard
NAND:	Interface for NAND Flash
PWM:	Pulse Width Modulation output
SD:	Secure Digital Memory Card (related to SDHC, MMC, CE-ATA, eMMC)
SDHC:	Secure Digital High Capacity (SD cards with capacity from 4 to 32 GB)
SPDIF:	S/PDIF (Sony-Philips Digital Interface I/O)
UART:	Universal Asynchronous Receiver/Transmitter
USB:	Universal Serial Bus

X1 Pin	i.MX6 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Reset State
1	NAND_DATA04	NAND_DATA04	SD2_DATA4				GPIO2_IO04			ALT5
3	NAND_DATA05	NAND_DATA05	SD2_DATA5				GPIO2_IO05			ALT5
5	NAND_DATA06	NAND_DATA06	SD2_DATA6				GPIO2_IO06			ALT5
7	NAND_DATA07	NAND_DATA07	SD2_DATA7				GPIO2_IO07			ALT5
11	NAND_READY	NAND_READY	IPU2_DI0_PIN01				GPIO6_IO10			ALT5
13	NAND_WP_B	NAND_WP_B	IPU2_SISG5				GPIO6_IO09			ALT5
15	GPIO02	ESAI_TX_FS		KEY_ROW6			GPIO1_IO02	SD2_WP	MLB_DATA	ALT5
17	GPIO06	ESAI_TX_CLK		I2C3_SDA			GPIO1_IO06	SD2_LCTL	MLB_SIG	ALT5
35	EIM_AD15	EIM_AD15	IPU1_DI1_PIN01	IPU1_DI1_PIN04			GPIO3_IO15		SRC_BOOT_CFG15	ALT0
37	GPIO04	ESAI_TX_HF_CLK		KEY_COL7			GPIO1_IO04	SD2_CD_B		ALT5
77	CSI0_DATA_EN	IPU1_CSI0_DATA_EN	EIM_DATA00				GPIO5_IO20		ARM_TRACE_CLK	ALT5
79	NAND_CS0_B	NAND_CE0_B					GPIO6_IO11			ALT5
83	NAND_CLE	NAND_CLE	IPU2_SISG4				GPIO6_IO07			ALT5
85	SD4_CLK	SD4_CLK	NAND_WE_B	UART3_RX_DATA			GPIO7_IO10			ALT5
89	NAND_CS3_B	NAND_CE3_B	IPU1_SISG1	ESAI_TX1	EIM_ADDR26		GPIO6_IO16	IPU2_SISG1		ALT5
91	NAND_ALE	NAND_ALE	SD4_RESET				GPIO6_IO08			ALT5
95	SD4_DATA0		SD4_DATA0	NAND_DQS			GPIO2_IO08			ALT5
99	SD4_CMD	SD4_CMD	NAND_RE_B	UART3_TX_DATA			GPIO7_IO09			ALT5
123	SD4_DATA3		SD4_DATA3				GPIO2_IO11			ALT5
135	EIM_DATA29	EIM_DATA29	IPU1_DI1_PIN15	ECSPI4_SS0		UART2_RTS_B	GPIO3_IO29	IPU2_CSI1_VSYNC	IPU1_DI0_PIN14	ALT5
159	EIM_WAIT	EIM_WAIT	EIM_DTACK_B				GPIO5_IO00		SRC_BOOT_CFG25	ALT0
173	CSI0_DATA19	IPU1_CSI0_DATA19	EIM_DATA15		UART5_CTS_B		GPIO6_IO05			ALT5
175	CSI0_DATA18	IPU1_CSI0_DATA18	EIM_DATA14		UART5_RTS_B		GPIO6_IO04		ARM_TRACE15	ALT5
177	CSI0_DATA17	IPU1_CSI0_DATA17	EIM_DATA13		UART4_CTS_B		GPIO6_IO03		ARM_TRACE14	ALT5
179	CSI0_DATA16	IPU1_CSI0_DATA16	EIM_DATA12		UART4_RTS_B		GPIO6_IO02		ARM_TRACE13	ALT5
181	CSI0_DATA15	IPU1_CSI0_DATA15	EIM_DATA11		UART5_RX_DATA		GPIO6_IO01		ARM_TRACE12	ALT5
183	CSI0_DATA14	IPU1_CSI0_DATA14	EIM_DATA10		UART5_TX_DATA		GPIO6_IO00		ARM_TRACE11	ALT5
185	CSI0_DATA13	IPU1_CSI0_DATA13	EIM_DATA09		UART4_RX_DATA		GPIO5_IO31		ARM_TRACE10	ALT5
187	CSI0_DATA12	IPU1_CSI0_DATA12	EIM_DATA08		UART4_TX_DATA		GPIO5_IO30		ARM_TRACE09	ALT5
191	CSI0_PIXCLK	IPU1_CSI0_PIXCLK					GPIO5_IO18		ARM_EVENTO	ALT5
193	NAND_CS2_B	NAND_CE2_B	IPU1_SISG0	ESAI_TX0	EIM_CRE	CCM_CLKO2	GPIO6_IO15	IPU2_SISG0		ALT5
195	CSI0_VSYNC	IPU1_CSI0_VSYNC	EIM_DATA01				GPIO5_IO21		ARM_TRACE00	ALT5
197	CSI0_MCLK	IPU1_CSI0_HSYNC			CCM_CLKO1		GPIO5_IO19		ARM_TRACE_CTL	ALT5
201	EIM_DATA18	EIM_DATA18	ECSPI1_MOSI	IPU1_DI0_PIN07	IPU2_CSI1_DATA17	IPU1_DI1_D0_CS	GPIO3_IO18	I2C3_SDA		ALT5
203	EIM_DATA17	EIM_DATA17	ECSPI1_MISO	IPU1_DI0_PIN06	IPU2_CSI1_PIXCLK	DCIC1_OUT	GPIO3_IO17	I2C3_SCL		ALT5
205	EIM_DATA16	EIM_DATA16	ECSPI1_SCLK	IPU1_DI0_PIN05	IPU2_CSI1_DATA18	HDMI_TX_DDC_SDA	GPIO3_IO16	I2C2_SDA		ALT5
207	EIM_EB2	EIM_EB2	ECSPI1_SS0		IPU2_CSI1_DATA19	HDMI_TX_DDC_SCL	GPIO2_IO30	I2C2_SCL	SRC_BOOT_CFG30	ALT5
209	CSI0_DATA08	IPU1_CSI0_DATA08	EIM_DATA06	ECSPI2_SCLK	KEY_COL7	I2C1_SDA	GPIO5_IO26		ARM_TRACE05	ALT5
211	CSI0_DATA09	IPU1_CSI0_DATA09	EIM_DATA07	ECSPI2_MOSI	KEY_ROW7	I2C1_SCL	GPIO5_IO27		ARM_TRACE06	ALT5
215	GPIO17	ESAI_TX0	ENET_1588_EVENT3_IN	CCM_PMIC_READY	SDMA_EXT_EVENT0	SPDIF_OUT	GPIO7_IO12			ALT5
217	GPIO16	ESAI_TX3_RX2	ENET_1588_EVENT2_IN	ENET_REF_CLK	SD1_LCTL	SPDIF_IN	GPIO7_IO11	I2C3_SDA	JTAG_DE_B	ALT5
221	CSI0_DATA04	IPU1_CSI0_DATA04	EIM_DATA02	ECSPI1_SCLK	KEY_COL5	AUD3_TXC	GPIO5_IO22		ARM_TRACE01	ALT5
223	CSI0_DATA06	IPU1_CSI0_DATA06	EIM_DATA04	ECSPI1_MISO	KEY_COL6	AUD3_TXFS	GPIO5_IO24		ARM_TRACE03	ALT5
225	CSI0_DATA05	IPU1_CSI0_DATA05	EIM_DATA03	ECSPI1_MOSI	KEY_ROW5	AUD3_TXD	GPIO5_IO23		ARM_TRACE02	ALT5

X1 Pin	i.MX6 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Reset State
227	CSI0_DATA07	IPU1_CSI0_DATA07	EIM_DATA05	ECSPI1_SS0	KEY_ROW6	AUD3_RXD	GPIO5_IO25		ARM_TRACE04	ALT5
229	EIM_OE	EIM_OE	IPU1_DI1_PIN07	ECSPI2_MISO			GPIO2_IO25			ALT0
231	EIM_CS1	EIM_CS1	IPU1_DI1_PIN06	ECSPI2_MOSI			GPIO2_IO24			ALT0
233	EIM_RW	EIM_RW	IPU1_DI1_PIN08	ECSPI2_SS0			GPIO2_IO26		SRC_BOOT_CFG29	ALT0
235	EIM_CS0	EIM_CS0	IPU1_DI1_PIN05	ECSPI2_SCLK			GPIO2_IO23			ALT0
239	EIM_AD14	EIM_AD14	IPU1_DI1_D1_CS				GPIO3_IO14		SRC_BOOT_CFG14	ALT0
243	EIM_ADDR16	EIM_ADDR16	IPU1_DI1_DISP_CLK	IPU2_CSI1_PIXCLK			GPIO2_IO22		SRC_BOOT_CFG16	ALT0
245	EIM_AD12	EIM_AD12	IPU1_DI1_PIN03	IPU2_CSI1_VSYNC			GPIO3_IO12		SRC_BOOT_CFG12	ALT0
247	EIM_AD11	EIM_AD11	IPU1_DI1_PIN02	IPU2_CSI1_HSYNC			GPIO3_IO11		SRC_BOOT_CFG11	ALT0
249	EIM_AD10	EIM_AD10	IPU1_DI1_PIN15	IPU2_CSI1_DATA_EN			GPIO3_IO10		SRC_BOOT_CFG10	ALT0
251	EIM_ADDR21	EIM_ADDR21	IPU1_DISP1_DATA16	IPU2_CSI1_DATA16			GPIO2_IO17		SRC_BOOT_CFG21	ALT0
253	EIM_ADDR22	EIM_ADDR22	IPU1_DISP1_DATA17	IPU2_CSI1_DATA17			GPIO2_IO16		SRC_BOOT_CFG22	ALT0
255	EIM_ADDR23	EIM_ADDR23	IPU1_DISP1_DATA18	IPU2_CSI1_DATA18	IPU2_SISG3	IPU1_SISG3	GPIO6_IO06		SRC_BOOT_CFG23	ALT0
257	EIM_ADDR24	EIM_ADDR24	IPU1_DISP1_DATA19	IPU2_CSI1_DATA19	IPU2_SISG2	IPU1_SISG2	GPIO5_IO04		SRC_BOOT_CFG24	ALT0
259	EIM_DATA31	EIM_DATA31	IPU1_DISP1_DATA20	IPU1_DI0_PIN12	IPU1_CSI0_DATA02	UART3_RTS_B	GPIO3_IO31	USB_H1_PWR		ALT5
261	EIM_DATA30	EIM_DATA30	IPU1_DISP1_DATA21	IPU1_DI0_PIN11	IPU1_CSI0_DATA03	UART3_CTS_B	GPIO3_IO30	USB_H1_OC		ALT5
263	EIM_DATA26	EIM_DATA26	IPU1_DI1_PIN11	IPU1_CSI0_DATA01	IPU2_CSI1_DATA14	UART2_TX_DATA	GPIO3_IO26	IPU1_SISG2	IPU1_DISP1_DATA22	ALT5
265	EIM_DATA27	EIM_DATA27	IPU1_DI1_PIN13	IPU1_CSI0_DATA00	IPU2_CSI1_DATA13	UART2_RX_DATA	GPIO3_IO27	IPU1_SISG3	IPU1_DISP1_DATA23	ALT5
269	EIM_AD01	EIM_AD01	IPU1_DISP1_DATA08	IPU2_CSI1_DATA08			GPIO3_IO01		SRC_BOOT_CFG01	ALT0
271	EIM_AD00	EIM_AD00	IPU1_DISP1_DATA09	IPU2_CSI1_DATA09			GPIO3_IO00		SRC_BOOT_CFG00	ALT0
273	EIM_EB1	EIM_EB1	IPU1_DISP1_DATA10	IPU2_CSI1_DATA10			GPIO2_IO29		SRC_BOOT_CFG28	ALT0
275	EIM_EB0	EIM_EB0	IPU1_DISP1_DATA11	IPU2_CSI1_DATA11		CCM_PMIC_READY	GPIO2_IO28		SRC_BOOT_CFG27	ALT0
277	EIM_ADDR17	EIM_ADDR17	IPU1_DISP1_DATA12	IPU2_CSI1_DATA12			GPIO2_IO21		SRC_BOOT_CFG17	ALT0
279	EIM_ADDR18	EIM_ADDR18	IPU1_DISP1_DATA13	IPU2_CSI1_DATA13			GPIO2_IO20		SRC_BOOT_CFG18	ALT0
281	EIM_ADDR19	EIM_ADDR19	IPU1_DISP1_DATA14	IPU2_CSI1_DATA14			GPIO2_IO19		SRC_BOOT_CFG19	ALT0
283	EIM_ADDR20	EIM_ADDR20	IPU1_DISP1_DATA15	IPU2_CSI1_DATA15			GPIO2_IO18		SRC_BOOT_CFG20	ALT0
287	EIM_AD09	EIM_AD09	IPU1_DISP1_DATA00	IPU2_CSI1_DATA00			GPIO3_IO09		SRC_BOOT_CFG09	ALT0
289	EIM_AD08	EIM_AD08	IPU1_DISP1_DATA01	IPU2_CSI1_DATA01			GPIO3_IO08		SRC_BOOT_CFG08	ALT0

X1 Pin	i.MX6 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Reset State
291	EIM_AD07	EIM_AD07	IPU1_DISP1_DATA02	IPU2_CSI1_DATA02			GPIO3_IO07		SRC_BOOT_CFG07	ALT0
293	EIM_AD06	EIM_AD06	IPU1_DISP1_DATA03	IPU2_CSI1_DATA03			GPIO3_IO06		SRC_BOOT_CFG06	ALT0
295	EIM_AD05	EIM_AD05	IPU1_DISP1_DATA04	IPU2_CSI1_DATA04			GPIO3_IO05		SRC_BOOT_CFG05	ALT0
297	EIM_AD04	EIM_AD04	IPU1_DISP1_DATA05	IPU2_CSI1_DATA05			GPIO3_IO04		SRC_BOOT_CFG04	ALT0
299	EIM_AD03	EIM_AD03	IPU1_DISP1_DATA06	IPU2_CSI1_DATA06			GPIO3_IO03		SRC_BOOT_CFG03	ALT0
301	EIM_AD02	EIM_AD02	IPU1_DISP1_DATA07	IPU2_CSI1_DATA07			GPIO3_IO02		SRC_BOOT_CFG02	ALT0
2	GPIO09	ESAI_RX_FS	WDOG1_B	KEY_COL6	CCM_REF_EN_B	PWM1_OUT	GPIO1_IO09	SD1_WP		ALT5
4	GPIO01	ESAI_RX_CLK	WDOG2_B	KEY_ROW5	USB_OTG_ID	PWM2_OUT	GPIO1_IO01	SD1_CD_B		ALT5
6	SD4_DATA1		SD4_DATA1	PWM3_OUT			GPIO2_IO09			ALT5
8	SD4_DATA2		SD4_DATA2	PWM4_OUT			GPIO2_IO10			ALT5
12	GPIO08	ESAI_TX5_RX0	XTALOSC_REF_CLK_32K	EPIT2_OUT	FLEXCAN1_RX	UART2_RX_DATA	GPIO1_IO08	SPDIF_SR_CLK	USB_OTG_PWR_CTL_WAKE	ALT5
14	GPIO07	ESAI_TX4_RX1	ECSPI5_RDY	EPIT1_OUT	FLEXCAN1_TX	UART2_TX_DATA	GPIO1_IO07	SPDIF_LOCK	USB_OTG_HOST_MODE	ALT5
16	KEY_ROW4	FLEXCAN2_RX	IPU1_SISG5	USB_OTG_PWR	KEY_ROW4	UART5_CTS_B	GPIO4_IO15			ALT5
18	KEY_COL4	FLEXCAN2_TX	IPU1_SISG4	USB_OTG_OC	KEY_COL4	UART5_RTS_B	GPIO4_IO14			ALT5
72	ENET_RX_ER	USB_OTG_ID	ENET_RX_ER	ESAI_RX_HF_CLK	SPDIF_IN	ENET_1588_EVENT2_OUT	GPIO1_IO24			ALT5
84	GPIO00	CCM_CLKO1		KEY_COL5	ASRC_EXT_CLK	EPIT1_OUT	GPIO1_IO00	USB_H1_PWR	SNVS_VIO_5	ALT5
96	GPIO03	ESAI_RX_HF_CLK		I2C3_SCL	XTALOSC_REF_CLK_24M	CCM_CLKO2	GPIO1_IO03	USB_H1_OC	MLB_CLK	ALT5
112	CSI0_DATA11	IPU1_CSI0_DATA11	AUD3_RXFS	ECSPI2_SS0	UART1_RX_DATA (1)		GPIO5_IO29		ARM_TRACE08	ALT5
110	EIM_DATA24	EIM_DATA24	ECSPI4_SS2	UART3_TX_DATA	ECSPI1_SS2	ECSPI2_SS2	GPIO3_IO24	AUD5_RXFS	UART1_DTR_B	ALT5
114	EIM_DATA20	EIM_DATA20	ECSPI4_SS0	IPU1_DI0_PIN16	IPU2_CSI1_DATA15	UART1_RTS_B	GPIO3_IO20	EPIT2_OUT		ALT5
116	EIM_DATA19	EIM_DATA19	ECSPI1_SS1	IPU1_DI0_PIN08	IPU2_CSI1_DATA16	UART1_CTS_B	GPIO3_IO19	EPIT1_OUT		ALT5
118	CSI0_DATA10	IPU1_CSI0_DATA10	AUD3_RXC	ECSPI2_MISO	UART1_TX_DATA (1)		GPIO5_IO28		ARM_TRACE07	ALT5
120	EIM_DATA25	EIM_DATA25	ECSPI4_SS3	UART3_RX_DATA	ECSPI1_SS3	ECSPI2_SS3	GPIO3_IO25	AUD5_RXC	UART1_DSR_B	ALT5
122	EIM_EB3	EIM_EB3	ECSPI4_RDY	UART3_RTS_B	UART1_RI_B	IPU2_CSI1_HSYNC	GPIO2_IO31	IPU1_DI1_PIN03	SRC_BOOT_CFG31	ALT5
124	EIM_DATA23	EIM_DATA23	IPU1_DI0_D0_CS	UART3_CTS_B	UART1_DCD_B	IPU2_CSI1_DATA_EN	GPIO3_IO23	IPU1_DI1_PIN02	IPU1_DI1_PIN14	ALT5
126	SD4_DATA4		SD4_DATA4	UART2_RX_DATA (1)			GPIO2_IO12			ALT5
128	SD4_DATA5		SD4_DATA5	UART2_RTS_B			GPIO2_IO13			ALT5
130	SD4_DATA6		SD4_DATA6	UART2_CTS_B			GPIO2_IO14			ALT5
132	SD4_DATA7		SD4_DATA7	UART2_TX_DATA (1)			GPIO2_IO15			ALT5
134	KEY_ROW0	ECSPI1_MOSI	ENET_TX_DATA3	AUD5_TXD	KEY_ROW0	UART4_RX_DATA (1)	GPIO4_IO07	DCIC2_OUT		ALT5
136	KEY_COL0	ECSPI1_SCLK	ENET_RX_DATA3	AUD5_TXC	KEY_COL0	UART4_TX_DATA (1)	GPIO4_IO06	DCIC1_OUT		ALT5
138	KEY_ROW1	ECSPI1_SS0	ENET_COL	AUD5_RXD	KEY_ROW1	UART5_RX_DATA (1)	GPIO4_IO09	SD2_VSELECT		ALT5
140	KEY_COL1	ECSPI1_MISO	ENET_MDIO	AUD5_TXFS	KEY_COL1	UART5_TX_DATA (1)	GPIO4_IO08	SD1_VSELECT		ALT5
144	SD1_DATA2	SD1_DATA2	ECSPI5_SS1	GPT_COMPARE2	PWM2_OUT	WDOG1_B	GPIO1_IO19	WDOG1_RESET_B_DEB		ALT5
146	SD1_DATA3	SD1_DATA3	ECSPI5_SS2	GPT_COMPARE3	PWM1_OUT	WDOG2_B	GPIO1_IO21	WDOG2_RESET_B_DEB		ALT5
148	NAND_DATA00	NAND_DATA00	SD1_DATA4				GPIO2_IO00			ALT5

X1 Pin	i.MX6 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Reset State
150	SD1_CMD	SD1_CMD	ECSPI5_MOSI	PWM4_OUT	GPT_COMPARE1		GPIO1_IO18			ALT5
152	NAND_DATA01	NAND_DATA01	SD1_DATA5				GPIO2_IO01			ALT5
154	SD1_CLK	SD1_CLK	ECSPI5_SCLK		GPT_CLKIN		GPIO1_IO20			ALT5
156	NAND_DATA02	NAND_DATA02	SD1_DATA6				GPIO2_IO02			ALT5
158	NAND_DATA03	NAND_DATA03	SD1_DATA7				GPIO2_IO03			ALT5
160	SD1_DATA0	SD1_DATA0	ECSPI5_MISO		GPT_CAPTURE1		GPIO1_IO16			ALT5
162	SD1_DATA1	SD1_DATA1	ECSPI5_SS0	PWM3_OUT	GPT_CAPTURE2		GPIO1_IO17			ALT5
164	DI0_PIN04	IPU1_DI0_PIN04	IPU2_DI0_PIN04	AUD6_RXD	SD1_WP		GPIO4_IO20			ALT5
176	SD2_DATA2	SD2_DATA2	ECSPI5_SS1	EIM_CS3	AUD4_TXD	KEY_ROW6	GPIO1_IO13			ALT5
178	SD2_DATA3	SD2_DATA3	ECSPI5_SS3	KEY_COL6	AUD4_TXC		GPIO1_IO12			ALT5
180	SD2_CMD	SD2_CMD	ECSPI5_MOSI	KEY_ROW5	AUD4_RXC		GPIO1_IO11			ALT5
184	SD2_CLK	SD2_CLK	ECSPI5_SCLK	KEY_COL5	AUD4_RXFS		GPIO1_IO10			ALT5
186	SD2_DATA0	SD2_DATA0	ECSPI5_MISO		AUD4_RXD	KEY_ROW7	GPIO1_IO15	DCIC2_OUT		ALT5
188	SD2_DATA1	SD2_DATA1	ECSPI5_SS0	EIM_CS2	AUD4_TXFS	KEY_COL7	GPIO1_IO14			ALT5
190	NAND_CS1_B	NAND_CE1_B	SD4_VSELECT	SD3_VSELECT			GPIO6_IO14			ALT5
194	GPIO19	KEY_COL5	ENET_1588_EVENT0_OUT	SPDIF_OUT	CCM_CLKO1	ECSPI1_RDY	GPIO4_IO05	ENET_TX_ER		ALT5
196	DISP0_DATA17	IPU1_DISP0_DATA17	IPU2_DISP0_DATA17	ECSPI2_MISO	AUD5_TXD	SDMA_EXT_EVENT1	GPIO5_IO11			ALT5
198	EIM_LBA	EIM_LBA	IPU1_DI1_PIN17	ECSPI2_SS1			GPIO2_IO27		SRC_BOOT_CFG26	ALT0
200	DISP0_DATA16	IPU1_DISP0_DATA16	IPU2_DISP0_DATA16	ECSPI2_MOSI	AUD5_TXC	SDMA_EXT_EVENT0	GPIO5_IO10			ALT5
202	DISP0_DATA19	IPU1_DISP0_DATA19	IPU2_DISP0_DATA19	ECSPI2_SCLK	AUD5_RXD	AUD4_RXC	GPIO5_IO13		EIM_CS3	ALT5
204	DISP0_DATA18	IPU1_DISP0_DATA18	IPU2_DISP0_DATA18	ECSPI2_SS0	AUD5_TXFS	AUD4_RXFS	GPIO5_IO12		EIM_CS2	ALT5
214	DI0_PIN02	IPU1_DI0_PIN02	IPU2_DI0_PIN02	AUD6_TXD			GPIO4_IO18			ALT5
216	DI0_PIN03	IPU1_DI0_PIN03	IPU2_DI0_PIN03	AUD6_TXFS			GPIO4_IO19			ALT5
220	KEY_ROW2	ECSPI1_SS2	ENET_TX_DATA2	FLEXCAN1_RX	KEY_ROW2	SD2_VSELECT	GPIO4_IO11	HDMI_TX_CEC_LINE		ALT5
262	EIM_DATA21	EIM_DATA21	ECSPI4_SCLK	IPU1_DI0_PIN17	IPU2_CSI1_DATA11	USB_OTG_OC	GPIO3_IO21	I2C1_SCL	SPDIF_IN	ALT5
274	EIM_DATA22	EIM_DATA22	ECSPI4_MISO	IPU1_DI0_PIN01	IPU2_CSI1_DATA10	USB_OTG_PWR	GPIO3_IO22	SPDIF_OUT		ALT5
286	EIM_AD13	EIM_AD13	IPU1_DI1_D0_CS				GPIO3_IO13		SRC_BOOT_CFG13	ALT0

Note:
(1) By default, the UARTS of the i.MX 6 are configured in DTE (Data Terminal Equipment) mode. In DTE mode, the UARTx_RX_DATA is transmitting the signals from the SoC (i.e. UARTx_TXD on the Apalis iMX6 module) and the UARTx_TX_DATA is receiving the signals from the SoC (i.e. UARTx_RXD on the Apalis iMX6 module). For more details, please refer to the Section 5.9, UART.

5. Interface Description

5.1 Power Signals

5.1.1 Digital Supply

Table 5-1 Digital Supply Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
10, 30, 36, 52, 58, 66, 78, 90, 102, 108	VCC	I	3.3V main power supply	Use decoupling capacitors on all pins.
9, 23, 29, 39, 45, 51, 57, 69, 75, 81, 93, 105, 111, 117, 129, 141, 147, 153, 165, 189, 199, 213, 219, 237, 241, 267, 285, 142, 182, 192, 206, 218, 226, 238, 244, 250, 256, 268, 280, 292, 298	GND	I	Digital Ground	
174	VCC_BACKUP	I/O	RTC Power supply can be connected to a backup battery.	Can be left unconnected if the internal RTC is not used.

5.1.2 Analogue Supply

Table 5-2 Analogue Supply Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
314, 320	AVCC	I	3.3V Analogue supply	Connect this pin to a 3.3V supply. For better Audio accuracy we recommend filtering this supply separately from the digital supply. This pin is only connected to the Audio Codec. If audio is not used, connect these pins to the VCC 3.3V input supply.
303, 313, 304, 308	AGND	I	Analogue Ground	Connect this pin to GND. For better Audio accuracy we recommend filtering this supply separate from the digital supply. Internally this pin is connected with Digital GND on the Apalis iMX6.

5.1.3 Power Management Signals

Table 5-3 Power Management Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Remarks
28	RESET_MICO#	I	Reset Input	This pin is low active and resets the Apalis module. This pin is connected to the power manger IC. There is a 100k pull up resistor on the module.
26	RESET_MOCI#	O	Reset Output	This reset signal is generated from the on module reset signal (see Figure 5). This is a CMOS output signal.
24	POWER_ENABLE_MOCI	O	Signal for the carrier board to enable the peripheral voltage rails	More information about the required power management on the carrier board can be found in the Apalis Carrier Board Design Guide

The RESET_MOCI# reset output for the peripherals on the carrier board is generated from the general module reset signal. This reset signal is provided by the power manager IC (RESETBMCU output) and is used for resetting the i.MX6 SoC as well as other on module peripherals. In order to meet the reset timing requirements of PCI Express, the external reset output RESET_MOCI# needs to be delayed. Figure 5 shows the circuit that is used for delaying the RESET_MOCI# signal. The transistor holds down the external reset signal until the bootloader is releasing the signal by driving the GPIO1_IO28 (ball ENET_TX_EN) low.

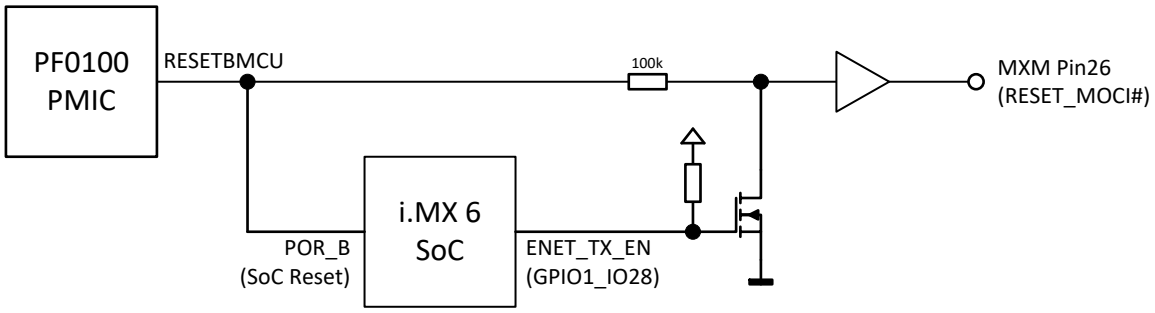


Figure 5 RESET_MOCI# circuit

5.2 GPIOs

Most of the pins have a GPIO (General Purpose Input/Output) function. All GPIO pins can be used as interrupt source.

5.2.1 Wakeup Source

In principle, all GPIOs can be used to wake up the Apalis module from a suspend state. In the Apalis module standard, Pin 37 is the default wakeup source. Only this pin is guaranteed to be wakeup compatible with other Apalis modules. Please use only this pin to wake up the module if the carrier board needs to be compatible with other Apalis modules.

The touch pen down interrupt signal from the touch controller is connected to the GPIO4_IO10 (KEY_COL2 ball) and can therefore also be used to wake up the system. The wake signal of the Ethernet PHY is connected to GPIO1_IO30 (ENET_TXD0 pad).

5.3 Ethernet

The Apalis Module features a 10/100/1000 Mbit Ethernet interface. The MAC is integrated in the i.MX 6 SoC and connected to a separate PHY located on the module, therefore only the magnetics are required on the carrier board. The Micrel KSZ9031 Gigabit Ethernet Transceiver chip is connected via RGMII to the NXP i.MX 6.

The Gigabit Ethernet MAC in the SoC features an accurate IEEE 1588 compliant timer for clock synchronization for clock synchronisation used in industrial automation applications. The clock that is used for the IEEE 1588 is routed internally trough the i.MX 6 ball GPIO16. If the IEEE 1588 function is used, the GIPO16 ball needs to be left unconnected. The GPIO16 ball is connected to the MXM3 pin 217 (SPDIF1_IN). This means, that the SPDIF IN signal cannot be used on the dedicated module edge pin if the IEEE 1588 is in use.

Table 5-4 Ethernet Pins

X1 Pin #	Apalis Signal Name	KSZ9031 Signal Name	I/O	Description	Remarks
50	ETH1_MDI0+	TXRXP_A	I/O	Media Dependent Interface	100BASE-TX: Transmit +
48	ETH1_MDI0-	TXRXM_A	I/O	Media Dependent Interface	100BASE-TX: Transmit -
56	ETH1_MDI1+	TXRXP_B	I/O	Media Dependent Interface	100BASE-TX: Receive +
54	ETH1_MDI1-	TXRXM_B	I/O	Media Dependent Interface	100BASE-TX: Receive -
32	ETH1_MDI2+	TXRXP_C	I/O	Media Dependent Interface	100BASE-TX: Unused
34	ETH1_MDI2-	TXRXM_C	I/O	Media Dependent Interface	100BASE-TX: Unused
38	ETH1_MDI3+	TXRXP_D	I/O	Media Dependent Interface	100BASE-TX: Unused
40	ETH1_MDI3-	TXRXM_D	I/O	Media Dependent Interface	100BASE-TX: Unused
46	ETH+_CTREF	NC	O	Centre tap supply	KSZ9031 does not need centre tap supply
42	ETH1_ACT	LED1	O	LED indication output	Toggles during RX/TX activity
44	ETH1_LINK	LED2	O	LED indication output	Is low if a link (any speed) is established

The Micrel KSZ9031 does not require a centre tap supply on the magnetics. Nevertheless, follow the Apalis Carrier Board Design Guide and connect the centre tap of the magnetics to pin 46 of the Apalis module. This guarantees the full compatibility with other Apalis modules which require a centre tap supply.

If only fast Ethernet is required, 10/100Mbit magnetics with only 2 lanes are sufficient. In this case, MDI2 and MDI3 can be left unconnected. Please follow the carrier board design guide.

5.4 USB

The Apalis module form factor features up to four USB interfaces, two USB 3.0 Super Speed (backward compatible) and two USB 2.0 High Speed interfaces. The NXP i.MX 6 features only two USB 2.0 High Speed (480 Mbit) interfaces with integrated physical layer. Therefore, the Apalis iMX6 module features an additional 4 port USB 2.0 Hub. The USB_OTG port of the SoC is directly available on the USBO1 interface of the module connector. USBO1 can also be used for the USB recovery mode. See the section 6 “Recovery Mode” for more information.

The SMSC USB2514 USB hub is connected to the USB_H1 port of the iMX6 SoC. Three USB hub ports are available at the USBH2, USBH3 and USBH4 interface of the module connector. Additionally, the fourth port is available in the type specific section of the module connector. This fourth port is not guaranteed to be compatible with other Apalis modules.

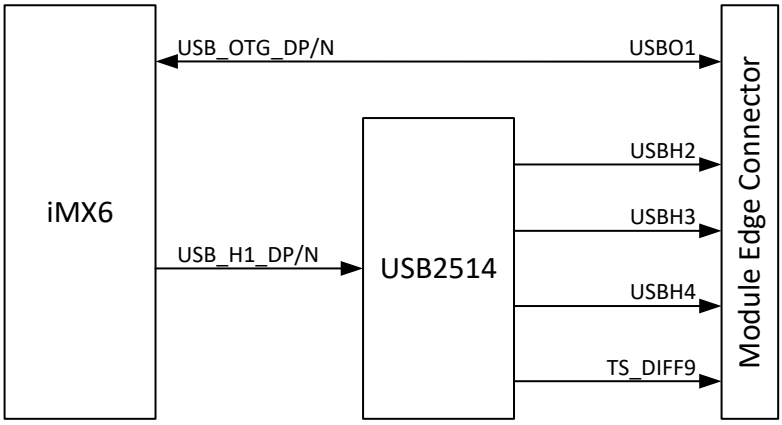


Figure 6: USB Block Diagram

5.4.1 USB Data Signal

Table 5-5 USBO1 Data Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
74	USBO1_D+	USB_OTG_DP	I/O	Positive Differential USB Signal, OTG capable
76	USBO1_D-	USB_OTG_DN	I/O	Negative Differential USB Signal, OTG capable
62	USBO1_SSRX+	NC	I	Not connected
64	USBO1_SSRX-	NC	I	Not connected
68	USBO1_SSTX+	NC	O	Not connected
70	USBO1_SSTX-	NC	O	Not connected

Table 5-6 USBH2 Data Pins

X1 Pin#	Apalis Signal Name	USB2514 Ball Name	I/O	Description
80	USBH2_D+	USBDM_DN1	I/O	Positive Differential USB Signal
82	USBH2_D-	USBDN_DN1	I/O	Negative Differential USB Signal

Table 5-7 USBH3 Data Pins

X1 Pin#	Apalis Signal Name	USB2514 Ball Name	I/O	Description
86	USBH3_D+	USBDM_DN2	I/O	Positive Differential USB Signal
88	USBH3_D-	USBDN_DN2	I/O	Negative Differential USB Signal

Table 5-8 USBH4 Data Pins

X1 Pin#	Apalis Signal Name	USB2514 Ball Name	I/O	Description
98	USBH4_D+	USBDM_DN3	I/O	Positive Differential USB Signal
100	USBH4_D-	USBDN_DN3	I/O	Negative Differential USB Signal
94	USBH4_SSRX+	NC	I	Not connected
92	USBH4_SSRX-	NC	I	Not connected
106	USBH4_SSTX+	NC	O	Not connected
104	USBH4_SSTX-	NC	O	Not connected

Table 5-9 Type Specific USB Data Pins

X1 Pin#	Apalis Signal Name	USB2514 Ball Name	I/O	Description
109	TS_DIFF9+	USBDM_DN4	I/O	Positive Differential USB Signal
107	TS_DIFF9-	USBDN_DN4	I/O	Negative Differential USB Signal

5.4.2 USB Control Signals

Table 5-10 USB OTG Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
72	USBO1_ID	ENET_RX_ER	I	Use this pin to detect the ID pin if you use USB OTG. This pin features a level shifter on the module. Therefore, it can only be used as USBO1_ID. None of the alternate functions for this pin are available.
60	USBO1_VBUS	USB_OTG_VBUS	I	Use this pin to detect if VBUS is present (5V USB supply). This pin is 5V tolerant and can be connected directly to the USB supply.

If you use the USB Host function, you need to provide the 5V USB supply voltage on your carrier board for the interfaces. The Apalis iMX6 provides additional signals for controlling the USB supply. We recommend using the following pins to guarantee the best possible compatibility. However, if required you can use other GPIOs or not use them at all. The USBH2, USBH3, and USBH4 interfaces share the bus power control signals whereas USBO1 has its own dedicated control signals.

Table 5-11 USB Power Control Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
274	USBO1_EN	EIM_DATA22	O	This pin enables the external USB voltage supply for the USBO1 interface
262	USBO1_OC#	EIM_DATA21	I	USB overcurrent, this pin can signal an over current condition in the USB supply of the USBO1 interface
84	USBH_EN	GPIO00	O	This pin enables the external USB voltage supply for the USBH2, USBH3, and USBH4 interfaces
96	USBH_OC#	GPIO03	I	USB overcurrent, this pin can signal an over current condition in the USB supply of the USBH2, USBH3, and USBH4 interfaces

5.5 Display

The Apalis iMX6 features up to two independent (identical) Image Processing Units (IPUs). These units provide the connectivity to cameras and displays, related processing synchronization and control. The output of the IPUs can be routed individually to each of the display output interfaces such as the parallel LCD, HDMI, VGA, LVDS (up to two displays), and DSI. Each IPU has 2 display ports (not to be confused with the DisplayPort standard). This means up to four external display output ports can be active at any given time.

Features of the Video Graphics Sub System include:
- Video Processing Unit (multi-standard video encoder/decoder)
- 3D GPU
- 2D GPU
- OpenVG acceleration
- Fully programmable display timing and resolution

5.5.1 Parallel RGB LCD interface

The Apalis iMX6 provides a parallel LCD interface on the MXM3 connector. It supports up to 24-bit colour per pixel. The 24bit colour mapping is guaranteed to be compatible with other Apalis modules. R7, G7 and B7 are the most significant bits (MSBs) and R0, G0 and B0 are the least significant bits (LSBs) for the respective colours. To ensure compatibility between modules, the display interface should always be used in 24-bit mode. To use displays which require fewer bits (e.g. 18 or 16 bit displays), simply do not connect the bottom n LSBs for each colour, where n is the number of signals that are not required for a specific colour. For instance, to connect an 18-bit display, R0, R1, G0, G1 B0 and B1 will remain unused, and R2, G2 and B2 become the LSBs for this configuration.

Features
- Up to WUXGA (1920x1200) resolution
- Up to 24-bit colour
- Supports parallel TTL displays and smart displays
- Max pixel clock 165MHz

The following list details the most common colour configurations.

Table 5-12 Colour Configuration

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	24 bit RGB	18 bit RGB	16 bit RGB
251	LCD1_R0	EIM_ADDR21	IPU1_DISP1_DATA16	R0		
253	LCD1_R1	EIM_ADDR22	IPU1_DISP1_DATA17	R1		
255	LCD1_R2	EIM_ADDR23	IPU1_DISP1_DATA18	R2	R0	
257	LCD1_R3	EIM_ADDR24	IPU1_DISP1_DATA19	R3	R1	R0
259	LCD1_R4	EIM_DATA31	IPU1_DISP1_DATA20	R4	R2	R1
261	LCD1_R5	EIM_DATA30	IPU1_DISP1_DATA21	R5	R3	R2
263	LCD1_R6	EIM_DATA26	IPU1_DISP1_DATA22	R6	R4	R3
265	LCD1_R7	EIM_DATA27	IPU1_DISP1_DATA23	R7	R5	R4
269	LCD1_G0	EIM_AD01	IPU1_DISP1_DATA08	G0		
271	LCD1_G1	EIM_AD00	IPU1_DISP1_DATA09	G1		
273	LCD1_G2	EIM_EB1	IPU1_DISP1_DATA10	G2	G0	G0
275	LCD1_G3	EIM_EB0	IPU1_DISP1_DATA11	G3	G1	G1
277	LCD1_G4	EIM_ADDR17	IPU1_DISP1_DATA12	G4	G2	G2
279	LCD1_G5	EIM_ADDR18	IPU1_DISP1_DATA13	G5	G3	G3
281	LCD1_G6	EIM_ADDR19	IPU1_DISP1_DATA14	G6	G4	G4
283	LCD1_G7	EIM_ADDR20	IPU1_DISP1_DATA15	G7	G5	G5
287	LCD1_B0	EIM_AD09	IPU1_DISP1_DATA00	B0		
289	LCD1_B1	EIM_AD08	IPU1_DISP1_DATA01	B1		
291	LCD1_B2	EIM_AD07	IPU1_DISP1_DATA02	B2	B0	
293	LCD1_B3	EIM_AD06	IPU1_DISP1_DATA03	B3	B1	B0
295	LCD1_B4	EIM_AD05	IPU1_DISP1_DATA04	B4	B2	B1
297	LCD1_B5	EIM_AD04	IPU1_DISP1_DATA05	B5	B3	B2
299	LCD1_B6	EIM_AD03	IPU1_DISP1_DATA06	B6	B4	B3
301	LCD1_B7	EIM_AD02	IPU1_DISP1_DATA07	B7	B5	B4

Table 5-13 Additional Display Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
249	LCD1_DE	EIM_AD10	O	Data Enable (other names: Output Enable) For Passive Displays you can use this pin as Bias/Modulation pin
243	LCD1_PCLK	EIM_ADDR16	O	Pixel Clock (other names: Dot Clock, L_PCLK_WR)
247	LCD1_HSYNC	EIM_AD11	O	Horizontal Sync (other names: Line Clock, L_LCKL_A0)
245	LCD1_VSYNC	EIM_AD12	O	Vertical Sync (other names: Frame Clock, L_FCLK)
239	BKL1_PWM	EIM_AD14	O	Backlight PWM for contrast or brightness control
286	BKL1_ON	EIM_AD13	O	Enable signal for the backlight.
205	I2C2_SDA	EIM_DATA16	I/O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces
207	I2C2_SCL	EIM_EB2	O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces

5.5.2 LVDS

The LVDS interface (official name: FPD-Link/FlatLink) serialises the parallel RGB and control signals into differential LVDS pairs. Each LVDS signal pair contains up to 7 parallel signals. For an 18-bit RGB interface including the control signals (Display Enable, Vertical and Horizontal Synch), each FPD_Link/FlatLink channel requires three LVDS data pairs. The additional colours bits for a 24-bit interface are serialized into a fourth LVDS data pair. There are two colour mapping standards for the 24-bit interface. The less common “24 bit compatible” (JEIDA format) standard packs the two low significant bits of each colour into the fourth LVDS pair. This standard is backward compatible with the 18bit mode. It is possible to connect an 18 bit display to a 24-bit interface or vice versa. The more common 18/24-bit colour mapping standard (VESA format) serializes the two most significant bits of each colour into the fourth LVDS pair. This mode is not backward compatible. The LVDS interface of Apalis iMX6 is configurable to support different colour mappings and depths. This ensures compatibility with 18bit and 24bit displays with both kinds of colour mappings.

Figure 7 shows the LVDS output signals for the “24 bit Compatible Colour Mapping” (JEIDA format). The names of the RGB bits correspond to the colour names in the “24 bit RGB” column in Table 5-12. In order to enable this mode, the bit_mapping_ch field in the LDB Control Register (LDB_CTRL) should be set to 1 (JEIDA standard) and the data_width_ch field set to 1 (24 bit).

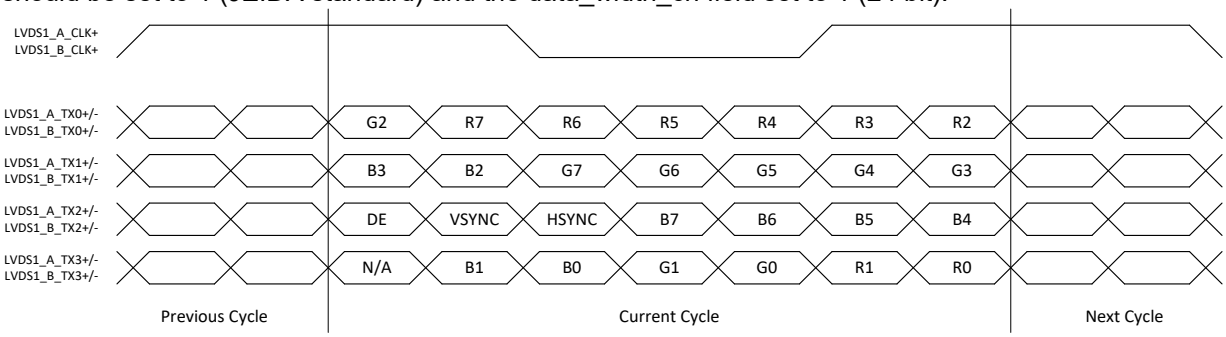


Figure 7: 24 bit / 18 bit Compatible Colour Mapping (bit_mapping_ch = 1, data_width_ch = 1)

Figure 8 shows the LVDS output signals for the common 24-bit colour mapping (VESA format). The names of the RGB bits correspond to the colour names in the “24 bit RGB” column in Table 5-12. In order to enable this mode, the bit_mapping_ch field in the LDB Control Register (LDB_CTRL) should be set to 0 (SPWG standard) and the data_width_ch field set to 1 (24 bit).

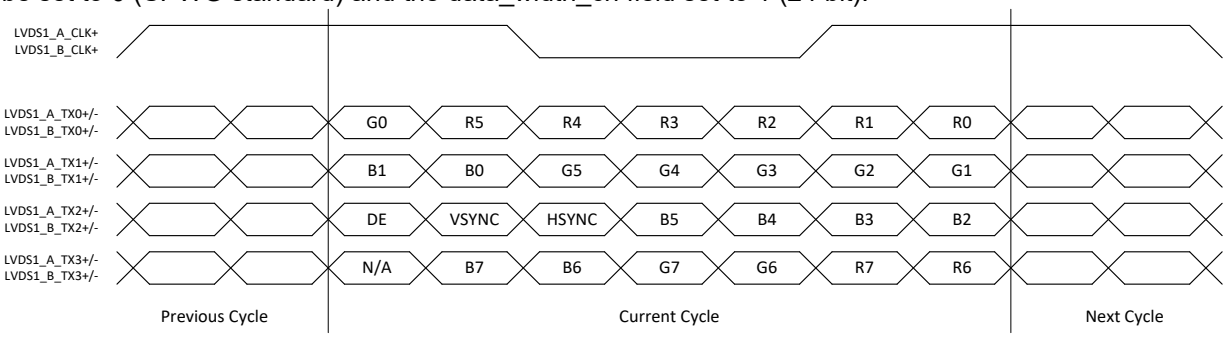


Figure 8: Common 24 bit VESA Colour Mapping (bit_mapping_ch = 0, data_width_ch = 1)

Figure 9 shows the LVDS output signals for the 18-bit interface. The names of the RGB bits correspond to the colour names in the “18 bit RGB” column in Table 5-12. In order to enable this mode, the bit_mapping_ch field in the LDB Control Register (LDB_CTRL) should to be set to 0 (SPWG standard) and the data_width_ch field set to 0 (18 bit).

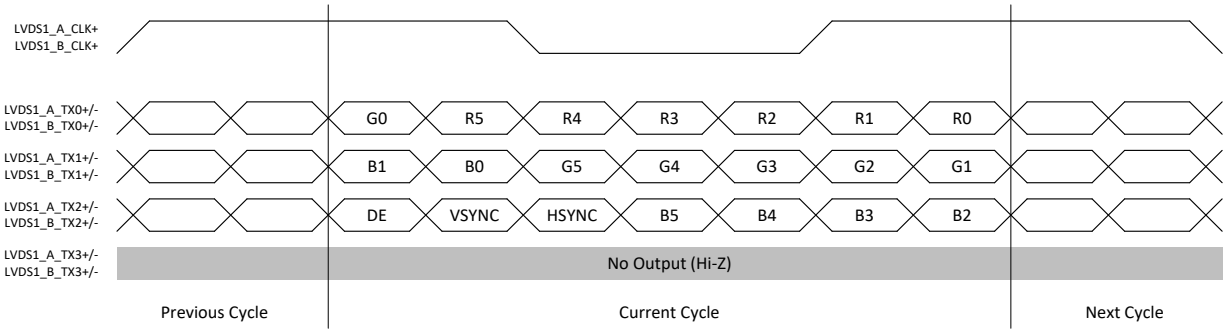


Figure 9: 18 bit Mode (bit_mapping_ch = 0, data_width_ch = 0)

A single channel LVDS interface can support resolutions up to 1366x768 pixels @60 frames per second (85MHz pixel clock maximum). For higher resolutions, a second LVDS channel is required. In dual channel configuration, the odd bits are transmitted in the first channel and the even bits transmitted in the second channel. The dual channel LVDS interface can support resolutions up to 1920x1200 @60fps (170MHz pixel clock maximum).

The single and dual channel mode is compatible with other Apalis modules including the Apalis T30. Additionally, the Apalis iMX6 is able to interface two single channel LVDS displays. The displays can have cloned content or can be driven independently from the IPUs. The ability to support independent display content on each channel may not be possible on all Apalis modules.

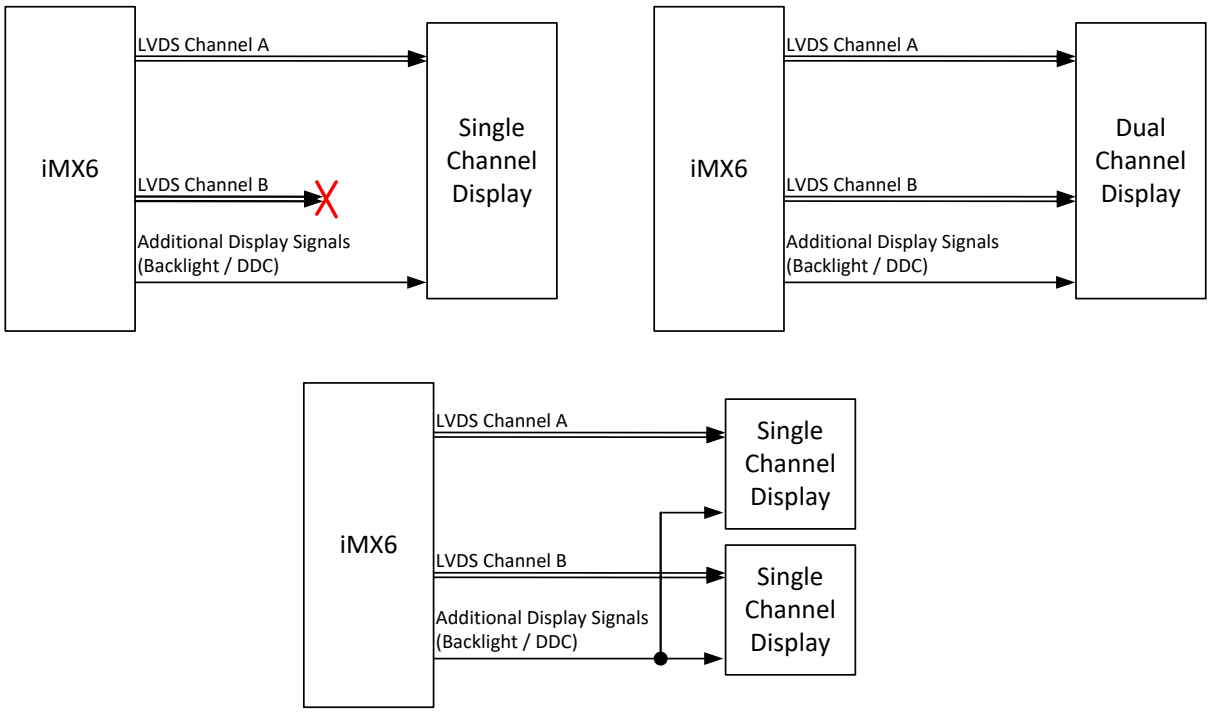


Figure 10: Available LVDS Display configurations

Table 5-14 LVDS interface signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
248	LVDS1_A_CLK+	LVDS0_CLK_P	O	LVDS Clock out for channel A (odd pixels/single channel)
246	LVDS1_A_CLK-	LVDS0_CLK_N	O	
254	LVDS1_A_TX0+	LVDS0_DATA0_P	O	LVDS data lane 0 for channel A (odd pixels/single channel)
252	LVDS1_A_TX0-	LVDS0_DATA0_N	O	
260	LVDS1_A_TX1+	LVDS0_DATA1_P	O	LVDS data lane 1 for channel A (odd pixels/single channel)
258	LVDS1_A_TX1-	LVDS0_DATA1_N	O	
266	LVDS1_A_TX2+	LVDS0_DATA2_P	O	LVDS data lane 2 for channel A (odd pixels/single channel)
264	LVDS1_A_TX2-	LVDS0_DATA2_N	O	
272	LVDS1_A_TX3+	LVDS0_DATA3_P	O	LVDS data lane 3 for channel A (odd pixels/single channel; unused for 18bit)
270	LVDS1_A_TX3-	LVDS0_DATA3_N	O	
278	LVDS1_B_CLK+	LVDS1_CLK_P	O	LVDS Clock out for channel B (even pixels/unused for single channel)
276	LVDS1_B_CLK-	LVDS1_CLK_N	O	
284	LVDS1_B_TX0+	LVDS1_DATA0_P	O	LVDS data lane 0 for channel B (odd pixels/unused for single channel)
282	LVDS1_B_TX0-	LVDS1_DATA0_N	O	
290	LVDS1_B_TX1+	LVDS1_DATA1_P	O	LVDS data lane 1 for channel B (odd pixels/unused for single channel)
288	LVDS1_B_TX1-	LVDS1_DATA1_N	O	
296	LVDS1_B_TX2+	LVDS1_DATA2_P	O	LVDS data lane 2 for channel B (odd pixels/unused for single channel)
294	LVDS1_B_TX2-	LVDS1_DATA2_N	O	
302	LVDS1_B_TX3+	LVDS1_DATA3_P	O	LVDS data lane 3 for channel B (odd pixels/unused for single channel; unused for 18bit)
300	LVDS1_B_TX3-	LVDS1_DATA3_N	O	

Table 5-15 Additional Display Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
239	BKL1_PWM	EIM_AD14	O	Backlight PWM for contrast or brightness control
286	BKL1_ON	EIM_AD13	O	Enable signal for the backlight
205	I2C2_SDA	EIM_DATA16	I/O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces
207	I2C2_SCL	EIM_EB2	O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces

5.5.3 HDMI

HDMI provides a unified method of transferring both video and audio data over a TMDS compatible physical link to an audio/visual display device. The HDMI interface is electrically compatible with the DVI standard.

Features
- HDMI 1.4a up to 1080p60
- Pixel Clock from 13.5MHz up to 266MHz
- Supports digital sound
- High-bandwidth Content Protection (HDCP, separate license needed)
- CEC interface

Table 5-16 HDMI Interface Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
240	HDMI1_TXC+	HDMI_TX_CLK_P	O	HDMI Differential Clock
242	HDMI1_TXC-	HDMI_TX_CLK_N	O	
234	HDMI1_TXD0+	HDMI_TX_DATA0_P	O	HDMI Differential Data
236	HDMI1_TXD0-	HDMI_TX_DATA0_N	O	
228	HDMI1_TXD1+	HDMI_TX_DATA1_P	O	HDMI Differential Data
230	HDMI1_TXD1-	HDMI_TX_DATA1_N	O	
222	HDMI1_TXD2+	HDMI_TX_DATA2_P	O	HDMI Differential Data
224	HDMI1_TXD2-	HDMI_TX_DATA2_N	O	
220	HDMI1_CEC	KEY_ROW2	I/O	HDMI Consumer Electronic Control.
232	HDMI1_HPD	HDMI_TX_HPD	I	Hot Plug Detect

Table 5-17 Additional Display Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
205	I2C2_SDA	EIM_DATA16	I/O	Display Data Channel, shared with the other display interfaces
207	I2C2_SCL	EIM_EB2	O	Display Data Channel, shared with the other display interfaces

5.5.4 Analogue VGA

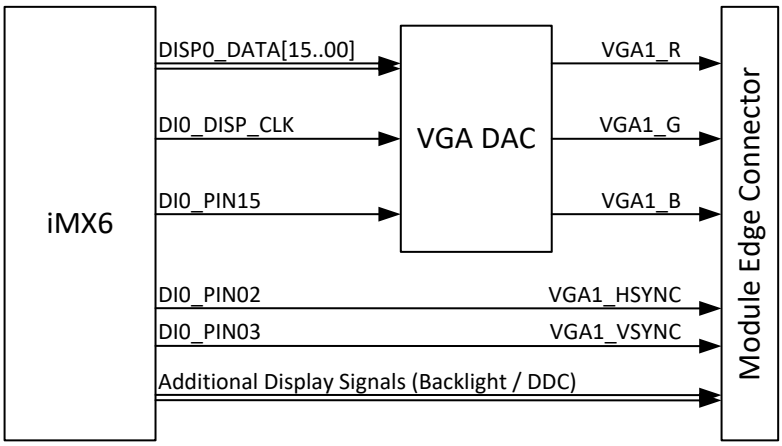


Figure 11: VGA Block Diagram

The analogue VGA interface can be used to connect a standard VGA monitor. As the i.MX 6 SOC does not feature a native VGA interface, there is a VGA DAC located on the module. The DAC is driven with a 16 bit parallel RGB interface from the SoC. This interface is independent from the primary parallel RGB interface. The analogue VGA (analogue RGB) output of the Apalis iMX6 does not support S-Video TV out.

The parallel RGB interface that is used for the VGA DAC needs to be configured as a 16bit interface. The RGB interface can be configured as IPU1_DISP0 or IPU2_DISP0. This provides maximum flexibility for the VGA interface.

Table 5-18 Colour Configuration

iMX6 Ball Name	iMX6 Port Name (ALT0)	iMX6 Port Name (ALT1)	16 bit RGB
DISP0_DATA11	IPU1_DISP0_DATA11	IPU2_DISP0_DATA11	R0
DISP0_DATA12	IPU1_DISP0_DATA12	IPU2_DISP0_DATA12	R1
DISP0_DATA13	IPU1_DISP0_DATA13	IPU2_DISP0_DATA13	R2
DISP0_DATA14	IPU1_DISP0_DATA14	IPU2_DISP0_DATA14	R3
DISP0_DATA15	IPU1_DISP0_DATA15	IPU2_DISP0_DATA15	R4
DISP0_DATA05	IPU1_DISP0_DATA05	IPU2_DISP0_DATA05	G0
DISP0_DATA06	IPU1_DISP0_DATA06	IPU2_DISP0_DATA06	G1
DISP0_DATA07	IPU1_DISP0_DATA07	IPU2_DISP0_DATA07	G2
DISP0_DATA08	IPU1_DISP0_DATA08	IPU2_DISP0_DATA08	G3
DISP0_DATA09	IPU1_DISP0_DATA09	IPU2_DISP0_DATA09	G4
DISP0_DATA10	IPU1_DISP0_DATA10	IPU2_DISP0_DATA10	G5
DISP0_DATA00	IPU1_DISP0_DATA00	IPU2_DISP0_DATA00	B0
DISP0_DATA01	IPU1_DISP0_DATA01	IPU2_DISP0_DATA01	B1
DISP0_DATA02	IPU1_DISP0_DATA02	IPU2_DISP0_DATA02	B2
DISP0_DATA03	IPU1_DISP0_DATA03	IPU2_DISP0_DATA03	B3
DISP0_DATA04	IPU1_DISP0_DATA04	IPU2_DISP0_DATA04	B4
DI0_DISP_CLK	IPU1_DI0_DISP_CLK	IPU2_DI0_DISP_CLK	PCLK
DI0_PIN15	IPU1_DI0_PIN15	IPU2_DI0_PIN15	DE

Depending on the Apalis iMX6 module variant, there are different VGA DACs assembled. The maximum resolution of the VGA port depends on the assembled DAC. For more information, see section 1.3.3 or contact Toradex.

Table 5-19 VGA Interface Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
208	VGA1_R		O	Analogue Red Signal
210	VGA1_G		O	Analogue Green Signal
212	VGA1_B		O	Analogue Blue Signal
214	VGA1_HSYNC	DI0_PIN02	O	Horizontal Sync, needs 5V level shifter on carrier board
216	VGA1_VSYNC	DI0_PIN03	O	Vertical Sync, needs 5V level shifter on carrier board

Table 5-20 Additional Display Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
205	I2C2_SDA	EIM_DATA16	I/O	Display Data Channel, shared with the other display interfaces
207	I2C2_SCL	EIM_EB2	O	Display Data Channel, shared with the other display interfaces

5.5.5 Display Serial Interface (DSI)

The i.MX 6 SoC supports one dual lane MIPI/DSI interfaces to connect compatible displays. Each data lane is capable of up to 1Gbps data rate. Lane 1 of the interface is bidirectional (high speed out, low power/speed in from display). The interface uses the MIPI D-PHY for the physical layer.
The DSI signals are located in the type specific area of the Apalis module. Therefore, it is not guaranteed that other Apalis modules will be compatible with this interface. If you are planning on using the DSI interface, please be aware that other Apalis modules might not be compatible with your carrier board.
As the DSI is a high speed interface, some additional layout requirements need to be met on the carrier board. These requirements are not detailed in the Apalis Carrier Board Design Guide as the interface is type specific.

Table 5-21 DSI Signal Routing Requirements

Parameter	Requirement
Max Frequency	500MHz (1GT/S per data lane)
Configuration/Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single ended
Max Intra-Pair Skew	<1ps ≈150µm
Max Trace Length Skew between clock and data lanes	<10ps ≈1.5mm
Max Trace Length from Module Connector	200mm

Table 5-22 DSI interface signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	DSI Signal Name	I/O	Description
127	TS_DIFF12+	DSI_CLK0_P	DSI1_CLK+	O	DSI clock
125	TS_DIFF12-	DSI_CLK0_N	DSI1_CLK-	O	
121	TS_DIFF11+	DSI_DATA0_P	DSI1_D1+	I/O	DSI data lane 1
119	TS_DIFF11-	DSI_DATA0_N	DSI1_D1-	I/O	
115	TS_DIFF10+	DSI_DATA1_P	DSI1_D2+	O	DSI data lane 2
113	TS_DIFF10-	DSI_DATA1_N	DSI1_D2-	O	

Table 5-23 Additional Display Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
239	BKL1_PWM	EIM_AD14	O	Backlight PWM for contrast or brightness control
286	BKL1_ON	EIM_AD13	O	Enable signal for the backlight.
205	I2C2_SDA	EIM_DATA16	I/O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces
207	I2C2_SCL	EIM_EB2	O	I^2C interface might be used for the extended display identification data (EDID), shared with the other display interfaces

5.6 PCI Express

The NXP i.MX 6 SoC features a single lane PCI Express (PCIe) interface. The PCIe interface is compliant with the PCIe 2.0 specification and supports 5Gb/s data rate. It is backward compatible with the PCIe 1.1 standard which supports 2.5Gb/s.

PCIe is a high speed interface that needs special layout requirements to be followed. Please carefully study the Apalis Carrier Board Design Guide for more information.

Table 5-24 PCIe Interface Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
55	PCIE1_CLK+	CLK1_P	O	Reference clock differential pair
53	PCIE1_CLK-	CLK1_N	O	
49	PCIE1_TX+	PCIE_TX_P	O	Transmit data
47	PCIE1_TX-	PCIE_TX_N	O	
43	PCIE1_RX+	PCIE_RX_P	I	Receive data
41	PCIE1_RX-	PCIE_RX_N	I	

Table 5-25 Additional PCIe Control Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
37	WAKE1_MICO	GPIO04	I	General purpose wake signal
26	RESET_MOCI#		O	General reset output
209	I2C1_SDA	CSI0_DATA08	I/O	Some PCIe devices need the SMB interface for special configurations. I2C1 should be used if interface is necessary
211	I2C1_SCL	CSI0_DATA09	O	

5.7 SATA

The Serial ATA (SATA) interface can be used to attach, for example, an external hard drive, SSD or a mSATA SSD. The interface is a single Gen 2 SATA link with a maximum transfer rate of 3Gb/s. The interface is backward compatible with Gen 1 (1.5Gb/s). SATA is a high speed interface that needs special layout requirements to be followed. Please carefully study the Apalis Carrier Board Design Guide for more information.

Table 5-26 Apalis standard SATA Interface Signals (x1)

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
33	SATA1_TX+	SATA_PHY_TX_P	O	SATA transmit data Series decoupling capacitor are provided on the module
31	SATA1_TX-	SATA_PHY_TX_N	O	
25	SATA1_RX+	SATA_PHY_RX_P	I	SATA receive data Series decoupling capacitor are provided on the module
27	SATA1_RX-	SATA_PHY_RX_N	I	
35	SATA1_ACT#	EIM_AD15	O	SATA activity indicator

5.8 I²C

The NXP i.MX 6 offers three I²C controllers plus one DDC controller. They implement the I²C V2.1 specification. All can be used in master or slave mode. The port I2C2 is used for power management and is not available externally. Port I2C1 is available as general purpose I²C on the module connector. Port I2C3 is intended to be used in combination with the camera interface but can also be used for other general purpose.

The HDMI DDC controller is a dedicated I²C controller. It is intended to be used for the DDC or EDID interface. It cannot be used as a general purpose I²C interface.

Features:
- Supports 100kbit/s and fast mode 400kbit/s data transfer
- Multimaster operation
- Software-selectable acknowledge bit
- Interrupt driven, byte by byte data transfer
- Start and stop signal generation and detection
- Repeated start signal generation
- Acknowledge bit generation and detection
- Bus-busy detection
- Calling address identification interrupts
- Master supports clock stretching by the slave

There are a lot of low speed devices which use I2C interfaces such as RTCs and sensors, but it is also commonly used to configure other devices such as cameras or displays. The I²C Bus can also be used to communicate with SMB Bus devices.

Table 5-27 I²C Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I2C Port	Description
209	I2C1_SDA	CSI0_DATA08	I2C1	Generic I²C
211	I2C1_SCL	CSI0_DATA09		
201	I2C3_SDA (CAM)	EIM_DATA18	I2C3	I²C port for the camera interface, can also be used for other purpose
203	I2C3_SCL (CAM)	EIM_DATA17		
205	I2C2_SDA (DDC)	EIM_DATA16	DDC	I²C port for the DDC interface, cannot be used for other purpose
207	I2C2_SCL (DDC)	EIM_EB2		

Table 5-28 Alternate I²C Signals (additional, not compatible with other Apalis family modules)

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I2C Port	Description
262	USBO1_OC#	EIM_DATA21	I2C1_SCL	I2C1	Alternate clock pin
17	GPIO8	GPIO06	I2C3_SDA	I2C3	Alternate data pin
217	SPDIF1_IN	GPIO16	I2C3_SDA		
96	USBH_OC#	GPIO03	I2C3_SCL	I2C3	Alternate clock pin

5.8.1 Real-Team Clock (RTC) recommendation

The Apalis module features a RTC circuit which is located inside the SoC. The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for time keeping. As long as the main power supply is provided to the module, the RTC is sourced from this rail. If the RTC need to be retained even without the module main voltage, a coin cell needs to be applied to the VCC_BACKUP (pin 174) supply pin.

The RTC on the module is not designed for ultra-low power consumption (typical current consumption can be found in section 8.3). Therefore, a standard lithium coin cell battery can be drain faster than required for certain designs. If a rechargeable RTC battery is not a solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, add the external RTC to the I2C1 interface of the module and leave the VCC_BACKUP pin unconnected. A suitable reference schematic can be found in the schematic diagram of the Apalis evaluation board.

5.9 UART

The Apalis iMX6 provides up to five serial UART interfaces. Four of them are available on dedicated UART pins as defined in the Apalis standard. The fifth UART is only available as an alternate function. This fifth UART is not compatible with other Apalis modules. Therefore, the fifth UART should only be used if compatibility with other Apalis modules is not required.

The i.MX 6 UART1 (provided as Apalis UART1 interface) is the only full featured UART and is used as standard debug interface for the Toradex Linux and Windows Embedded Compact operating systems. It is desirable to keep this port accessible for system debugging.

The UARTS of the i.MX 6 can be configured either in the DTE (Data Terminal Equipment) or DCE (Data Communication Equipment) mode. Changing the mode will change the direction of all UART pins (data and all control signals). In order to be compatible with the Apalis family, the UARTs need to be set to the DTE mode.

The names of the i.MX 6 ports for the data signals of the UARTs are confusing. In the DTE mode, the UARTx_RX_DATA is transmitting the signals from the SoC while the UARTx_TX_DATA port is receiving them. Therefore, the RX and TX signals need to be swapped. In the following signal descriptions, the port direction is always listed for the DTE mode.

UART Features
- High-speed TIA/EIA-232F compatible (up to 5 Mbit/s)
- IrDA-compatible (up to 115.2kbit/s
- 7 or 8 data bits (9 bit for RS485)
- 1 or 2 stop bits
- Optional parity bit (even or odd)
- Hardware flow control
- Auto detect baud rate
- 32 entries FIFO for receive and transmit

Table 5-29 UART1 Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
118	UART1_RXD	CSI0_DATA10	UART1_TX_DATA	I	Received Data
112	UART1_TXD	CSI0_DATA11	UART1_RX_DATA	O	Transmitted Data
114	UART1_RTS	EIM_DATA20	UART1_RTS_B	O	Request to Send
116	UART1_CTS	EIM_DATA19	UART1_CTS_B	I	Clear to Send
110	UART1_DTR	EIM_DATA24	UART1_DTR_B	O	Data Terminal Ready
120	UART1_DSR	EIM_DATA25	UART1_DSR_B	I	Data Set Ready
122	UART1_RI	EIM_EB3	UART1_RI_B	I	Ring Indicator
124	UART1_DCD	EIM_DATA23	UART1_DCD_B	I	Data Carrier Detect

Table 5-30 UART2 Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
132	UART2_RXD	SD4_DATA7	UART2_TX_DATA	I	Received Data
126	UART2_TXD	SD4_DATA4	UART2_RX_DATA	O	Transmitted Data
128	UART2_RTS	SD4_DATA5	UART2_RTS_B	O	Request to Send
130	UART2_CTS	SD4_DATA6	UART2_CTS_B	I	Clear to Send

Table 5-31 UART3 Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
136	UART3_RXD	KEY_COL0	UART4_TX_DATA	I	Received Data
134	UART3_TXD	KEY_ROW0	UART4_RX_DATA	O	Transmitted Data

Table 5-32 UART4 Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
140	UART4_RXD	KEY_COL1	UART5_TX_DATA	I	Received Data
138	UART4_TXD	KEY_ROW1	UART5_RX_DATA	O	Transmitted Data

Table 5-33 Signal Pins of additional UART Port

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
99	TS_3	SD4_CMD	UART3_TX_DATA	I	Received Data
110	UART1_DTR	EIM_DATA24			
85	TS_DIFF5+	SD4_CLK	UART3_RX_DATA	O	Transmitted Data
120	UART1_DSR	EIM_DATA25			
122	UART1_RI	EIM_EB3	UART3_RTS_B	O	Request to Send
259	LCD1_R4	EIM_DATA31			
124	UART1_DCD	EIM_DATA23	UART3_CTS_B	I	Clear to Send
261	LCD1_R5	EIM_DATA30			

This UART port is only available as an Alternate function. Compatibility with other Apalis modules cannot be guaranteed, as it is not part of the Apalis module specification.

Table 5-34 Alternate UART Signals (additional, not compatible with other Apalis family modules)

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
14	CAN1_TX	GPIO07	UART2_TX_DATA	I	Alternate Received Data
263	LCD1_R6	EIM_DATA26			
12	CAN1_RX	GPIO08	UART2_RX_DATA	O	Alternate Transmitted Data
265	LCD1_R7	EIM_DATA27			
135	TS_5	EIM_DATA29	UART2_RTS_B	O	Alternate Request to Send
187	CAM1_D0	CSI0_DATA12	UART4_TX_DATA	I	Alternate Received Data
185	CAM1_D1	CSI0_DATA13	UART4_RX_DATA	O	Alternate Transmitted Data
179	CAM1_D4	CSI0_DATA16	UART4_RTS_B	O	Request to Send
177	CAM1_D5	CSI0_DATA17	UART4_CTS_B	I	Clear to Send
183	CAM1_D2	CSI0_DATA14	UART5_TX_DATA	I	Alternate Received Data
181	CAM1_D3	CSI0_DATA15	UART5_RX_DATA	O	Alternate Transmitted Data
18	CAN2_TX	KEY_COL4	UART5_RTS_B	O	Request to Send
175	CAM1_D6	CSI0_DATA18			
16	CAN2_RX	KEY_ROW4	UART5_CTS_B	I	Clear to Send
173	CAM1_D7	CSI0_DATA19			

5.10 SPI

The i.MX 6 Dual and Quad SoC have 5 SPI controllers (in the reference manual called Enhanced Configurable SPI, ECSPI) of which 3 can be accessed at the module edge connector. Two SPI interfaces are available as Apalis module standard. These two interfaces are compatible with other modules of the Apalis family. A third SPI interface is available as alternate function of other pins. This interface is not compatible with other Apalis modules. Please first use the dedicated Apalis SPI ports before using the third one.

The SPI ports operate at up to 18 Mbps and provide full duplex, synchronous, serial communication between the Apalis module and internal or external peripheral devices. Each SPI port consists of four signals; clock, chip select (frame), data in and data out. There are some additional chip select signals available as alternate function to support multiple peripherals.

Features:
- Up to 18 Mbps
- 32bit x 64 deep FIFO (RX and TX)
- Master/Slave configurable
- Simultaneous receive and transmit
- Low power mode

Each SPI channel supports four different modes of the SPI protocol:

Table 5-35 SPI Modes

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	Clock is positive polarity and the data is latched on the positive edge of SCK
1	0	1	Clock is positive polarity and the data is latched on the negative edge of SCK
2	1	0	Clock is negative polarity and the data is latched on the positive edge of SCK
4	1	1	Clock is negative polarity and the data is latched on the negative edge of SCK

SPI can be used as a fast interface for ADCs, DACs, FPGAs, etc. Some LCD displays require configuration over SPI prior to being driven via the RGB or LVDS interface.

Pay attention to the data direction of the signals in master respectively slave mode. The following table describes the data direction of the signals at the module side.

Table 5-36 SPI Signal Direction in Master and Slave Mode

iMX6 Port Name	Master Mode		Slave Mode	
	I/O	Description	I/O	Description
ECSPIx_MOSI	O	Master Output, Slave Input	I	Master Output, Slave Input
ECSPIx_MISO	I	Master Input, Slave Output	O	Master Input, Slave Output
ECSPIx_SS0	O	Slave Select	I	Slave Select
ECSPIx_SCLK	O	Serial Clock	I	Serial Clock

In the Apalis module standard, only the SPI master mode is specified. Therefore, the slave mode might not be compatible with other modules. The signal direction in the following tables corresponds to the SPI master mode.

Table 5-37 Apalis SPI Port 1 Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
225	SPI1_MOSI	CSI0_DATA05	ECSPI1_MOSI	O	Master Output, Slave Input
223	SPI1_MISO	CSI0_DATA06	ECSPI1_MISO	I	Master Input, Slave Output
227	SPI1_CS	CSI0_DATA07	ECSPI1_SS0	O	Slave Select
221	SPI1_CLK	CSI0_DATA04	ECSPI1_SCLK	O	Serial Clock

Table 5-38 Apalis SPI Port 2 Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
231	SPI2_MOSI	EIM_CS1	ECSPI2_MOSI	O	Master Output, Slave Input
229	SPI2_MISO	EIM_OE	ECSPI2_MISO	I	Master Input, Slave Output
233	SPI2_CS	EIM_RW	ECSPI2_SS0	O	Slave Select
235	SPI2_CLK	EIM_CS0	ECSPI2_SCLK	O	Serial Clock

Table 5-39 Signal pins of additional SPI Port

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
150	MMC1_CMD	SD1_CMD	ECSPI5_MOSI	O	Master Output, Slave Input
180	SD1_CMD	SD2_CMD			
160	MMC1_D0	SD1_DATA0	ECSPI5_MISO	I	Master Input, Slave Output
186	SD1_D0	SD2_DATA0			
162	MMC1_D1	SD1_DATA1	ECSPI5_SS0	O	Slave Select 0
188	SD1_D1	SD2_DATA1			
144	MMC1_D2	SD1_DATA2	ECSPI5_SS1	O	Slave Select 1
176	SD1_D2	SD2_DATA2			
146	MMC1_D3	SD1_DATA3	ECSPI5_SS2	O	Slave Select 2
178	SD1_D3	SD2_DATA3	ECSPI5_SS3	O	Slave Select 3
154	MMC1_CLK	SD1_CLK	ECSPI5_SCLK	O	Serial Clock
184	SD1_CLK	SD2_CLK			
14	CAN1_TX	GPIO07	ECSPI5_RDY	I	Data ready signal

This SPI port is only available as an alternate function of the SD or MMC signals. This is not compatible with other Apalis modules as it is not part of the Apalis module specification.

Table 5-40 Alternate SPI Port 1 Signals (additional, not compatible with other Apalis family modules)

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
134	UART3_TXD	KEY_ROW0	ECSPI1_MOSI	O	Alternate Master Output, Slave Input
201	I2C3_SDA (CAM)	EIM_DATA18			
140	UART4_RXD	KEY_COL1	ECSPI1_MISO	I	Alternate Master Input, Slave Output
203	I2C3_SCL (CAM)	EIM_DATA17			
138	UART4_TXD	KEY_ROW1	ECSPI1_SS0	O	Alternate Slave Select 0
207	I2C2_SCL (DDC)	EIM_EB2			
116	UART1_CTS	EIM_DATA19	ECSPI1_SS1	O	Slave Select 1
110	UART1_DTR	EIM_DATA24	ECSPI1_SS2	O	Slave Select 2
220	HDMI1_CEC	KEY_ROW2			
120	UART1_DSR	EIM_DATA25	ECSPI1_SS3	O	Slave Select 3
136	UART3_RXD	KEY_COL0	ECSPI1_SCLK	O	Alternate Serial Clock
205	I2C2_SDA (DDC)	EIM_DATA16			
194	DAP1_MCLK	GPIO19	ECSPI1_RDY	I	Data ready signal

Table 5-41 Alternate SPI Port 2 Signals (additional, not compatible with other Apalis family modules)

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
200	DAP1_BIT_CLK	DISP0_DATA16	ECSPI2_MOSI	O	Alternate Master Output, Slave Input
211	I2C1_SCL	CSI0_DATA09			
118	UART1_RXD	CSI0_DATA10	ECSPI2_MISO	I	Alternate Master Input, Slave Output
196	DAP1_D_OUT	DISP0_DATA17			
112	UART1_TXD	CSI0_DATA11	ECSPI2_SS0	O	Alternate Slave Select 0
204	DAP1_SYNC	DISP0_DATA18			
198	DAP1_RESET#	EIM_LBA	ECSPI2_SS1	O	Slave Select 1
110	UART1_DTR	EIM_DATA24	ECSPI2_SS2	O	Slave Select 2
120	UART1_DSR	EIM_DATA25	ECSPI2_SS3	O	Slave Select 3
202	DAP1_D_IN	DISP0_DATA19	ECSPI2_SCLK	O	Alternate Serial Clock
209	I2C1_SDA	CSI0_DATA08			

5.11 PWM (Pulse Width Modulation)

The Apalis iMX6 features a four channel Pulse Width Modulator (PWM). Each PWM features a 16-bit up-counter with clock source selection. There is a 16bit 4 level deep FIFO available in order to minimize the interrupt overhead. There is a 12-bit prescaler available for dividing the clock.

The PWM interface can be used as an easy way to emulate a DAC and generate a variable DC voltage if used with a suitable RC circuit. Other uses include control of LED brightness, display backlights or servo motors.

The Apalis standard defines a fifth, dedicated PWM output for the display backlight. As the i.MX 6 SoC features only four PWM controllers, the backlight PWM is shared with PWM4. The following figure shows the buffer between the PWM4 and the backlight output.

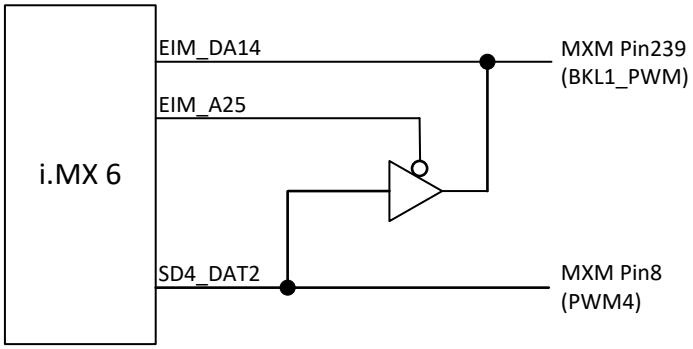


Figure 12: Backlight PWM output circuit

Table 5-42 PWM Interface Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Remarks
2	PWM1	GPIO09	PWM1_OUT	O	
4	PWM2	GPIO01	PWM2_OUT	O	
6	PWM3	SD4_DATA1	PWM3_OUT	O	
8	PWM4	SD4_DATA2	PWM4_OUT	O	Shared PWM output with BKL1_PWM
239	BKL1_PWM	SD4_DATA2	PWM4_OUT	O	Shared PWM output with PWM4

5.12 OWR (One Wire)

The Apalis iMX6 does not feature a One Wire interface.

5.13 SD/MMC

The i.MX 6 SoC provides 4 SDIO interfaces; one is used internally for the eMMC Flash and the other 3 are available on the module edge connector Pins. To ensure carrier board design compatibility with other Apalis modules, only the two SD/MMC interfaces that are available at the pins defined in the Apalis standard should be used. The third SD/MMC interface is available as an alternate function.

The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards and eMMC devices. The controllers can act as both master and slave simultaneously.

Features
- Supports SD Memory Card Specification 3.0
- Supports SDIO Card Specification Version 3.0
- Supports MMC System Specification Version 4.2, 4.3, 4.4, and 4.41
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TByte
- Support SPI mode
- The IO voltage is 3.3V on the SODIMM pins.

i.MX 6 SDIO interface	Max Bus Width	Description
USDHC1	8bit	Apalis Standard MMC1 interface
USDHC2	4bit (8bit)	Apalis Standard SD1 interface, additional data bits for 8bit interface available as alternate function
USDHC3	8bit	Connected to internal eMMC. Not available at the module edge connector
USDHC4	8bit	Available as secondary function, not compatible with Apalis standard

Table 5-43 Apalis MMC1 Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
150	MMC1_CMD	SD1_CMD	SD1_CMD	I/O	Command
160	MMC1_D0	SD1_DATA0	SD1_DATA0	I/O	Serial Data 0
162	MMC1_D1	SD1_DATA1	SD1_DATA1	I/O	Serial Data 1
144	MMC1_D2	SD1_DATA2	SD1_DATA2	I/O	Serial Data 2
146	MMC1_D3	SD1_DATA3	SD1_DATA3	I/O	Serial Data 3
148	MMC1_D4	NAND_DATA00	SD1_DATA4	I/O	Serial Data 4
152	MMC1_D5	NAND_DATA01	SD1_DATA5	I/O	Serial Data 5
156	MMC1_D6	NAND_DATA02	SD1_DATA6	I/O	Serial Data 6
158	MMC1_D7	NAND_DATA03	SD1_DATA7	I/O	Serial Data 7
154	MMC1_CLK	SD1_CLK	SD1_CLK	O	Serial Clock
164	MMC1_CD#	DI0_PIN04	GPIO4_IO20	I	Card Detect (standard GPIO)

Table 5-44 Apalis SD1 Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
184	SD1_CLK	SD2_CLK	SD2_CLK	I/O	Serial Clock
186	SD1_D0	SD2_DATA0	SD2_DATA0	I/O	Serial Data 0
188	SD1_D1	SD2_DATA1	SD2_DATA1	I/O	Serial Data 1
176	SD1_D2	SD2_DATA2	SD2_DATA2	I/O	Serial Data 2
178	SD1_D3	SD2_DATA3	SD2_DATA3	I/O	Serial Data 3
180	SD1_CMD	SD2_CMD	SD2_CMD	O	Command
190	SD1_CD#	NAND_CS1_B	GPIO6_IO14	I	Card Detect (standard GPIO)

Table 5-45 Additional Signals for the SD1 interface on nonstandard Apalis Pin

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
1	GPIO1	NAND_DATA04	SD2_DATA4	I/O	Serial Data 4
3	GPIO2	NAND_DATA05	SD2_DATA5	I/O	Serial Data 5
5	GPIO3	NAND_DATA06	SD2_DATA6	I/O	Serial Data 6
7	GPIO4	NAND_DATA07	SD2_DATA7	I/O	Serial Data 7

With the help of these signals, the SD1 interface can also be used as an 8bit interface. The pins are not compatible with other Apalis modules, as it is not part of the Apalis module specification. It is recommended to use the MMC1 interface if only one 8 bit SD/MMC interface is required.

Table 5-46 Additional USDHC4 interface on nonstandard Apalis Pin

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
99	TS_3	SD4_CMD	SD4_CMD	I/O	Command
95	TS_DIFF7-	SD4_DATA0	SD4_DATA0	I/O	Serial Data 0
6	PWM3	SD4_DATA1	SD4_DATA1	I/O	Serial Data 1
8	PWM4	SD4_DATA2	SD4_DATA2	I/O	Serial Data 2
123	TS_4	SD4_DATA3	SD4_DATA3	I/O	Serial Data 3
126	UART2_TXD	SD4_DATA4	SD4_DATA4	I/O	Serial Data 4
128	UART2_RTS	SD4_DATA5	SD4_DATA5	I/O	Serial Data 5
130	UART2_CTS	SD4_DATA6	SD4_DATA6	I/O	Serial Data 6
132	UART2_RXD	SD4_DATA7	SD4_DATA7	I/O	Serial Data 7
85	TS_DIFF5+	SD4_CLK	SD4_CLK	O	Serial Clock
91	TS_DIFF6+	NAND_ALE	SD4_RESET	O	Reset (only used by some devices, common reset or GPIO could also be used instead)

This interface is only available as alternate functions of UART2, PWM and type specific pins. This interface is not compatible with other Apalis modules and should be used only if the other two SD/MMC interfaces are already used. For the card detect, any free GPIO can be used.

5.14 Analogue Audio

The Apalis iMX6 offers analogue audio input and output channels. On the module, a NXP SGTL5000 chip handles the analogue audio interface. The SGTL5000 is connected over I2S (AUD4) with the NXP i.MX 6. Please consult the NXP SGTL5000 datasheet for more information.

Table 5-47 Analogue Audio Interface Pins

X1 Pin #	Apalis Signal Name	I/O	Description	Pin on the SGTL5000 (20pin QFN)
306	AAP1_MICIN	Analogue Input	Microphone input	10
310	AAP1_LIN_L	Analogue Input	Left Line Input	9
312	AAP1_LIN_R	Analogue Input	Right Line Input	8
316	AAP1_HP_L	Analogue Output	Headphone Left Output	4
318	AAP1_HP_R	Analogue Output	Headphone Right Output	1

5.15 Digital Audio

The Apalis module standard provides one digital audio interface. In addition to this interface, there are a further two interfaces available on alternate functions of other interfaces. The interfaces can be used as Intel® Audio Codec ’97 (also known as AC’97 or AC97) or as I2S (also known as Inter-IC Sound, Integrated Interchip Sound or IIS). The interfaces can be used to connect an additional external audio codec that can provide up to 5.1 channel audio. Please be aware that some Apalis modules may provide different codec standards such as HD Audio or just a subset of AC97 and I2S on this interface.

The i.MX 6 SoC features internally three synchronous serial interfaces (SSI). The three SSI controllers are connected to a digital audio multiplexer (AUDMUX). This multiplexer has four ports of which three are available at the X1 MXM3 connector. In total, the multiplexer has seven ports which are essentially equal. All ports can be configured as four wire (input synchronous to the output stream) or six wire interfaces (input and output stream with independent clocks and frame signal). The multiplexer has the full flexibility to connect any port to another (independent whether it is an internal or external port). Each host can be connected to one (point to point) or many (point to multipoint) hosts. With the TXRXEN bit, it is possible to reverse the transmitting and receiving data lines.

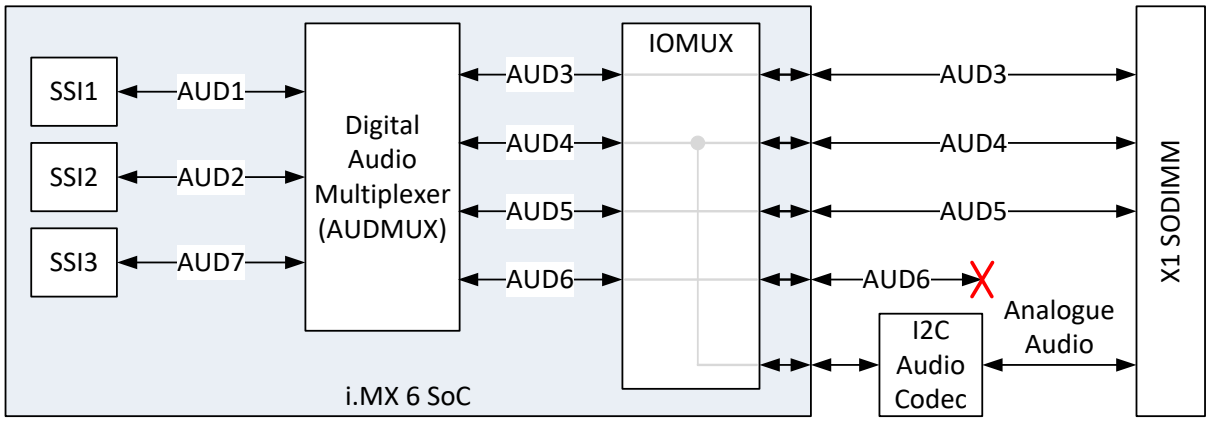


Figure 13 Audio Multiplexing

The audio codec on the module which provides the analogue audio interface is connected to the AUD4 interface of the digital audio multiplexer and is used in the I²S mode. If the analogue audio interface is in use, the external AUD4 signal pins cannot be used externally.

Table 5-48 Digital Audio Port Signals (compatible with other modules)

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
202	DAP1_D_IN	DISP0_DATA19	AUD5_RXD	I/O	Data Input to i.MX 6
196	DAP1_D_OUT	DISP0_DATA17	AUD5_TXD	I/O	Data Output from i.MX 6
204	DAP1_SYNC	DISP0_DATA18	AUD5_TXFS	I/O	Field Select
200	DAP1_BIT_CLK	DISP0_DATA16	AUD5_TXC	I/O	Serial Clock
194	DAP1_MCLK	GPIO19	CCM_CLKO1	I/O	External Peripheral Clock (shared clock source with master clock of internal codec)

For controlling the I²S codec, an additional I²C interface is required, and the generic I²C interface I2C1is recommended for this purpose. Some codecs need an external master reference clock, for which it is recommended the DAP1_MCLK output is used. The DAP1_MCLK pin uses the CCM_CLKO1 as clock source. This is the same clock source that is used for the master clock of the on module audio codec. If both audio codecs are used and a different master clock frequency is required, please use a different clock source for the external codec.

Table 5-49 Additional Digital Audio Port Signals (not compatible with other modules)

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
138	UART4_TXD	KEY_ROW1	AUD5_RXD	I/O	Alternate Data Receive
110	UART1_DTR	EIM_DATA24	AUD5_RXFS	I/O	Receive Frame Sync
120	UART1_DSR	EIM_DATA25	AUD5_RXC	I/O	Receive Clock
134	UART3_TXD	KEY_ROW0	AUD5_TXD	I/O	Alternate Data Transmit
140	UART4_RXD	KEY_COL1	AUD5_TXFS	I/O	Alternate Transmit Frame Sync
136	UART3_RXD	KEY_COL0	AUD5_TXC	I/O	Alternate Transmit Clock

Table 5-50 Additional Digital Audio Ports (not compatible with other modules)

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
227	SPI1_CS	CSI0_DATA07	AUD3_RXD	I/O	Data Receive
112	UART1_TXD	CSI0_DATA11	AUD3_RXFS	I/O	Receive Frame Sync
118	UART1_RXD	CSI0_DATA10	AUD3_RXC	I/O	Receive Clock
225	SPI1_MOSI	CSI0_DATA05	AUD3_TXD	I/O	Data Transmit
223	SPI1_MISO	CSI0_DATA06	AUD3_TXFS	I/O	Transmit Frame Sync
221	SPI1_CLK	CSI0_DATA04	AUD3_TXC	I/O	Transmit Clock
186	SD1_D0	SD2_DATA0	AUD4_RXD	I/O	Data Receive
204	DAP1_SYNC	DISP0_DATA18	AUD4_RXFS	I/O	Receive Frame Sync
184	SD1_CLK	SD2_CLK			
202	DAP1_D_IN	DISP0_DATA19	AUD4_RXC	I/O	Receive Clock
180	SD1_CMD	SD2_CMD			
176	SD1_D2	SD2_DATA2	AUD4_TXD	I/O	Data Transmit
188	SD1_D1	SD2_DATA1	AUD4_TXFS	I/O	Transmit Frame Sync
178	SD1_D3	SD2_DATA3	AUD4_TXC	I/O	Transmit Clock

These Audio interfaces are available as alternate functions of the SPI1 and SD1 pins. These interfaces are not compatible with other Apalis modules and should only be used if the standard digital audio interface is already in use. The AUD4 port is also used for the on module audio codec. If this audio codec is used, the external AUD4 port signals cannot be used and are not available.

5.15.1 Digital Audio Port used as I²S

The SSI interfaces can be used as I²S interfaces with the following features:

- PCM, Network and TDM mode Support
- Master or Slave
- 15x32 bit FIFO for Transmitter and Receiver
- Maximum audio sampling rate 196 kHz

The following signals are used for the I²S interface:

Table 5-51 Digital Audio port used as Maser I²S

iMX6 Port Name	I²S Signal Name (Names at Codec)	I/O (at iMX6)	Description
AUDx_TXD	SDIN	O	Serial Data Output from i.MX 6
AUDx_RXD	SDOUT	I	Serial Data Input to i.MX 6
AUDx_TXFS	WS	O	Word Select, also known as Field Select or LRCLK
AUDx_TXC	SCK	O	Serial Continuous Clock

Table 5-52 Digital Audio port used as Slave I²S

iMX6 Port Name	I²S Signal Name (Names at Codec)	I/O (at iMX6)	Description
AUDx_RXD	SDOUT	I	Serial Data Input to i.MX 6
AUDx_TXD	SDIN	O	Serial Data Output from i.MX 6
AUDx_TXFS	WS	I	Word Select, also known as Field Select or LRCLK
AUDx_TXC	SCK	I	Serial Continuous Clock

The audio codecs often require an additional I²C interface for control and a master clock input. As I²C any of the given interfaces can be used (see section 5.8). The master clock can be provided by the clock output signal (see section 5.21). The internal audio codec is using the I2C2 port of the i.MX 6 which is also used for power management purpose. The master clock is provided by the CCM_CLKO1.

5.15.2 Digital Audio Port used as AC'97

The SSI interface can be configured as AC'97 compatible interface with a maximum frame rate of 48kHz. The AC'97 Audio interface does not need an additional I²C for the control communication. The codec is controlled directly through the AC'97 Audio interface. The AC'97Audio codec does require a master reference clock, but instead a separate crystal/oscillator can be used. Please take care with the pin naming of some codecs. Some devices name their data input pin as SDATA_OUT and the data output pin as SDATA_IN. The names refer to the signals they should be connected to on the host, and not to the signal direction.

Table 5-53 Digital Audio port used as AC'97

iMX6 Port Name	I²S Signal Name (Names at Codec)	I/O (at iMX6)	Description
AUDx_RXD	SDATA_IN	I	AC'97 Audio Serial Input to i.MX 6
AUDx_TXD	SDATA_OUT	O	AC'97 Audio Serial Output from i.MX 6
AUDx_TXFS	SYNC	O	AC'97 Audio Sync
AUDx_TXC	BIT_CLK	I	AC'97 Audio Bit Clock
GPIOx	RESET#	O	AC'97 Master H/W Reset (use any GPIO)

5.16 S/PDIF (Sony-Philips Digital Interface I/O)

The S/PDIF interface supports both input and output of serial audio digital interface format. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard.

Features:
- Internal data width: 24-bit
- Left and right channel 16x24bit FIFO (receive and transmit)

Table 5-54 S/PDIF Data Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
215	SPDIF1_OUT	GPIO17	SPDIF_OUT	O	Serial data output
217	SPDIF1_IN	GPIO16	SPDIF_IN	I	Serial data input, this pin must left unconnected if the Ethernet IEEE1588 function is used

If the Ethernet port requires the precise IEEE 1588 timer for clock synchronization, the GPIO16 ball of the i.MX 6 SoC is required to be left unconnected since the clock signal is routed internally through this ball (see also section 5.3). Therefore, if IEEE 1588 and the SPDIF1_IN are required, the SPDIF IN signal needs to be used as alternate function on a different ball.

Table 5-55 Alternate S/PDIF Data Pins (not compatible with other Apalis family modules)

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
274	USBO1_EN	EIM_DATA22	SPDIF_OUT	O	Alternate serial data output
194	DAP1_MCLK	GPIO19			
262	USBO1_OC#	EIM_DATA21	SPDIF_IN	I	Alternate serial data input
72	USBO1_ID	ENET_RX_ER			

5.17 Enhanced Serial Audio Interface (ESAI)

The ESAI provides a full-duplex serial port for communication with a variety of serial audio devices including industry-standard codecs, S/PDIF transceivers, and other DSPs. The interface is only available as an alternate function as it is not part of the Apalis module standard.

Features
- Independent (asynchronous) mode or shared (synchronous) mode of the transmitter and receiver
- Master or slave mode
- Up to 5 transmitters and up to 3 receivers
- Programmable data interface modes (I2S, LSB aligned, MSB aligned)
- Programmable word length (8, 12, 16, 20 or 24bit)
- AC97 support
- 128word FIFO shared by all transmitters
- 128word FIFO shared by all receivers

Table 5-56 ESAI Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
17	GPIO8	GPIO06	ESAI_TX_CLK	I/O	TX serial bit clock
15	GPIO7	GPIO02	ESAI_TX_FS	I/O	Frame sync for transmitters and receivers in the synchronous mode and for the transmitters only in asynchronous mode
37	WAKE1_MICO	GPIO04	ESAI_TX_HF_CLK	I/O	TX high frequency clock
193	CAM1_MCLK	NAND_CS2_B	ESAI_TX0	I/O	TX data 0
215	SPDIF1_OUT	GPIO17			
89	TS_DIFF6-	NAND_CS3_B	ESAI_TX1	I/O	TX data 1
217	SPDIF1_IN	GPIO16	ESAI_TX3_RX2	I/O	TX data 3 or RX data 2
14	CAN1_TX	GPIO07	ESAI_TX4_RX1	I/O	TX data 4 or RX data 1
12	CAN1_RX	GPIO08	ESAI_TX5_RX0	I/O	TX data 5 or RX data 0
4	PWM2	GPIO01	ESAI_RX_CLK	I/O	RX serial bit clock
2	PWM1	GPIO09	ESAI_RX_FS	I/O	RX frame sync signal in asynchronous mode
96	USBH_OC#	GPIO03	ESAI_RX_HF_CLK	I/O	RX high frequency clock

5.18 Touch Panel Interface

The Apalis iMX6 offers a 4-wire resistive touch interface. The ST Microelectronics STMPE811 provides the touch interface. The Microelectronics STMPE811 is
connected with the NXP i.MX 6 via the power management I2C interface (I2C2).
Please consult the Microelectronics STMPE811 documentation for more information.

Table 5-57 Touch Interface Pins

X1 Pin #	Apalis Signal Name	Pin on the STMPE811	I/O	Description
315	AN1_TSPX	13	Analogue Input	X+ (4-wire)
317	AN1_TSMX	16	Analogue Input	X- (4-wire)
319	AN1_TSPY	15	Analogue Input	Y+ (4-wire)
321	AN1_TSMY	1	Analogue Input	Y- (4-wire)

5.19 Analogue Inputs

The ST Microelectronics STMPE811 provides 4 analogue input channels. Please consult the ST Microelectronics STMPE811 documentation for more information. All AD inputs are protected with a 10k Ohm series resistor between the module edge connector pins and the ADC.

Features
- 12-bit ADC
- 0 to 3.3V rail to rail

Table 5-58 Analogue Inputs Pins

X1 Pin #	Apalis Signal Name	Pin on the STMPE811	I/O	Description
305	AN1_ADC0	8	Analogue Input	ADC input (3.3V max)
307	AN1_ADC1	9	Analogue Input	ADC input (3.3V max). The ADC pin is pulled to GND (10k Ohm) for 6µs while booting.
309	AN1_ADC2	11	Analogue Input	ADC input (3.3V max)
311	AN1_TSWIP_ADC3	12	Analogue Input	ADC input (3.3V max).

5.20 Camera Interface

The i.MX 6 Dual/Quad SoC features two Image Processing Units (IPU). The IPUs can receive data from TV decoder chips, CMOS sensors, graphics accelerators, and other devices. The IPUs are also responsible for sending image data to a display device (see also section 5.5).

Each IPU has two camera sensor interfaces (CSI). The SoC itself features three camera input ports, two parallel and one MIPI/CSI-2. The first parallel camera port (IPU1.CSI0) is available as an Apalis standard interface. The MIPI/CSI-2 port is available in the type specific part of the MXM3 connector, while the second parallel camera port is only available as alternate function of other pins. The multiplexing scheme of the SoC allows routing the different input ports only to certain camera sensor interfaces of the IPUs.

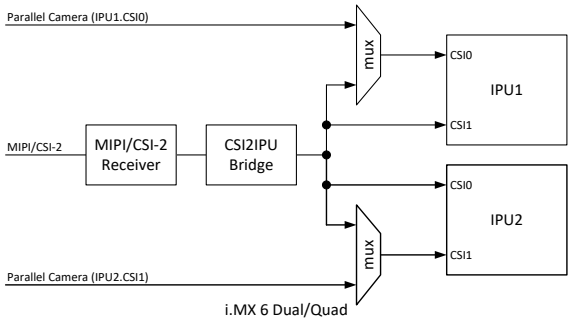


Figure 14: Camera Interface input connectivity

5.20.1 Parallel Camera Interface

The Apalis iMX6 features up to two 20-bit parallel camera interfaces. Only 8 bits of the first camera interface (IPU1.CSI0) are available on dedicated camera pins as defined in the Apalis standard. The remaining bits and the second parallel camera interface are only available as alternate functions. These pins are not guaranteed to be compatible with other Apalis modules.

Features
- Raw (Bayer), RGB, YUV input
- Frame size up to 8192x4096 pixels
- 8/16/20bit parallel video interface
- Dedicated synchronisation signals (VSYNC, HSYNC) or embedded in data stream (BT.656)

Only the 8 bit YUV mode is compatible with other Apalis modules. The additional signal bits for the 16 and 20bit interface are located as alternate functions. Other Apalis modules may have different signals on these pins. Even if the additional signal pins are available on another module the colour mapping for 16/20bit input is not guaranteed to be compatible.

Table 5-59 Apalis Standard Camera Interface Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
187	CAM1_D0	CSI0_DATA12	IPU1_CSI0_DATA12	I	Camera pixel data 0 (8bit _YUV)
185	CAM1_D1	CSI0_DATA13	IPU1_CSI0_DATA13	I	Camera pixel data1 (8bit _YUV)
183	CAM1_D2	CSI0_DATA14	IPU1_CSI0_DATA14	I	Camera pixel data 2 (8bit _YUV)
181	CAM1_D3	CSI0_DATA15	IPU1_CSI0_DATA15	I	Camera pixel data 3 (8bit _YUV)
179	CAM1_D4	CSI0_DATA16	IPU1_CSI0_DATA16	I	Camera pixel data 4 (8bit _YUV)
177	CAM1_D5	CSI0_DATA17	IPU1_CSI0_DATA17	I	Camera pixel data 5 (8bit _YUV)
175	CAM1_D6	CSI0_DATA18	IPU1_CSI0_DATA18	I	Camera pixel data 6 (8bit _YUV)
173	CAM1_D7	CSI0_DATA19	IPU1_CSI0_DATA19	I	Camera pixel data 7 (8bit _YUV)
191	CAM1_PCLK	CSI0_PIXCLK	IPU1_CSI0_PIXCLK	I	Camera pixel clock
195	CAM1_VSYNC	CSI0_VSYNC	IPU1_CSI0_VSYNC	I	Camera vertical sync
197	CAM1_HSYNC	CSI0_MCLK	IPU1_CSI0_HSYNC	I	Camera horizontal sync

Table 5-60 Additional Camera Interface Signals (shared with CSI, Apalis Standard)

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
193	CAM1_MCLK	NAND_CS2_B	CCM_CLKO2	O	Master clock output for camera (shared with CSI)
201	I2C3_SDA (CAM)	EIM_DATA18	I2C3_SDA	I/O	Camera control I^2C (shared with CSI)
203	I2C3_SCL (CAM)	EIM_DATA17	I2C3_SCL	O	Camera control I^2C (shared with CSI)

Table 5-61 Additional IPU1_CS0 Signals for 20bit Interface on nonstandard Apalis Pin

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
265	LCD1_R7	EIM_DATA27	IPU1_CSI0_DATA00	I	Additional camera pixel data
263	LCD1_R6	EIM_DATA26	IPU1_CSI0_DATA01	I	Additional camera pixel data
259	LCD1_R4	EIM_DATA31	IPU1_CSI0_DATA02	I	Additional camera pixel data
261	LCD1_R5	EIM_DATA30	IPU1_CSI0_DATA03	I	Additional camera pixel data
221	SPI1_CLK	CSI0_DATA04	IPU1_CSI0_DATA04	I	Additional camera pixel data
225	SPI1_MOSI	CSI0_DATA05	IPU1_CSI0_DATA05	I	Additional camera pixel data
223	SPI1_MISO	CSI0_DATA06	IPU1_CSI0_DATA06	I	Additional camera pixel data
227	SPI1_CS	CSI0_DATA07	IPU1_CSI0_DATA07	I	Additional camera pixel data
209	I2C1_SDA	CSI0_DATA08	IPU1_CSI0_DATA08	I	Additional camera pixel data
211	I2C1_SCL	CSI0_DATA09	IPU1_CSI0_DATA09	I	Additional camera pixel data
118	UART1_RXD	CSI0_DATA10	IPU1_CSI0_DATA10	I	Additional camera pixel data
112	UART1_TXD	CSI0_DATA11	IPU1_CSI0_DATA11	I	Additional camera pixel data
77	TS_DIFF4-	CSI0_DATA_EN	IPU1_CSI0_DATA_EN	I	Pixel data enable

Table 5-62 IPU2_CS1 Signals 20bit Interface on non-standard Apalis Pin

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
287	LCD1_B0	EIM_AD09	IPU2_CSI1_DATA00	I	Camera pixel data
289	LCD1_B1	EIM_AD08	IPU2_CSI1_DATA01	I	Camera pixel data
291	LCD1_B2	EIM_AD07	IPU2_CSI1_DATA02	I	Camera pixel data
293	LCD1_B3	EIM_AD06	IPU2_CSI1_DATA03	I	Camera pixel data
295	LCD1_B4	EIM_AD05	IPU2_CSI1_DATA04	I	Camera pixel data
297	LCD1_B5	EIM_AD04	IPU2_CSI1_DATA05	I	Camera pixel data
299	LCD1_B6	EIM_AD03	IPU2_CSI1_DATA06	I	Camera pixel data
301	LCD1_B7	EIM_AD02	IPU2_CSI1_DATA07	I	Camera pixel data
269	LCD1_G0	EIM_AD01	IPU2_CSI1_DATA08	I	Camera pixel data
271	LCD1_G1	EIM_AD00	IPU2_CSI1_DATA09	I	Camera pixel data
273	LCD1_G2	EIM_EB1	IPU2_CSI1_DATA10	I	Camera pixel data
274	USBO1_EN	EIM_DATA22			
262	USBO1_OC#	EIM_DATA21	IPU2_CSI1_DATA11	I	Camera pixel data
275	LCD1_G3	EIM_EB0			
277	LCD1_G4	EIM_ADDR17	IPU2_CSI1_DATA12	I	Camera pixel data
265	LCD1_R7	EIM_DATA27	IPU2_CSI1_DATA13	I	Camera pixel data
279	LCD1_G5	EIM_ADDR18			
263	LCD1_R6	EIM_DATA26	IPU2_CSI1_DATA14	I	Camera pixel data
281	LCD1_G6	EIM_ADDR19			
114	UART1_RTS	EIM_DATA20	IPU2_CSI1_DATA15	I	Camera pixel data
283	LCD1_G7	EIM_ADDR20			
116	UART1_CTS	EIM_DATA19	IPU2_CSI1_DATA16	I	Camera pixel data
251	LCD1_R0	EIM_ADDR21			
201	I2C3_SDA (CAM)	EIM_DATA18	IPU2_CSI1_DATA17	I	Camera pixel data
253	LCD1_R1	EIM_ADDR22			
205	I2C2_SDA (DDC)	EIM_DATA16	IPU2_CSI1_DATA18	I	Camera pixel data
255	LCD1_R2	EIM_ADDR23			
207	I2C2_SCL (DDC)	EIM_EB2	IPU2_CSI1_DATA19	I	Camera pixel data
257	LCD1_R3	EIM_ADDR24			
203	I2C3_SCL (CAM)	EIM_DATA17	IPU2_CSI1_PIXCLK	I	Camera pixel clock
243	LCD1_PCLK	EIM_ADDR16			
135	TS_5	EIM_DATA29	IPU2_CSI1_VSYNC	I	Camera vertical sync
245	LCD1_VSYNC	EIM_AD12			
122	UART1_RI	EIM_EB3	IPU2_CSI1_HSYNC	I	Camera horizontal sync
247	LCD1_HSYNC	EIM_AD11			
124	UART1_DCD	EIM_DATA23	IPU2_CSI1_DATA_EN	I	Pixel data enable
249	LCD1_DE	EIM_AD10			

Table 5-63 Camera Interface Colour Pin Mapping

iMX6 Port Name	RGB565 8bit 2 cycle	RGB565 8bit 3 cycle	RGB666 8bit 3 cycle	RGB888 8bit 3 cycle	YCbCr 8bit 2 cycle	RGB565 16bit 1 cycle	YCbCr 16bit 1 cycle	YCbCr 16bit 1 cycle	YCbCr 20bit 1 cycle
IPUx_CSIx_DATA00								0	C0
IPUx_CSIx_DATA01								0	C1
IPUx_CSIx_DATA02								C0	C2
IPUx_CSIx_DATA03								C1	C3
IPUx_CSIx_DATA04						B0	C0	C2	C4
IPUx_CSIx_DATA05						B1	C1	C3	C5
IPUx_CSIx_DATA06						B2	C2	C4	C6
IPUx_CSIx_DATA07						B3	C3	C5	C7
IPUx_CSIx_DATA08						B4	C4	C6	C8
IPUx_CSIx_DATA09						G0	C5	C7	C9
IPUx_CSIx_DATA10						G1	C6	0	Y0
IPUx_CSIx_DATA11						G2	C7	0	Y1
IPUx_CSIx_DATA12	B0,G3	R2,G4,B2	R/G/B4	R/G/B0	Y/C0	G3	Y0	Y0	Y2
IPUx_CSIx_DATA13	B1,G4	R3,G5,B3	R/G/B5	R/G/B1	Y/C1	G4	Y1	Y1	Y3
IPUx_CSIx_DATA14	B2,G5	R4,G0,B4	R/G/B0	R/G/B2	Y/C2	G5	Y2	Y2	Y4
IPUx_CSIx_DATA15	B3,R0	R0,G1,B0	R/G/B1	R/G/B3	Y/C3	R0	Y3	Y3	Y5
IPUx_CSIx_DATA16	B4,R1	R1,G2,B1	R/G/B2	R/G/B4	Y/C4	R1	Y4	Y4	Y6
IPUx_CSIx_DATA17	G0,R2	R2,G3,B2	R/G/B3	R/G/B5	Y/C5	R2	Y5	Y5	Y7
IPUx_CSIx_DATA18	G1,R3	R3,G4,B3	R/G/B4	R/G/B6	Y/C6	R3	Y6	Y6	Y8
IPUx_CSIx_DATA19	G2,R4	R4,G5,B4	R/G/B5	R/G/B7	Y/C7	R4	Y7	Y7	Y9

5.20.2 Camera Serial Interface (MIPI/CSI-2)

The NXP i.MX 6 supports one quad lane MIPI/CSI-2 interface for connecting compatible cameras. The interface is compatible with single and dual lane CSI cameras. The interface uses MIPI D-PHY as the physical layer. The interface supports RGB, YUV and RAW colour space definitions. 24-bit down to 6-bit per pixel are supported.

The CSI signals are located in the type specific area of the Apalis specifications. This means that it is not guaranteed that other Apalis modules will be compatible with this interface. If you are planning to use the CSI interface, please be aware that other modules may not be compatible with your carrier board.

As the CSI is a high speed interface, some additional layout requirements need to be followed on the carrier board. These requirements are not defined in the Apalis Carrier Board Design Guide as this interface is type specific.

Table 5-64 CSI Signal Routing Requirements

Parameter	Requirement
Max Frequency	500MHz (1GT/S per data lane)
Configuration/Device Organisation	1 load
Reference Plane	GND or PWR (if PWR, add 10nF stitching capacitors between PWR and GND on both sides of the connection for the return current)
Trace Impedance	90Ω ±15% differential; 50Ω ±15% single ended
Max Intra-Pair Skew	<1ps ≈150µm
Max Trace Length Skew between clock and data lanes	<10ps ≈1.5mm
Max Trace Length from Module Connector	200mm

Table 5-65 Quad Lane CSI interface signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	CSI Signal Name	I/O	Description
163	TS_DIFF18+	CSI_CLK0_P	CSI1_CLK+	I	CSI clock
161	TS_DIFF18-	CSI_CLK0_N	CSI1_CLK-	I	
157	TS_DIFF17+	CSI_DATA0_P	CSI1_D1+	I/O	CSI data lane 1
155	TS_DIFF17-	CSI_DATA0_N	CSI1_D1-	I/O	
151	TS_DIFF16+	CSI_DATA1_P	CSI1_D2+	I	CSI data lane 2
149	TS_DIFF16-	CSI_DATA1_N	CSI1_D2-	I	
145	TS_DIFF15+	CSI_DATA2_P	CSI1_D3+	I	CSI data lane 3
143	TS_DIFF15-	CSI_DATA2_N	CSI1_D3-	I	
139	TS_DIFF14+	CSI_DATA3_P	CSI1_D4+	I	CSI data lane 4
137	TS_DIFF14-	CSI_DATA3_N	CSI1_D4-	I	

Table 5-66 Additional Camera Interface Signals (shared with parallel camera, Apalis Standard)

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
193	CAM1_MCLK	NAND_CS2_B	CCM_CLKO2	O	Master clock output for camera (shared with parallel camera interface)
201	I2C3_SDA (CAM)	EIM_DATA18	I2C3_SDA	I/O	Camera control I^2C (shared with parallel camera interface)
203	I2C3_SCL (CAM)	EIM_DATA17	I2C3_SCL	O	Camera control I^2C (shared with parallel camera interface)

5.21 Clock Output

The Apalis iMX6 provides up to two external clock outputs on the module edge connector. One output is dedicated for the camera interface while the other is for the digital audio interface. If the clock outputs are not required for those interfaces, they can also be used as general purpose clock outputs.

The NXP i.MX 6 SoC has two general purpose clock output channels (CLKO1 and CLKO2) which are available on different SoC balls. The audio codec on the module requires a reference clock which is provided by CLKO1 on the GPIO05 ball of the SoC. If the CLKO1 (available on the MXM3 pin DAP1_MCLK) is used, the internal audio master clock cannot be used. Therefore, the internal audio codec can only be used if the CLKO1 is not used externally.

Table 5-67 Clock Output Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
194	DAP1_MCLK	GPIO19	CCM_CLKO1	O	Clock output for the digital audio interface, see section 5.15, same clock source as used for on module audio code.
193	CAM1_MCLK	NAND_CS2_B	CCM_CLKO2	O	Clock output for the parallel and serial camera interface, see section 5.20

In addition to the dedicated Apalis clock output pins, the CLKO1 and CLKO2 are available as alternate functions on some other pins. Please use these pins only if the dedicated pins cannot be used due to conflicts with alternate functions of DAP1_MCLK or CAM1_MCLK. Please be aware of losing compatibility with other Apalis modules when using the alternate outputs of the clock signals.

Table 5-68 Alternate Clock Output Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
197	CAM1_HSYNC	CSI0_MCLK	CCM_CLKO1	O	Alternate output of CLKO1
84	USBH_EN	GPIO00			
96	USBH_OC#	GPIO03	CCM_CLKO2	O	Alternate output of CLKO2

The PCIe interface requires a 100MHz reference clock for all the peripherals and switches. The Apalis standard defines one differential pair for the reference clock. Zero delay clock buffers can be used if more than one reference clock sink is present on the carrier board. Since the i.MX 6 SoC features two PICe clock reference outputs, the second signal pair is available in the type specific part. Please be aware when using this second instance that other Apalis module might not feature this second PCIe clock reference output.

Table 5-69 PCIe Reference clock Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	I/O	Description
55	PCIE1_CLK+	CLK1_P	O	Apalis standard reference clock differential pair
53	PCIE1_CLK-	CLK1_N	O	
133	TS_DIFF13+	CLK2_P	O	Additional reference clock differential pair
131	TS_DIFF13-	CLK2_N	O	

5.22 Keypad

You can use any free GPIOs to realize a Matrix keypad interface. Additionally, the i.MX 6 SoC features a keyboard controller. As the keyboard controller is only available as an alternate function on

certain pins, this interface is not compatible with other Apalis modules and can only be used if the required pins are not occupied by their primary function.

The i.MX 6 keyboard controller eliminates the requirement for de-bounce capacitors and pull up resistors. It can handle up to two buttons pressed without need of de-ghosting diodes. If the diodes are available, any combination of pressed keys can be detected. The row and column pins can be configured for a keyboard matrix of up to 7 by 6, as not all signals are available at the module edge connector.

Features
- Open drain design
- Glitch suppression circuit
- Multiple-key detection
- Long key-press detection
- Standby key-press detection

Table 5-70 Keyboard Matrix Interface Signals

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
134	UART3_TXD	KEY_ROW0	KEY_ROW0	I	Keyboard row 0
138	UART4_TXD	KEY_ROW1	KEY_ROW1	I	Keyboard row 1
220	HDMI1_CEC	KEY_ROW2	KEY_ROW2	I	Keyboard row 2
16	CAN2_RX	KEY_ROW4	KEY_ROW4	I	Keyboard row 4
180	SD1_CMD	SD2_CMD			
225	SPI1_MOSI	CSI0_DATA05	KEY_ROW5	I	Keyboard row 5
4	PWM2	GPIO01			
15	GPIO7	GPIO02			
176	SD1_D2	SD2_DATA2	KEY_ROW6	I	Keyboard row 6
227	SPI1_CS	CSI0_DATA07			
186	SD1_D0	SD2_DATA0	KEY_ROW7	I	Keyboard row 7
211	I2C1_SCL	CSI0_DATA09			
136	UART3_RXD	KEY_COL0	KEY_COL0	O	Keyboard column 0
140	UART4_RXD	KEY_COL1	KEY_COL1	O	Keyboard column 1
18	CAN2_TX	KEY_COL4	KEY_COL4	O	Keyboard column 4
184	SD1_CLK	SD2_CLK			
194	DAP1_MCLK	GPIO19	KEY_COL5	O	Keyboard column 5
221	SPI1_CLK	CSI0_DATA04			
84	USBH_EN	GPIO00			
178	SD1_D3	SD2_DATA3			
2	PWM1	GPIO09	KEY_COL6	O	Keyboard column 6
223	SPI1_MISO	CSI0_DATA06			
188	SD1_D1	SD2_DATA1			
209	I2C1_SDA	CSI0_DATA08	KEY_COL7	O	Keyboard column 7
37	WAKE1_MICO	GPIO04			

5.23 Controller Area Network (CAN)

The Flexible Controller Area Network (FlexCAN) module of the NXP i.MX 6 SoC implements the CAN protocol according to the CAN 2.0B specification. It features a buffer for up to 64 messages and supports both standard and extended message frames.

Features
- Bit rate up to 1Mb/s
- Content-related addressing
- Flexible mailboxes of eight bytes data length (configurable as RX or TX)
- Powerful Rx FIFO ID filtering
- Listen-only mode
- Loop-back mode
- Time stamp based on 16bit free running timer
- Low power modes, wake up on bus activity
- Maskable interrupts

Table 5-71 CAN Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
14	CAN1_TX	GPIO07	FLEXCAN1_TX	O	CAN port 1 transmit pin
12	CAN1_RX	GPIO08	FLEXCAN1_RX	I	CAN port 1 receive pin
18	CAN2_TX	KEY_COL4	FLEXCAN2_TX	O	CAN port 2 transmit pin
16	CAN2_RX	KEY_ROW4	FLEXCAN2_RX	I	CAN port 2 receive pin

5.24 NAND

The Apalis iMX6 supports connecting up to four NAND flash devices on the carrier board. As the NAND interface is not part of the Apalis module specifications, this interface is not compatible with other Apalis modules. In the NXP documentation, the NAND interface is called General Purpose Media Interface (GPMI). It is compatible with ONFI 2.2 specifications and supports DDR mode. It is also compatible with the Samsung/Toshiba Toggle NAND protocol.

Table 5-72 NAND Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
91	TS_DIFF6+	NAND_ALE	NAND_ALE	O	Address latch enable
79	TS_DIFF4+	NAND_CS0_B	NAND_CE0_B	O	Chip Enable 0
190	SD1_CD#	NAND_CS1_B	NAND_CE1_B	O	Chip Enable 1
193	CAM1_MCLK	NAND_CS2_B	NAND_CE2_B	O	Chip Enable 2
89	TS_DIFF6-	NAND_CS3_B	NAND_CE3_B	O	Chip Enable 3
83	TS_DIFF5-	NAND_CLE	NAND_CLE	O	Command latch enable
148	MMC1_D4	NAND_DATA00	NAND_DATA00	I/O	Data signal 0
152	MMC1_D5	NAND_DATA01	NAND_DATA01	I/O	Data signal 1
156	MMC1_D6	NAND_DATA02	NAND_DATA02	I/O	Data signal 2
158	MMC1_D7	NAND_DATA03	NAND_DATA03	I/O	Data signal 3
1	GPIO1	NAND_DATA04	NAND_DATA04	I/O	Data signal 4
3	GPIO2	NAND_DATA05	NAND_DATA05	I/O	Data signal 5

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
5	GPIO3	NAND_DATA06	NAND_DATA06	I/O	Data signal 6
7	GPIO4	NAND_DATA07	NAND_DATA07	I/O	Data signal 7
95	TS_DIFF7-	SD4_DATA0	NAND_DQS	I/O	Data strobe
11	GPIO5	NAND_READY	NAND_READY	I/O	Ready signal
99	TS_3	SD4_CMD	NAND_RE_B	O	Read enable
85	TS_DIFF5+	SD4_CLK	NAND_WE_B	O	Write enable
13	GPIO6	NAND_WP_B	NAND_WP_B	O	Wait polarity

5.25 Media Local Bus (MLB150)

The Media Local Bus is predominantly used in automotive for high-bandwidth audio video and control information transport. MLB is a standardized on-PCB, inter-chip communication bus for MOST (Media Oriented Systems Transport) based devices. The MLB is not available for all variants of the i.MX 6 SoC. The industrial temperature graded versions do not feature this interface. As MLB is not part of the Apalis module specifications, the interface is not compatible with other Apalis modules. The Apalis iMX6 features a 3-pin (single ended) and a 6-pin (differential pair) interface for the MLB. Only one interface can be active at a time.

Table 5-73 MLB Signal Pins

X1 Pin#	Apalis Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
59	TS_DIFF1-	MLB_CLK_N	MLB_CLK_N	I	Differential pair clock
61	TS_DIFF1+	MLB_CLK_P	MLB_CLK_P		
65	TS_DIFF2-	MLB_DATA_N	MLB_DATA_N	I/O	Differential pair data
67	TS_DIFF2+	MLB_DATA_P	MLB_DATA_P		
71	TS_DIFF3-	MLB_SIG_N	MLB_SIG_N	I/O	Differential pair signal
73	TS_DIFF3+	MLB_SIG_P	MLB_SIG_P		
96	USBH_OC#	GPIO03	MLB_CLK	I	Single ended clock
15	GPIO7	GPIO02	MLB_DATA	I/O	Single ended data
17	GPIO8	GPIO06	MLB_SIG	I/O	Single ended signal

5.26 JTAG

The JTAG interface is not normally required for software development with the Apalis iMX6. There is always the possibility of reprogramming the module using the Recovery Mode over USB. To flash the module in recovery mode and for debug reasons, it is strongly recommended that the USBO1 interface is accessible even if not needed in the production system. Additionally, UART1 should also be accessible.

The JTAG interface is located as test points on the bottom side of the module. The location is standardised by the Apalis specification. The reference voltage for the interface is 3.3V.

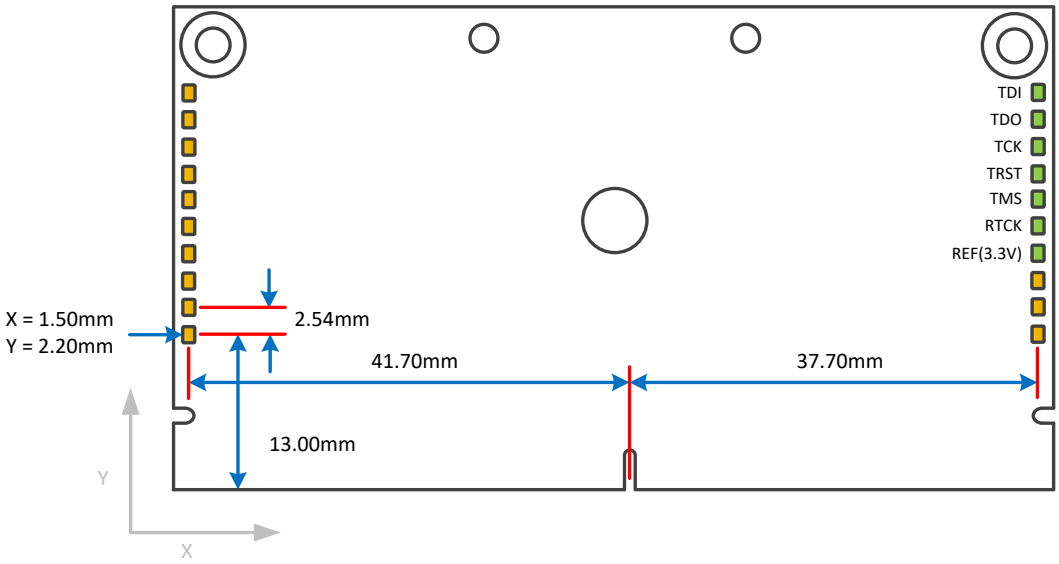


Figure 15 JTAG test point location on bottom side of module

6. Recovery Mode

The recovery mode (USB serial loader) can be used to download new software to the Apalis iMX6 even if the bootloader is no longer capable of booting the module. In the normal development process, this mode is not needed. When the module is in the recovery mode, the USBO1 interface is used to connect it to a host computer. You will find additional information at our Developer Centre: http://developer.toradex.com.

In order to enter recovery mode, the recovery mode pads need to be shorted during the initial power-on (cold boot) of the module. Figure 16 show the location of the pads that need to be shorted for entering the recovery mode.

It is also possible to enter the recovery mode by pulling up pin 63 of the module edge connector (TS_1) with a 1kΩ resistor while booting. This pin is located in the type specific area. It is not guaranteed that other Apalis modules will be able to be placed into recovery mode in the same way.

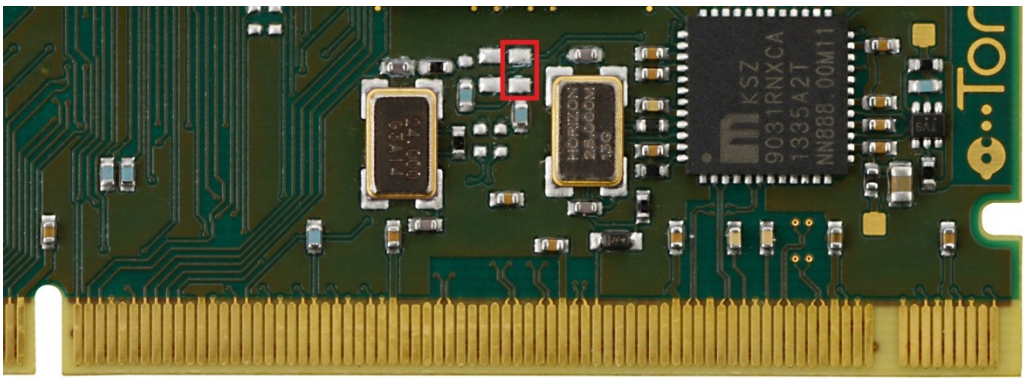


Figure 16 Location of recovery mode pads

7. Known Issues

Up-to-date information about all known hardware issues can be found in the errata document which can be downloaded on our website at:

https://developer.toradex.com/products/apalis-imx6#errata

8. Technical Specifications

8.1 Absolute Maximum Ratings

Table 8-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
Vmax_VCC	Main power supply	-0.3	3.6	V
Vmax_AVCC	Analogue power supply	-0.3	3.6	V
Vmax_VCC_BACKUP	RTC power supply	-0.3	3.6	V
Vmax_IO	IO pins with GPIO function	-0.5	3.6	V
Vmax_AN1	ADC and touch analogue input	-0.3	3.9	V
Vmax USBO1_VBUS	Input voltage at USBO1_VBUS	-0.5	5.25	V

8.2 Recommended Operation Conditions

Table 8-2 Recommended Operation Conditions

Symbol	Description	Min	Typical	Max	Unit
VCC	Main power supply	3.135	3.3	3.465	V
AVCC	Analogue power supply	3.0	3.3	3.6	V
VCC_BACKUP	RTC power supply	2.8	3.3	3.6	V

8.3 Electrical Characteristics

Table 8-3 Typical Power Consumption (room temperature)

Symbol	Description (VCC = 3.3V)	Typical Apalis iMX6Q	Typical Apalis iMX6D	Unit
IDD_IDL	CPU Idle	470	510	mA
IDD_IDL_HL	CPU Idle, Headless	360	350	mA
IDD_HIGHCPU1	Maximal CPU Load 1 Core	670	630	mA
IDD_HIGHCPU2	Maximal CPU Load 2 Cores	820	730	mA
IDD_HIGHCPU3	Maximal CPU Load 3 Cores	990	-	mA
IDD_HIGHCPU4	Maximal CPU Load 4 Cores	1160	-	mA
IDD_3D	3D-Engine with full CPU load (all cores)	1410	1400	mA
IDD_SUSPEND	Module in Suspend State	65	80	mA
IDD_BACKUP	Current consumption of internal RTC	45	45	µA

The actual power consumption can vary between different modules. The power consumption depends on the SoC temperature. As a general rule, a warmer core consumes more power as a colder. Therefore, suitable cooling solution can reduce the current consumption.

8.4 Power Ramp-Up Time Requirements

The carrier board needs to follow the power supply ramp-up requirements of the Apalis module. This specification can be found in the Apalis Carrier Board Design Guide.

8.5 Mechanical Characteristics

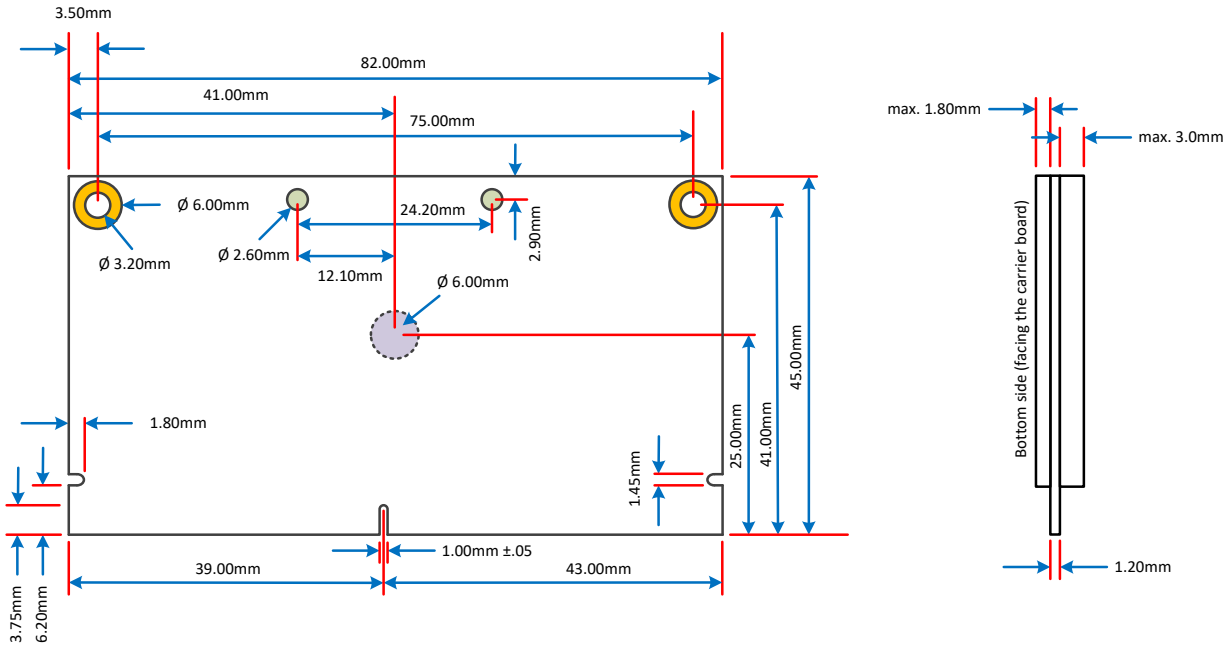


Figure 17 Mechanical dimensions of the Apalis module (top view)
Tolerance for all measures: +/- 0.1mm

The mechanical dimensions of the NXP i.MX 6 depend on the version of the SoC. The industrial temperature graded versions (IT, -40 to 85°C) feature an additional lid (heat spreader) on top of the silicon.

Figure 18 left side: commercial temperature module without lid;
right side: industrial temperature module with lid

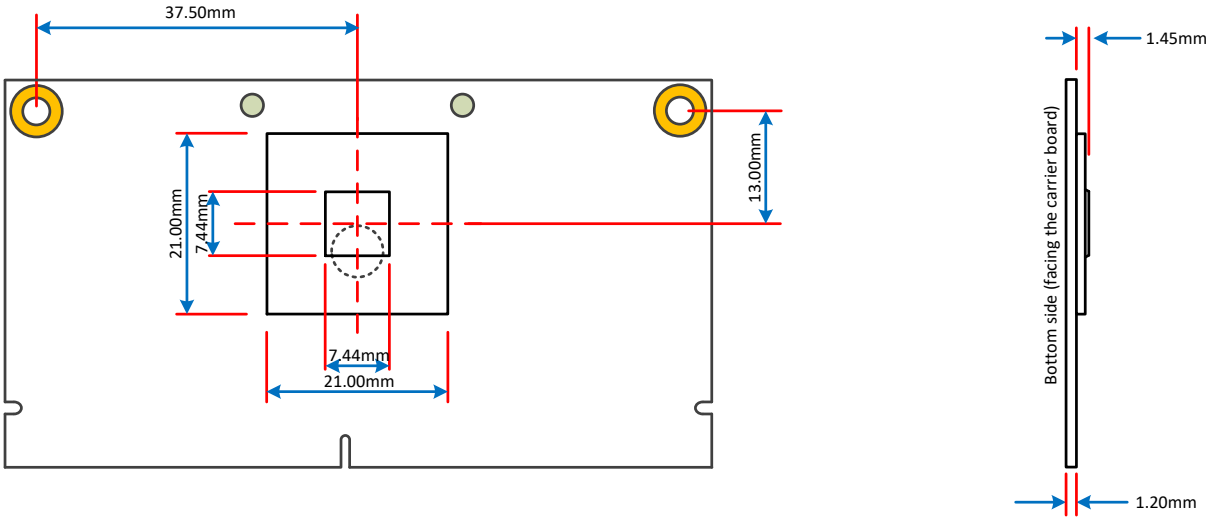


Figure 19 Mechanical position of NXP i.MX 6 commercial temperature version (top view)
Tolerance for all measures: +/- 0.1mm

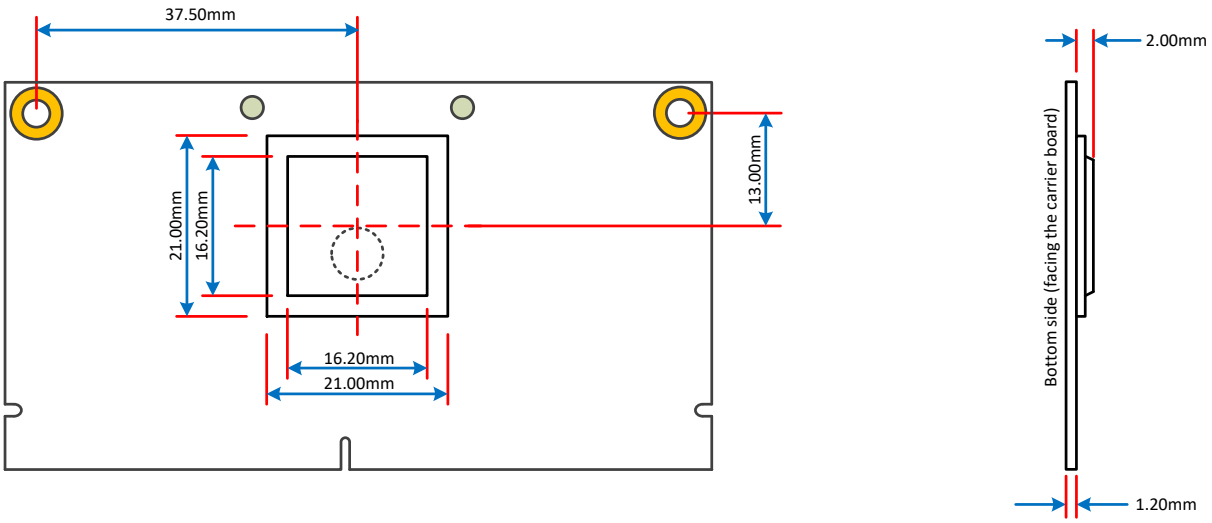


Figure 20 Mechanical position of NXP i.MX 6 industrial temperature version (top view)
Tolerance for all measures: +/- 0.1mm

8.5.1 Sockets for the Apalis Modules

The Apalis module uses the MXM3 (Mobile PCI-Express Module) edge connector. This connector is available from different manufacturers in different board to board stacking heights from 2.3mm to 11.1mm. Toradex recommends using the JAE MM70-314B1-2-R300 which has a board to board height of 3.0mm. This stacking height allows using the MXM SnapLock system for easy fixing of the module to the carrier board.

You can refer to a list of other MXM3 connectors on the developer website.

8.6 Thermal Specification

The Apalis iMX6 incorporates DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling which enables the system to continuously adjust operating frequency and voltage in

response to changes in workload and temperature. This allows the Apalis iMX6 to deliver higher performance at lower average power consumption compared to other solutions. The NXP i.MX 6 SoC has an integrated temperature sensor for monitoring the temperature of the CPU.

Here some general considerations:

- If you need the full CPU/Graphics performance over a long period of time, we recommend adding a heat sink solution.
- If you only use the peak performance for a short time period, heat dissipation is less of a problem because the advanced power management reduces power consumption when full performance is not required.
- A lower die temperature will also lower the power consumption due to smaller leakage currents.

In general, the more effective the thermal solution is, the more performance you can get out of the Apalis iMX6 Module.

Table 8-4 Thermal Specification

Module	Description	Min	Typ	Max	Unit
Apalis iMX6	Module operating temperature range	0		70[1]	°C
Apalis iMX6 IT	Module operating temperature range	-40		85[1]	°C
Apalis iMX6 Apalis iMX6 IT	Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Apalis iMX6	Junction temperature SoC	-20		105	°C
Apalis iMX6 IT	Junction temperature SoC	-40		105	°C
Apalis iMX6	Thermal Resistance Junction-to-Ambient, i.MX 6 only. (Theta-JA)[2]		22		°C/W
Apalis iMX6 IT	Thermal Resistance Junction-to-Ambient, i.MX 6 only, with lid. (Theta-JA)[2]		15		°C/W
Apalis iMX6	Thermal Resistance Junction-to-Top of i.MX 6 chip case. (Psi-JCtop)[2]			0.1	°C/W
Apalis iMX6 IT	Thermal Resistance Junction-to-Top of i.MX 6 chip case, with lid. (Psi- JCtop)[2]		1		°C/W

[1] Depending on cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-6, board mounted horizontal, natural convection.

Toradex provides a heatsink for the Apalis iMX6 modules. This solution can be used passively as well as in combination with a fan. Please check carefully which version is compatible with the according Apalis iMX6 module. Please find more information and datasheets here: http://developer.toradex.com/products/apalis-heatsink

Table 8-5 Compatible Heatsinks

Module	Heatsink Version
Apalis iMX6Q 1GB	Type 3, V1.0A
Apalis iMX6Q 2GB IT	Type 1, V1.0A
Apalis iMX6D 512MB	Type 3, V1.0A
Apalis iMX6D 1GB IT	Type 1, V1.0A

8.7 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH etc. can be found on our website at: http://www.toradex.com/support/product-compliance