

# Colibri iMX7

## Datasheet



## Revision History

Date	Doc. Rev.	Colibri iMX7 Version	Changes
16-Feb-2016	Rev. 0.9	V1.1	Initial Release
15-Jun-2016	Rev. 1.0	V1.1	Minor changes and corrections
21-Dec-2016	Rev. 1.1	V1.1	Remove SODIMM pin 157 and 163 Update maximum UART speed (section 5.10) Update maximum pixel clock frequency of Camera input (section 5.21) Information added that EPDC is currently not supported (section 5.5.6)
13-Feb-2017	Rev. 1.2	V1.1	Changed heading to "Colibri Carrier Board Schematics" (Section 1.4.6) Updated web-links (section 1.3, 1.4, and 9.3.1)
28-Aug-2017	Rev. 1.3	V1.1	Add new module variant Colibri iMX7D 1GB V1.1A with eMMC memory Minor changes and corrections
01-May-2018	Rev. 1.4	V1.1	Added typical power consumption for Colibri iMX7D 1GB (section 9.2) Updated typical power consumption for Colibri iMX7D 512MB and Colibri iMX7S (section 9.2)
16-Oct-2018	Rev. 1.5	V1.1	Section 4.2: Update drive strength information Section 4.4.1: Correction of TX_EN Section 5.3: Correction of TX_EN Section 5.16.1: Correct I2S Slave pins Section 9.2: Add GPIO parameters

## Contents

1.	Introduction .....	<b>5</b>
1.1	Hardware .....	5
1.2	Main Features .....	6
1.2.1	CPU .....	6
1.2.2	Memory .....	6
1.2.3	Interfaces .....	6
1.2.4	Supported Operating Systems .....	7
1.3	Interface Overview .....	8
1.4	Reference Documents .....	9
1.4.1	NXP (Freescale) i.MX 7 .....	9
1.4.2	Ethernet Transceiver .....	9
1.4.3	Audio Codec .....	9
1.4.4	Touch Screen Controller / ADC .....	9
1.4.5	Toradex Developer Center .....	9
1.4.6	Colibri Carrier Board Schematics .....	9
1.4.7	Toradex Pinout Designer .....	9
2.	Architecture Overview .....	<b>10</b>
2.1	Block Diagram .....	10
3.	Colibri iMX7 Connectors .....	<b>11</b>
4.	I/O Pins .....	<b>17</b>
4.1	Function Multiplexing .....	17
4.2	Pin Control .....	18
4.3	Pin Reset Status .....	19
4.4	Functions List .....	19
4.4.1	SODIMM 200 .....	20
5.	Interface Description .....	<b>23</b>
5.1	Power Signals .....	23
5.1.1	Digital Supply .....	23
5.1.2	Analogue Supply .....	23
5.1.3	Power Management Signals .....	23
5.2	GPIOs .....	24
5.2.1	Wakeup Source .....	24
5.3	Ethernet .....	24
5.4	USB .....	27
5.4.1	USB Data Signal .....	27
5.4.2	USB Control Signals .....	27
5.5	Display .....	28
5.5.1	Parallel RGB LCD interface .....	28
5.5.2	LVDS .....	31
5.5.3	HDMI .....	31
5.5.4	Analogue VGA .....	31
5.5.5	Display Serial Interface (DSI) .....	31
5.5.6	Electrophoretic Display Controller (EPDC) .....	31
5.6	PCI Express .....	32
5.7	IDE .....	32
5.8	External Memory Bus .....	32
5.8.1	Non-Multiplexed Mode .....	32
5.8.2	Multiplexed Mode .....	32
5.8.3	Memory Bus Signals .....	33
5.9	I <sup>2</sup> C .....	35
5.9.1	Real-Time Clock (RTC) recommendation .....	36
5.10	UART .....	36

5.11	SPI .....	39
5.12	PWM (Pulse Width Modulation) .....	41
5.13	OWR (One Wire) .....	43
5.14	SD/MMC .....	43
5.15	Analogue Audio .....	45
5.16	Audio Codec Interface.....	46
5.16.1	Digital Audio Port used as I <sup>2</sup> S .....	47
5.16.2	Digital Audio Port used as AC'97 .....	47
5.17	Medium Quality Sound (MQS) .....	48
5.18	S/PDIF (Sony-Philips Digital Interface I/O).....	48
5.19	Touch Panel Interface .....	48
5.20	Analogue Inputs .....	48
5.21	Camera Interface.....	49
5.22	Clock Output .....	52
5.23	Keypad .....	53
5.24	Controller Area Network (CAN).....	54
5.25	Quad Serial Peripheral Interface (QuadSPI) .....	55
5.26	JTAG .....	56
6.	Power Management.....	57
6.1	No Supply .....	57
6.2	RTC Only.....	57
6.3	Shut Down .....	58
6.4	RUN .....	58
6.5	Low Power .....	58
6.6	LPSR.....	58
7.	Recovery Mode .....	59
8.	Known Issues.....	60
9.	Technical Specifications .....	61
9.1	Absolute Maximum Ratings .....	61
9.2	Electrical Characteristics .....	61
9.3	Mechanical Characteristics .....	62
9.3.1	Sockets for the Colibri Modules .....	62
9.4	Thermal Specification.....	63
9.5	Product Compliance.....	63

## 1. Introduction

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### 1.1 Hardware

The Colibri iMX7 is a computer module based on the NXP®/Freescale i.MX 7 embedded System on Chip (SoC). The SoC features a single or dual-core ARM® Cortex® A7 processor with an additional ARM Cortex M4 processor. This heterogeneous dual-core system allows for running a second real-time operating system on the M4 core for time and security critical tasks.

Despite the relative high computing performance, the Colibri iMX7 is designed for extremely low-power consumption. The module features several low-power modes that reduce the consumption in idle and sleep states.

The module targets a wide range of applications, including: medical devices, navigation, industrial automation, HMIs, avionics, POS, data acquisition, robotics and much more.

It offers a wide range of interfaces from simple GPIOs, industry standard I2C, SPI, CAN, and UART buses to high-speed USB 2.0 interfaces and a 16-bit external memory bus (multiplexed parallel bus). Both Colibri iMX7 modules feature a Fast Ethernet PHY with IEEE1588 time stamping on the module. Additionally, the Colibri iMX7D allows connecting an additional (gigabit) Ethernet PHY on the customer carrier board by using the RGMII, RMII, or MII interface.

The Colibri iMX7 module encapsulates the complexity associated with modern day electronic design, such as high-speed impedance controlled layouts with high component density utilising blind and buried via technology. This allows the customer to create a simple carrier board which provides his application-specific electronics. The module is compatible with a wide range of other computer modules within the Colibri family. This allows the customer to scale their product without the need to build different carrier boards for each project.

## 1.2 Main Features

### 1.2.1 CPU

	Colibri iMX7D 1GB	Colibri iMX7D 512MB	Colibri iMX7S 256MB
NXP SoC	MCIMX7D5EVM10S	MCIMX7D5EVM10S	MCIMX7S5EVM08S
SoC Family	i.MX 7 Dual	i.MX 7 Dual	i.MX 7 Solo
ARM Cortex-A7 CPU Cores	2	2	1
ARM Cortex-M4 CPU Cores	1	1	1
L1 Instruction Cache (each core)	32KByte (A7) 16KByte (M4)	32KByte (A7) 16KByte (M4)	32KByte (A7) 16KByte (M4)
L1 Data Cache (each core)	32KByte (A7) 16KByte (M4)	32KByte (A7) 16KByte (M4)	32KByte (A7) 16KByte (M4)
L2 Cache (shared by A7 cores)	512KByte (A7)	512KByte (A7)	512KByte (A7)
Tightly-Coupled Memory for M4 Core	64KByte (M4)	64KByte (M4)	64KByte (M4)
NEON MPE	✓	✓	✓
Maximum CPU frequency	1GHz (A7) 200MHz (M4)	1GHz (A7) 200MHz (M4)	800MHz (A7) 200MHz (M4)
ARM TrustZone	✓	✓	✓
Advanced High Assurance Boot	✓	✓	✓
Cryptographic Acceleration and Assurance Module	✓	✓	✓
Secure Real-Time Clock	✓	✓	✓
Secure JTAG Controller	✓	✓	✓

### 1.2.2 Memory

	Colibri iMX7D 1GB	Colibri iMX7D 512MB	Colibri iMX7S 256MB
DDR3L RAM Size	1GByte	512MByte	256MByte
DDR3L RAM Speed	1066MT/s	1066MT/s	1066MT/s
DDR3L RAM Memory Width	32bit	32bit	32bit
SLC NAND Flash (8bit)*		512MByte	512MByte
eMMC NAND Flash (8bit)*	4GByte		

\* eMMC is based on MLC NAND flash memory. As with all flash memories (this includes SLC NAND Flash), the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear levelling in the eMMC controller makes sure the cells are getting worn out evenly. More information can be found here <http://developer.toradex.com/knowledge-base/flash-memory> and here [https://en.wikipedia.org/wiki/Flash\\_memory#Write\\_endurance](https://en.wikipedia.org/wiki/Flash_memory#Write_endurance).

### 1.2.3 Interfaces

	Colibri iMX7D 1GB	Colibri iMX7D 512MB	Colibri iMX7S 256MB
LCD RGB (24bit, 150MHz)	1	1	1
Resistive Touch Screen	4 Wire	4 Wire	4 Wire
Analogue Audio Headphone out	1 (Stereo)	1 (Stereo)	1 (Stereo)
Analogue Audio Line in	1 (Stereo)	1 (Stereo)	1 (Stereo)
Analogue Audio Mic in	1 (Mono)	1 (Mono)	1 (Mono)
SAI (AC97/I <sup>2</sup> S)	2* (Stereo)	2* (Stereo)	2* (Stereo)

	Colibri iMX7D 1GB	Colibri iMX7D 512MB	Colibri iMX7S 256MB
Medium Quality Sound (MQS)	1*	1*	1*
Parallel Camera Interface	1	1	1
I2C	1+2*	1+2*	1+2*
SPI	1+3*	1+3*	1+3*
UART	3+4*	3+4*	3+4*
SD/SDIO/MMC	1+1*	1+1*	1+1*
GPIO	Up to 126	Up to 124	Up to 124
USB 2.0 OTG (host/device)	1	1	1
USB 2.0 host	1	1	-
10/100 MBit/s Ethernet	1	1	1
RGMII/RMII/MII interface for 2 <sup>nd</sup> Ethernet PHY on Baseboard	1	1	-
PWM	4+16*	4+16*	4+16*
Analogue Inputs (maximum 1.8V)	4	4	4
CAN	2*	2*	2*
External Memory Bus	16bit Multiplexed*	16bit Multiplexed*	16bit Multiplexed*
QSPI	2*	2*	2*
SIM	4*	4*	4*

\*These additional interfaces are available on pins that are not defined as standard interfaces in the Colibri architecture. They are alternate functions for pins which provide primary interfaces. There are restrictions on using different interfaces simultaneously. Please check the available alternate functions to understand any constraints. For more information, please also check the list in section 4.4.1 and the description of the associated interface in section 5.

#### 1.2.4 Supported Operating Systems

- ✓ Windows Embedded Compact 7 (Q4 2016)
- ✓ Windows Embedded Compact 2013 (Q4 2016)
- ✓ Embedded Linux
- ✓ Green Hills Integrity available through Toradex partners
- ✓ For other operating systems, please contact Toradex

### 1.3 Interface Overview

The table in Figure 1 shows the interfaces that are supported on the Colibri iMX7 module, and whether an interface is provided as a standard (primary) function or as an alternate function. The UART interface is an example of an interface that makes use of standard and alternate functions – three UART interfaces are provided as standard functions which are compatible with other Colibri modules while four additional interfaces are available as alternate functions. Using alternate function UART interfaces limits the compatibility of the Colibri iMX7 module with other Colibri modules. The alternate function of a pin can only be used if the standard function is not used. Check section 4.4 for a list of all alternate functions of the SODIMM pins. The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Colibri iMX7 Module. The tool allows comparing the interfaces of different Colibri modules. More information to this tool can be found here: <http://developer.toradex.com/carrier-board-design/pinout-designer-tool>

Feature	Total	Standard	Alternate Function
4 Wire Resistive Touch	1	1	
Analogue Inputs	4	4 (limited to 1.8V)	
Analogue Audio (Line in/out, Mic in)	1	1	
Medium Quality Sound (MQS)	1		1
CAN	2		2
Fast Ethernet	1	1	
RGMI/II/MII interface	1*		1*
GPIO	126*		126*
SAI (AC97/I <sup>2</sup> S)	2		2
I2C	3	1	2
Parallel Camera	1	1	
Parallel LCD	1	1	
PWM	20	4	16
SD/SDIO/MMC	2	1	1
SPI	4	1	3
UART	7	3	4
USB 2.0 OTG (host/device)	1	1	
USB 2.0 host	1*	1*	
External Memory Bus 16 bit multiplexed	1		1
QSPI	2		2
SIM	4		4

Figure 1: Colibri iMX7 Module Interfaces

\*These interfaces are not available on all versions of the Colibri iMX7 module. Please see section 0 for more information.



## 1.4 Reference Documents

### 1.4.1 NXP (Freescale) i.MX 7

You will find the details about i.MX 7 SoC in the Datasheet and Reference Manual provided by NXP.  
<http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/i.mx-applications-processors-based-on-arm-cores/i.mx-7-processors:IMX7-SERIES>

### 1.4.2 Ethernet Transceiver

Colibri iMX7 uses the Microchip/Micrel KSZ8041NL Ethernet PHY:  
<http://www.microchip.com/wwwproducts/en/KSZ8041>

### 1.4.3 Audio Codec

Colibri iMX7 uses the NXP SGT5000 Audio Codec.  
<http://www.nxp.com/products/interface-and-connectivity/interface-and-system-management/switch-monitoring-ics/ultra-low-power-audio-codec:SGTL5000>

### 1.4.4 Touch Screen Controller / ADC

Colibri iMX7 uses the Analog Device AD7879-1 Touchscreen Controller.  
<http://www.analog.com/en/products/analog-to-digital-converters/integrated-special-purpose-converters/capacitive-to-digital-and-touch-screen-controllers/ad7879.html>

### 1.4.5 Toradex Developer Center

You can find a lot of additional information on the Toradex Developer Center, which is regularly updated with the latest product support information.

Please note that the Developer Center is common for all Toradex products. You should always check to ensure if information is valid or relevant for the Colibri iMX7.  
<http://developer.toradex.com>

### 1.4.6 Colibri Carrier Board Schematics

We provide the complete schematics and the Altium project file (which includes library symbols and IPC-7351 compliant footprints for the Colibri Evaluation Board and other Carrier Boards free of charge. This is a great help when designing your own Carrier Board.  
<http://developer.toradex.com/carrier-board-design/reference-designs>

### 1.4.7 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Apalis and Colibri Modules. The tool allows comparing the interfaces of different modules.  
<http://developer.toradex.com/carrier-board-design/pinout-designer-tool>

## 2. Architecture Overview

### 2.1 Block Diagram

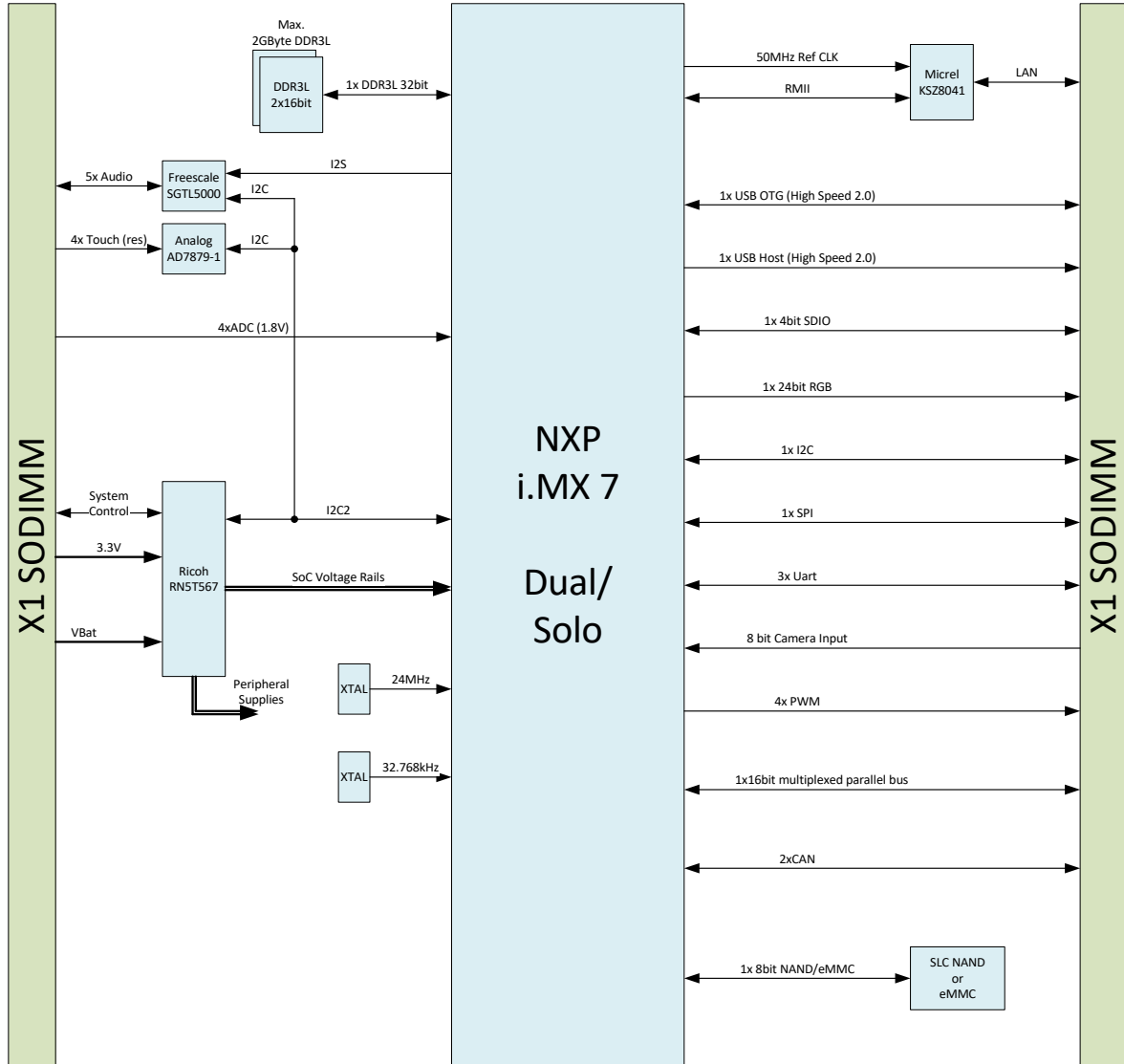


Figure 2 Colibri iMX7 Block Diagram

### 3. Colibri iMX7 Connectors

The Colibri iMX7 is equipped with a 200-Pin SODIMM edge connector (X1). The table below details the SODIMM 200-way connector pin functionality.

It should be noted that some of the pins are multiplexed; that is, there is more than one i.MX 7 SoC pin connected to one SODIMM pin. For example, ECSPi2\_SCLK and GPIO1\_IO11 are both connected to SODIMM pin 67. Care should be taken to ensure that multiplexed pins are tri-stated when they are not being used (e.g. if i.MX 7 pin A and pin B are tied to SODIMM pin 1, then if i.MX 7 pin A is being driven, pin B should be tri-stated). Additional information can be found in chapter 4.1: Function Multiplexing.

Please note, the maximum voltage of the ADC input (Pin 2, 4, 6, and 8) is only 1.8V. Other Colibri modules allow input voltages up to 3.3V.

- X1 Pin: Pin number on the SODIMM connector (X1).
- Compatible function: The default function which is compatible with all Colibri modules. **IMPORTANT:** There are a few limitations. You can find more information about pin compatibility in the “**Colibri Compatibility Guide**”.
- i.MX 7 CPU Ball: The name of the ball (a.k.a. pin) of the i.MX 7 SoC.
- Non i.MX 7 CPU Ball: Peripheral functions which are not directly provided by the i.MX 7 SoC.
- Note: Additional information. Some pins are noted as “no standard function”. These pins can provide only the GPIO functionality and the listed alternate function, but not the Colibri compatible function. Some of the Colibri compatible functions might be emulated by programmatically manipulating the GPIO.

Table 3-1 X1 Connector

X1 Pin	Compatible Function	i.MX 7 Ball	Non i.MX 7 Ball	Note
1	Audio Analogue Microphone Input		MIC_IN	SGTL5000 Pin 10
3	Audio Analogue Microphone GND		MIC_GND	GND switched, controlled with GPIO6_IO21
5	Audio Analogue Line-In Left		LINEIN_L	SGTL5000 Pin 9
7	Audio Analogue Line-In Right		LINEIN_R	SGTL5000 Pin 8
9	Audio_Analogue GND		VSS_AUDIO	GND
11	Audio_Analogue GND		VSS_AUDIO	GND
13	Audio Analogue Headphone GND		HEADPHONE_GND	Virtual GND, do not connect to normal GND
15	Audio Analogue Headphone Left		HEADPHONE_L	SGTL5000 Pin 4
17	Audio Analogue Headphone Right		HEADPHONE_R	SGTL5000 Pin 1
19	UART_C RXD	UART3_TXD		
21	UART_C TXD	UART3_RXD		
23	UART_A DTR	SD2_DATA0		no standard function
25	UART_A CTS, Keypad_In<0>	SAI2_TXFS		
27	UART_A RTS	SAI2_TXC		
29	UART_A DSR	GPIO1_IO07		no standard function
31	UART_A DCD	SD2_DATA1		no standard function
33	UART_A RXD	UART1_TXD		
35	UART_A TXD	UART1_RXD		

X1 Pin	Compatible Function	i.MX 7 Ball	Non i.MX 7 Ball	Note
37	UART_A RI, Keypad_In<4>	GPIO1_IO06		no standard function
39	GND		GND	
41	GND		GND	
43	WAKEUP Source<0>, SDCard CardDetect	GPIO1_IO00		no standard function
45	WAKEUP Source<1>	GPIO1_IO01		no standard function
47	SDCard CLK	SD1_CLK		IO voltage 3.3V/1.8V (see also section 5.14)*
49	SDCard DAT<1>	SD1_DATA1		IO voltage 3.3V/1.8V (see also section 5.14)*
51	SDCard DAT<2>	SD1_DATA2		IO voltage 3.3V/1.8V (see also section 5.14)*
53	SDCard DAT<3>	SD1_DATA3		IO voltage 3.3V/1.8V (see also section 5.14)*
55	PS2 SDA1	ENET1_RD3		no standard function
57	LCD RGB Data<16>	LCD_DAT16		
59	PWM<A>, Camera Input Data<7>	ECSPI2_MOSI/ GPIO1_IO08		Multiplexed (Two i.MX 7 Pins)
61	LCD RGB Data<17>	LCD_DAT17		
63	PS2 SCL1	ENET1_RD2		no standard function
65	Camera Input Data<9>, Keypad_Out<3>, PS2 SDA2	ECSPI2_SS0		Only camera input supported
67	PWM<D>, Camera Input Data<6>	ECSPI2_SCLK/ GPIO1_IO11		Multiplexed (Two i.MX 7 Pins)
69	PS2 SCL2	SD1_CD_B		no standard function, IO voltage 3.3V/1.8V (see also section 5.14)*
71	Camera Input Data<0>, LCD Back-Light GPIO	SD1_WP		no standard function, IO voltage 3.3V/1.8V (see also section 5.14)*
73		SD1_RESET_B		IO voltage 3.3V/1.8V (see also section 5.14)*
75	Camera Input MCLK	I2C4_SDA		
77		SAI1_RXFS		
79	Camera Input Data<4>	ECSPI1_MISO		
81	Camera Input VSYNC	I2C3_SCL		
83	GND		GND	
85	Camera Input Data<8>, Keypad_Out<4>	ECSPI2_MISO		Only camera input supported
87	nReset Out		PMIC Reset Out	
89	nWE	EPDC_D9		
91	nOE	EPDC_D8	Recovery glue logic	Pull to GND while releasing reset for entering the Serial loader
93	RDnWR	LCD_RESET		no standard function
95	RDY	EPDC_D13		
97	Camera Input Data<5>	ECSPI1_SS0		
99	nPWE	ENET1_TXC		no standard function
101	Camera Input Data<2>	ECSPI1_SCLK		

X1 Pin	Compatible Function	i.MX 7 Ball	Non i.MX 7 Ball	Note
103	Camera Input Data<3>	ECSPI1_MOSI		
105	nCS0	EPDC_D10		
107	nCS1	EPDC_D15		
109	GND		GND	
111	ADDRESS0	EPDC_D0		
113	ADDRESS1	EPDC_D1		
115	ADDRESS2	EPDC_D2		
117	ADDRESS3	EPDC_D3		
119	ADDRESS4	EPDC_D4		
121	ADDRESS5	EPDC_D5		
123	ADDRESS6	EPDC_D6		
125	ADDRESS7	EPDC_D7		
127		EPDC_SDCE2		
129	USB Host Power Enable	UART3_CTS		
131	Usb Host Over-Current Detect	UART3_RTS		
133		EPDC_GDRL		
135	SPDIF_IN	GPIO1_IO02		no standard function
137	USB Client Cable Detect, SPDIF_OUT	USB_OTG1_VBUS/ ENET1_CRCS		Multiplexed (Two i.MX 7 Pins), only USB VBUS function supported
139	USB Host DP	USB_OTG2_DP		<b>Not available on Solo</b>
141	USB Host DM	USB_OTG2_DN		<b>Not available on Solo</b>
143	USB Client DP	USB_OTG1_DP		
145	USB Client DM	USB_OTG1_DN		
147	GND		GND	
149	DATA0			no connection
151	DATA1			no connection
153	DATA2			no connection
155	DATA3			no connection
157	DATA4	SAI1_TXC		<b>Only available on iMX7D 1GB</b>
159	DATA5			no connection
161	DATA6			no connection
163	DATA7	SAI1_TXD		<b>Only available on iMX7D 1GB</b>
165	DATA8			no connection
167	DATA9			no connection
169	DATA10	SAI1_RXD		no standard function
171	DATA11			no connection
173	DATA12			no connection
175	DATA13			no connection
177	DATA14			no connection
179	DATA15			no connection
181	GND		GND	

X1 Pin	Compatible Function	i.MX 7 Ball	Non i.MX 7 Ball	Note
183	Ethernet Link/Activity Status		LINK_AKT	KSZ8041 LED0
185	Ethernet Speed Status		SPEED100	KSZ8041 LED1
187	Ethernet TXO-		TXO-	KSZ8041 Pin 6
189	Ethernet TXO+		TXO+	KSZ8041 Pin 7
191	Ethernet GND		AGND_LAN	
193	Ethernet RXI-		RXI-	KSZ8041 Pin 4
195	Ethernet RXI+		RXI+	KSZ8041 Pin 5
197	GND		GND	
199	GND		GND	
2	Analogue Input <3>	ADC1_IN3		<b>Maximum input voltage 1.8V</b>
4	Analogue Input <2>	ADC1_IN2		<b>Maximum input voltage 1.8V</b>
6	Analogue Input <1>	ADC1_IN1		<b>Maximum input voltage 1.8V</b>
8	Analogue Input <0>	ADC1_IN0		<b>Maximum input voltage 1.8V</b>
10	Audio_Analogue VDD		AVDD_AUDIO	3.3V Supply
12	Audio_Analogue VDD		AVDD_AUDIO	3.3V Supply
14	Resistive Touch PX		TSPX	AD7819 Ball A3
16	Resistive Touch MX		TSMX	AD7819 Ball C3
18	Resistive Touch PY		TSPY	AD7819 Ball B3
20	Resistive Touch MY		TSMY	AD7819 Ball D3
22	VDD Fault Detect	GPIO1_IO03		no standard function
24	Battery Fault Detect	SAI1_RXC		no standard function
26	nReset In		Reset input	
28	PWM<B>	GPIO1_IO09		
30	PWM<C>	GPIO1_IO10		
32	UART_B CTS	SAI2_RXD		
34	UART_B RTS	SAI2_TXD		
36	UART_B RXD	UART2_TXD		
38	UART_B TXD	UART2_RXD		
40	VCC_BATT		VCC_BATT	RTC supply
42	3V3		3V3	
44	LCD RGB DE	LCD_ENABLE		
46	LCD RGB Data<7>	LCD_DAT7		
48	LCD RGB Data<9>	LCD_DAT9		
50	LCD RGB Data<11>	LCD_DAT11		
52	LCD RGB Data<12>	LCD_DAT12		
54	LCD RGB Data<13>	LCD_DAT13		
56	LCD RGB PCLK	LCD_CLK		
58	LCD RGB Data<3>	LCD_DAT3		
60	LCD RGB Data<2>	LCD_DAT2		
62	LCD RGB Data<8>	LCD_DAT8		

X1 Pin	Compatible Function	i.MX 7 Ball	Non i.MX 7 Ball	Note
64	LCD RGB Data<15>	LCD_DAT15		
66	LCD RGB Data<14>	LCD_DAT14		
68	LCD RGB HSYNC	LCD_HSYNC		
70	LCD RGB Data<1>	LCD_DAT1		
72	LCD RGB Data<5>	LCD_DAT5		
74	LCD RGB Data<10>	LCD_DAT10		
76	LCD RGB Data<0>	LCD_DAT0		
78	LCD RGB Data<4>	LCD_DATA4		
80	LCD RGB Data<6>	LCD_DAT6		
82	LCD RGB VSYNC	LCD_VSYNC		
84	3V3		3V3	
86	SPI CS	I2C2_SDA		
88	SPI CLK	I2C2_SCL		
90	SPI RXD	I2C1_SCL		
92	SPI TXD	I2C1_SDA		
94	Camera Input HSYNC	I2C3_SDA		
96	Camera Input PCLK	I2C4_SCL		
98	Camera Input Data<1>	SD2_RESET_B		no standard function
100	Keypad_Out<1>	SD2_DATA2		no standard function
102		SD2_DATA3		no standard function
104		EPDC_GDSP		no standard function
106	nCS2	EPDC_BDR0		no standard function
108	3V3		3V3	
110	ADDRESS8	EPDC_BDR1		
112	ADDRESS9	EPDC_PWRCOM		
114	ADDRESS10	EPDC_SDCLK		
116	ADDRESS11	EPDC_SDLE		
118	ADDRESS12	EPDC_SDOE		
120	ADDRESS13	EPDC_SDSHR		
122	ADDRESS14	EPDC_SDCE0		
124	ADDRESS15	EPDC_SDCE1		
126	DQM0	EPDC_D14		
128	DQM1	EPDC_PWRSTAT		
130	DQM2	EPDC_SDCE3		no standard function
132	DQM3	EPDC_GDCLK		no standard function
134	ADDRESS25	EPDC_GDOE		no standard function
136	ADDRESS24	LCD_DAT18		no standard function
138	ADDRESS23	LCD_DAT19		no standard function
140	ADDRESS22	LCD_DAT20		no standard function
142	ADDRESS21	LCD_DAT21		no standard function
144	ADDRESS20	LCD_DAT22		no standard function
146	ADDRESS19	LCD_DAT23		no standard function
148	3V3		3V3	

X1 Pin	Compatible Function	i.MX 7 Ball	Non i.MX 7 Ball	Note
150	DATA16	EPDC_D12		
152	DATA17	EPDC_D11		
154	DATA18			no connection
156	DATA19			no connection
158	DATA20			no connection
160	DATA21			no connection
162	DATA22			no connection
164	DATA23			no connection
166	DATA24			no connection
168	DATA25			no connection
170	DATA26			no connection
172	DATA27			no connection
174	DATA28			no connection
176	DATA29			no connection
178	DATA30	GPIO1_IO15		no standard function
180	DATA31			no connection
182	3V3		3V3	
184	ADDRESS18	SD2_CLK		no standard function
186	ADDRESS17	SD2_CMD		no standard function
188	ADDRESS16	GPIO1_IO14		no standard function
190	SDCard CMD	SD1_CMD		IO voltage 3.3V/1.8V (see also section 5.14)*
192	SDCard DAT<0>	SD1_DATA0		IO voltage 3.3V/1.8V (see also section 5.14)*
194	I2C SDA	ENET1_TD3		
196	I2C SCL	ENET1_TD2		
198	3V3		3V3	
200	3V3		3V3	

\*It is possible to change the IO voltage of the main SD interface from 3.3V (default) to 1.8V in order to support SD UHS-I speeds. Please note that the voltage can only be changed for all the pins simultaneously, and not individually. Therefore, use these pins with care. More information can be found in section 5.14.



## 4. I/O Pins

### 4.1 Function Multiplexing

Each NXP i.MX 7 SoC I/O pin can be configured to one of the up to nine alternate functions. Most of the pins can also be used as “normal” GPIOs (General Purpose I/O, sometimes also referred to as Digital I/O). For example the i.MX7 signal pin on the SODIMM pin 33 has the primary function `uart1.TX` (Colibri standard function `UART_A_RXD`), but can also provide the following alternate functions: `gpio4.IO[1]` (GPIO), `i2c1.SDA` (I<sup>2</sup>C interface), `sai3.MCLK` (digital audio interface), `ecspi1.SS2` (SPI interface), or `enet2.1588_EVENT0_OUT` (Ethernet interface).

The default setting for this pin is the primary function `uart1.TX`. It is strongly recommended that whenever it’s possible to use the primary interfaces before using any alternate interfaces. This ensures the best compatibility between the Toradex standard software, operating systems/BSPs, and other modules in the Colibri family.

Most of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behaviour.

In the table in chapter 4.4 you will find a list of all pins which have alternate functions. There you can find which alternate functions are available for each individual pin.

Some of the i.MX 7 pins are paired and share the same SODIMM pin. When using one of these pins, make sure that the unused pin of each multiplexed pair is tri-stated or configured as input to avoid undesired behaviour and/or hardware damage. The following table lists all SODIMM pins that have more than one i.MX 7 pin connected:

Table 4-1 Multiplexed pins

X1 Pin #	i.MX 7 Pin 1	i.MX 7 Pin 2	Remarks
59	ECSPI2_MOSI	GPIO1_IO08	
67	ECSPI2_SCLK	GPIO1_IO11	
137	USB_OTG1_VBUS	ENET1_CRS	USB_OTG1_VBUS is always an input and cannot be used as GPIO. ENET1_CRS is placed in order to provide the GPIO functionality to pin 137
91	EPDC_D8	BOOT_MODE0 (Recovery glue logic)	The glue logic allows entering the serial loader by pulling down pin 91 while releasing the reset.

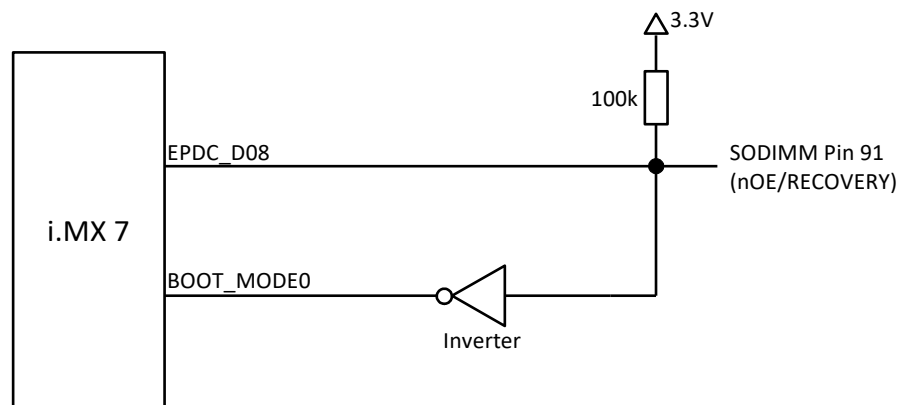


Figure 3: Recovery Glue Logic

## 4.2 Pin Control

The alternate function of each pin can be changed independently. Every pin has a Pad Mux Register in which the following settings can be configured (some settings might not be available for certain pins). The register is called IOMUXC\_SW\_MUX\_CTL\_PAD\_x where x is the name of the i.MX 7 pin. More information about the available register settings can be found in the i.MX 7 Reference Manual.

Table 4-2 Pad Mux Register

Bit	Field	Description	Remarks
31-5	Reserved		
4	SION	0 Software Input On Field disabled 1 Software Input On Field enabled	Force the selected mux mode input path
3-0	MUX_MODE	0000 Select mux mode: ALT0 mux port 0001 Select mux mode: ALT1 mux port 0010 Select mux mode: ALT2 mux port 0011 Select mux mode: ALT3 mux port 0100 Select mux mode: ALT4 mux port 0101 Select mux mode: ALT5 mux port (GPIO) 0110 Select mux mode: ALT6 mux port 0111 Select mux mode: ALT7 mux port 1000 Select mux mode: ALT8 mux port	Check chapter 4.4 for the available alternate function of the pin

The pins have an additional register which allows configuration of pull up/down resistors, drive strength, and other settings. The register is called IOMUXC\_SW\_PAD\_CTL\_PAD\_x where x is the name of the i.MX 7 pin. Some settings might not be available on certain pins. More information about the available register settings can be found in the i.MX 7 Reference Manual.

Table 4-3 Pad Control Register

Bit	Field	Description	Remarks
31-7	Reserved		
6-5	PS	00 100 kOhm Pull Down 01 5 kOhm Pull Up 10 47 kOhm Pull Up 11 100 kOhm Pull Up	
4	PE	0 Pull Disabled 1 Pull Enabled	Enable pull up/down function
3	HYS	0 Hysteris Disabled (CMOS input) 1 Hysteris Enabled (Schmitt trigger input)	
2	SRE	0 Fast Slew Rate 1 Slow Slew Rate	Use slow slew rate if possible for reducing EMC problems
1-0	DSE	00 Drive strength X1 01 Drive strength X4 10 Drive strength X2 11 Drive strength X6	If possible decrease the drive strength by increasing the resistance in order to reduce EMC problems. X1 is the weakest drive strength level while X6 is the strongest.

Input functions that are available at more than one physical pin require an additional input multiplexer. This multiplexer is configured by a register called IOMUXC\_x\_SELECT\_INPUT where x is the name of the input function. More information about this register can be found in the i.MX 7 Reference Manual.

### 4.3 Pin Reset Status

After a reset, the pins can be at any of the different modes. Most of them are configured as GPIO input with a 100k pull down resistor enabled. Please check the table in chapter 4.4 for the reset states for each of the pins. For pins that are not configured as GPIO by default, please check the i.MX 7 Reference Manual for the corresponding default configuration state. As soon as the bootloader is executing, it is possible to reconfigure the pins and their states.

Please be aware, the pin reset status is only guaranteed during the release of the reset signal. During the power up sequence, the states of the pins might be undefined until the IO bank voltage is enabled on the module.

### 4.4 Functions List

Below is a list of all the i.MX7 pins which are available on the SODIMM connector. It shows the alternate functions that are available for each pin. For most of the pins, the GPIO functionality is defined as the ALT5 function. The alternate functions which are used to provide the primary interfaces to ensure best compatibility with other Colibri modules are highlighted.

#### Function Short Forms

CAN:	Controller Area Network
CCM:	Clock Control Module
CSI:	Camera Sensor Interface
ECSPI:	Enhanced Configurable Serial Peripheral Interface Bus
ENET:	Ethernet MAC interface
EPDC:	Electrophoretic Display Controller (Electronic Paper Display)
FLEXTIMER:	Flexible Timer Module
GPIO:	General Purpose Input Output
GPT:	General Purpose Timer
I2C:	Inter Integrated Circuit
KPP:	Keypad Port
LCDIF:	LCD Interface
MQS:	Medium Quality Sound
PWM:	Pulse Width Modulation output
QSPI:	Quad Serial Peripheral Interface
RAWNAND:	Interface for NAND Flash
SAI:	Serial Interface for Audio (I2S and AC97)
SIM:	Subscriber Identification Module
UART:	Universal Asynchronous Receiver/Transmitter
USB:	Universal Serial Bus
USDHC:	Ultra-Secured Digital Host Controller (interface for SD and MMC cards)
WDOG:	Watchdog Timer
WEIM:	External Interface Module (External Memory Bus)

### 4.4.1 SODIMM 200

X1 Pin	i.MX7 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Reset State	Pull
19	UART3_TXD	uart3.TX	usb.OTG1_PWR	sai3.TX_BCLK	ecspi1.MOSI	enet1.1588_EVENT0_OUT	gpio4.IO[5]	usdhc2.LCTL			ALT5	100k PD
21	UART3_RXD	uart3.RX	usb.OTG1_OC	sai3.RX_SYNC	ecspi1.MISO	enet1.1588_EVENT0_IN	gpio4.IO[4]	usdhc1.LCTL			ALT5	100k PD
23	SD2_DATA0	usdhc2.DATA0	sai2.RX_DATA[0]	uart4.RX	gpt4.CAPTURE2	sim2.PORT1_CLK	gpio5.IO[14]				ALT5	100k PD
25	SAI2_TXFS	sai2.TX_SYNC	ecspi3.MISO	uart4.RX	uart1.CTS_B	flextimer2.CH[4]	gpio6.IO[19]				ALT5	100k PD
27	SAI2_TXC	sai2.TX_BCLK	ecspi3.MOSI	uart4.TX	uart1.RTS_B	flextimer2.CH[5]	gpio6.IO[20]				ALT5	100k PD
29	GPIO1_IO07	gpio1.IO[7]	usb.OTG2_PWR*	flextimer1.CH[7]	uart5.TX	i2c2.SDA		kpp.COL[4]			ALT0	100k PD
31	SD2_DATA1	usdhc2.DATA1	sai2.TX_BCLK	uart4.TX	gpt4.COMPARE1	sim2.PORT1_RST_B	gpio5.IO[15]				ALT5	100k PD
33	UART1_TXD	uart1.TX	i2c1.SDA	sai3.MCLK	ecspi1.SS2	enet2.1588_EVENT0_OUT*	gpio4.IO[1]	enet1.MDC			ALT5	100k PD
35	UART1_RXD	uart1.RX	i2c1.SCL	gpc.PMIC_RDY	ecspi1.SS1	enet2.1588_EVENT0_IN*	gpio4.IO[0]	enet1.MDIO			ALT5	100k PD
37	GPIO1_IO06	gpio1.IO[6]	usb.OTG2_OC*	flextimer1.CH[6]	uart5.RX	i2c2.SCL		kpp.ROW[4]			ALT0	100k PD
43	GPIO1_IO00	gpio1.IO[0]	pwm4.OUT	global wdog	wdog1.WDOG_B	wdog1.WDOG_RST_B_DE B					ALT0	100k PU
45	GPIO1_IO01	gpio1.IO[1]	pwm1.OUT	ccm.ENET3_REF_CL K_ROOT	sai1.MCLK	anatop.24M_OUT					ALT0	100k PD
47	SD1_CLK	usdhc1.CLK	sai3.RX_SYNC	uart6.CTS_B	ecspi4.SS0	flextimer1.CH[3]	gpio5.IO[3]				ALT5	100k PD
49	SD1_DATA1	usdhc1.DATA1	sai3.TX_BCLK	uart7.TX	ecspi4.SS3	flextimer2.CH[2]	gpio5.IO[6]	ccm.EXT_CLK2			ALT5	100k PD
51	SD1_DATA2	usdhc1.DATA2	sai3.TX_SYNC	uart7.CTS_B	ecspi4.RDY	flextimer2.CH[3]	gpio5.IO[7]	ccm.EXT_CLK3			ALT5	100k PD
53	SD1_DATA3	usdhc1.DATA3	sai3.TX_DATA[0]	uart7.RTS_B	ecspi3.SS1	flextimer1.PHA	gpio5.IO[8]	ccm.EXT_CLK4			ALT5	100k PD
55	ENET1_RD3	enet1.RGMII_RD3	can1.TX	ecspi2.MOSI	uart1.TX	epdc.SDCE[5]*	gpio7.IO[3]	kpp.COL[2]			ALT5	100k PD
57	LCD_DAT16	lcdif.DATA[16]	flextimer1.CH[4]	coresight.TRACE_CL K	csi1.DATA[1]	weim.CRE	gpio3.IO[21]	src.BT_CFG[16]			ALT5	100k PD
59	ECSPI2_MOSI	ecspi2.MOSI	uart7.TX	usdhc1.DATA5	csi1.DATA[7]	lcdif.DATA[14]	gpio4.IO[21]	epdc.PWRCTRL[1]			ALT5	100k PD
	GPIO1_IO08	gpio1.IO[8]	usdhc1.VSELECT	wdog1.WDOG_B	uart3.RX	i2c3.SCL		kpp.COL[5]	pwm1.OUT		ALT0	100k PD
61	LCD_DAT17	lcdif.DATA[17]	flextimer1.CH[5]	coresight.TRACE_CT L	csi1.DATA[0]	weim.ACLK_FREERUN	gpio3.IO[22]	src.BT_CFG[17]			ALT5	100k PD
63	ENET1_RD2	enet1.RGMII_RD2	can1.RX	ecspi2.SCLK	uart1.RX	epdc.SDCE[4]*	gpio7.IO[2]	kpp.ROW[2]			ALT5	100k PD
65	ECSPI2_SS0	ecspi2.SS0	uart7.CTS_B	usdhc1.DATA7	csi1.DATA[9]	lcdif.RESET	gpio4.IO[23]	epdc.PWRWAKE*			ALT5	100k PD
67	ECSPI2_SCLK	ecspi2.SCLK	uart7.RX	usdhc1.DATA4	csi1.DATA[6]	lcdif.DATA[13]	gpio4.IO[20]	epdc.PWRCTRL[0]			ALT5	100k PD
	GPIO1_IO11	gpio1.IO[11]	usdhc3.LCTL	enet1.MDC	uart3.CTS_B	i2c4.SDA	flextimer1.PHB	kpp.ROW[6]	pwm4.OUT		ALT0	100k PD
69	SD1_CD_B	usdhc1.CD_B		uart6.RX	ecspi4.MISO	flextimer1.CH[0]	gpio5.IO[10]				ALT5	100k PD
71	SD1_WP	usdhc1.WP		uart6.TX	ecspi4.MOSI	flextimer1.CH[1]	gpio5.IO[1]				ALT5	100k PD
73	SD1_RESET_B	usdhc1.RESET_B	sai3.MCLK	uart6.RTS_B	ecspi4.SCLK	flextimer1.CH[2]	gpio5.IO[2]				ALT5	100k PD
75	I2C4_SDA	i2c4.SDA	uart5.TX	wdog4.WDOG_RST_ B_DEB	csi1.MCLK	usb.OTG2_ID*	gpio4.IO[15]	epdc.VCOM[1]*			ALT5	100k PD
77	SAI1_RXFS	sai1.RX_SYNC	rawnand.CE2_B	sai2.RX_SYNC	i2c4.SCL	sim1.PORT1_PD	gpio6.IO[16]	mqs.RIGHT			ALT5	100k PD
79	ECSPI1_MISO	ecspi1.MISO	uart6.RTS_B	usdhc2.DATA6	csi1.DATA[4]		gpio4.IO[18]	epdc.PWRIRQ*			ALT5	100k PD
81	I2C3_SCL	i2c3.SCL	uart5.CTS_B	can2.RX	csi1.VSYNC	sdma.EXT_EVENT[0]	gpio4.IO[12]	epdc.BDR[0]*			ALT5	100k PD
85	ECSPI2_MISO	ecspi2.MISO	uart7.RTS_B	usdhc1.DATA6	csi1.DATA[8]	lcdif.DATA[15]	gpio4.IO[22]	epdc.PWRCTRL[2]*			ALT5	100k PD
89	EPDC_D9	epdc.SDDO[9]*	sim1.PORT1_CLK	qspi.B_DATA[1]	uart6.TX	weim.RW	gpio2.IO[9]	lcdif.DATA[9]	lcdif.DATA[0]	EPDC_SDLE*	ALT5	100k PD
91	EPDC_D8	epdc.SDDO[8]*	sim1.PORT1_TRXD	qspi.B_DATA[0]	uart6.RX	weim.OE	gpio2.IO[8]	lcdif.DATA[8]	lcdif.BUSY	EPDC_SDCLK *	ALT5	100k PD
93	LCD_RESET	lcdif.RESET	gpt1.COMPARE1	coresight.EVENTI	csi1.FIELD	weim.DTACK_B	gpio3.IO[4]				ALT5	100k PD
95	EPDC_D13	epdc.SDDO[13]*	sim2.PORT1_TRXD	qspi.B_SCLK	uart7.TX	weim.WAIT	gpio2.IO[13]	lcdif.DATA[13]	lcdif.CS	EPDC_GDOE*	ALT5	100k PD
97	ECSPI1_SS0	ecspi1.SS0	uart6.CTS_B	usdhc2.DATA7	csi1.DATA[5]		gpio4.IO[19]	epdc.PWRCTRL[3]**			ALT5	100k PD
99	ENET1_TXC	enet1.RGMII_TXC	enet1.TX_ER	sai1.RX_BCLK	gpt2.COMPARE2	epdc.PWRCTRL[3]*	gpio7.IO[11]				ALT5	100k PD
101	ECSPI1_SCLK	ecspi1.SCLK	uart6.RX	usdhc2.DATA4	csi1.DATA[2]		gpio4.IO[16]	epdc.PWRCOM			ALT5	100k PD
103	ECSPI1_MOSI	ecspi1.MOSI	uart6.TX	usdhc2.DATA5	csi1.DATA[3]		gpio4.IO[17]	epdc.PWRSTAT*			ALT5	100k PD
105	EPDC_D10	epdc.SDDO[10]*	sim1.PORT1_RST_B	qspi.B_DATA[2]	uart6.RTS_B	weim.CS0_B	gpio2.IO[10]	lcdif.DATA[10]	lcdif.DATA[9]	EPDC_SDOE*	ALT5	100k PD
107	EPDC_D15	epdc.SDDO[15]*	sim2.PORT1_RST_B	qspi.B_SS1_B	uart7.CTS_B	weim.CS1_B	gpio2.IO[15]	lcdif.DATA[15]	lcdif.WR_RWN	EPDC_PWRC* OM*	ALT5	100k PD
111	EPDC_D0	epdc.SDDO[0]*	sim1.PORT2_TRXD	qspi.A_DATA[0]	kpp.ROW[3]	weim.AD[0]	gpio2.IO[0]	lcdif.DATA[0]	lcdif.CLK		ALT5	100k PD

X1 Pin	i.MX7 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Reset State	Pull
113	EPDC_D1	epdc.SDDO[1]*	sim1.PORT2_CLK	qspi.A_DATA[1]	kpp.COL[3]	weim.AD[1]	gpio2.IO[1]	lcdif.DATA[1]	lcdif.ENABLE		ALT5	100k PD
115	EPDC_D2	epdc.SDDO[2]*	sim1.PORT2_RST_B	qspi.A_DATA[2]	kpp.ROW[2]	weim.AD[2]	gpio2.IO[2]	lcdif.DATA[2]	lcdif.VSYNC		ALT5	100k PD
117	EPDC_D3	epdc.SDDO[3]*	sim1.PORT2_SVEN	qspi.A_DATA[3]	kpp.COL[2]	weim.AD[3]	gpio2.IO[3]	lcdif.DATA[3]	lcdif.HSYNC		ALT5	100k PD
119	EPDC_D4	epdc.SDDO[4]*	sim1.PORT2_PD	qspi.A_DQS	kpp.ROW[1]	weim.AD[4]	gpio2.IO[4]	lcdif.DATA[4]			ALT5	100k PD
121	EPDC_D5	epdc.SDDO[5]*	sim2.PORT2_TRXD	qspi.A_SCLK	kpp.COL[1]	weim.AD[5]	gpio2.IO[5]	lcdif.DATA[5]			ALT5	100k PD
123	EPDC_D6	epdc.SDDO[6]*	sim2.PORT2_CLK	qspi.A_SS0_B	kpp.ROW[0]	weim.AD[6]	gpio2.IO[6]	lcdif.DATA[6]			ALT5	100k PD
125	EPDC_D7	epdc.SDDO[7]*	sim2.PORT2_RST_B	qspi.A_SS1_B	kpp.COL[0]	weim.AD[7]	gpio2.IO[7]	lcdif.DATA[7]			ALT5	100k PD
127	EPDC_SDCE2	epdc.SDCE[2]*	sim2.PORT1_SVEN	enet2.RGMII_TD0*	enet2.RGMII_TX_CT L*	weim.ADDR[16]	gpio2.IO[22]	lcdif.DATA[21]	lcdif.DATA[3]		ALT5	100k PD
129	UART3_CTS	uart3.CTS_B	usb.OTG2_PWR*	sai3.TX_SYNC	ecspi1.SS0	enet1.1588_EVENT1_OUT	gpio4.IO[7]	usdhc1.VSELECT			ALT5	100k PD
131	UART3_RTS	uart3.RTS_B	usb.OTG2_OC*	sai3.TX_DATA[0]	ecspi1.SCLK	enet1.1588_EVENT1_IN	gpio4.IO[6]	usdhc3.LCTL*			ALT5	100k PD
133	EPDC_GDRL	epdc.GDRL*	fleximer2.CH[2]			weim.ADDR[20]	gpio2.IO[26]	lcdif.RD_E	lcdif.DATA[19]		ALT5	100k PD
135	GPIO1_IO02	gpio1.IO[2]	pwm2.OUT	ccm.ENET1_REF_CLK_ROOT	sai2.MCLK	anatop.32K_OUT			usb.OTG1_ID		ALT0	100k PD
137	ENET1_CRS	enet1.CRS	wdog2.WDOG_RST_B_DEB	sai1.TX_SYNC	gpt2.CAPTURE1	epdc.PWRCTRL[0]*	gpio7.IO[14]	ccm.EXT_CLK3			ALT5	100k PD
157	SAI1_TXC <sup>1)</sup>	sai1.TX_BCLK <sup>1)</sup>	rawnand.CE0_B <sup>1)</sup>	uart5.TX <sup>1)</sup>	can1.TX <sup>1)</sup>	sim1.PORT1_CLK <sup>1)</sup>	gpio6.IO[13] <sup>1)</sup>				ALT5	100k PD
163	SAI1_TXD <sup>1)</sup>	sai1.TX_DATA[0] <sup>1)</sup>	rawnand.READY_B <sup>1)</sup>	uart5.RTS_B <sup>1)</sup>	can2.TX <sup>1)</sup>	sim1.PORT1_SVEN <sup>1)</sup>	gpio6.IO[15] <sup>1)</sup>				ALT5	100k PD
169	SAI1_RXD	sai1.RX_DATA[0]	rawnand.CE1_B	uart5.RX	can1.RX	sim1.PORT1_TRXD	gpio6.IO[12]				ALT5	100k PD
22	GPIO1_IO03	gpio1.IO[3]	pwm3.OUT	ccm.ENET2_REF_CLK_ROOT*	sai3.MCLK	osc32k.32K_OUT			usb.OTG2_ID*		ALT0	100k PD
24	SAI1_RXC	sai1.RX_BCLK	rawnand.CE3_B	sai2.RX_BCLK	i2c4.SDA	fleximer2.PHA	gpio6.IO[17]	mqs.LEFT			ALT5	100k PD
28	GPIO1_IO09	gpio1.IO[9]	usdhc1.LCTL	ccm.ENET3_REF_CLK_ROOT	uart3.TX	i2c3.SDA	gpc.PMIC_RDY	kpp.ROW[5]	pwm2.OUT		ALT0	100k PD
30	GPIO1_IO10	gpio1.IO[10]	usdhc2.LCTL	enet1.MDIO	uart3.RTS_B	i2c4.SCL	fleximer1.PHA	kpp.COL[6]	pwm3.OUT		ALT0	100k PD
32	SAI2_RXD	sai2.RX_DATA[0]	ecspi3.SCLK	uart4.CTS_B	uart2.CTS_B	fleximer2.CH[6]	gpio6.IO[21]	kpp.COL[7]			ALT5	100k PD
34	SAI2_TXD	sai2.TX_DATA[0]	ecspi3.SS0	uart4.RTS_B	uart2.RTS_B	fleximer2.CH[7]	gpio6.IO[22]	kpp.ROW[7]			ALT5	100k PD
36	UART2_TXD	uart2.TX	i2c2.SDA	sai3.RX_DATA[0]	ecspi1.RDY	enet2.1588_EVENT1_OUT*	gpio4.IO[3]	enet2.MDC*			ALT5	100k PD
38	UART2_RXD	uart2.RX	i2c2.SCL	sai3.RX_BCLK	ecspi1.SS3	enet2.1588_EVENT1_IN*	gpio4.IO[2]	enet2.MDIO*			ALT5	100k PD
44	LCD_ENABLE	lcdif.ENABLE	ecspi4.MOSI	enet1.1588_EVENT3_IN	csi1.DATA[17]	uart2.TX	gpio3.IO[1]				ALT5	100k PD
46	LCD_DAT7	lcdif.DATA[7]		coresight.TRACE[7]	csi1.MCLK	weim.DATA[7]	gpio3.IO[12]	src.BT_CFG[7]			ALT5	100k PD
48	LCD_DAT9	lcdif.DATA[9]		coresight.TRACE[9]	csi1.DATA[8]	weim.DATA[9]	gpio3.IO[14]	src.BT_CFG[9]			ALT5	100k PD
50	LCD_DAT11	lcdif.DATA[11]		coresight.TRACE[11]	csi1.DATA[6]	weim.DATA[11]	gpio3.IO[16]	src.BT_CFG[11]			ALT5	100k PD
52	LCD_DAT12	lcdif.DATA[12]		coresight.TRACE[12]	csi1.DATA[5]	weim.DATA[12]	gpio3.IO[17]	src.BT_CFG[12]			ALT5	100k PD
54	LCD_DAT13	lcdif.DATA[13]		coresight.TRACE[13]	csi1.DATA[4]	weim.DATA[13]	gpio3.IO[18]	src.BT_CFG[13]			ALT5	100k PD
56	LCD_CLK	lcdif.CLK	ecspi4.MISO	enet1.1588_EVENT2_IN	csi1.DATA[16]	uart2.RX	gpio3.IO[0]				ALT5	100k PD
58	LCD_DAT3	lcdif.DATA[3]	gpt1.CAPTURE1	coresight.TRACE[3]	csi1.DATA[23]	weim.DATA[3]	gpio3.IO[8]	src.BT_CFG[3]			ALT5	100k PD
60	LCD_DAT2	lcdif.DATA[2]	gpt1.CLK	coresight.TRACE[2]	csi1.DATA[22]	weim.DATA[2]	gpio3.IO[7]	src.BT_CFG[2]			ALT5	100k PD
62	LCD_DAT8	lcdif.DATA[8]		coresight.TRACE[8]	csi1.DATA[9]	weim.DATA[8]	gpio3.IO[10]	src.BT_CFG[8]			ALT5	100k PD
64	LCD_DAT15	lcdif.DATA[15]		coresight.TRACE[15]	csi1.DATA[2]	weim.DATA[15]	gpio3.IO[23]	src.BT_CFG[15]			ALT5	100k PD
66	LCD_DAT14	lcdif.DATA[14]		coresight.TRACE[14]	csi1.DATA[3]	weim.DATA[14]	gpio3.IO[19]	src.BT_CFG[14]			ALT5	100k PD
68	LCD_HSYNC	lcdif.HSYNC	ecspi4.SCLK	enet2.1588_EVENT2_IN*	csi1.DATA[18]	uart2.RTS_B	gpio3.IO[2]				ALT5	100k PD
70	LCD_DAT1	lcdif.DATA[1]	gpt1.COMPARE3	coresight.TRACE[1]	csi1.DATA[21]	weim.DATA[1]	gpio3.IO[6]	src.BT_CFG[1]			ALT5	100k PD
72	LCD_DAT5	lcdif.DATA[5]		coresight.TRACE[5]	csi1.HSYNC	weim.DATA[5]	gpio3.IO[10]	src.BT_CFG[5]			ALT5	100k PD
74	LCD_DAT10	lcdif.DATA[10]		coresight.TRACE[10]	csi1.DATA[7]	weim.DATA[10]	gpio3.IO[15]	src.BT_CFG[10]			ALT5	100k PD
76	LCD_DAT0	lcdif.DATA[0]	gpt1.COMPARE2	coresight.TRACE[0]	csi1.DATA[20]	weim.DATA[0]	gpio3.IO[5]	src.BT_CFG[0]			ALT5	100k PD
78	LCD_DAT4	lcdif.DATA[4]	gpt1.CAPTURE2	coresight.TRACE[4]	csi1.VSYNC	weim.DATA[4]	gpio3.IO[9]	src.BT_CFG[4]			ALT5	100k PD
80	LCD_DAT6	lcdif.DATA[6]		coresight.TRACE[6]	csi1.PIXCLK	weim.DATA[6]	gpio3.IO[11]	src.BT_CFG[6]			ALT5	100k PD
82	LCD_VSYNC	lcdif.VSYNC	ecspi4.SS0	enet2.1588_EVENT3_IN*	csi1.DATA[19]	uart2.CTS_B	gpio3.IO[3]				ALT5	100k PD
86	I2C2_SDA	i2c2.SDA	uart4.TX	wdog3.WDOG_RST_B_DEB	ecspi3.SS0	ccm.ENET3_REF_CLK_ROOT	gpio4.IO[11]	usdhc3.WP*			ALT5	100k PD

X1 Pin	i.MX7 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Reset State	Pull
88	I2C2_SCL	i2c2.SCL	uart4.RX	wdog3.WDOG_B	ecspi3.SCLK	ccm.ENET2_REF_CLK_RO OT	gpio4.IO[10]	usdhc3.CD_B*			ALT5	100k PD
90	I2C1_SCL	i2c1.SCL	uart4.CTS_B	can1.RX	ecspi3.MISO	anatop.24M_OUT	gpio4.IO[8]	usdhc2.VSELECT			ALT5	100k PD
92	I2C1_SDA	i2c1.SDA	uart4.RTS_B	can1.TX	ecspi3.MOSI	ccm.ENET1_REF_CLK_RO OT*	gpio4.IO[9]	usdhc3.VSELECT*			ALT5	100k PD
94	I2C3_SDA	i2c3.SDA	uart5.RTS_B	can2.TX	csi1.HSYN	sdma.EXT_EVENT[1]	gpio4.IO[13]	epdc.BDR[1]*			ALT5	100k PD
96	I2C4_SCL	i2c4.SCL	uart5.RX	wdog4.WDOG_B	csi1.PIXCLK	usb.OTG1_ID	gpio4.IO[14]	epdc.VCOM[0]*			ALT5	100k PD
98	SD2_RESET_B	usdhc2.RESET_B	sai2.MCLK	usdhc2.RESET	ecspi3.RDY	usb.OTG2_ID*	gpio5.IO[11]				ALT5	100k PD
100	SD2_DATA2	usdhc2.DATA2	sai2.TX_SYNC	uart4.CTS_B	gpt4.COMPARE2	sim2.PORT1_SVEN	gpio5.IO[16]				ALT5	100k PD
102	SD2_DATA3	usdhc2.DATA3	sai2.TX_DATA[0]	uart4.RTS_B	gpt4.COMPARE3	sim2.PORT1_PD	gpio5.IO[17]				ALT5	100k PD
104	EPDC_GDSP	epdc.GDSP*	flextimer2.CH[3]	enet2.RGMII_TXC	enet2.TX_ER*	enet2.ADDR[21]	gpio2.IO[27]	lcdif.BUSY	lcdif.DATA[17]		ALT5	100k PD
106	EPDC_BDR0	epdc.BDR[0]*		enet2.TX_CLK*	ccm.ENET2_REF_CLK_ROOT*	weim.ADDR[22]	gpio2.IO[28]	lcdif.CS	lcdif.DATA[7]		ALT5	100k PD
110	EPDC_BDR1	epdc.BDR[1]*	epdc.SDCLKN*	enet2.RX_CLK*		weim.AD[8]	gpio2.IO[29]	lcdif.ENABLE	lcdif.DATA[6]		ALT5	100k PD
112	EPDC_PWRCOM	epdc.PWRCOM*	flextimer2.PHA	enet2.CRS*		weim.AD[9]	gpio2.IO[30]	lcdif.HSYN	lcdif.DATA[11]		ALT5	100k PD
114	EPDC_SDCLK	epdc.SDCLK*	sim2.PORT2_SVEN	enet2.RGMII_RD0*	kpp.ROW[4]	weim.AD[10]	gpio2.IO[16]	lcdif.CLK	lcdif.DATA[20]		ALT5	100k PD
116	EPDC_SDL	epdc.SDL*	sim2.PORT2_PD	enet2.RGMII_RD1*	kpp.COL[4]	weim.AD[11]	gpio2.IO[17]	lcdif.DATA[16]	lcdif.DATA[8]		ALT5	100k PD
118	EPDC_SDOE	epdc.SDOE*	flextimer1.CH[0]	enet2.RGMII_RD2*	kpp.COL[5]	weim.AD[12]	gpio2.IO[18]	lcdif.DATA[17]	lcdif.DATA[23]		ALT5	100k PD
120	EPDC_SDSHR	epdc.SDSHR*	flextimer1.CH[1]	enet2.RGMII_RD3*	kpp.ROW[5]	weim.AD[13]	gpio2.IO[19]	lcdif.DATA[18]	lcdif.DATA[10]		ALT5	100k PD
122	EPDC_SDCE0	epdc.SDCE[0]*	flextimer1.CH[2]	enet2.RGMII_RX_CTL*	enet2.RX_EN*	weim.AD[14]	gpio2.IO[20]	lcdif.DATA[19]	lcdif.DATA[5]		ALT5	100k PD
124	EPDC_SDCE1	epdc.SDCE[1]*	flextimer1.CH[3]	enet2.RGMII_RXC*	enet2.RX_ER*	weim.AD[15]	gpio2.IO[21]	lcdif.DATA[20]	lcdif.DATA[4]		ALT5	100k PD
126	EPDC_D14	epdc.SDDO[14]*	sim2.PORT1_CLK	qspi.B_SSO_B	uart7.RTS_B	weim.EB_B[0]	gpio2.IO[14]	lcdif.DATA[14]	lcdif.DATA[22]	EPDC_GDSP*	ALT5	100k PD
128	EPDC_PWRSTAT	epdc.PWRSTAT*	flextimer2.PHB	enet2.COL*		weim.EB_B[1]	gpio2.IO[31]	lcdif.VSYN	lcdif.DATA[12]		ALT5	100k PD
130	EPDC_SDCE3	epdc.SDCE[3]*	sim2.PORT1_PD	enet2.RGMII_TD1*	kpp.ROW[6]	weim.ADDR[17]	gpio2.IO[23]	lcdif.DATA[22]	lcdif.DATA[2]		ALT5	100k PD
132	EPDC_GDCLK	epdc.GDCLK*	flextimer2.CH[0]	enet2.RGMII_TD2*	kpp.COL[7]	weim.ADDR[18]	gpio2.IO[24]	lcdif.DATA[23]	lcdif.DATA[16]		ALT5	100k PD
134	EPDC_GDOE	epdc.GDOE*	flextimer2.CH[1]	enet2.RGMII_TD3*	kpp.ROW[7]	weim.ADDR[19]	gpio2.IO[25]	lcdif.WR_RWN	lcdif.DATA[18]		ALT5	100k PD
136	LCD_DAT18	lcdif.DATA[18]	flextimer1.CH[6]	coresight.EVENTO	csi1.DATA[15]	weim.CS2_B	gpio3.IO[23]	src.BT_CFG[18]			ALT5	100k PD
138	LCD_DAT19	lcdif.DATA[19]	flextimer1.CH[7]		csi1.DATA[14]	weim.CS3_B	gpio3.IO[24]	src.BT_CFG[19]			ALT5	100k PD
140	LCD_DAT20	lcdif.DATA[20]	flextimer2.CH[4]	enet1.1588_EVENT2_OUT	csi1.DATA[13]	weim.ADDR[23]	gpio3.IO[25]	I2C3_SCL			ALT5	100k PD
142	LCD_DAT21	lcdif.DATA[21]	flextimer2.CH[5]	enet1.1588_EVENT3_OUT	csi1.DATA[12]	weim.ADDR[24]	gpio3.IO[26]	I2C3_SDA			ALT5	100k PD
144	LCD_DAT22	lcdif.DATA[22]	flextimer2.CH[6]	enet2.1588_EVENT2_OUT*	csi1.DATA[11]	weim.ADDR[25]	gpio3.IO[27]	I2C4_SCL			ALT5	100k PD
146	LCD_DAT23	lcdif.DATA[23]	flextimer2.CH[7]	enet2.1588_EVENT3_OUT*	csi1.DATA[10]	weim.ADDR[26]	gpio3.IO[28]	I2C4_SDA			ALT5	100k PD
150	EPDC_D12	epdc.SDDO[12]*	sim1.PORT1_PD	qspi.B_DQS	uart7.RX	weim.LBA_B	gpio2.IO[12]	lcdif.DATA[12]	lcdif.DATA[21]	EPDC_GDCLK*	ALT5	100k PD
152	EPDC_D11	epdc.SDDO[11]*	sim1.PORT1_SVEN	qspi.B_DATA[3]	uart6.CTS_B	weim.BCLK	gpio2.IO[11]	lcdif.DATA[11]	lcdif.DATA[1]	EPDC_SDCE0*	ALT5	100k PD
178	GPIO1_IO15	gpio1.IO[15]	usdhc3.WP	enet2.MDC*	can2.TX	wdog4.WDOG_B	ccm.EXT_CLK4	sdma.EXT_EVENT[1]			ALT0	100k PD
184	SD2_CLK	usdhc2.CLK	sai2.RX_SYNC	mqs.RIGHT	gpt4.CLK		gpio5.IO[12]				ALT5	100k PD
186	SD2_CMD	usdhc2.CMD	sai2.RX_BCLK	mqs.LEFT	gpt4.CAPTURE1	sim2.PORT1_TRXD	gpio5.IO[13]				ALT5	100k PD
188	GPIO1_IO14	gpio1.IO[14]	usdhc3.CD_B	enet2.MDIO*	can2.RX	wdog3.WDOG_B	ccm.EXT_CLK3	sdma.EXT_EVENT[0]			ALT0	100k PD
190	SD1_CMD	usdhc1.CMD	sai3.RX_BCLK		ecspi4.SS1	flextimer2.CH[0]	gpio5.IO[4]				ALT5	100k PD
192	SD1_DATA0	usdhc1.DATA0	sai3.RX_DATA[0]	uart7.RX	ecspi4.SS2	flextimer2.CH[1]	gpio5.IO[5]	ccm.EXT_CLK1			ALT5	100k PD
194	ENET1_TD3	enet1.RGMII_TD3	can2.TX	ecspi2.SS0	i2c4.SDA	epdc.SDOEZ*	gpio7.IO[9]				ALT5	100k PD
196	ENET1_TD2	enet1.RGMII_TD2	can2.RX	ecspi2.MISO	i2c4.SCL	epdc.SDOED*	gpio7.IO[8]				ALT5	100k PD

\*This function is only available on the Colibri iMX7D and not on iMX7S.

1) This pins is only available on Colibri iMX7D 1GB, not on the iMX7D 512MB or the iMX7S 256MB

## 5. Interface Description

### 5.1 Power Signals

#### 5.1.1 Digital Supply

Table 5-1 Digital Supply Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Remarks
42, 84, 108, 148, 182, 198, 200	3V3	I	3.3V main power supply	Use decoupling capacitors on all pins.
39, 41, 83, 109, 147, 181, 197, 199	GND	I	Digital Ground	
40	VCC_BATT	I	RTC Power supply can be connected to a backup battery.	Connect this pin to 3.3V even if the internal RTC is not used.

#### 5.1.2 Analogue Supply

Table 5-2 Analogue Supply Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Remarks
10, 12	AVDD_AUDIO	I	3.3V Analogue supply	Connect this pin to a <b>3.3V supply</b> . For better Audio accuracy we recommend filtering this supply separately from the digital supply. This pin is only connected to the Audio Codec. If audio is not used, connect these pins to the 3V3 input supply.
9, 11	VSS_AUDIO	I	Analogue Ground	Connect this pin to GND. This pin is connected with Digital GND on the Colibri iMX7. For better Audio accuracy, use the module connector as star point and route the grounds individual for the audio.

#### 5.1.3 Power Management Signals

Table 5-3 Power Management Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Remarks
26	nRESET_EXT	I	Reset Input	This pin is active low and resets the Colibri module. There is a 100k Ohm pull-up on this pin.
87	nRESET_OUT	O	Reset Output	This pin is active low. This pin is driven low at boot up. This signal is a push/pull output.

## 5.2 GPIOs

Most of the pins have a GPIO (General Purpose Input/Output) function. The GPIO functionality is configured by selecting the correct alternate function. For most of the pins, this is ALT5, while some have the GPIO function on the alternative function ALT0. All GPIO pins can be used as an interrupt source.

### 5.2.1 Wakeup Source

The Colibri iMX7 uses different sleep modes. In principle, all GPIOs can be used to wake up the Colibri module from the System Idle, Low Power Idle, and Deep Sleep state. The exception is the LPSR mode. In this mode, only the following IO pins are retained and therefore only these pins can be used as the wakeup source from the LPSR mode. More information about the different sleep modes can be found in section 6.

X1 Pin#	Colibri STD Function	iMX7 Ball Name	Remarks
29	UART_A DSR	GPIO1_IO07	
37	UART_A RI, Keypad_In<4>	GPIO1_IO06	
43	WAKEUP Source<0>, SDCard CardDetect	GPIO1_IO00	Preferred wakeup source
45	WAKEUP Source<1>	GPIO1_IO01	Preferred wakeup source
59	PWM<A>, Camera Input Data<7>	GPIO1_IO08	This pin is multiplexed with a non-LPSR capable pin. Therefore, do not use this pin in LPSR mode.
67	PWM<D>, Camera Input Data<6>	GPIO1_IO11	This pin is multiplexed with a non-LPSR capable pin. Therefore, do not use this pin in LPSR mode.
135	SPDIF_IN	GPIO1_IO02	
22	VDD Fault Detect	GPIO1_IO03	
28	PWM<B>	GPIO1_IO09	
30	PWM<C>	GPIO1_IO10	
178	DATA30	GPIO1_IO15	
188	ADDRESS16	GPIO1_IO14	
29	UART_A DSR	GPIO1_IO07	
37	UART_A RI, Keypad_In<4>	GPIO1_IO06	

Even though, there are many pins available with the wake functionality, it is recommended that, whenever possible, use pin 43 (WAKEUP Source<0>) and 45 (WAKEUP Source<1>). This ensures that the design is compatible with other Colibri modules.

The touch pen down interrupt signal from the touch controller is shared with the power management interrupt signal. This interrupt signal is connected to the GPIO1\_IO13 ball of the SoC. Even though this pin is also LPSR capable, it is not possible to wake up the system from the LPSR mode by using the touch interrupt since the resistive touch controller is not running in LPSR mode.

## 5.3 Ethernet

The Colibri iMX7D as well as the iMX7S feature both a 10/100 Mbit/s Ethernet interface with Medium Dependent Interface (MDI). The PHY of this interface is located on the module. Therefore, only the magnetics and the connector are needed on the carrier board. The module features the Micrel KSZ8041 Fast Ethernet Transceiver as PHY which is connected over RMII with the MAC in the



NXP i.MX 7. The MAC in the SoC features an accurate IEEE 1588 compliant timer for clock synchronisation which is commonly used in industrial automation applications.

Table 5-4 Ethernet Pins

X1 Pin#	Colibri STD Function	PHY Signal Name	I/O	Description
189	TXO+	TX+	O	100BASE-TX: Transmit + (Auto MDIX: Receive +)
187	TXO-	TX-	O	100BASE-TX: Transmit - (Auto MDIX: Receive -)
195	RXI+	RX+	I	100BASE-TX: Receive + (Auto MDIX: Transmit +)
193	RXI-	RX-	I	100BASE-TX: Receive - (Auto MDIX: Transmit -)
191	AGND_LAN	GND		Ethernet ground, on the module connected to common GND
183	LINK_AKT	LED0	O	Link activity indication LED
185	SPEED100	LED1	O	100Mbit/s indication LED

The Colibri iMX7D features a second Ethernet port (**not available on Colibri iMX7S**). If this port is required, an additional PHY needs to be implemented on the carrier board. The second MAC in the SoC is able to provide three different interface standards for the connection with the PHY:

- **RGMI**: Reduced Gigabit Media Independent Interface. This interface allows connecting a Gigabit Ethernet PHY.
- **RMII**: Reduced Media Independent Interface. This is the preferred mode for interfacing a 10/100 Mbit/s Ethernet PHY such as the KSZ8041.
- **MII**: Media Independent Interface. This is second option for interfacing a 10/100 Mbit/s Ethernet PHY. This mode requires more data pins than the RMII, with the advantage of a more relaxed routing of the interface due to lower operation frequency.

Table 5-5 RGMII signals (incompatible with other modules, only available on iMX7D)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Function	I/O	Description
122	ADDRESS14	EPDC_SDCE0	enet2.RGMII_RX_CTL	I	RGMII_RX_CTL
124	ADDRESS15	EPDC_SDCE1	enet2.RGMII_RXC	I	RGMII_RXC
114	ADDRESS10	EPDC_SDCLK	enet2.RGMII_RD0	I	RGMII_RXD0
116	ADDRESS11	EPDC_SDLE	enet2.RGMII_RD1	I	RGMII_RXD1
118	ADDRESS12	EPDC_SDOE	enet2.RGMII_RD2	I	RGMII_RXD2
120	ADDRESS13	EPDC_SDSHR	enet2.RGMII_RD3	I	RGMII_RXD3
133		EPDC_GDRL	enet2.RGMII_TX_CTL	O	RGMII_TX_CTL
104		EPDC_GDSP	enet2.RGMII_TXC	O	RGMII_TXC
127		EPDC_SDCE2	enet2.RGMII_TD0	O	RGMII_TXD0
130	DQM2	EPDC_SDCE3	enet2.RGMII_TD1	O	RGMII_TXD1
132	DQM3	EPDC_GDCLK	enet2.RGMII_TD2	O	RGMII_TXD2
134	ADDRESS25	EPDC_GDOE	enet2.RGMII_TD3	O	RGMII_TXD3
178	DATA30	GPIO1_IO15	enet2.MDC	O	RGMII_MDC
36	UART_B RXD	UART2_TXD			
188	ADDRESS16	GPIO1_IO14	enet2.MDIO	I/O	RGMII_MDIO
38	UART_B TXD	UART2_RXD			

Table 5-6 RMII signals (incompatible with other modules and only available on iMX7D)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Function	I/O	Description
114	ADDRESS10	EPDC_SDCLK	enet2.RGMII_RD0	I	RMII_RXD0
116	ADDRESS11	EPDC_SDLE	enet2.RGMII_RD1	I	RMII_RXD1
124	ADDRESS15	EPDC_SDCE1	enet2.RX_ER	I	RMII_RXER
127		EPDC_SDCE2	enet2.RGMII_TD0	O	RMII_TXD0
130	DQM2	EPDC_SDCE3	enet2.RGMII_TD1	O	RMII_TXD1
133		EPDC_GDRL	enet2.RGMII_TX_CTL	O	RMII_TXEN
122	ADDRESS14	EPDC_SDCE0	enet2.RGMII_RX_CTL	I	RMII_CRS_DV
178	DATA30	GPIO1_IO15	enet2.MDC	O	RMII_MDC
36	UART_B RXD	UART2_TXD			
38	UART_B TXD	UART2_RXD	enet2.MDIO	I/O	RMII_MDIO
188	ADDRESS16	GPIO1_IO14			
22	VDD Fault Detect	GPIO1_IO03	ccm.ENET2_REF_CLK_ROOT	I/O	50MHz Reference clock that is provided from the MAC to the PHY or from the PHY to the MAC
106	nCS2	EPDC_BDR0			
88	SPI CLK	I2C2_SCL			

Table 5-7 MII signals (incompatible with other modules and only available on iMX7D)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Function	I/O	Description
128	DQM1	EPDC_PWRSTAT	enet2.COL	I	MII_COL
112	ADDRESS9	EPDC_PWRCOM	enet2.CRS	I	MII_CRS
114	ADDRESS10	EPDC_SDCLK	enet2.RGMII_RD0	I	MII_RD0
116	ADDRESS11	EPDC_SDLE	enet2.RGMII_RD1	I	MII_RD1
118	ADDRESS12	EPDC_SDOE	enet2.RGMII_RD2	I	MII_RD2
120	ADDRESS13	EPDC_SDSHR	enet2.RGMII_RD3	I	MII_RD3
110	ADDRESS8	EPDC_BDR1	enet2.RX_CLK	I	MII_RX_CLK
122	ADDRESS14	EPDC_SDCE0	enet2.RX_EN	I	MII_RX_DV
124	ADDRESS15	EPDC_SDCE1	enet2.RX_ER	I	MII_RX_ER
127		EPDC_SDCE2	enet2.RGMII_TD0	O	MII_TD0
130	DQM2	EPDC_SDCE3	enet2.RGMII_TD1	O	MII_TD1
132	DQM3	EPDC_GDCLK	enet2.RGMII_TD2	O	MII_TD2
134	ADDRESS25	EPDC_GDOE	enet2.RGMII_TD3	O	MII_TD3
106	nCS2	EPDC_BDR0	enet2.TX_CLK	O	MII_TX_CLK
133		EPDC_GDRL	enet2.RGMII_TX_CTL	O	MII_TX_EN
104		EPDC_GDSP	enet2.TX_ER	O	MII_TX_ER
178	DATA30	GPIO1_IO15	enet2.MDC	O	MII_MDC
36	UART_B RXD	UART2_TXD			
38	UART_B TXD	UART2_RXD	enet2.MDIO	I/O	MII_MDIO
188	ADDRESS16	GPIO1_IO14			

## 5.4 USB

The Colibri iMX7D provides two USB 2.0 High-Speed (480 Mbit/s) ports while the Colibri iMX7S provides only one. The port available on both modules is the USBC interface. This port is a dual use USB interface that can be configured as host or client. The port cannot be used as a true OTG controller. The USBC controller is also used for the serial loader mode (recovery mode). For more information, see chapter 6. The second USB 2.0 High-Speed port is only supported on the Colibri iMX7D. Even though this port is also a dual use interface, the Colibri standard intends to use this port (USBH) as host only.

### 5.4.1 USB Data Signal

Table 5-8 USB Data Pins

X1 Pin#	Colibri STD Function	iMX7 Ball Name	I/O	Description
143	USBC_P	USB_OTG1_DP	I/O	Differential Signal for the shared USB Host / Client port Available on Colibri iMX7D as well as iMX7S
145	USBC_N	USB_OTG1_DN	I/O	
139	USBH_P	USB_OTG2_DP	I/O	Differential Signal for USB Host port <b>Only available on Colibri iMX7D</b>
141	USBH_N	USB_OTG2_DN	I/O	

### 5.4.2 USB Control Signals

Table 5-9 USB OTG Pins

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Function	I/O	Description
135	SPDIF_IN	GPIO1_IO02			USB OTG ID
96	Camera Input PCLK	I2C4_SCL	usb.OTG1_ID	I	Alternative instance of ID pin, incompatible with other Colibri modules.
137	USB Client Cable Detect, SPDIF_OUT	USB_OTG1_VBUS	USB_OTG1_VBUS	I	Use this pin to detect if VBUS is present (5V USB supply). Please note that this pin is only 3.3V tolerant This signal is connected to two pins of the i.MX 7 SoC. For more information about the configuration, see section 4.1.

The Colibri iMX7 module does not support true OTG, but the interface can be configured as host or client. Due to compatibility with other Colibri modules, the current evaluation board as well as the other Toradex carrier board do not use the USB OTG ID pin for detecting whether a Type A or Type B cable is plugged in. Instead, the VBUS is used for detecting the Host or Client mode. We recommend implementing the same circuit as on the evaluation board for making sure the design is compatible with the provided Toradex OS images.

If you use the USB Host function, you need to generate the 5V USB supply voltage on your carrier board. The Colibri iMX7 provides two optional signals for USB power supply control. We recommend using the following pins to ensure best possible compatibility, however, use of these signals is not mandatory and maybe other GPIOs can be used instead. The USB OTG jack features an ID pin which allows detecting whether a type A or type B plug is plugged in. The Colibri iMX7 module does not support true OTG, but the interface can be configured as host or client.

Table 5-10 USB Power Control Pins

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Function	I/O	Description
129	USB Host Power Enable	UART3_CTS	usb.OTG2_PWR	O	This pin enables the external USB voltage supply.
29	UART_A DSR	GPIO1_IO07			Alternative instance of PWR enable pin, incompatible with other Colibri modules.
131	Usb Host Over-Current Detect	UART3_RTS	usb.OTG2_OC	I	USB overcurrent, this pin can Signal an over current condition in the USB supply
37	UART_A RI, Keypad_In<4>	GPIO1_IO06			Alternative instance of over current pin, incompatible with other Colibri modules.

## 5.5 Display

The NXP i.MX 7 features a dedicated image processing unit with hardware accelerators. Even though the SoC itself provides an MIPI DSI interface, only the parallel LCD interface can be used. Some of the required pins for the DSI interface are missing on the SODIMM edge connector.

### 5.5.1 Parallel RGB LCD interface

The Colibri iMX7 provides one parallel LCD interface on the SODIMM connector. It supports up to 24-bit colour per pixel. The 24-bit colour mapping is compatible with the Colibri iMX6 but not with other Colibri modules. Therefore, only the 18-bit mode is ensured to be compatible with the other modules.

#### Features

- Up to 1920x1080 resolution at 60Hz
- Up to 24-bit colour
- Supports parallel TTL displays and smart displays
- Max pixel clock 150MHz

Table 5-11 Standard Parallel RGB LCD Interface Pins

X1 Pin#	Colibri STD Function	iMX7 Ball Name	I/O	24bit RGB Interface	18bit RGB Interface	16bit RGB Interface
76	LCD RGB Data<0>	LCD_DAT0	O	B0	B0	B0
70	LCD RGB Data<1>	LCD_DAT1	O	B1	B1	B1
60	LCD RGB Data<2>	LCD_DAT2	O	B2	B2	B2
58	LCD RGB Data<3>	LCD_DAT3	O	B3	B3	B3
78	LCD RGB Data<4>	LCD_DAT4	O	B4	B4	B4
72	LCD RGB Data<5>	LCD_DAT5	O	B5	B5	G0
80	LCD RGB Data<6>	LCD_DAT6	O	B6	G0	G1
46	LCD RGB Data<7>	LCD_DAT7	O	B7	G1	G2
62	LCD RGB Data<8>	LCD_DAT8	O	G0	G2	G3
48	LCD RGB Data<9>	LCD_DAT9	O	G1	G3	G4
74	LCD RGB Data<10>	LCD_DAT10	O	G2	G4	G5
50	LCD RGB Data<11>	LCD_DAT11	O	G3	G5	R0
52	LCD RGB Data<12>	LCD_DAT12	O	G4	R0	R1
54	LCD RGB Data<13>	LCD_DAT13	O	G5	R1	R2
66	LCD RGB Data<14>	LCD_DAT14	O	G6	R2	R3
64	LCD RGB Data<15>	LCD_DAT15	O	G7	R3	R4
57	LCD RGB Data<16>	LCD_DAT16	O	R0	R4	
61	LCD RGB Data<17>	LCD_DAT17	O	R1	R5	
136	ADDRESS24	LCD_DAT18	O	R2		
138	ADDRESS23	LCD_DAT19	O	R3		
140	ADDRESS22	LCD_DAT20	O	R4		
142	ADDRESS21	LCD_DAT21	O	R5		
144	ADDRESS20	LCD_DAT22	O	R6		
146	ADDRESS19	LCD_DAT23	O	R7		
44	LCD RGB DE	LCD_ENABLE	O	Data Enable (other names: Output Enable, L_BIAS)		
68	LCD RGB HSYNC	LCD_HSYNC	O	Horizontal Sync (other names: Line Clock, L_LCKL)		
82	LCD RGB VSYNC	LCD_VSYNC	O	Vertical Sync (other names: Frame Clock, L_FCLK)		
56	LCD RGB PCLK	LCD_CLK	O	Pixel Clock (other names: Dot Clock, L_PCLK_WR)		

Many applications will also require some signals to control the backlight and/or display enabling. You can use any of the free GPIOs for these functions but we recommend using the same signals as used on our standard carrier boards to ensure minimal software configuration overhead. PWM capable signals can be used to control the backlight brightness on many display panels - see section 5.12.

Some of the LCD interface signals are available on alternative pins. Use this pins with care since the location is incompatible with other Colibri modules.

Table 5-12 Alternative location of Parallel RGB LCD Interface Pins

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Function	I/O	Description
89	nWE	EPDC_D9	lcdif.DATA[0]	O	Alternative location of LCD_DAT0
111	ADDRESS0	EPDC_D0			
113	ADDRESS1	EPDC_D1	lcdif.DATA[1]	O	Alternative location of LCD_DAT1
152	DATA17	EPDC_D11			
115	ADDRESS2	EPDC_D2	lcdif.DATA[2]	O	Alternative location of LCD_DAT2
130	DQM2	EPDC_SDCE3			
117	ADDRESS3	EPDC_D3	lcdif.DATA[3]	O	Alternative location of LCD_DAT3
127		EPDC_SDCE2			
119	ADDRESS4	EPDC_D4	lcdif.DATA[4]	O	Alternative location of LCD_DAT4
124	ADDRESS15	EPDC_SDCE1			
121	ADDRESS5	EPDC_D5	lcdif.DATA[5]	O	Alternative location of LCD_DAT5
122	ADDRESS14	EPDC_SDCE0			
110	ADDRESS8	EPDC_BDR1	lcdif.DATA[6]	O	Alternative location of LCD_DAT6
123	ADDRESS6	EPDC_D6			
106	nCS2	EPDC_BDR0	lcdif.DATA[7]	O	Alternative location of LCD_DAT7
125	ADDRESS7	EPDC_D7			
91	nOE, Recovery Mode	EPDC_D8	lcdif.DATA[8]	O	Alternative location of LCD_DAT8
116	ADDRESS11	EPDC_SDLE			
89	nWE	EPDC_D9	lcdif.DATA[9]	O	Alternative location of LCD_DAT9
105	nCS0	EPDC_D10			
105	nCS0	EPDC_D10	lcdif.DATA[10]	O	Alternative location of LCD_DAT10
120	ADDRESS13	EPDC_SDSHR			
112	ADDRESS9	EPDC_PWRCOM	lcdif.DATA[11]	O	Alternative location of LCD_DAT11
152	DATA17	EPDC_D11			
128	DQM1	EPDC_PWRSTAT	lcdif.DATA[12]	O	Alternative location of LCD_DAT12
150	DATA16	EPDC_D12			
67	PWM<D>, Camera Input Data<6>	ECSPI2_SCLK	lcdif.DATA[13]	O	Alternative location of LCD_DAT13
95	RDY	EPDC_D13			
59	PWM<A>, Camera Input Data<7>	ECSPI2_MOSI	lcdif.DATA[14]	O	Alternative location of LCD_DAT14
126	DQM0	EPDC_D14			
85	Camera Input Data<8>, Keypad_Out<4>	ECSPI2_MISO	lcdif.DATA[15]	O	Alternative location of LCD_DAT15
107	nCS1	EPDC_D15			
116	ADDRESS11	EPDC_SDLE	lcdif.DATA[16]	O	Alternative location of LCD_DAT16
132	DQM3	EPDC_GDCLK			
104		EPDC_GDSP	lcdif.DATA[17]	O	Alternative location of LCD_DAT17
118	ADDRESS12	EPDC_SDOE			
120	ADDRESS13	EPDC_SDSHR	lcdif.DATA[18]	O	Alternative location of LCD_DAT18

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Function	I/O	Description
134	ADDRESS25	EPDC_GDOE			
122	ADDRESS14	EPDC_SDCE0	lcdif.DATA[19]	O	Alternative location of LCD_DAT19
133		EPDC_GDRL			
114	ADDRESS10	EPDC_SDCLK	lcdif.DATA[20]	O	Alternative location of LCD_DAT20
124	ADDRESS15	EPDC_SDCE1			
127		EPDC_SDCE2	lcdif.DATA[21]	O	Alternative location of LCD_DAT21
150	DATA16	EPDC_D12			
126	DQM0	EPDC_D14	lcdif.DATA[22]	O	Alternative location of LCD_DAT22
130	DQM2	EPDC_SDCE3			
118	ADDRESS12	EPDC_SDOE	lcdif.DATA[23]	O	Alternative location of LCD_DAT23
132	DQM3	EPDC_GDCLK			
110	ADDRESS8	EPDC_BDR1	lcdif.ENABLE	O	Alternative location of LCD_ENABLE
113	ADDRESS1	EPDC_D1			
112	ADDRESS9	EPDC_PWRCOM	lcdif.HSYNC	O	Alternative location of LCD_HSYNC
117	ADDRESS3	EPDC_D3			
115	ADDRESS2	EPDC_D2	lcdif.VSYNC	O	Alternative location of LCD_VSYNC
128	DQM1	EPDC_PWRSTAT			
111	ADDRESS0	EPDC_D0	lcdif.CLK	O	Alternative location of LCD_CLK
114	ADDRESS10	EPDC_SDCLK			

## 5.5.2 LVDS

The Colibri iMX7 does not have a native LVDS interface. However, it is possible to use the parallel LCD port with a LVDS transmitter. The Colibri Evaluation board provides a reference design for a LVDS interface implementation.

## 5.5.3 HDMI

The Colibri iMX7 does not have a native HDMI interface. However, it is possible to implement a parallel RGB to HDMI converter on the carrier board.

## 5.5.4 Analogue VGA

The Colibri iMX7 does not have a native Analogue VGA interface. However, it is possible to implement a VGA interface on the carrier board using a VGA DAC. The Colibri Evaluation board features a reference design for such a VGA DAC.

## 5.5.5 Display Serial Interface (DSI)

The Colibri iMX7 does not support the Display Serial Interface that is available on the NXP i.MX 7 SoC.

## 5.5.6 Electrophoretic Display Controller (EPDC)

The standard Colibri iMX7 modules do not support the EPDC interface.

## 5.6 PCI Express

The Colibri iMX7 does not support the PCI Express Interface that is available on the NXP i.MX 7 SoC.

## 5.7 IDE

The Colibri iMX7 does not support the Integrated Drive Electronics interface (IDE).

## 5.8 External Memory Bus

The Colibri iMX7 features an external memory bus. NXP refers to this bus in its documentation as the “External Interface Module” EIM. No internal devices are connected to the external memory bus; hence, the memory bus configuration can be optimized for any application-specific requirement without restrictions. The external memory bus is typically used to connect high-speed devices like FPGAs, DSPs, secondary Ethernet controllers, CAN controllers, etc.

The compatibility of the External Memory Bus with other Colibri modules is very limited. The data pins for the non-multiplexed mode are not located at the position that is compatible with other modules. Only the major signals of the multiplexed 16-bit interface is compatible with the Colibri iMX6 module, but not with any other currently available modules. Therefore, use the interface with care and check for conflicts with other pins.

### Features

- Non-multiplexed mode: 16-bit data bus width (incompatible with other Colibri modules)
- Multiplexed mode up to 16-bit data bus width (limited compatibility with Colibri iMX6 modules)
- Up to 27-bit address bus width
- Asynchronous and burst mode
- Multiplexed and de-multiplexed address/data mode
- Maximum main clock frequency of 132 MHz
- Up to four chip select signals

### 5.8.1 Non-Multiplexed Mode

This mode uses different pins for the addresses and data signals. The interface is incompatible with any other Colibri modules. The following configurations can be used in the non-multiplexed mode:

Table 5-13 Non-Multiplexed Signal Mapping

Peripheral Signals	8bit		16Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 001
A[15:0]	EIM_AD[15:0]	EIM_AD[15:0]	EIM_AD[15:0]
A[26:16]	EIM_ADDR[26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]
D[7:0]	EIM_DATA[7:0]	EIM_DATA [15:8]	EIM_DATA [7:0]
DQM0	EIM_EB0	EIM_EB1	EIM_EB0
D[15:8]			EIM_DATA[15:8]
DQM1			EIM_EB1

### 5.8.2 Multiplexed Mode

In multiplexed mode, AD[15:0] is used for both the data and address signals. This reduces the number of signals required to connect to a device. The multiplexed mode is compatible with the



Colibri iMX6 module with some limitation (not all signals are located at the same place). The EIM\_LBA signal (X1 pin 150) is used for selecting between address and data.

Table 5-14 Multiplexed Signal Mapping

Peripheral Signals (demultiplexed)	16Bit
	MUM = 1, DSZ = 001
A[15:0]	EIM_AD[15:0]
A[25:16]	EIM_ADDR[25:16]
D[7:0]	EIM_AD[7:0]
DQM0	EIM_EB0
D[15:8]	EIM_AD[15:8]
DQM1	EIM_EB1

### 5.8.3 Memory Bus Signals

Table 5-15 Memory Bus Signals

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
111	ADDRESS0	EPDC_D0	weim.AD[0]	I/O	
113	ADDRESS1	EPDC_D1	weim.AD[1]	I/O	
115	ADDRESS2	EPDC_D2	weim.AD[2]	I/O	
117	ADDRESS3	EPDC_D3	weim.AD[3]	I/O	
119	ADDRESS4	EPDC_D4	weim.AD[4]	I/O	
121	ADDRESS5	EPDC_D5	weim.AD[5]	I/O	
123	ADDRESS6	EPDC_D6	weim.AD[6]	I/O	
125	ADDRESS7	EPDC_D7	weim.AD[7]	I/O	Non-multiplexed mode: address bits 15 to 0
110	ADDRESS8	EPDC_BDR1	weim.AD[8]	I/O	Multiplexed mode: address and data bits 15 to 0
112	ADDRESS9	EPDC_PWRCOM	weim.AD[9]	I/O	
114	ADDRESS10	EPDC_SDCLK	weim.AD[10]	I/O	
116	ADDRESS11	EPDC_SDLE	weim.AD[11]	I/O	
118	ADDRESS12	EPDC_SDOE	weim.AD[12]	I/O	
120	ADDRESS13	EPDC_SDSHR	weim.AD[13]	I/O	
122	ADDRESS14	EPDC_SDCE0	weim.AD[14]	I/O	
124	ADDRESS15	EPDC_SDCE1	weim.AD[15]	I/O	
76	LCD RGB Data<0>	LCD_DAT0	weim.DATA[0]	I/O	
70	LCD RGB Data<1>	LCD_DAT1	weim.DATA[1]	I/O	
60	LCD RGB Data<2>	LCD_DAT2	weim.DATA[2]	I/O	Non-multiplexed mode: data bits 15 to 0
58	LCD RGB Data<3>	LCD_DAT3	weim.DATA[3]	I/O	Multiplexed mode: not used
78	LCD RGB Data<4>	LCD_DAT4	weim.DATA[4]	I/O	
72	LCD RGB Data<5>	LCD_DAT5	weim.DATA[5]	I/O	

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
80	LCD RGB Data<6>	LCD_DAT6	weim.DATA[6]	I/O	
46	LCD RGB Data<7>	LCD_DAT7	weim.DATA[7]	I/O	
62	LCD RGB Data<8>	LCD_DAT8	weim.DATA[8]	I/O	
48	LCD RGB Data<9>	LCD_DAT9	weim.DATA[9]	I/O	
74	LCD RGB Data<10>	LCD_DAT10	weim.DATA[10]	I/O	
50	LCD RGB Data<11>	LCD_DAT11	weim.DATA[11]	I/O	
52	LCD RGB Data<12>	LCD_DAT12	weim.DATA[12]	I/O	
54	LCD RGB Data<13>	LCD_DAT13	weim.DATA[13]	I/O	
66	LCD RGB Data<14>	LCD_DAT14	weim.DATA[14]	I/O	
64	LCD RGB Data<15>	LCD_DAT15	weim.DATA[15]	I/O	
127		EPDC_SDCE2	weim.ADDR[16]	O	
130	DQM2	EPDC_SDCE3	weim.ADDR[17]	O	
132	DQM3	EPDC_GDCLK	weim.ADDR[18]	O	
134	ADDRESS25	EPDC_GDOE	weim.ADDR[19]	O	
133		EPDC_GDRL	weim.ADDR[20]	O	Additional address bits 26 to 16, can be used for multiplexed and non-multiplexed mode
104		EPDC_GDSP	weim.ADDR[21]	O	
106	nCS2	EPDC_BDR0	weim.ADDR[22]	O	
140	ADDRESS22	LCD_DAT20	weim.ADDR[23]	O	
142	ADDRESS21	LCD_DAT21	weim.ADDR[24]	O	
144	ADDRESS20	LCD_DAT22	weim.ADDR[25]	O	
146	ADDRESS19	LCD_DAT23	weim.ADDR[26]	O	
61	LCD RGB Data<17>	LCD_DAT17	weim.ACLK_FREERUN	I	AXI clock signal
152	DATA17	EPDC_D11	weim.BCLK	O	Burst Clock
57	LCD RGB Data<16>	LCD_DAT16	weim.CRE	O	CRE/PS signal for CellularRam memory
93	RDnWR	LCD_RESET	weim.DTACK_B	I	Data Acknowledge
126	DQM0	EPDC_D14	weim.EB_B[0]	O	Byte Enable Mask, corresponds to D[7:0]
128	DQM1	EPDC_PWRSTAT	weim.EB_B[1]	O	Byte Enable Mask, corresponds to D[15:8]
105	nCS0	EPDC_D10	weim.CS0_B	O	Chip select signals
107	nCS1	EPDC_D15	weim.CS1_B	O	
136	ADDRESS24	LCD_DAT18	weim.CS2_B	O	
138	ADDRESS23	LCD_DAT19	weim.CS3_B	O	
91	nOE, Recovery Mode	EPDC_D8	weim.OE	O	Output Enable
89	nWE	EPDC_D9	weim.RW	O	Write Enable
95	RDY	EPDC_D13	weim.WAIT	I	Ready/Busy/Wait signal
150	DATA16	EPDC_D12	weim.LBA_B	O	Address Valid, used for multiplexed bus only

## 5.9 I<sup>2</sup>C

The NXP i.MX 7 SoC features four I<sup>2</sup>C controllers; up to three of which can be used externally. They implement the I<sup>2</sup>C V2.1 specification. All of them can be used in master or slave mode. The port I2C1 is used for power management and is not available externally. Port I2C4 is available as standard I<sup>2</sup>C on the module connector. The ports I2C2 and I2C3 are only available as alternate function.

### Features:

- Supports 100kbit/s and fast mode 400kbit/s data transfer
- Multi-master operation
- Software-selectable acknowledge bit
- Interrupt driven, byte-by-byte data transfer
- Start and stop signal generation and detection
- Repeated start signal generation
- Acknowledge bit generation and detection
- Bus-busy detection
- Calling address identification interrupts

There are a lot of low-speed devices which use I<sup>2</sup>C interfaces such as RTCs and sensors, but it is also commonly used to configure other devices such as cameras or displays. The I<sup>2</sup>C Bus can also be used to communicate with SMB (System Management Bus) devices.

Table 5-16 I<sup>2</sup>C Signals (Colibri family compatible interface)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
194	I2C SDA	ENET1_TD3	i2c4.SDA	I/O	Open Drain Data Signal Port 4
196	I2C SCL	ENET1_TD2	i2c4.SCL	I/O	Clock Signal Port 4

Table 5-17 Alternate I<sup>2</sup>C Signals (additional and incompatible with other Colibri family modules)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
146	ADDRESS19	LCD_DAT23			
24	Battery Fault Detect	SAI1_RXC			
67	PWM<D>, Camera Input Data<6>	GPIO1_IO11	i2c4.SDA	I/O	Alternate Open Drain Data Signal Port 4
75	Camera Input MCLK	I2C4_SDA			
144	ADDRESS20	LCD_DAT22			
30	PWM<C>	GPIO1_IO10	i2c4.SCL	I/O	Alternate Clock Signal Port 4
77		SAI1_RXFS			
96	Camera Input PCLK	I2C4_SCL			
29	UART_A DSR	GPIO1_IO07			
36	UART_B RXD	UART2_TXD	i2c2.SDA	I/O	Open Drain Data Signal Port 2
86	SPI CS	I2C2_SDA			
37	UART_A RI, Keypad_In<4>	GPIO1_IO06			
38	UART_B TXD	UART2_RXD	i2c2.SCL	I/O	Clock Signal Port 2
88	SPI CLK	I2C2_SCL			

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
142	ADDRESS21	LCD_DAT21			
28	PWM<B>	GPIO1_IO09	i2c3.SDA	I/O	Open Drain Data Signal Port 3
94	Camera Input HSYNC	I2C3_SDA			
140	ADDRESS22	LCD_DAT20			
59	PWM<A>, Camera Input Data<7>	GPIO1_IO08	i2c3.SCL	I/O	Clock Signal Port 3
81	Camera Input VSYNC	I2C3_SCL			

### 5.9.1 Real-Time Clock (RTC) recommendation

The Colibri iMX7 module features a RTC circuit which is located inside the SoC. The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for time keeping. The RTC is sourced from the VCC\_BATT (pin 40) supply pin.

The RTC on the module is not designed for ultra-low power consumption (typical current consumption can be found in section 9.2). Therefore, a standard lithium coin cell battery can be drained faster than required for certain designs. If a rechargeable RTC battery is not the solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, add the external RTC to the standard interface (pin 194/196) of the module and source the VCC\_BACKUP pin from the 3.3V rail that sources also the main module rail. A suitable reference schematic can be found in the schematic diagram of the Colibri evaluation board. See also section 6.2.

### 5.10 UART

The Colibri iMX7 provides up to seven serial UART interfaces. Three of them are available on dedicated UART pins which are compatible with other Colibri modules. The other four UARTs are only available as an alternate function. These UARTs are incompatible with other Colibri modules. Therefore, the additional four UART should only be used if compatibility with other Colibri modules is not required and more than the three UARTs are required.

The UART\_A interface of the Colibri is defined as a full featured UART. Unfortunately, the NXP i.MX 7 SoC does not feature the DTR, DSR, DCD, and RI as dedicated signals. However, these signals can be emulated by using GPIOs which are located on these SODIMM pins.

The UART\_A is used as standard debug interface for the Toradex Embedded Linux and Windows Embedded Compact operating systems. It is recommended that at least the RXD and TXD lines of this port are kept accessible for system debugging.

The UARTs of the i.MX 7 can be configured either in the DTE (Data Terminal Equipment) or DCE (Data Communication Equipment) mode. Changing the mode will change the direction of all UART pins (data and all control signals). To ensure compatibility with the entire Colibri family, UARTs need to be configured in DTE mode.

Particular attention should be paid to the names of the i.MX 7 data signals. In DTE mode, the UARTx\_RX\_DATA port is transmitting data from the SoC while the UARTx\_TX\_DATA port is receiving it. Therefore, the RX and TX signals need to be swapped. In the following signal descriptions, the port direction is always described for DTE mode.

### UART Features

- High-speed TIA/EIA-232F compatible (up to 4 Mbit/s)
- IrDA-compatible (up to 115.2kbit/s)
- 7 or 8 data bits (9 bit for RS485)
- 1 or 2 stop bits
- Optional parity bit (even or odd)
- Hardware flow control
- Auto detect baud rate
- 32 entries FIFO for receive and transmit

Table 5-18 UART\_A Signal Pins

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
33	UART_A RXD	UART1_TXD	uart1.TX	I	Received Data
35	UART_A TXD	UART1_RXD	uart1.RX	O	Transmitted Data
27	UART_A RTS	SAI2_TXC	uart1.RTS_B	O	Request to Send
25	UART_A CTS, Keypad_In<0>	SAI2_TXFS	uart1.CTS_B	I	Clear to Send
23	UART_A DTR	SD2_DATA0	gpio5.IO[14]	O	GPIO only, DTR need to be emulated
29	UART_A DSR	GPIO1_IO07	gpio1.IO[7]	I	GPIO only, DSR need to be emulated
31	UART_A DCD	SD2_DATA1	gpio5.IO[15]	I	GPIO only, DCD need to be emulated
37	UART_A RI, Keypad_In<4>	GPIO1_IO06	gpio1.IO[6]	I	GPIO only, RI need to be emulated

Table 5-19 UART\_B Signal Pins

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
36	UART_B RXD	UART2_TXD	uart2.TX	I	Received Data
38	UART_B TXD	UART2_RXD	uart2.RX	O	Transmitted Data
34	UART_B RTS	SAI2_TXD	uart2.RTS_B	O	Request to Send
32	UART_B CTS	SAI2_RXD	uart2.CTS_B	I	Clear to Send

Table 5-20 UART\_C Signal Pins

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
19	UART_C RXD	UART3_TXD	uart3.TX	I	Received Data
21	UART_C TXD	UART3_RXD	uart3.RX	O	Transmitted Data

Table 5-21 Signal Pins of additional UART Ports

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
27	UART_A RTS	SAI2_TXC			
31	UART_A DCD	SD2_DATA1	uart4.TX	I	Received Data
86	SPI CS	I2C2_SDA			
23	UART_A DTR	SD2_DATA0			
25	UART_A CTS, Keypad_In<0>	SAI2_TXFS	uart4.RX	O	Transmitted Data
88	SPI CLK	I2C2_SCL			

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
34	UART_B RTS	SAI2_TXD			
92	SPI TXD	I2C1_SDA	uart4.RTS_B	O	Request to Send
102		SD2_DATA3			
32	UART_B CTS	SAI2_RXD			
90	SPI RXD	I2C1_SCL	uart4.CTS_B	I	Clear to Send
100	Keypad_Out<1>	SD2_DATA2			
29	UART_A DSR	GPIO1_IO07	uart5.TX	I	Received Data
75	Camera Input MCLK	I2C4_SDA			
37	UART_A RI, Keypad_In<4>	GPIO1_IO06	uart5.RX	O	Transmitted Data
96	Camera Input PCLK	I2C4_SCL			
169	DATA10	SAI1_RXD			
94	Camera Input HSYNC	I2C3_SDA	uart5.RTS_B	O	Request to Send
81	Camera Input VSYNC	I2C3_SCL	uart5.CTS_B	I	Clear to Send
71	Camera Input Data<0>,LCD Back-Light GPIO	SD1_WP			
89	nWE	EPDC_D9	uart6.TX	I	Received Data
103	Camera Input Data<3>	ECSPI1_MOSI			
69	PS2 SCL2	SD1_CD_B			
91	nOE,Recovery Mode	EPDC_D8	uart6.RX	O	Transmitted Data
101	Camera Input Data<2>	ECSPI1_SCLK			
73		SD1_RESET_B			
79	Camera Input Data<4>	ECSPI1_MISO	uart6.RTS_B	O	Request to Send
105	nCS0	EPDC_D10			
47	SDCard CLK	SD1_CLK			
97	Camera Input Data<5>	ECSPI1_SS0	uart6.CTS_B	I	Clear to Send
152	DATA17	EPDC_D11			
49	SDCard DAT<1>	SD1_DATA1			
59	PWM<A>,Camera Input Data<7>	ECSPI2_MOSI	uart7.TX	I	Received Data
95	RDY	EPDC_D13			
67	PWM<D>,Camera Input Data<6>	ECSPI2_SCLK	uart7.RX	O	Transmitted Data
150	DATA16	EPDC_D12			
192	SDCard DAT<0>	SD1_DATA0			
53	SDCard DAT<3>	SD1_DATA3			
85	Camera Input Data<8>, Keypad_Out<4>	ECSPI2_MISO	uart7.RTS_B	O	Request to Send
126	DQM0	EPDC_D14			
51	SDCard DAT<2>	SD1_DATA2	uart7.CTS_B	I	Clear to Send

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
65	Camera Input Data<9>, Keypad_Out<3>, PS2 SDA2	ECSPI2_SS0			
107	nCS1	EPDC_D15			

These UART ports are only available as alternate functions. Compatibility with other Colibri modules cannot be guaranteed, as they are not standard Colibri module interfaces.

Table 5-22 Alternate UART Signals (additional and incompatible with other Colibri family modules)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
55	PS2 SDA1	ENET1_RD3	uart1.TX	I	Alternate Received Data for UART_A
63	PS2 SCL1	ENET1_RD2	uart1.RX	O	Alternate Transmitted Data for UART_A
44	LCD RGB DE	LCD_ENABLE	uart2.TX	I	Alternate Received Data for UART_B
56	LCD RGB PCLK	LCD_CLK	uart2.RX	O	Alternate Transmitted Data for UART_B
68	LCD RGB HSYNC	LCD_HSYNC	uart2.RTS_B	O	Alternate Request to Send for UART_B
82	LCD RGB VSYNC	LCD_VSYNC	uart2.CTS_B	I	Alternate Clear to Send for UART_B
28	PWM<B>	GPIO1_IO09	uart3.TX	I	Alternate Received Data for UART_C
59	PWM<A>, Camera Input Data<7>	GPIO1_IO08	uart3.RX	O	Alternate Transmitted Data for UART_C
30	PWM<C>	GPIO1_IO10			
131	Usb Host Over-Current Detect	UART3_RTS	uart3.RTS_B	O	Request to Send for UART_C
67	PWM<D>, Camera Input Data<6>	GPIO1_IO11			
129	USB Host Power Enable	UART3_CTS	uart3.CTS_B	I	Clear to Send for UART_C

## 5.11 SPI

The i.MX 7 provides 4 SPI controllers (which are called Enhanced Configurable SPI, ECSPI in the reference manual) all of which are available on the module edge connector. One SPI interface is available as the standard Colibri module interface. This interface is compatible with other Colibri modules. The other SPI interfaces are available as alternate functions. These interfaces are incompatible with other Colibri modules. Please use the standard Colibri SPI interface first before using others.

The SPI ports operate at up to 52 Mbps and provide full duplex, synchronous, serial communication between the Colibri module and internal or external peripheral devices. Each SPI port consists of four signals; clock, chip select (frame), data in, and data out. There are additional chip select signals available as alternate functions to support multiple peripherals.

### Features:

- Up to 52 Mbps
- 32bit x 64 deep FIFO (RX and TX)
- Master/Slave configurable
- Simultaneous receive and transmit
- Low power mode
- DMA support

Each SPI channel supports four different modes of the SPI protocol:

Table 5-23 SPI Modes

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	Clock is positive polarity and the data is latched on the positive edge of SCK
1	0	1	Clock is positive polarity and the data is latched on the negative edge of SCK
2	1	0	Clock is negative polarity and the data is latched on the positive edge of SCK
4	1	1	Clock is negative polarity and the data is latched on the negative edge of SCK

SPI can be used as a fast interface for ADCs, DACs, FPGAs, etc. Some LCD displays require configuration over SPI prior to being driven via the RGB or LVDS interface.

Table 5-24 SPI Signals (Colibri family compatible interface)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
92	SPI TXD	I2C1_SDA	ecspi3.MOSI	O	Master Output, Slave Input
90	SPI RXD	I2C1_SCL	ecspi3.MISO	I	Master Input, Slave Output
86	SPI CS	I2C2_SDA	ecspi3.SS0	O	Slave Select
88	SPI CLK	I2C2_SCL	ecspi3.SCLK	O	Serial Clock

Table 5-25 SPI Signals (additional and incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
19	UART_C RXD	UART3_TXD	ecspi1.MOSI	O	Master Output, Slave Input
103	Camera Input Data<3>	ECSPI1_MOSI			
21	UART_C TXD	UART3_RXD	ecspi1.MISO	I	Master Input, Slave Output
79	Camera Input Data<4>	ECSPI1_MISO			
97	Camera Input Data<5>	ECSPI1_SS0	ecspi1.SS0	O	Slave Select 0
129	USB Host Power Enable	UART3_CTS			
35	UART_A TXD	UART1_RXD	ecspi1.SS1	O	Slave Select 1
33	UART_A RXD	UART1_TXD	ecspi1.SS2	O	Slave Select 2
38	UART_B TXD	UART2_RXD	ecspi1.SS3	O	Slave Select 3
101	Camera Input Data<2>	ECSPI1_SCLK	ecspi1.SCLK	O	Serial Clock
131	Usb Host Over-Current Detect	UART3_RTS			
36	UART_B RXD	UART2_TXD	ecspi1.RDY	I	Data ready signal
55	PS2 SDA1	ENET1_RD3	ecspi2.MOSI	O	Master Output, Slave Input
59	PWM<A>, Camera Input Data<7>	ECSPI2_MOSI			
85	Camera Input Data<8>, Keypad_Out<4>	ECSPI2_MISO	ecspi2.MISO	I	Master Input, Slave Output
196	I2C SCL	ENET1_TD2			



X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
63	PS2 SCL1	ENET1_RD2			
67	PWM<D>, Camera Input Data<6>	ECSPI2_SCLK	ecspi2.SCLK	O	Serial Clock
65	Camera Input Data<9>, Keypad_Out<3>, PS2 SDA2	ECSPI2_SS0	ecspi2.SS0	O	Slave Select 0
194	I2C SDA	ENET1_TD3			
44	LCD RGB DE	LCD_ENABLE			
71	Camera Input Data<0>, LCD Back-Light GPIO	SD1_WP	ecspi4.MOSI	O	Master Output, Slave Input
56	LCD RGB PCLK	LCD_CLK			
69	PS2 SCL2	SD1_CD_B	ecspi4.MISO	I	Master Input, Slave Output
68	LCD RGB HSYNC	LCD_HSYNC			
73		SD1_RESET_B	ecspi4.SCLK	O	Serial Clock
47	SDCard CLK	SD1_CLK			
82	LCD RGB VSYNC	LCD_VSYNC	ecspi4.SS0	O	Slave Select 0
190	SDCard CMD	SD1_CMD	ecspi4.SS1	O	Slave Select 1
192	SDCard DAT<0>	SD1_DATA0	ecspi4.SS2	O	Slave Select 2
49	SDCard DAT<1>	SD1_DATA1	ecspi4.SS3	O	Slave Select 3
51	SDCard DAT<2>	SD1_DATA2	ecspi4.RDY	I	Data ready signal

Table 5-26 Alternate Signals of main SPI (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
27	UART_A RTS	SAI2_TXC	ecspi3.MOSI	O	Alternate Master Output, Slave Input
25	UART_A CTS, Keypad_In<0>	SAI2_TXFS	ecspi3.MISO	I	Alternate Master Input, Slave Output
34	UART_B RTS	SAI2_TXD	ecspi3.SS0	O	Alternate Slave Select 0
53	SDCard DAT<3>	SD1_DATA3	ecspi3.SS1	O	Additional Slave Select 1
32	UART_B CTS	SAI2_RXD	ecspi3.SCLK	O	Alternate Serial Clock
98	Camera Input Data<1>	SD2_RESET_B	ecspi3.RDY	I	Additional Data ready signal

## 5.12 PWM (Pulse Width Modulation)

The Colibri iMX7 features a dedicated Pulse Width Modulator (PWM) with four channels. Each PWM channel features a 16 bit up-counter with clock source selection. There is a 16 bit 4 level deep FIFO available in order to minimize the interrupt overhead. There is a 12 bit prescaler available for dividing the clock.

Additional to the dedicated PWM, the i.MX 7 SoC features a FlexTimer Module (FTM). This module features two eight-channel timers that support input capture, output compare, and the generation of PWM signals. This means that additional 16 PWM outputs are available to the four dedicated PWM channels. These additional PWM channels are only available at alternative functions of the module edge pins and therefore are incompatible with other Colibri modules.

The PWM interface can be used as an easy way to emulate a DAC and generate a variable DC voltage if used with a suitable RC circuit. Other uses include control of LED brightness, display backlights, or servo motors.

Table 5-27 PWM Interface Signals

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Remarks
59	PWM<A>, Camera Input Data<7>	GPIO1_IO08	pwm1.OUT	O	PWM Output 1
28	PWM<B>	GPIO1_IO09	pwm2.OUT	O	PWM Output 2
30	PWM<C>	GPIO1_IO10	pwm3.OUT	O	PWM Output 3
67	PWM<D>, Camera Input Data<6>	GPIO1_IO11	pwm4.OUT	O	PWM Output 4

Table 5-28 Locations of FlexTimer Interface Signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Remarks
71	Camera Input Data<0>, LCD Back-Light GPIO	SD1_WP	flextimer1.CH[1]	I/O	FTM channel (PWM Output/ input capture/ output compare)
120	ADDRESS13	EPDC_SDSHR			
73		SD1_RESET_B	flextimer1.CH[2]	I/O	FTM channel (PWM Output/ input capture/ output compare)
122	ADDRESS14	EPDC_SDCE0			
47	SDCard CLK	SD1_CLK	flextimer1.CH[3]	I/O	FTM channel (PWM Output/ input capture/ output compare)
124	ADDRESS15	EPDC_SDCE1			
57	LCD RGB Data<16>	LCD_DAT16	flextimer1.CH[4]	I/O	FTM channel (PWM Output/ input capture/ output compare)
61	LCD RGB Data<17>	LCD_DAT17	flextimer1.CH[5]	I/O	FTM channel (PWM Output/ input capture/ output compare)
37	UART_A RI, Keypad_In<4>	GPIO1_IO06	flextimer1.CH[6]	I/O	FTM channel (PWM Output/ input capture/ output compare)
136	ADDRESS24	LCD_DAT18			
29	UART_A DSR	GPIO1_IO07	flextimer1.CH[7]	I/O	FTM channel (PWM Output/ input capture/ output compare)
138	ADDRESS23	LCD_DAT19			
69	PS2 SCL2	SD1_CD_B	flextimer1.CH[0]	I/O	FTM channel (PWM Output/ input capture/ output compare)
118	ADDRESS12	EPDC_SDOE			
132	DQM3	EPDC_GDCLK	flextimer2.CH[0]	I/O	FTM channel (PWM Output/ input capture/ output compare)
190	SDCard CMD	SD1_CMD			
51	SDCard DAT<2>	SD1_DATA2	flextimer2.CH[3]	I/O	FTM channel (PWM Output/ input capture/ output compare)
104		EPDC_GDSP			
134	ADDRESS25	EPDC_GDOE	flextimer2.CH[1]	I/O	FTM channel (PWM Output/ input capture/ output compare)
192	SDCard DAT<0>	SD1_DATA0			
49	SDCard DAT<1>	SD1_DATA1	flextimer2.CH[2]	I/O	FTM channel (PWM Output/ input capture/ output compare)
133		EPDC_GDRL			
25	UART_A CTS, Keypad_In<0>	SAI2_TXFS	flextimer2.CH[4]	I/O	FTM channel (PWM Output/ input capture/ output compare)
140	ADDRESS22	LCD_DAT20			
27	UART_A RTS	SAI2_TXC	flextimer2.CH[5]	I/O	

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Remarks
142	ADDRESS21	LCD_DAT21			FTM channel (PWM Output/ input capture/ output compare)
32	UART_B CTS	SAI2_RXD	flextimer2.CH[6]	I/O	FTM channel (PWM Output/ input capture/ output compare)
144	ADDRESS20	LCD_DAT22			
34	UART_B RTS	SAI2_TXD	flextimer2.CH[7]	I/O	FTM channel (PWM Output/ input capture/ output compare)
146	ADDRESS19	LCD_DAT23			

Table 5-29 Alternate Locations of main PWM Interface Signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Remarks
45	WAKEUP Source<1>	GPIO1_IO01	pwm1.OUT	O	Alternate Pin for PWM Output 1
135	SPDIF_IN	GPIO1_IO02	pwm2.OUT	O	Alternate Pin for PWM Output 2
22	VDD Fault Detect	GPIO1_IO03	pwm3.OUT	O	Alternate Pin for PWM Output 3
43	WAKEUP Source<0>,SDCard CardDetect	GPIO1_IO00	pwm4.OUT	O	Alternate Pin for PWM Output 4

### 5.13 OWR (One Wire)

The Colibri iMX7 does not feature a One Wire interface.

### 5.14 SD/MMC

The i.MX 7 SoC Dual as well as Solo provides two SDIO interfaces that are available on the module edge connector. The i.MX 7 Dual features an additional third SDIO interface which is not available externally since the pins are shared with the internal NAND interface. To ensure carrier board design compatibility with other Colibri modules, only the standard Colibri SD/MMC interface should be used. The second SD/MMC interface is available as alternate functions.

The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards, and eMMC devices. The controllers can act as both master and slave simultaneously.

The Colibri iMX7 supports UHS-I which allows up to 104 Mbyte/s transfer speed on its standard SD card interface. But UHS-I requires 1.8V IO level which is not in the Colibri module specification. Since the 1.8V capability is not mandatory in the Colibri module specification, other modules may support only 3.3V logic level. Pay attention to the SD card signal pull-up resistors on the carrier board. If the interface is used in the 1.8V mode, it is recommended to remove the pull-up resistors on the carrier board. The i.MX 7 features internal pull-up resistors which can be used instead.

Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage	Remarks
Default Speed	25 MHz	12.5 MByte/s	3.3V	Colibri Standard
High Speed	50 MHz	25 MByte/s	3.3V	
SDR12	25 MHz	12.5 MByte/s	1.8V	UHS-I May not compatible with other modules
SDR25	50 MHz	25 MByte/s	1.8V	
DDR50	50 MHz	50 MByte/s	1.8V	
SDR50	100 MHz	50 MByte/s	1.8V	
SDR104	208 MHz	104 MByte/s	1.8V	

Since the SODIMM pin 69, 71, and 73 are connected to SoC balls that share in the same voltage bank as the main SD interface, these pins will also change their voltage level to 1.8V if the SD card IO voltage is changed. Therefore, use pin **69**, **71**, and **73** with special care. Only the CLK, CMD, and DATA[0..3] signals of the standard SD interface can change the voltage to 1.8V. The additional DATA[4..7] support only 3.3V. Therefore, it is not possible to use the 8bit eMMC with the reduced signal voltage.

#### Features

- Supports SD Memory Card Specification 3.0
- Supports SDIO Card Specification Version 3.0
- Supports MMC System Specification Version 4.2, 4.3, 4.4, 4.41, 4.5, and 5.0
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TByte
- Supports SPI mode
- Up to 8 bit interface (only 4 bit compatible with other modules)
- Supports SD UHS-I mode (up to 208MHz) with 1.8V IO voltage level (only standard SD port).

i.MX 7 SDIO interface	Max Bus Width	Description
USDHC1	4bit (8bit)	Colibri Standard SD/MMC interface, additional data bits for 8 bit interface available as alternate function
USDHC2	8bit	Available as an alternate function incompatible with Colibri standard
USDHC3	-	Unavailable at the module edge connector

Table 5-30 Colibri SD/MMC Signal Pins

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
190	SDCard CMD	SD1_CMD	usdhc1.CMD	I/O	Command
192	SDCard DAT<0>	SD1_DATA0	usdhc1.DATA0	I/O	Serial Data 0
49	SDCard DAT<1>	SD1_DATA1	usdhc1.DATA1	I/O	Serial Data 1
51	SDCard DAT<2>	SD1_DATA2	usdhc1.DATA2	I/O	Serial Data 2
53	SDCard DAT<3>	SD1_DATA3	usdhc1.DATA3	I/O	Serial Data 3
47	SDCard CLK	SD1_CLK	usdhc1.CLK	O	Serial Clock
43	WAKEUP Source<0>,SDCard CardDetect	GPIO1_IO00	gpio1.IO[0]	I	Card Detect (regular GPIO)

Table 5-31 Additional SD/MMC Signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
67	PWM<D>,Camera Input Data<6>	ECSPI2_SCLK	usdhc1.DATA4	I/O	Serial Data 4 (only for 8bit MMC)
59	PWM<A>,Camera Input Data<7>	ECSPI2_MOSI	usdhc1.DATA5	I/O	Serial Data 5 (only for 8bit MMC)
85	Camera Input Data<8>, Keypad_Out<4>	ECSPI2_MISO	usdhc1.DATA6	I/O	Serial Data 6 (only for 8bit MMC)
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	ECSPI2_SS0	usdhc1.DATA7	I/O	Serial Data 7 (only for 8bit MMC)
73		SD1_RESET_B	usdhc1.RESET_B	O	Dedicated Card Reset (usually not needed)
71	Camera Input Data<0>,LCD Back- Light GPIO	SD1_WP	usdhc1.WP	I	Dedicated Write Protect

The additional SD/MMC signals allow the SD/MMC interface to be used as an 8 bit interface. The pins are incompatible with other Colibri modules, as it is not part of the Colibri module specification.

Table 5-32 Additional SD/MMC interface (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
186	ADDRESS17	SD2_CMD	usdhc2.CMD	I/O	Command
23	UART_A DTR	SD2_DATA0	usdhc2.DATA0	I/O	Serial Data 0
31	UART_A DCD	SD2_DATA1	usdhc2.DATA1	I/O	Serial Data 1
100	Keypad_Out<1>	SD2_DATA2	usdhc2.DATA2	I/O	Serial Data 2
102		SD2_DATA3	usdhc2.DATA3	I/O	Serial Data 3
101	Camera Input Data<2>	ECSPI1_SCLK	usdhc2.DATA4	I/O	Serial Data 4 (only for 8bit MMC)
103	Camera Input Data<3>	ECSPI1_MOSI	usdhc2.DATA5	I/O	Serial Data 5 (only for 8bit MMC)
79	Camera Input Data<4>	ECSPI1_MISO	usdhc2.DATA6	I/O	Serial Data 6 (only for 8bit MMC)
97	Camera Input Data<5>	ECSPI1_SS0	usdhc2.DATA7	I/O	Serial Data 7 (only for 8bit MMC)
184	ADDRESS18	SD2_CLK	usdhc2.CLK	O	Serial Clock
98	Camera Input Data<1>	SD2_RESET_B	usdhc2.RESET_B	O	Dedicated Card Reset (usually not needed)

## 5.15 Analogue Audio

The Colibri iMX7 offers analogue audio input and output channels. The module features a NXP SGTL5000 chip to provide the analogue audio interface. The SGTL5000 is connected over I2S (SAI1) with the i.MX 7 SoC. Please consult the NXP SGTL5000 datasheet for more information.

Table 5-33 Analogue Audio Interface Pins

X1 Pin #	Colibri STD Function	I/O	Description	Pin on the SGTL5000 (20pin QFN)
1	MIC_IN	I	Microphone input	10
3	MIC_GND		Microphone pseudo-ground. Possible to connect to GND. Controlled by GPIO6_IO21 (ball RGMII_TD1)	
5	LINEIN_L	I	Left Line Input	9
7	LINEIN_R	I	Right Line Input	8
15	HEADPHONE_L	O	Headphone Left Output	4
17	HEADPHONE_R	O	Headphone Right Output	1
13	HEADPHONE_GND		Headphone pseudo-ground (do not connect to ground!)	2

## 5.16 Audio Codec Interface

The Colibri module does not feature an audio codec interface as standard. Nevertheless, it is possible to access two of the internal three synchronous audio interfaces (SAI) of the i.MX 7 SoC at the module edge connector as alternate functions. The interfaces can be used as Intel® Audio Codec '97 (also known as AC'97 or AC97) or as I2S (also known as Inter-IC Sound, Integrated Interchip Sound, or IIS). The interfaces can be used to connect an additional external audio codec that can provide up to 5.1 channel audio.

The audio codec on the module which provides the analogue audio interface is connected to the SAI1 interface of the digital audio multiplexer and is used in the I<sup>2</sup>S mode.

Table 5-34 Synchronous Serial Interface (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
19	UART_C RXD	UART3_TXD			
49	SDCard DAT<1>	SD1_DATA1	sai3.TX_BCLK	I/O	Transmit Clock
51	SDCard DAT<2>	SD1_DATA2			
129	USB Host Power Enable	UART3_CTS	sai3.TX_SYNC	I/O	Transmit Frame Sync
53	SDCard DAT<3>	SD1_DATA3			
131	Usb Host Over-Current Detect	UART3_RTS	sai3.TX_DATA[0]	O	Data Transmit
38	UART_B TXD	UART2_RXD			
190	SDCard CMD	SD1_CMD	sai3.RX_BCLK	I/O	Receive Clock
21	UART_C TXD	UART3_RXD			
47	SDCard CLK	SD1_CLK	sai3.RX_SYNC	I/O	Receive Frame Sync
36	UART_B RXD	UART2_TXD			
192	SDCard DAT<0>	SD1_DATA0	sai3.RX_DATA[0]	I	Data Receive
22	VDD Fault Detect	GPIO1_IO03			
33	UART_A RXD	UART1_TXD	sai3.MCLK	I/O	Master Clock
73		SD1_RESET_B			
27	UART_A RTS	SAI2_TXC			
31	UART_A DCD	SD2_DATA1	sai2.TX_BCLK	I/O	Transmit Clock
25	UART_A CTS, Keypad_In<0>	SAI2_TXFS			
100	Keypad_Out<1>	SD2_DATA2	sai2.TX_SYNC	I/O	Transmit Frame Sync
34	UART_B RTS	SAI2_TXD			
102		SD2_DATA3	sai2.TX_DATA[0]	O	Data Transmit
24	Battery Fault Detect	SAI1_RXC			
186	ADDRESS17	SD2_CMD	sai2.RX_BCLK	I/O	Receive Clock
77		SAI1_RXFS			
184	ADDRESS18	SD2_CLK	sai2.RX_SYNC	I/O	Receive Frame Sync
23	UART_A DTR	SD2_DATA0			
32	UART_B CTS	SAI2_RXD	sai2.RX_DATA[0]	I	Data Receive

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
98	Camera Input Data<1>	SD2_RESET_B	sai2.MCLK	I/O	Master Clock
135	SPDIF_IN	GPIO1_IO02			

### 5.16.1 Digital Audio Port used as I<sup>2</sup>S

The following signals are used for the I<sup>2</sup>S interface:

Table 5-35 Digital Audio port used as Master I<sup>2</sup>S

iMX7 Port Name	I <sup>2</sup> S Signal Name (Names at Codec)	I/O (at iMX7)	Description
TX_DATA[0]	SDIN	O	Serial Data Output from i.MX 7 SoC
RX_DATA[0]	SDOUT	I	Serial Data Input to i.MX 7 SoC
TX_SYNC	WS	O	Word Select, also known as Field Select or LRCLK
TX_BCLK	SCK	O	Serial Continuous Clock

Table 5-36 Digital Audio port used as Slave I<sup>2</sup>S

iMX7 Port Name	I <sup>2</sup> S Signal Name (Names at Codec)	I/O (at iMX7)	Description
RX_DATA[0]	SDOUT	I	Serial Data Input to i.MX 7 SoC
TX_DATA[0]	SDIN	O	Serial Data Output from i.MX 7 SoC
TX_SYNC	WS	I	Word Select, also known as Field Select or LRCLK
TX_BCLK	SCK	I	Serial Continuous Clock

The audio codecs require a master clock input and often an I<sup>2</sup>C interface for control. Any of the available I<sup>2</sup>C interfaces can be used (see section 5.9). Every SAI channel has a dedicated master clock signal that can be configured as input or output according to the need of the codec.

### 5.16.2 Digital Audio Port used as AC'97

The SAI interface can be configured as an AC'97 compatible interface. The AC'97 Audio interface does not require an additional I<sup>2</sup>C for the control communication. The codec is controlled directly through the AC'97 Audio interface. The AC'97 Audio codec requires a master reference clock. Since every SAI has a dedicated master clock output, this clock signal can be used. However, it is also possible to use a separate crystal/oscillator. Please take care with the pin naming of some codecs. Some devices name their data input pin as SDATA\_OUT and the data output pin as SDATA\_IN. The names refer to the signals they should be connected to on the host (e.g. i.MX 7 SoC), and not to the signal direction.

Table 5-37 Digital Audio port used as AC'97

iMX7 Port Name	I <sup>2</sup> S Signal Name (Names at Codec)	I/O (at iMX7)	Description
RX_DATA[0]	SDATA_IN	I	AC'97 Audio Serial Input to i.MX 7
TX_DATA[0]	SDATA_OUT	O	AC'97 Audio Serial Output from i.MX 7
TX_SYNC	SYNC	O	AC'97 Audio Sync
TX_BCLK	BIT_CLK	I	AC'97 Audio Bit Clock
GPIOx	RESET#	O	AC'97 Master H/W Reset (use any GPIO)

## 5.17 Medium Quality Sound (MQS)

The medium quality sound interface can be used to generate medium quality audio via a standard GPIO. The PWM output signal does not require an external DAC or codec chip. The advantage over using the high quality analogue audio output of the on module SGT5000 is the option to use a simple switching power amplifier circuit (Class-D amplifier).

The MQS is sourced by SAI1 with a 2 channel 16 bit 44.1 kHz or 48 kHz audio signals which is basically an I<sup>2</sup>S signal. Since this is the same SAI channel that is used by the on module audio codec, it is not possible to use MQS simultaneous with the analogue audio output. The signal to noise ratio (SNR) is expected to be no more than 20 dB for signals below 10 kHz. For signals with higher frequencies, the SNR is even worse.

Table 5-38 MQS Interface Signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
186	ADDRESS17	SD2_CMD	mqs.LEFT	O	Left MQS Channel
24	Battery Fault Detect	SAI1_RXC			
77		SAI1_RXFS	mqs.RIGHT	O	Right MQS Channel
184	ADDRESS18	SD2_CLK			

## 5.18 S/PDIF (Sony-Philips Digital Interface I/O)

The Colibri iMX7 does not features an S/PDIF interface.

## 5.19 Touch Panel Interface

The Colibri iMX7 provides a 4-wire resistive touch interface using the Analog Device AD7879-1 Touchscreen Controller. It is connected with the i.MX 7 SoC via the power management I<sup>2</sup>C interface (I2C1). The AD7879-1 does not support 5-wire operation mode. Please consult the Analog Device AD7879-1 documentation for more information.

Table 5-39 Touch Interface Pins

X1 Pin#	Colibri STD Function	AD7879 Pin#	AD7879 Pin Name	I/O	Description
14	TSPX	A3	X+	I/O	X+ (4-wire)
16	TSMX	C3	X-	I/O	X- (4-wire)
18	TSPY	B3	Y+	I/O	Y+ (4-wire)
20	TSMY	D3	Y-	I/O	Y- (4-wire)

## 5.20 Analogue Inputs

The analogue inputs are provided by the NXP i.MX 7 SoC itself. The SoC features two ADCs with both 4 channel inputs. Only ADC1 is available on the SODIMM connector and therefore can be used. Pay attention, the input voltage range is only 1.8V and not 3.3V as on other Colibri modules. On the module, there are 10k series resistors placed in the ADC lines in order to protect the SoC input.



#### Features

- 12-bit ADC
- 0 to 1.8V (full scale)
- Sample rate up to 1MHz
- DMA support
- Conversion complete, hardware average complete, and compare interrupt
- Automatic compare for less than, greater than, equal to, within range, or out of range

Table 5-40 Analogue Inputs Pins

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Function	I/O	Description
8	Analogue Input <0>	ADC1_IN0	ADC1_IN0	I	Analog input 1 (1.8V max)
6	Analogue Input <1>	ADC1_IN1	ADC1_IN1	I	Analog input 1 (1.8V max)
4	Analogue Input <2>	ADC1_IN2	ADC1_IN2	I	Analog input 1 (1.8V max)
2	Analogue Input <3>	ADC1_IN3	ADC1_IN3	I	Analog input 1 (1.8V max)

## 5.21 Camera Interface

The i.MX 7 SoC itself has two camera inputs; a parallel camera interface that is called camera sensor interface (CSI) and a two data lane MIPI/CSI-2. It is important not to confuse these two interfaces since their names are quite similar. CSI is the parallel camera interface while MIPI/CSI-2 is the serial one. Since the Colibri module standard does not contain the serial MIPI/CSI-2 interface, this camera is not available on the module edge connector. Only the parallel interface is available.

The Colibri iMX7 features up to one 24 bit parallel camera interfaces. Only 8 bits of the camera interface are available on pins that are compatible with other Colibri modules. The remaining bits of the interface are only available as alternate functions. These pins are not guaranteed to be compatible with other Colibri modules.

#### Features

- Raw (Bayer), RGB, YUV input
- Maximum pixel clock frequency 133 MHz
- 8/10/16/24bit parallel video interface
- Dedicated synchronisation signals (VSYNC, HSYNC) or embedded in data stream (BT.656)

Although the location for the 8 bits of the camera interface is equal to other modules, the colour mapping might be different. Please carefully read the datasheets of the other Colibri modules for more information regarding available colour modes.

Table 5-41 Parallel Camera Interface Pins

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
101	Camera Input Data<2>	ECSPI1_SCLK	csi1.DATA[2]	I	Camera pixel data
103	Camera Input Data<3>	ECSPI1_MOSI	csi1.DATA[3]	I	Camera pixel data
79	Camera Input Data<4>	ECSPI1_MISO	csi1.DATA[4]	I	Camera pixel data
97	Camera Input Data<5>	ECSPI1_SS0	csi1.DATA[5]	I	Camera pixel data
67	PWM<D>, Camera Input Data<6>	ECSPI2_SCLK	csi1.DATA[6]	I	Camera pixel data

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
59	PWM<A>, Camera Input Data<7>	ECSPI2_MOSI	csi1.DATA[7]	I	Camera pixel data
85	Camera Input Data<8>, Keypad_Out<4>	ECSPI2_MISO	csi1.DATA[8]	I	Camera pixel data
65	Camera Input Data<9>, Keypad_Out<3>, PS2 SDA2	ECSPI2_SS0	csi1.DATA[9]	I	Camera pixel data
96	Camera Input PCLK	I2C4_SCL	csi1.PIXCLK	I	Camera pixel clock
94	Camera Input HSYNC	I2C3_SDA	csi1.HSYNC	I	Camera horizontal sync
81	Camera Input VSYNC	I2C3_SCL	csi1.VSYNC	I	Camera vertical sync
75	Camera Input MCLK	I2C4_SDA	csi1.MCLK	O	Camera reference clock output

The camera modules often require an additional I<sup>2</sup>C interface for control purposes. Any available I<sup>2</sup>C interface can be used (see section 5.9). The following table shows the additional signals for the CSI camera interface for up to 24 bit connections. Please be aware that these signals are alternate functions and are incompatible with other modules.

Table 5-42 Additional Camera Input Signals for 20-bit Interface on non-standard Colibri Pin

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
61	LCD RGB Data<17>	LCD_DAT17	csi1.DATA[0]	I	Additional camera pixel data [0..1]
57	LCD RGB Data<16>	LCD_DAT16	csi1.DATA[1]	I	
64	LCD RGB Data<15>	LCD_DAT15	csi1.DATA[2]	I	
66	LCD RGB Data<14>	LCD_DAT14	csi1.DATA[3]	I	Alternate pin for camera pixel data [2..9]
54	LCD RGB Data<13>	LCD_DAT13	csi1.DATA[4]	I	
52	LCD RGB Data<12>	LCD_DAT12	csi1.DATA[5]	I	
50	LCD RGB Data<11>	LCD_DAT11	csi1.DATA[6]	I	
74	LCD RGB Data<10>	LCD_DAT10	csi1.DATA[7]	I	
48	LCD RGB Data<9>	LCD_DAT9	csi1.DATA[8]	I	
62	LCD RGB Data<8>	LCD_DAT8	csi1.DATA[9]	I	
146	ADDRESS19	LCD_DAT23	csi1.DATA[10]	I	
144	ADDRESS20	LCD_DAT22	csi1.DATA[11]	I	Additional camera pixel data [10..23]
142	ADDRESS21	LCD_DAT21	csi1.DATA[12]	I	
140	ADDRESS22	LCD_DAT20	csi1.DATA[13]	I	
138	ADDRESS23	LCD_DAT19	csi1.DATA[14]	I	
136	ADDRESS24	LCD_DAT18	csi1.DATA[15]	I	
56	LCD RGB PCLK	LCD_CLK	csi1.DATA[16]	I	
44	LCD RGB DE	LCD_ENABLE	csi1.DATA[17]	I	
68	LCD RGB HSYNC	LCD_HSYNC	csi1.DATA[18]	I	
82	LCD RGB VSYNC	LCD_VSYNC	csi1.DATA[19]	I	
76	LCD RGB Data<0>	LCD_DAT0	csi1.DATA[20]	I	
70	LCD RGB Data<1>	LCD_DAT1	csi1.DATA[21]	I	Alternate pin for pixel clock
60	LCD RGB Data<2>	LCD_DAT2	csi1.DATA[22]	I	
58	LCD RGB Data<3>	LCD_DAT3	csi1.DATA[23]	I	
80	LCD RGB Data<6>	LCD_DAT6	csi1.PIXCLK	I	Alternate pin for pixel clock
72	LCD RGB Data<5>	LCD_DAT5	csi1.HSYNC	I	Alternate pin for horizontal sync
78	LCD RGB Data<4>	LCD_DAT4	csi1.VSYNC	I	Alternate pin for vertical sync
46	LCD RGB Data<7>	LCD_DAT7	csi1.MCLK	O	Alternate pin for master clock
93	RDnWR	LCD_RESET	csi1.FIELD	I	Field Identification (optional, identification of the upper or lower field for interlaced input formats)

Table 5-43 Camera Interface Colour Pin Mapping

iMX7 Port Name	Bayer 10bit Generic	BT656/ YUV 8bit/ CCIR656	RGB888 8bit 3 cycle	YCbCr 8bit 2 cycle	RGB565 16bit 1 cycle	YCbCr 16bit 1 cycle	RGB666 18bit 1 cycle	RGB888 24bit 1 cycle	YCbCr 24bit 1 cycle
csi1.DATA[0]	D0				B0	C0	B4	B0	Cr0
csi1.DATA[1]	D1				B1	C1	B5	B1	Cr1
csi1.DATA[2]	D2	Y/C0	R/G/B0	Y/C0	B2	C2	B0	B2	Cr2
csi1.DATA[3]	D3	Y/C1	R/G/B1	Y/C1	B3	C3	B1	B3	Cr3
csi1.DATA[4]	D4	Y/C2	R/G/B2	Y/C2	B4	C4	B2	B4	Cr4
csi1.DATA[5]	D5	Y/C3	R/G/B3	Y/C3	G0	C5	B3	B5	Cr5
csi1.DATA[6]	D6	Y/C4	R/G/B4	Y/C4	G1	C6	B4	B6	Cr6
csi1.DATA[7]	D7	Y/C5	R/G/B5	Y/C5	G2	C7	B5	B7	Cr7
csi1.DATA[8]	D8	Y/C6	R/G/B6	Y/C6	G3	Y0	G4	G0	Cb0
csi1.DATA[9]	D9	Y/C7	R/G/B7	Y/C7	G4	Y1	G5	G1	Cb1
csi1.DATA[10]					G5	Y2	G0	G2	Cb2
csi1.DATA[11]					R0	Y3	G1	G3	Cb3
csi1.DATA[12]					R1	Y4	G2	G4	Cb4
csi1.DATA[13]					R2	Y5	G3	G5	Cb5
csi1.DATA[14]					R3	Y6	G4	G6	Cb6
csi1.DATA[15]					R4	Y7	G5	G7	Cb7
csi1.DATA[16]							R4	R0	Y0
csi1.DATA[17]							R5	R1	Y1
csi1.DATA[18]							R0	R2	Y2
csi1.DATA[19]							R1	R3	Y3
csi1.DATA[20]							R2	R4	Y4
csi1.DATA[21]							R3	R5	Y5
csi1.DATA[22]							R4	R6	Y6
csi1.DATA[23]							R5	R7	Y7

## 5.22 Clock Output

The i.MX 7 SoC has two general purpose clock output channels (CLKO1 and CLKO2) which are available on different SoC pins. Since the SAI (audio), CSI (camera), as well as RMII (Ethernet) interfaces feature dedicated reference clock outputs, the general purpose clock outputs are not reserved for the internal audio codec or the Ethernet PHY.

Additionally to the two general purpose clock outputs, the i.MX 7 features four external clock inputs. The clock control module (CCM) of the SoC allows routing these clock inputs to different peripheral clocks. Further information can be found in the NXP i.MX 7 reference manual.

Table 5-44 External Clock Signal Pins (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
69	PS2_SCL2	SD1_CD_B	ccm.CLKO1	O	General Purpose Clock Output 1
135	SPDIF_IN	GPIO1_IO02			

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
22	VDD Fault Detect	GPIO1_IO03			
71	Camera Input Data<0>,LCD Back-Light GPIO	SD1_WP	ccm.CLKO2	O	General Purpose Clock Output 2
192	SDCard DAT<0>	SD1_DATA0	ccm.EXT_CLK1	I	External Clock Input 1
49	SDCard DAT<1>	SD1_DATA1	ccm.EXT_CLK2	I	External Clock Input 2
51	SDCard DAT<2>	SD1_DATA2			
137	USB Client Cable Detect,SPDIF_OUT	ENET1_CRS	ccm.EXT_CLK3	I	External Clock Input 3
188	ADDRESS16	GPIO1_IO14			
53	SDCard DAT<3>	SD1_DATA3	ccm.EXT_CLK4	I	External Clock Input 4
178	DATA30	GPIO1_IO15			

## 5.23 Keypad

You can use any free GPIOs to realize a matrix keypad interface. Such a software solution does not come with any additional hardware support. This is the preferred solution if a carrier board needs to be compatible with different Colibri modules.

Additionally, the i.MX 7 SoC features a keyboard controller with hardware support. As the keyboard controller is only available as an alternate function, this interface is incompatible with other Colibri modules and can only be used if the required pins are being used for their primary function.

The keyboard controller eliminates the requirement for de-bounce capacitors and pull-up resistors. It can handle up to two buttons being pressed without the need for de-ghosting diodes. If the diodes are available, any combination of pressed keys can be detected. The row and column pins can be configured for a keyboard matrix of up to 8 by 8.

### Features

- Open drain design
- Glitch suppression circuit
- Multiple-key detection
- Long key-press detection
- Standby key-press detection
- 2-point as well as 3-point key matrix supported

Table 5-45 Keyboard Matrix Interface Signals

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
125	ADDRESS7	EPDC_D7	kpp.COL[0]	O	Keyboard column 0
121	ADDRESS5	EPDC_D5	kpp.COL[1]	O	Keyboard column 1
55	PS2 SDA1	ENET1_RD3	kpp.COL[2]	O	Keyboard column 2
117	ADDRESS3	EPDC_D3			
113	ADDRESS1	EPDC_D1	kpp.COL[3]	O	Keyboard column 3
29	UART_A DSR	GPIO1_IO07	kpp.COL[4]	O	Keyboard column 4
116	ADDRESS11	EPDC_SDLE			
59	PWM<A>, Camera Input Data<7>	GPIO1_IO08	kpp.COL[5]	O	Keyboard column 5
118	ADDRESS12	EPDC_SDOE	kpp.COL[6]	O	Keyboard column 6
30	PWM<C>	GPIO1_IO10			
127		EPDC_SDCE2			
32	UART_B CTS	SAI2_RXD	kpp.COL[7]	O	Keyboard column 7
132	DQM3	EPDC_GDCLK			
123	ADDRESS6	EPDC_D6	kpp.ROW[0]	I	Keyboard row 0
119	ADDRESS4	EPDC_D4	kpp.ROW[1]	I	Keyboard row 1
63	PS2 SCL1	ENET1_RD2	kpp.ROW[2]	I	Keyboard row 2
115	ADDRESS2	EPDC_D2			
111	ADDRESS0	EPDC_D0	kpp.ROW[3]	I	Keyboard row 3
37	UART_A RI, Keypad_In<4>	GPIO1_IO06	kpp.ROW[4]	I	Keyboard row 4
114	ADDRESS10	EPDC_SDCLK			
28	PWM<B>	GPIO1_IO09	kpp.ROW[5]	I	Keyboard row 5
120	ADDRESS13	EPDC_SDSHR			
67	PWM<D>, Camera Input Data<6>	GPIO1_IO11	kpp.ROW[6]	I	Keyboard row 6
130	DQM2	EPDC_SDCE3			
34	UART_B RTS	SAI2_TXD	kpp.ROW[7]	I	Keyboard row 7
134	ADDRESS25	EPDC_GDOE			

## 5.24 Controller Area Network (CAN)

The NXP i.MX 7 SoC Flexible Controller Area Network (FlexCAN) peripheral implements the CAN protocol according to the CAN 2.0B specifications. It features a buffer for up to 64 messages and supports both standard and extended message frames. The CAN interface is not part of the standard Colibri interfaces and therefore, it is incompatible with the complete Colibri module family. However, the CAN interface that is located at pin 63/55 is compatible with the Colibri iMX6 as well as Colibri VFxx modules. Therefore, whenever only one CAN interface is required, it is recommended to use the one available at pin 63/55.

Additionally, the CAN interface on pin 178/188 is compatible with the Colibri iMX6 but not with the VFxx. On the other hand, the CAN interface on pin 194/196 is compatible with the VFxx modules but not with the iMX6. For more information, check the Toradex Pinout Designer Tool.

### Features

- Bit rate up to 1Mb/s
- Content-related addressing

- Flexible mailboxes of eight bytes data length (configurable as RX or TX)
- Powerful Rx FIFO ID filtering
- Listen-only mode
- Loop-back mode
- Time stamp based on 16bit free running timer
- Low power modes, wake up on bus activity
- Maskable interrupts

Table 5-46 CAN Signal Pins

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
63	PS2 SCL1	ENET1_RD2	can1.RX	I	CAN receive pin, compatible with Colibri iMX6 and VFxx
90	SPI RXD	I2C1_SCL			Alternate CAN receive pin
169	DATA10	SAI1_RXD			
55	PS2 SDA1	ENET1_RD3	can1.TX	O	CAN transmit pin, compatible with Colibri iMX6 and VFxx
92	SPI TXD	I2C1_SDA			Alternate CAN transmit pin
188	ADDRESS16	GPIO1_IO14	can2.RX	I	CAN receive pin, compatible with Colibri iMX6
196	I2C SCL	ENET1_TD2			CAN receive pin, compatible with Colibri VFxx
81	Camera Input VSYNC	I2C3_SCL			Alternate CAN receive pin
178	DATA30	GPIO1_IO15	can2.TX	O	CAN transmit pin, compatible with Colibri iMX6
194	I2C SDA	ENET1_TD3			CAN transmit pin, compatible with Colibri VFxx
94	Camera Input HSYNC	I2C3_SDA			Alternate CAN transmit pin

## 5.25 Quad Serial Peripheral Interface (QuadSPI)

The Quad Serial Peripheral Interface is an SPI interface with four bidirectional data lines instead of one transmit and one receive data line. The interface is mainly used for connecting to flash devices. The QuadSPI is incompatible with the Colibri family. The pins are located on the SODIMM connector as secondary functions.

### Features

- Various flash vendor devices supported
- Double Data Rate (DDR) and Single Data Rate (SDR) supported
- Two identical serial flash devices can be connected and accessed in parallel for data read operations with doubled readout bandwidth
- DMA support
- Memory mapped read access to connected flash devices
- Execute in place (XiP) possible

Table 5-47 QuadSPI Signals (incompatible with other modules)

X1 Pin#	Colibri STD Function	iMX7 Ball Name	iMX7 Port Name	I/O	Description
123	ADDRESS6	EPDC_D6	qspi.A_SS0_B	O	Chip Select 0
125	ADDRESS7	EPDC_D7	qspi.A_SS1_B	O	Chip Select 1, used to select second instance of QuadSPI device (dual die flash require CS0 and CS1)
121	ADDRESS5	EPDC_D5	qspi.A_SCLK	O	Serial Clock
111	ADDRESS0	EPDC_D0	qspi.A_DATA[0]	I/O	Serial I/O for command, address, and data
113	ADDRESS1	EPDC_D1	qspi.A_DATA[1]	I/O	Serial I/O for command, address, and data
115	ADDRESS2	EPDC_D2	qspi.A_DATA[2]	I/O	Serial I/O for command, address, and data
117	ADDRESS3	EPDC_D3	qspi.A_DATA[3]	I/O	Serial I/O for command, address, and data
119	ADDRESS4	EPDC_D4	qspi.A_DQS	I	Data Strobe signal, required on some high speed DDR devices
126	DQM0	EPDC_D14	qspi.B_SS0_B	O	Chip Select 0
107	nCS1	EPDC_D15	qspi.B_SS1_B	O	Chip Select 1, used to select second instance of QuadSPI device (dual die flash require CS0 and CS1)
95	RDY	EPDC_D13	qspi.B_SCLK	O	Serial Clock
91	nOE, Recovery Mode	EPDC_D8	qspi.B_DATA[0]	I/O	Serial I/O for command, address, and data
89	nWE	EPDC_D9	qspi.B_DATA[1]	I/O	Serial I/O for command, address, and data
105	nCS0	EPDC_D10	qspi.B_DATA[2]	I/O	Serial I/O for command, address, and data
152	DATA17	EPDC_D11	qspi.B_DATA[3]	I/O	Serial I/O for command, address, and data
150	DATA16	EPDC_D12	qspi.B_DQS	I	Data Strobe signal, required on some high-speed DDR devices

## 5.26 JTAG

The JTAG interface is not normally required for software development with the Colibri iMX7. There is always the possibility of reprogramming the module using the Recovery Mode over USB. To flash the module in recovery mode and for debug reasons, it is strongly recommended that the USBC (USB\_OTG1) interface is accessible even if not needed in the production system. Additionally, UART1 should also be accessible.

The JTAG interface is located on test points on the underside of the module. The location is the same for all modules in the Colibri family. On the Evaluation Board 3.1 the signals are accessible through pogo pins. The interface voltage is 3.3V. Hence jumper JP 29 must be in position 2-3.



## 6. Power Management

The Colibri iMX7 has been designed for low power consumption. In order to achieve a minimum consumption, the module features different run and sleep states. Depending on the operating system, maybe the software support of some of the sleep states that are presented in this section is limited. Please check the latest state of the provided OS images at the developer website.

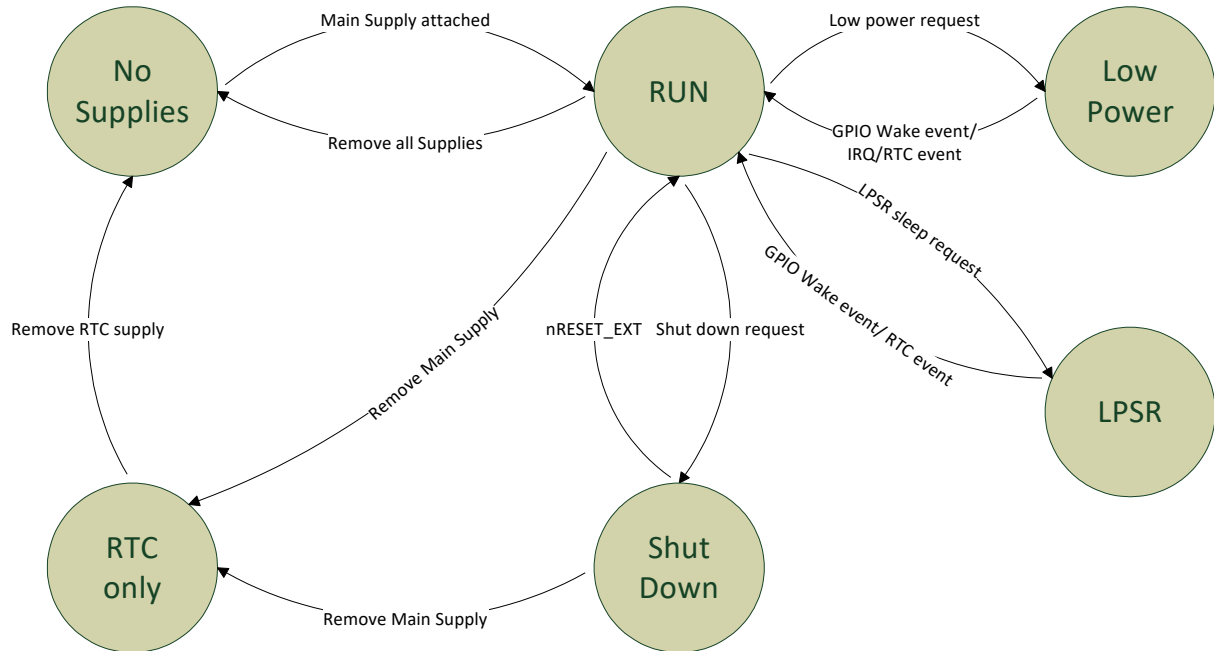


Figure 4: Run and Sleep States

Table 6-1 1.1 Power States

Power Rail	No Supply	RTC Only	Shut Down	RUN	Low Power	LPSR
VCC_BATT (RTC Supply)	OFF	ON	ON	ON	ON	ON
3V3 (Module Main Supply)	OFF	OFF	ON	ON	ON	ON
VDD_ARM (CPU Cores)	OFF	OFF	OFF	ON	ON/OFF	OFF
VDD_SOC	OFF	OFF	OFF	ON	ON	OFF
VDD_DRAM	OFF	OFF	OFF	ON	ON	ON/OFF
On module Peripheral 3.3V	OFF	OFF	OFF	ON	ON	OFF
LPSR IO pins	OFF	OFF	OFF	ON	ON	ON
Ethernet	OFF	OFF	OFF	ON/OFF	ON/OFF	OFF
nRESET_OUT	Undefined	Undefined	LOW	HIGH	HIGH	HIGH

### 6.1 No Supply

All power rails are removed from the module.

### 6.2 RTC Only

All power rails are removed from the module, except the VCC\_BATT is provided to the module. The RTC on the module is kept running for keeping the time. The RTC on the module is not designed

for ultra-low power consumption (typical current consumption can be found in section 9.2). Therefore, a standard lithium coin cell battery can drain faster than required for certain designs. If a rechargeable RTC battery is not the solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, do not provide the VCC\_BATT voltage rail at pin 40 during the RTC state. Nevertheless, the VCC\_BATT voltage is required in RUN, Low Power, and LPSR states, but can be sourced from the same rail as the 3V3 main supply of the module. A suitable reference schematic can be found in the schematic diagram of the Colibri evaluation board.

### 6.3 Shut Down

The module has been shut down. Only the software is able to put the module in shut down state. All 'On' module rails are switched 'Off', but the carrier board still provides the 3V3 main supply as well as the VCC\_BATT. The 'On' module RTC is kept running in order to keep the time. The system can be reactivated from the Shut Down state by pressing the reset button (this option is not available on all Colibri modules) or by removing and reapplying the 3V3 main supply voltage rail.

### 6.4 RUN

The system is up and running. The CPU(s) are active and the peripheral modules are enabled. In this mode, the VDD\_ARM voltage might be adjusted according to the CPU frequency in order to save energy. If the Ethernet port is not required, the PMIC is able to switch off the supply rails of the PHY in order to reduce the consumption.

### 6.5 Low Power

When the CPU is not running, the processor can enter the low power mode (sleep mode). The Colibri iMX7 supports different level of low power modes:

- System Idle: The CPU can enter this mode automatically if there is no thread running anymore. All peripherals can be kept working. The CPU state is retained, so the interrupt response can be very short.
- Low Power Idle: Some of the peripherals are kept still alive while others are shut off. The interrupt response in this state is longer than in the System Idle, but the power consumption is much lower.
- Suspend: All clocks, unused peripherals and PHYs are off. The DDR3L RAM stays in Self-Refresh mode. The exit time from this mode is much longer. The SoC can request the PMIC to switch off the VDD\_ARM rail if L2 Cache does not need to be retained. All other rails are still available.

### 6.6 LPSR

The LPSR is considered as an extension of the RTC Only state. In this state, all CPUs, peripherals, and IO rails are switched off except for the special LPSR IO pins. The DDR3L RAM can be kept in Self-Refresh mode or switched off. A number of LPSR pins will keep their state in the LPSR mode and can be configured for waking up the system. The list of these pins can be found in section 5.2.1.

In order to prevent backfeeding, the carrier board is not allowed to provide any voltage on all other SODIMM pins (USB OTG data pins can be left connected to a host device). Use one of the LPSR capable GPIO pins for switching off peripherals on the carrier board that would backfeed to the regular GPIO pins.

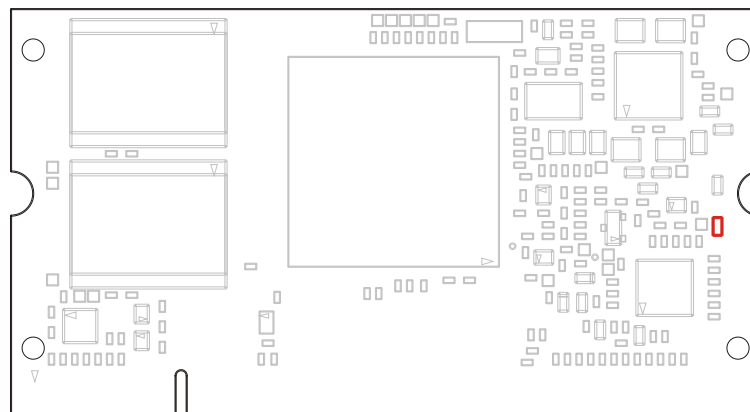
The supported wake up sources from the LPSR mode is RTC alarm as well as any configured wake event of the LPSR capable GPIO pins.

## 7. Recovery Mode

The recovery mode (USB serial loader) can be used to download new software to the Colibri iMX7 even if the bootloader is no longer capable of booting the module. In the normal development process, this mode is not needed. When the module is in the recovery mode, the USBC (USB\_OTG1) interface is used to connect it to a host computer. You will find additional information at our Developer Center: <http://developer.toradex.com>.

To enter the recovery mode, either connect the recovery mode pads on the front of the module together (see picture below) or pull SODIMM pin 91 to GND with a 10 KOhm resistor while power up the module. If the Colibri Evaluation Board V3.x is used, the SW9 button can be pressed during switching on the power supply for the module.

**Important:** make sure that there is no bootable SD card plugged into the slot. Otherwise, the module will try to boot from the external SD card instead of the USB serial loader.



**Figure 5: Location of recovery mode pads**

## 8. Known Issues

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Up-to-date information about all known hardware issues. can be found in the errata document which can be downloaded on our website at:

<http://developer.toradex.com/products/colibri-imx7#errata>

## 9. Technical Specifications

### 9.1 Absolute Maximum Ratings

Table 9-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
$V_{\max\_3V3}$	Main power supply	-0.3	3.6	V
$V_{\max\_AVDD}$	Analogue power supply	-0.3	3.6	V
$V_{\max\_VCC\_BATT}$	RTC power supply	-0.3	3.6	V
$V_{\max\_IO}$	IO pins with GPIO function	-0.5	3.6	V
$V_{\max\_AN1}$	ADC and touch analogue input	-0.3	2.1	V

### 9.2 Electrical Characteristics

Table 9-2 Recommended Operation Conditions

Symbol	Description	Min	Typical	Max	Unit
3V3	Main power supply	3.135	3.3	3.465	V
AVDD	Analogue power supply	3.0	3.3	3.6	V
VCC_BATT	RTC power supply	2.4	3.3	3.6	V

Table 9-3 GPIO Parameters

Symbol	Description	Min	Typical	Max	Unit
$V_{OH}$	High-Level output voltage (@10.8mA)	0.8 x 3V3	3.3	3V3	V
$V_{OL}$	Low-Level output voltage (@10.8mA)	0	0	0.2 x 3V3	V
$V_{IH}$	High-Level input voltage	0.7 x 3V3	3.3	3V3 + 0.3	V
$V_{IL}$	Low-Level input voltage	-0.3	0	0.3x 3V3	V
$V_{HYS}$	Input hysteresis	0.15			V
5kΩ PU	Pull-up resistor (configurable in SoC)	4.8		5.3	kΩ
47kΩ PU	Pull-up resistor (configurable in SoC)	45.8		49.8	kΩ
100kΩ PU	Pull-up resistor (configurable in SoC)	101		105	kΩ
100kΩ PD	Pull-down resistor (configurable in SoC)	101		108	kΩ
$I_{OZ}$	Input current without pull resistor enabled	-5		5	μA
$I_{\max\_GPIO}$	Sink/source current in push-pull mode	-32.9		32.9	mA

Table 9-4 Typical Power Consumption Colibri iMX7D 1GB

Symbol	Description (VCC = 3.3V)	Typical	Unit
IDD_HIGHCPU	Maximal CPU Load	255	mA
IDD_IDL	CPU Idle	175	mA
IDD_LP_IDL	CPU in Low Power Idle	164	mA
IDD_SUSPEND	Module in Suspend State	22	mA
IDD_LPSR	Module in LPSR State	TBD	mA
IDD_BATT	Current consumption of internal RTC	4	μA

Table 9-4 Typical Power Consumption Colibri iMX7D 512MB

Symbol	Description (VCC = 3.3V)	Typical	Unit
IDD_HIGHCPU	Maximal CPU Load	235	mA
IDD_IDL	CPU Idle	169	mA
IDD_LP_IDL	CPU in Low Power Idle	162	mA
IDD_SUSPEND	Module in Suspend State	18	mA
IDD_LPSR	Module in LPSR State	TBD	mA
IDD_BATT	Current consumption of internal RTC	4	µA

Table 9-5 Typical Power Consumption Colibri iMX7S

Symbol	Description (VCC = 3.3V)	Typical	Unit
IDD_HIGHCPU	Maximal CPU Load	209	mA
IDD_IDL	CPU Idle	169	mA
IDD_LP_IDL	CPU in Low Power Idle	158	mA
IDD_SUSPEND	Module in Suspend State	16	mA
IDD_LPSR	Module in LPSR State	TBD	mA
IDD_BATT	Current consumption of internal RTC	4	µA

### 9.3 Mechanical Characteristics

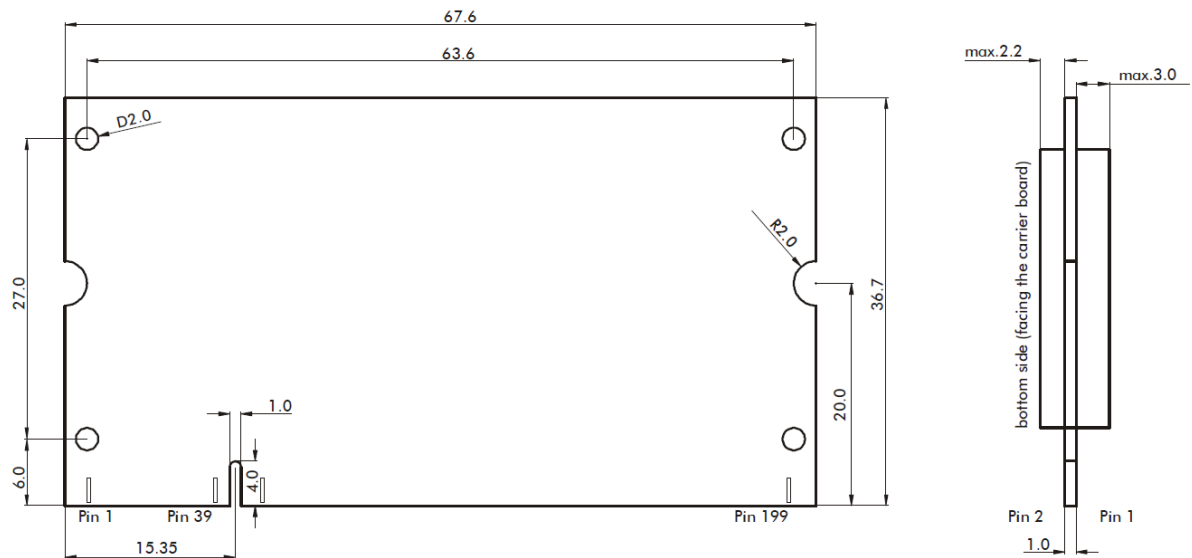


Figure 6 Mechanical dimensions of the Colibri module (top view)  
Tolerance for all measures: +/- 0.1mm

#### 9.3.1 Sockets for the Colibri Modules

The Colibri modules fit into a regular 2.5V (DDR1) SODIMM200 memory socket. A selection of SODIMM200 socket manufacturers is detailed below:

- AUK Connectors: <http://www.aukconnector.com/>
- CONCRAFT: [http://www.concraft.com.tw/connector\\_products\\_ddr.html](http://www.concraft.com.tw/connector_products_ddr.html)
- Morethanall Co Ltd.: <http://www.morethanall.com/>
- Tyco Electronics (AMP): <http://www.te.com/usa-en/home.html>
- NEXUS COMPONENTS GmbH: <https://www.nexus-de.com/en>

## 9.4 Thermal Specification

The Colibri iMX7 incorporates DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling which enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. This allows the Colibri iMX7 to deliver higher performance at lower average power consumption compared to other solutions. The NXP i.MX 7 SoC has an integrated temperature sensor for monitoring the temperature of the CPU.

Here some general considerations:

- If you only use the peak performance for a short time period, heat dissipation is less of a problem because the advanced power management reduces power consumption when full performance is not required.
- A lower die temperature will also lower the power consumption due to smaller leakage currents.

Since the overall power consumption of the Colibri iMX7 is dramatically lower than for example the Colibri iMX6, for most of the application there is no need for a cooling solution.

Table 9-5 1.1 Thermal Specification

Module	Description	Min	Typ	Max	Unit
Colibri iMX7x	Operating temperature range	-20		85 <sup>1</sup>	°C
Colibri iMX7S 256MB Colibri iMX7D 512MB	Storage Temperature	-40		100	°C
Colibri iMX7D 1GB	Storage Temperature (eMMC is limiting to 85°C)	-40		85	°C
Colibri iMX7x	Junction temperature SoC	-20		105	°C
Colibri iMX7x	Thermal Resistance Junction-to-Ambient, i.MX 7 only. (Theta-JA) <sup>2</sup>		30.2		°C/W
Colibri iMX7x	Thermal Resistance Junction-to-Top of i.MX 7 chip case. (Psi-JCtop) <sup>2</sup>		0.2		°C/W

<sup>1</sup> Depending on cooling solution.

<sup>2</sup> A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-6, board mounted horizontal, natural convection.

## 9.5 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH etc. can be found on our website at: <http://www.toradex.com/support/product-compliance>

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