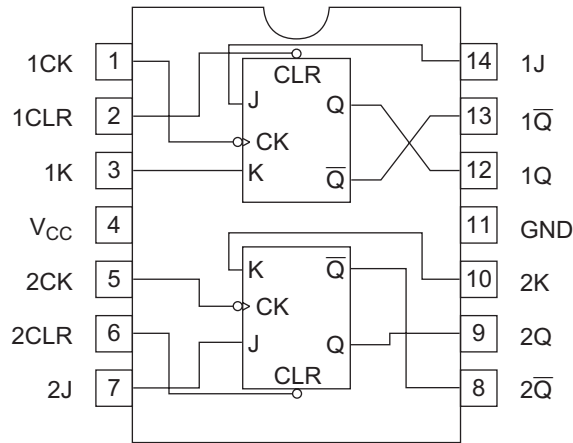


**Pin Arrangement**



(Top view)

**Function Table**

Inputs				Outputs	
Clear	Clock	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

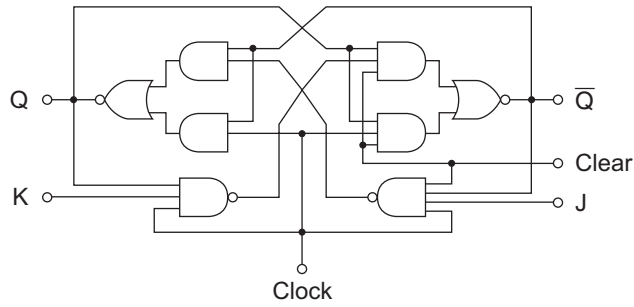
H; high level, L; low level, X; irrelevant, ↓; transition from high to low level,

Q<sub>0</sub>; level of Q before the indicated steady-state input conditions were established.

$\bar{Q}_0$ ; complement of  $\bar{Q}_0$  or level of Q before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

**Block Diagram (1/2)**



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	$V_{IN}$	7	V
Power dissipation	$P_T$	400	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

**Recommended Operating Conditions**

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output current	$I_{OH}$	—	—	-400	μA
	$I_{OL}$	—	—	8	mA
Operating temperature	$T_{opr}$	-20	25	75	°C
Clock frequency	$f_{clock}$	0	—	30	MHz
Pulse width	$t_w$ (Clock High)	20	—	—	ns
	$t_w$ (Clear Low)	25	—	—	
Setup time	$t_{su}$ ("H" Data)	20↓	—	—	ns
	$t_{su}$ ("L" Data)	20↓	—	—	
Hold time	$t_h$	0↓	—	—	ns

Note: ↓; The arrow indicates the falling edge.

**Electrical Characteristics**

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V <sub>IH</sub>	2.0	—	—	V	
	V <sub>IL</sub>	—	—	0.8	V	
Output voltage	V <sub>OH</sub>	2.7	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA
	V <sub>OL</sub>	—	—	0.5	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V
—		—	0.4			
Input current	J, K	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V
	Clear	—	—	60		
	Clock	—	—	80		
	J, K	—	—	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V
	Clear	—	—	-0.8		
	Clock	—	—	-0.8		
	J, K	—	—	0.1	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V
	Clear	—	—	0.3		
	Clock	—	—	0.4		
Short-circuit output current	I <sub>OS</sub>	-20	—	-100	mA	V <sub>CC</sub> = 5.25 V
Supply current**	I <sub>CC</sub>	—	4	6	mA	V <sub>CC</sub> = 5.25 V
Input clamp voltage	V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA

Notes: \* V<sub>CC</sub> = 5 V, Ta = 25°C

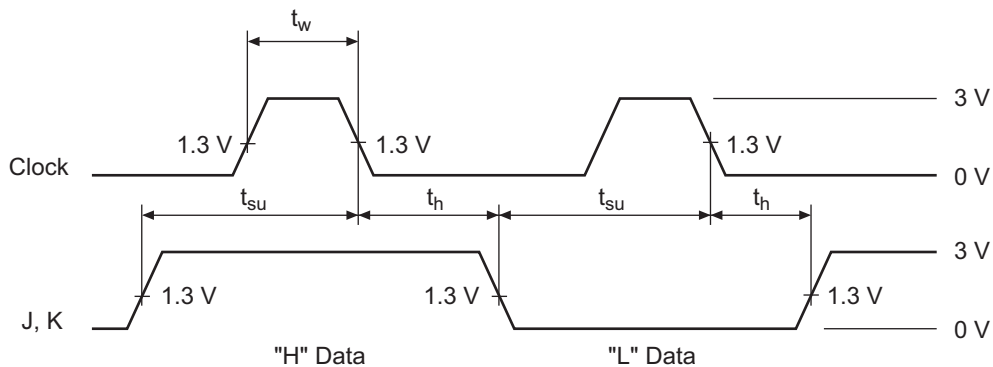
\*\* With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At time of measurement, the clock input is founded.

**Switching Characteristics**

(V<sub>CC</sub> = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f <sub>max</sub>			30	45	—	MHz	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ
Propagation delay time	t <sub>PLH</sub>	Clear	Q, $\bar{Q}$	—	15	20	ns	
	t <sub>PHL</sub>	Clock		—	15	20	ns	

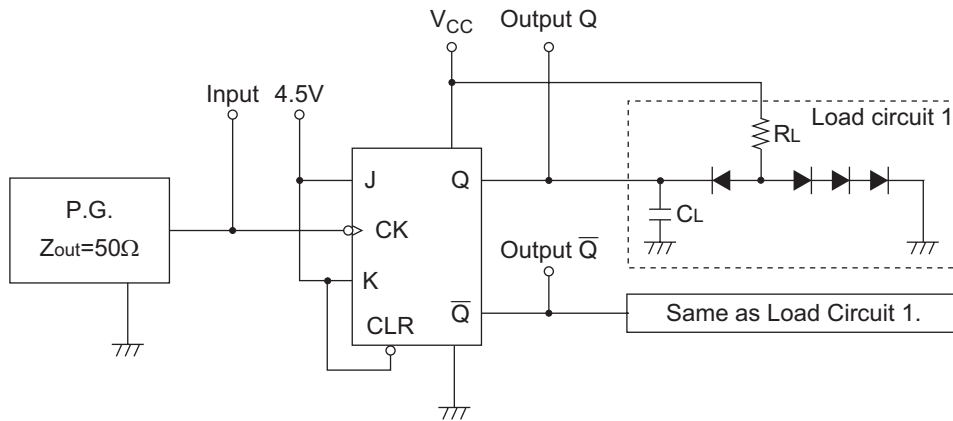
**Timing Definition**



## Testing Method

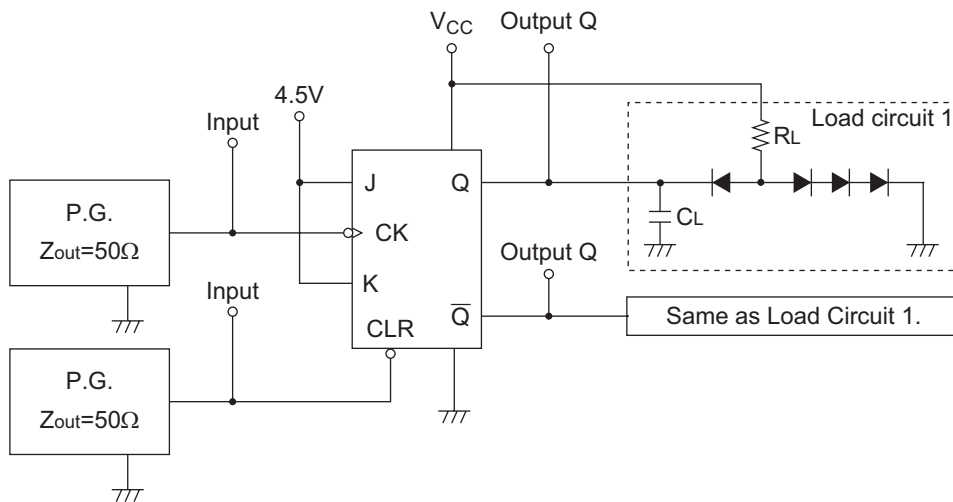
### Test Circuit

1.  $f_{max}$ ,  $t_{PLH}$ ,  $t_{PHL}$ , (Clock $\rightarrow$ Q,  $\bar{Q}$ )



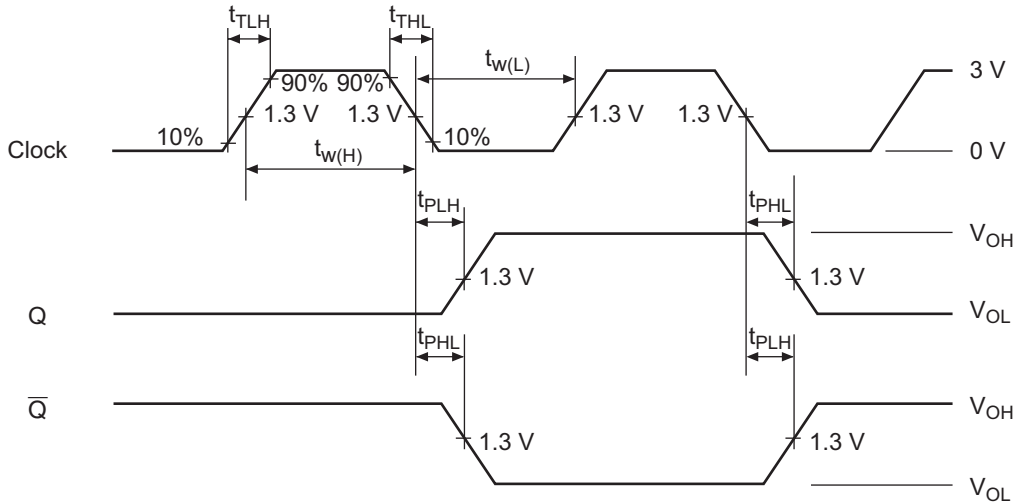
- Notes:
1. Test is put into the each flip-flop.
  2.  $C_L$  includes probe and jig capacitance.
  3. All diodes are 1S2074(H).

2.  $t_{PHL}$  (Clear $\rightarrow$ Q),  $t_{PLH}$  (Clear $\rightarrow$  $\bar{Q}$ )



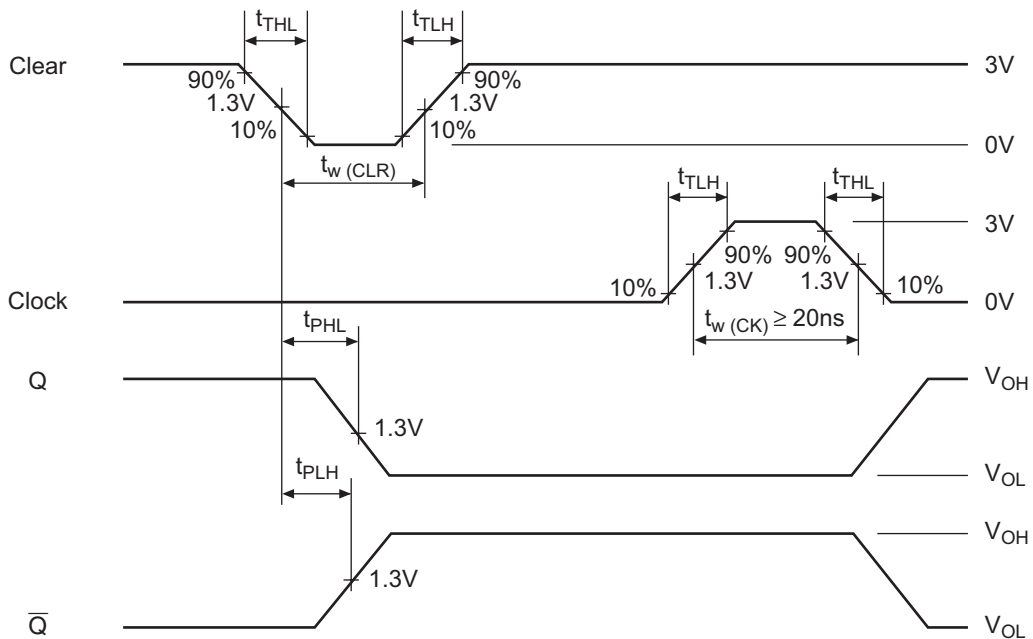
- Notes:
1. Test is put into the each flip-flop.
  2.  $C_L$  includes probe and jig capacitance.
  3. All diodes are 1S2074(H).

Waveforms 1



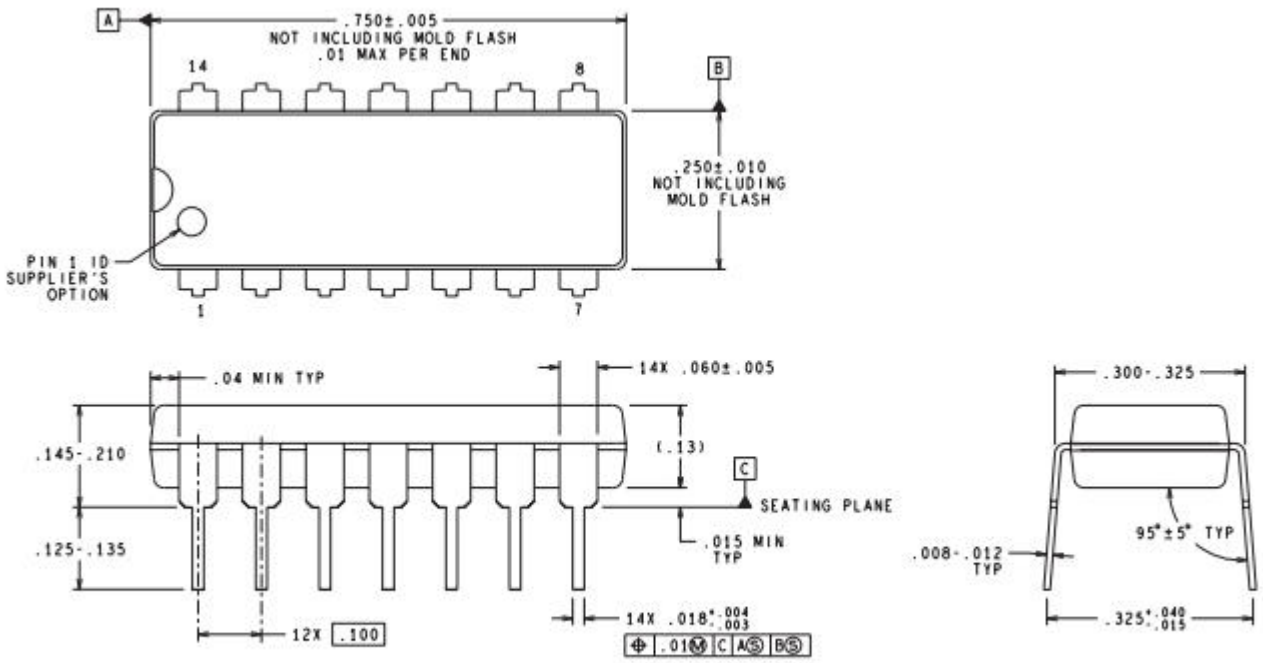
Note: Clock input pulse;  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, PRR = 1 MHz, duty cycle = 50% and for  $f_{max}$ ,  $t_{TLH} = t_{THL} \leq 2.5$  ns

Waveforms 2



Note: Clear and clock input pulse;  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, PRR = 1 MHz,

DIP14



**DIMENSIONS ARE IN INCHES**  
 DIMENSIONS IN ( ) FOR REFERENCE ONLY

以上信息仅供参考. 如需帮助联系客服人员。谢谢 XINLUDA