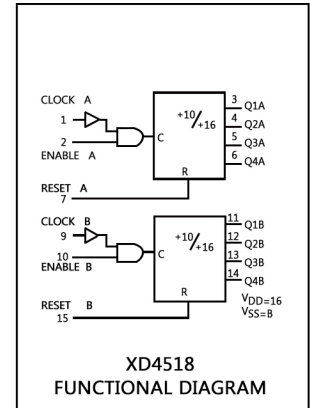


High-Voltage Types(20-Volt Rating) XD4518 Dual BCD UP-Counter

■ XD4518 Dual BCD Up-Counter
nous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines. The counter can be cascaded in the ripple mode by connecting Q4 to the enable input

Features:

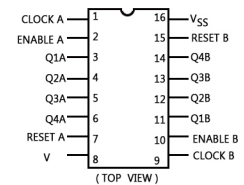
- Medium speed operation-
6-MHz typical clock frequency at 10 V
- Positive- or negative-edge triggering
- Synchronous internal carry propagation
- 100% tested for quiescent current at 20 V
- Maximum input current of 1μA at 18 V
over full package-temperature range:
100 nA at 18V and 25°C
- Noise margin(over full package-temperature range): 1 V at $V_{DD} = 5 V$
2 V at $V_{DD} = 10 V$
2.5 V at $V_{DD} = 15 V$
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'b' Series CMOS Devices"



Applications:

- Multistage synchronous counting
- Multistage ripple counting
- frequency dividers

TRUTH TABLE



**XD4518
TERMINAL ASSIGNMENT**

MAXIMUM RATINGS, Absolute- Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT $\pm 10\mu A$
POWER DISSIPATION PER PACKAGE (P_D):
For $T_A = -55^\circ C$ to $+100^\circ C$ 500mW
For $T_A = +100^\circ C$ to $+125^\circ C$ Derate Linearly at 12mW/ $^\circ C$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) $-55^\circ C$ to $+125^\circ C$
STORAGE TEMPERATURE RANGE (T_{stg}) $-65^\circ C$ to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING):
At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79mm$) from case for 10s max $+265^\circ C$

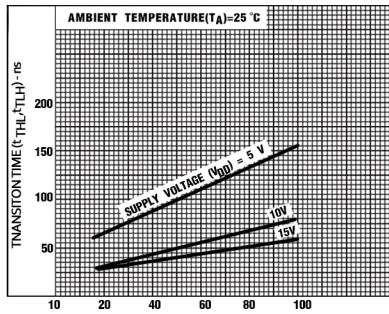
CLOCK	ENABLE	RESET	ACTION
	1	0	Increment Counter
0		0	Increment Counter
	X	0	No Change
X		0	No Change
	0	0	No Change
1		0	No Change
X	X	0	Q1 thru Q4 = 0

X = Don't Care 1 = High State 0 = Low State

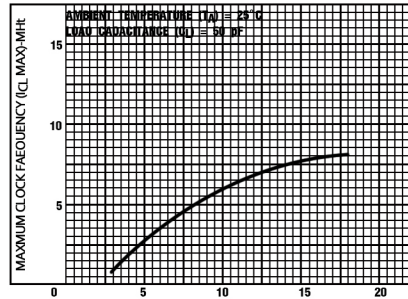
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STATIC ELECTRICAL CHARACTERISTICS

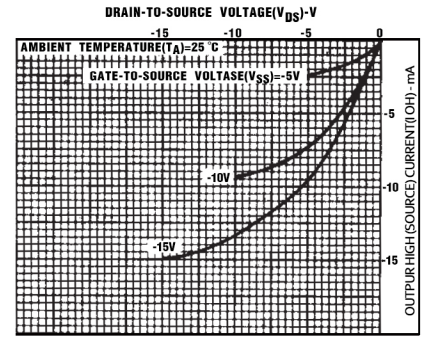
CHRACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES(°C)							UNITS
	VO (V)	VIN (V)	VDD (V)	+25							
				-55	-40	+85	+125	Min	Typ	Max	
Quiescent Device Current IDD Max.	—	0, 5	5	5	5	150	150	—	0. 04	5	μA
	—	0, 10	10	10	10	300	300	—	0. 04	10	
	—	0, 15	15	20	20	600	600	—	0. 04	20	
	—	0, 20	20	100	100	3000	3000	—	0. 08	100	
Output Low (Sink)Current IOL Min.	0. 4	0, 5	5	0. 64	0. 61	0. 42	0. 36	0. 51	1	—	mA
	0. 5	0, 10	10	1. 6	1. 5	1. 1	0. 9	1. 3	2. 6	—	
	1. 5	0, 15	15	4. 2	4	2. 8	2. 4	3. 4	6. 8	—	
Output High (Source) Current, IOH Min.	4. 6	0, 5	5	-0. 64	-0. 61	-0. 42	-0. 36	-0. 51	-1	—	mA
	2. 5	0, 5	5	-2	-1. 8	-1. 3	-1. 15	-1. 6	-3. 2	—	
	9. 5	0, 10	10	-1. 6	-1. 5	-1. 1	-0. 9	-1. 3	-2. 6	—	
	13. 5	0, 15	15	-4. 2	-4	-2. 8	-2. 4	-3. 4	-6. 8	—	
Output Voltage: Low-Level, VOLMax.	—	0, 5	5	0. 05				—	0	0. 05	V
	—	0, 10	10	0. 05				—	0	0. 02	
	—	0, 15	15	0. 05				—	0	0. 02	
Output Voltage: High-Level, VOHMin.	—	0, 5	5	4. 95				4. 95	5	—	V
	—	0, 10	10	9. 95				9. 95	10	—	
	—	0, 15	15	14. 95				14. 95	15	—	
Input Low Voltage, VIL Max.	0. 5, 4. 5	—	5	1. 5				—	—	1. 5	V
	1, 9	—	10	3				—	—	3	
	1. 5, 3. 5	—	15	4				—	—	4	
Input High Voltage, VIH Min.	0. 5, 4. 5	—	5	3. 5				3. 5	—	—	V
	1, 9	—	10	7				7	—	—	
	1. 5, 13. 5	—	15	11				11	—	—	
Input Current IIN Max.	—	0, 18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA



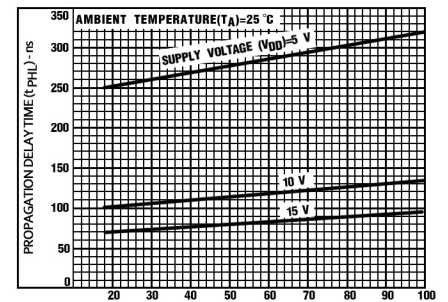
Typical transition time vs. load capacitance.



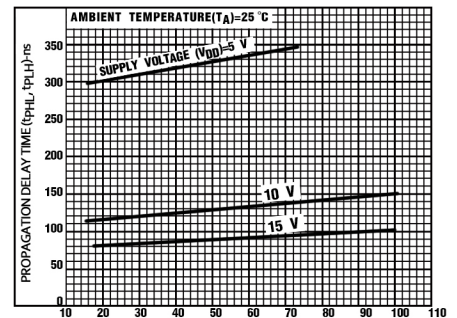
Typical maximum-clock-frequency vs. supply voltage.



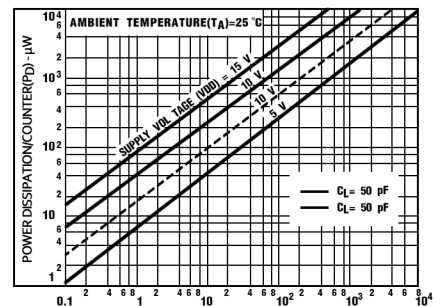
Minimum output high (source) current characteristics.



Typical propagation delay vs. load capacitance, clock or enable to output.



Typical propagation delay time vs. load capacitance, reset to output.



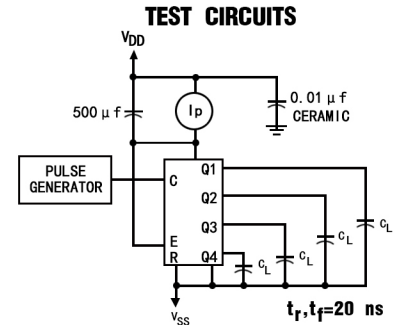
Typical power dissipation characteristics.

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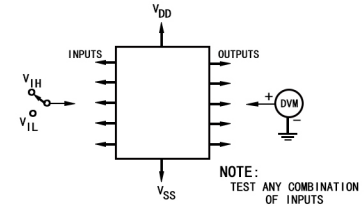
RECOMMENDED OPERATING CONDITIONS at TA = 25 °C, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V _{DD} (V)	LIMITS		UNITS
		Min	Max	
Supply-Voltage Range (For TA = Full Pack age Temperature Range)		3	18	V
Enable pulse Width, 't _W	5	400	–	ns
	10	200	–	
	15	140	–	
Clock Pulse Width, 't _W	5	200	–	ns
	10	100	–	
	15	70	–	
Clock Input Frequency, f _{CL}	5		1.5	MHz
	10	dc	3	
	15		4	
Clock Rise or Fall Time, t _r CL or t _f CL:	5		15	μs
	10	–	5	
	15		5	
Reset Pulse Width, t _W	5	250	–	ns
	10	110	–	
	15	80	–	



Dynamic power dissipation

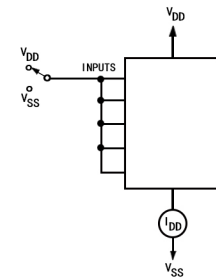


Input voltage.

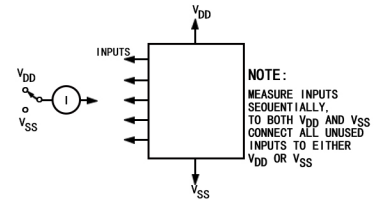
DYNAMIC ELECTRICAL CHARACTERISTICS at TA = 25 °C:

Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		V _{DD} V	Min	Typ	Max	
Propagation Delay Time, t _{PHL} , t _{PLH} : Clock or Enable to Output		5		280	560	ns
		10	–	115	230	
		15		80	160	
Reset to Output		5		330	650	ns
		10	–	130	225	
		15		90	170	
Transition time, t _{THL} t _{TLH}		5		100	200	ns
		10	–	50	100	
		15		40	80	
Maximum Clock Input Frequency, f _{CL}		5	1.5	3		MHz
		10		6	–	
		15		8		
Maximum Clock Pulse Width, t _W		5		100	200	ns
		10		50	100	
		15		35	80	
Clock Rise or Fall Time t _r or t _f :		5			15	μs
		10, 15	–	–	5	
Minimum Reset Pulse Width, t _W		5		125	250	ns
		10	–	55	110	
		15		40	80	
Minimum Enable Pulse Width, t _W		5		200	400	ns
		10	–	100	200	
		15		70	140	
Input Capacitance, C _{IN}	Any Input			5	7.5	pF

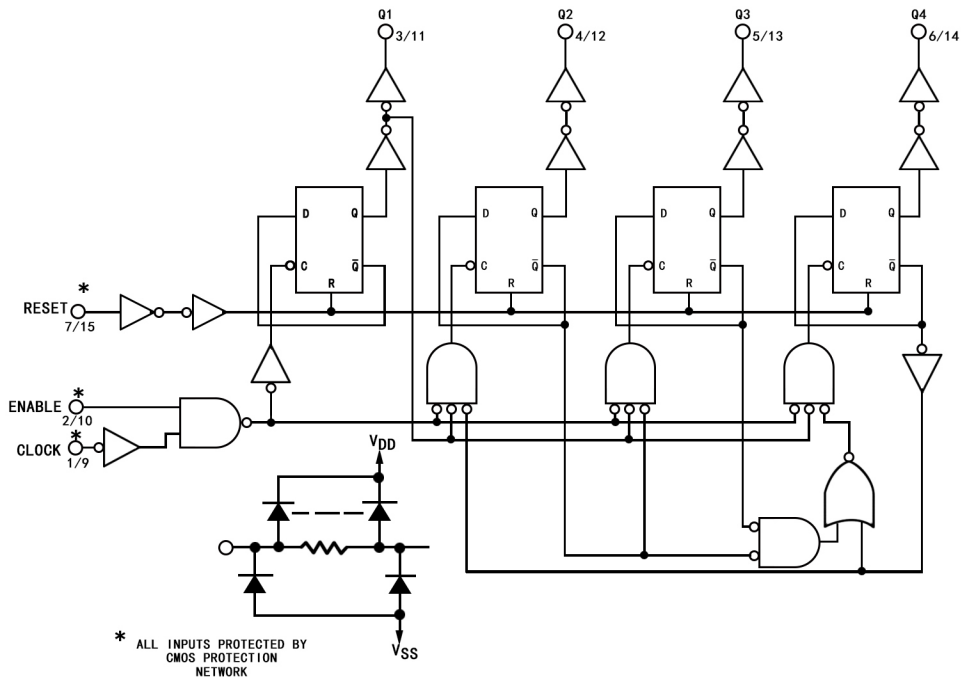


Quiescent device current test circuit.

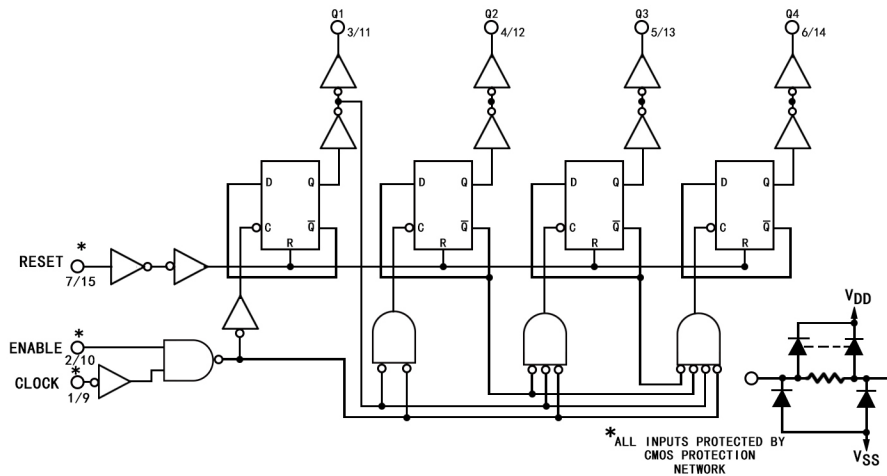


Input leakage-current test circuit

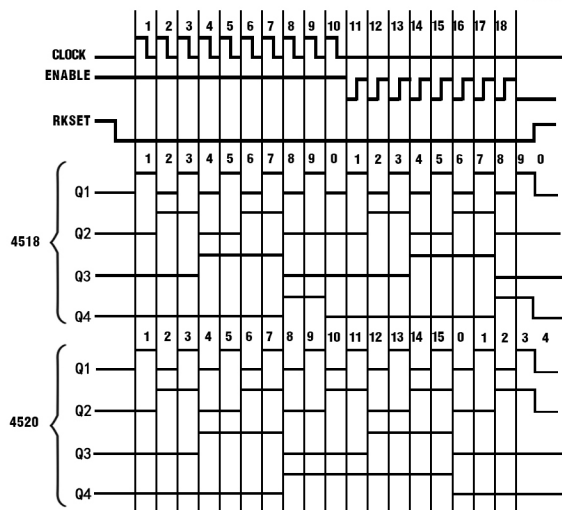
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Decade counter (XD4518) logic diagram for one of two identical counters.

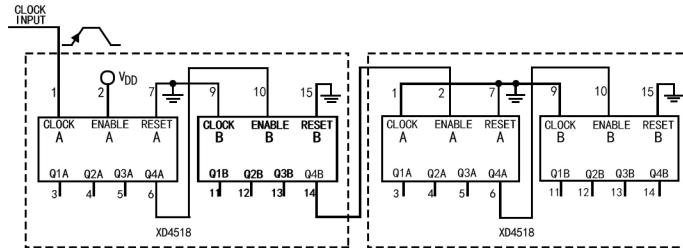


Binary counter (XD4518) logic diagram for one of two identical counters.

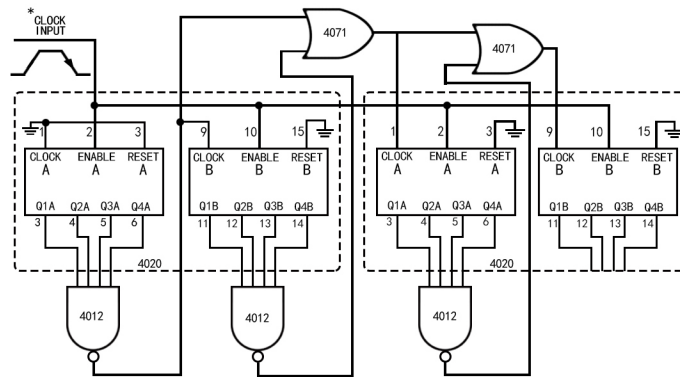


Timing diagrams for XD4518.

XD4518 DIP-16



Ripple cascading of four counters with positive edge teiggering.

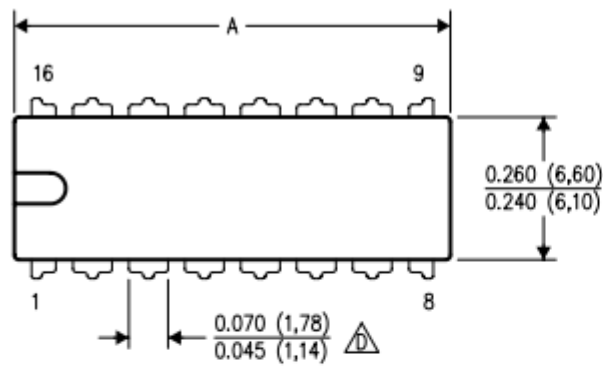


* NOTE:
FOR SYNCHRONOUS CCASCADING THE CLOCK TRANSITION
TIME SHOULD BE MADE LESS THAN OR EQUAL TO THE
SUM OF THE FIXED PROPAGATION DELAY AT 15pF AND
THE TRANSITION TIME OF THE OUTPUT DRIVER STAGE
FOR THE ESTIMATED CAPACITATIVE LOAD.

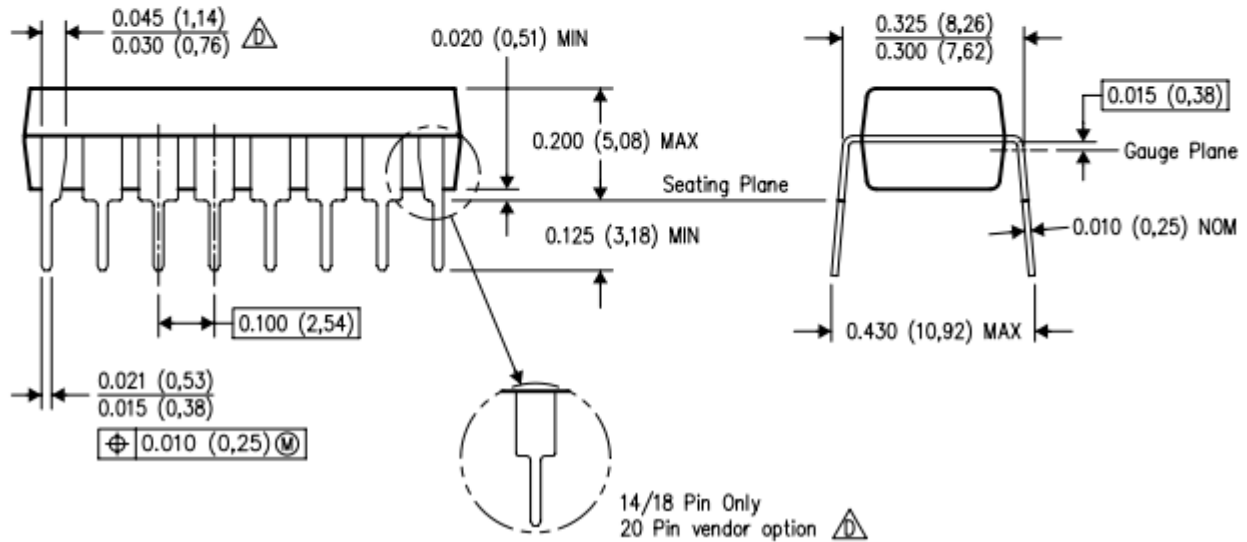
Synchronous cascading of four binary counters with negative edge teiggering.

XD4518 DIP-16

DIP



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



以上信息仅供参考. 如需帮助联系客服人员。谢谢 XINLUDA