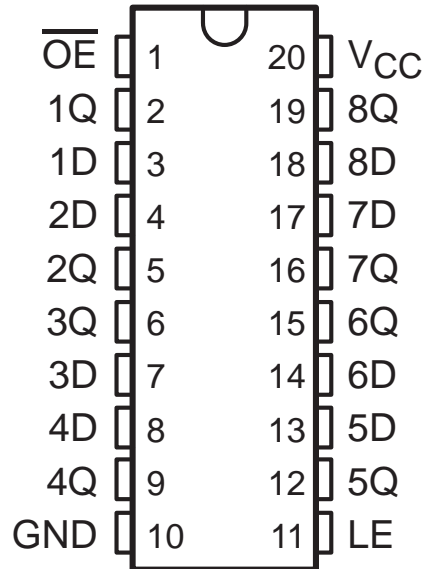


- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State True Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 13$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Eight High-Current Latches in a Single Package
- Full Parallel Access for Loading

**74HC373
 (TOP VIEW)**



description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 74HC373 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

description/ordering information (continued)

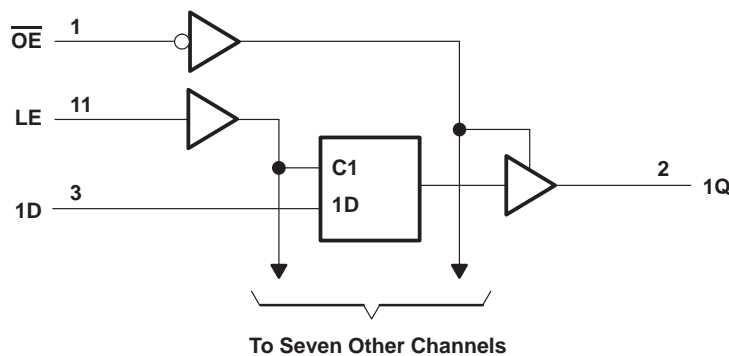
An output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2) 74HC373	69°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		74HC373			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 4.5 V	3.15		
		V _{CC} = 6 V	4.2		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		V
		V _{CC} = 4.5 V	1.35		
		V _{CC} = 6 V	1.8		
V _I	Input voltage	0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		V
Δt/Δv	Input transition rise/fall time	V _{CC} = 2 V	1000		ns
		V _{CC} = 4.5 V	500		
		V _{CC} = 6 V	400		
T _A	Operating free-air temperature	-40	85		°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998	1.9		V	
			4.5 V	4.4	4.499	4.4			
			6 V	5.9	5.999	5.9			
		I _{OH} = -6 mA	4.5 V	3.98	4.3	3.84			
		I _{OH} = -7.8 mA	6 V	5.48	5.8	5.34			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V	0.002		0.1		V	
			4.5 V	0.001		0.1			
			6 V	0.001		0.1			
		I _{OL} = 6 mA	4.5 V	0.17		0.26			
		I _{OL} = 7.8 mA	6 V	0.15		0.26			
I _I	V _I = V _{CC} or 0		6 V	±0.1	±100	±1000		nA	
I _{OZ}	V _O = V _{CC} or 0		6 V	±0.01	±0.5	±5		μA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V	8		80		μA	
C _i			2 V to 6 V	3	10	10		pF	

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25°C		74HC373		UNIT
		MIN	MAX	MIN	MAX	
t _w Pulse duration, LE high	2 V	80	100			ns
	4.5 V	16	20			
	6 V	14	17			
t _{su} Setup time, data before LE↓	2 V	50	63			ns
	4.5 V	10	13			
	6 V	9	11			
t _h Hold time, data after LE↓	2 V	20	24			ns
	4.5 V	10	12			
	6 V	10	12			

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	D	Q	2 V		58	150	190		ns
			4.5 V		15	30	38		
			6 V		13	26	32		
	LE	Any Q	2 V		73	175	220		
			4.5 V		18	35	44		
			6 V		15	30	38		
t _{en}	$\overline{\text{OE}}$	Any Q	2 V		65	150	190		
			4.5 V		17	30	38		
			6 V		14	26	32		
t _{dis}	$\overline{\text{OE}}$	Any Q	2 V		50	150	190		
			4.5 V		15	30	38		
			6 V		13	26	32		
t _t		Any Q	2 V		28	60	75		
			4.5 V		8	12	15		
			6 V		6	10	13		

XD74HC373 DIP-20 XL74HC373 SOP-20

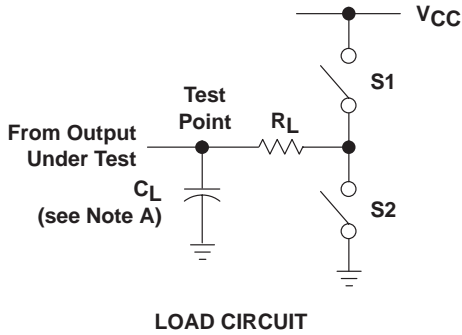
switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		82	200		250	ns
			4.5 V		22	40		50	
			6 V		19	34		43	
	LE	Any Q	2 V		100	225		285	
			4.5 V		24	45		57	
			6 V		20	38		48	
t_{en}	\overline{OE}	Any Q	2 V		90	200		250	ns
			4.5 V		23	40		50	
			6 V		19	34		43	
t_t		Any Q	2 V		45	210		265	ns
			4.5 V		17	42		53	
			6 V		13	36		45	

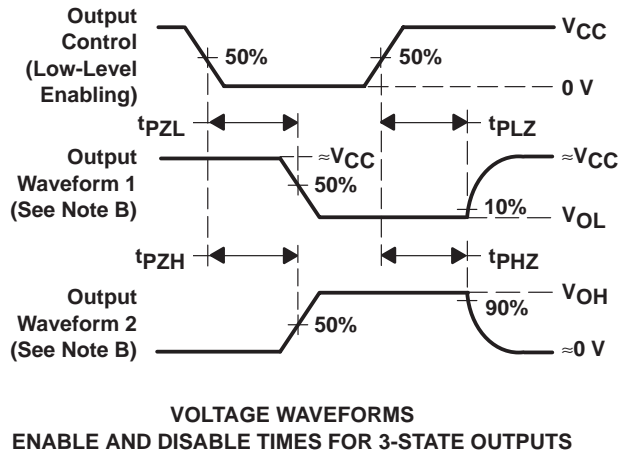
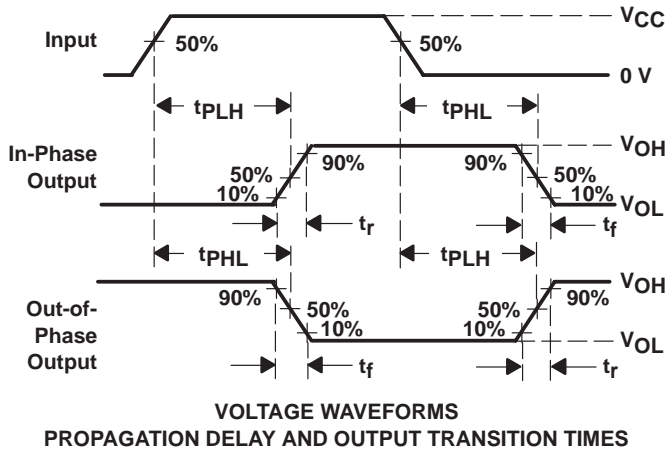
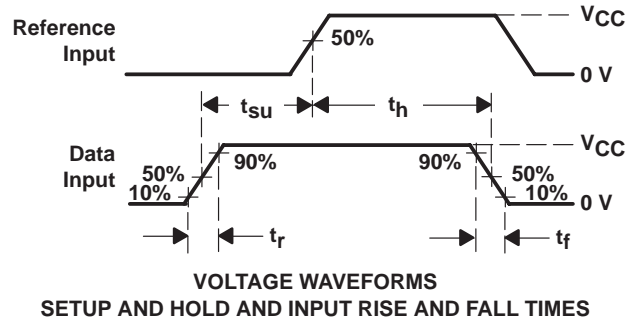
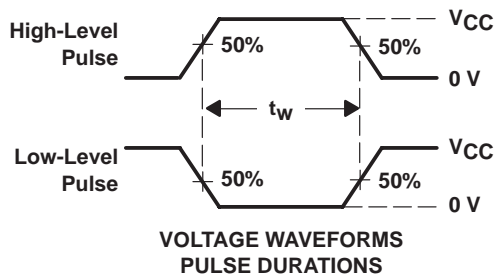
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per latch	No load	100	pF

PARAMETER MEASUREMENT INFORMATION

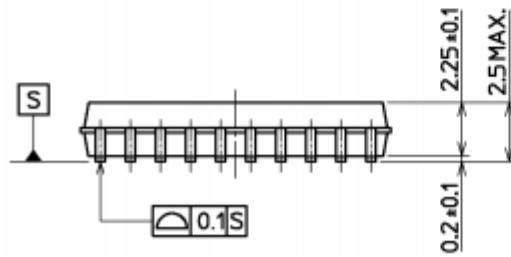
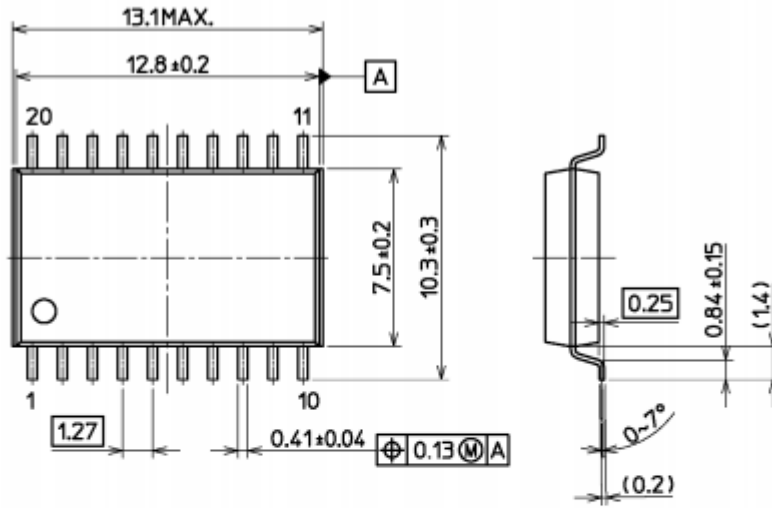


PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	--	50 pF or 150 pF	Open	Open

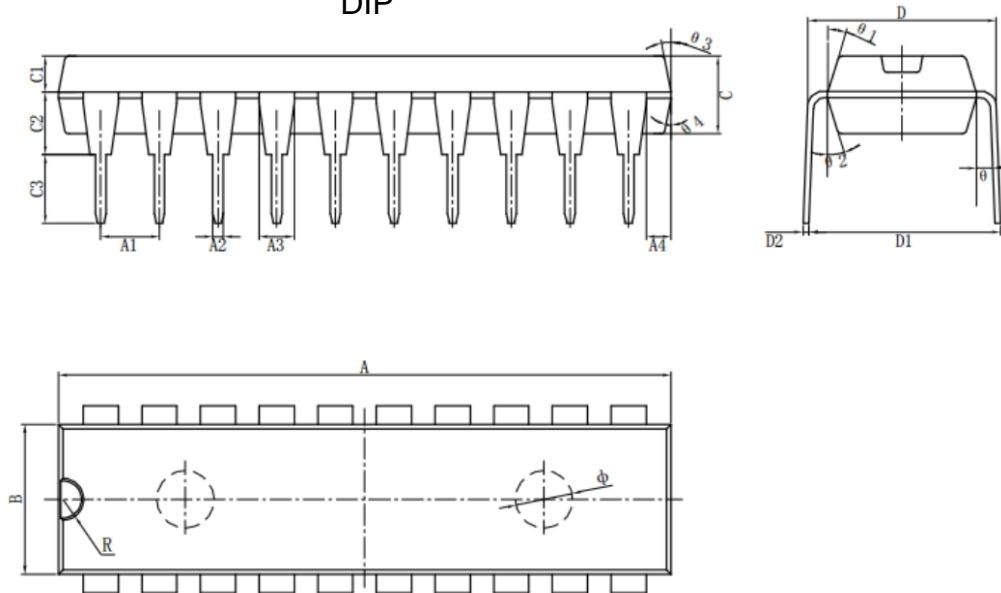


- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



DIP



以上信息仅供参考. 如需帮助联系客服人员. 谢谢 XINLUDA