

**1 Features**

- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays

**2 Applications**

- AV Receivers
- Audio Docks: Portable
- Blu-ray Players and Home Theaters
- MP3 Players or Recorders
- Personal Digital Assistants (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid-State Drives (SSD): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

**3 Description**

These hex buffers and drivers feature high-voltage open-collector outputs to interface with high-level circuits or for driving high-current loads. They are also characterized for use as buffers for driving TTL inputs. The XD74LS07 devices have a rated output voltage of 30 V. The maximum sink current is 40 mA.

These circuits are compatible with most TTL families. Inputs are diode-clamped to minimize transmission-line effects, which simplifies design. Typical power dissipation is 140 mW, and average propagation delay time is 12 ns.

**4 Device Information<sup>(1)</sup>**

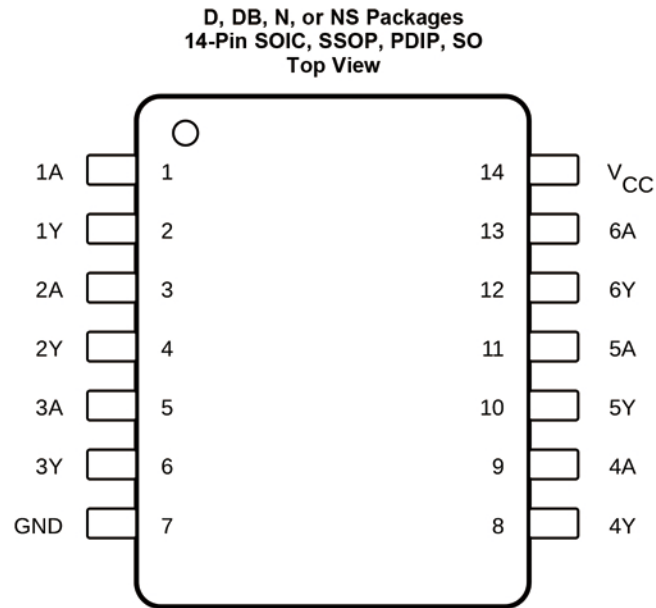
| PART NUMBER | PACKAGE (PINS) | BODY SIZE (NOM)    |
|-------------|----------------|--------------------|
| XL74LS07    | SOIC (14)      | 8.65 mm × 3.90 mm  |
| XD74LS07-SS | SSOP (14)      | 6.20 mm × 5.30 mm  |
| XD74LS07    | PDIP (14)      | 19.30 mm × 6.35 mm |
| XL74LS07-N  | SO (14)        | 10.30 mm × 5.30 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram (Positive Logic)**



## 5 Pin Configuration and Functions



**Pin Functions**

| PIN |                 | I/O | DESCRIPTION |
|-----|-----------------|-----|-------------|
| NO. | NAME            |     |             |
| 1   | 1A              | I   | Input 1     |
| 2   | 1Y              | O   | Output 1    |
| 3   | 2A              | I   | Input 2     |
| 4   | 2Y              | O   | Output 2    |
| 5   | 3A              | I   | Input 3     |
| 6   | 3Y              | O   | Output 3    |
| 7   | GND             | —   | Ground pin  |
| 8   | 4Y              | O   | Output 4    |
| 9   | 4A              | I   | Input 4     |
| 10  | 5Y              | O   | Output 5    |
| 11  | 5A              | I   | Input 5     |
| 12  | 6Y              | O   | Output 6    |
| 13  | 6A              | I   | Input 6     |
| 14  | V <sub>CC</sub> | —   | Power pin   |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                       | MIN | MAX | UNIT |
|-------------------------------------------------------|-----|-----|------|
| V <sub>CC</sub> Supply voltage                        |     | 7   | V    |
| V <sub>I</sub> Input voltage <sup>(2)</sup>           |     | 7   | V    |
| V <sub>O</sub> Output voltage <sup>(2)(3)</sup>       |     | 30  | V    |
| T <sub>J</sub> Operating virtual junction temperature |     | 150 | °C   |
| T <sub>stg</sub> Storage temperature                  | –65 | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) This is the maximum voltage that should be applied to any output when it is in the off state.

### 6.2 ESD Ratings

|                                            | VALUE                                                                          | UNIT  |
|--------------------------------------------|--------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|                                            | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                               | MIN  | NOM | MAX  | UNIT |
|-----------------------------------------------|------|-----|------|------|
| V <sub>CC</sub> Supply voltage                | 4.75 | 5   | 5.25 | V    |
| V <sub>IH</sub> High-level input voltage      | 2    |     |      | V    |
| V <sub>IL</sub> Low-level input voltage       |      |     | 0.8  | V    |
| V <sub>OH</sub> High-level output voltage     |      |     | 30   | V    |
| I <sub>OL</sub> Low-level output current      |      |     | 40   | mA   |
| T <sub>A</sub> Operating free-air temperature | 0    |     | 70   | °C   |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | XD74LS07    |              |             |            | UNIT |
|-------------------------------|----------------------------------------------|-------------|--------------|-------------|------------|------|
|                               |                                              | D<br>(SOIC) | DB<br>(SSOP) | N<br>(PDIP) | NS<br>(SO) |      |
|                               |                                              | 14 PINS     | 14 PINS      | 14 PINS     | 14 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 85.2        | 97.4         | 50.2        | 82.8       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 43.5        | 49.8         | 37.5        | 40.9       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 39.7        | 44.5         | 30          | 41.4       | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 10.9        | 16.5         | 22.3        | 12.4       | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 39.4        | 44           | 29.9        | 41.1       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS <sup>(1)</sup>                |                             | MIN | TYP | MAX  | UNIT          |
|-----------|-----------------------------------------------|-----------------------------|-----|-----|------|---------------|
| $V_{IK}$  | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$   |                             |     |     | -1.5 | V             |
| $I_{OH}$  | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$   | $V_{OH} = 30 \text{ V}$     |     |     | 0.25 | mA            |
| $V_{OL}$  | $V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}$ | $I_{OL} = 16 \text{ mA}$    |     |     | 0.4  | V             |
|           |                                               | $I_{OL} = \text{MAX}^{(2)}$ |     |     | 0.7  |               |
| $I_I$     | $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$      |                             |     |     | 1    | mA            |
| $I_{IH}$  | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$    |                             |     |     | 20   | $\mu\text{A}$ |
| $I_{IL}$  | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$    |                             |     |     | -0.2 | mA            |
| $I_{CCH}$ | $V_{CC} = \text{MAX}$                         |                             |     |     | 14   | mA            |
| $I_{CCL}$ | $V_{CC} = \text{MAX}$                         |                             |     |     | 45   | mA            |

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

(2)  $I_{OL} = 40 \text{ mA}$

## 6.6 Switching Characteristics

$V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$  (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS                         | MIN | TYP | MAX | UNIT |
|-----------|--------------|-------------|-----------------------------------------|-----|-----|-----|------|
| $t_{PLH}$ | A            | Y           | $R_L = 110 \Omega, C_L = 15 \text{ pF}$ |     | 6   | 10  | ns   |
| $t_{PHL}$ |              |             |                                         |     | 19  | 30  |      |

## 6.7 Typical Characteristics

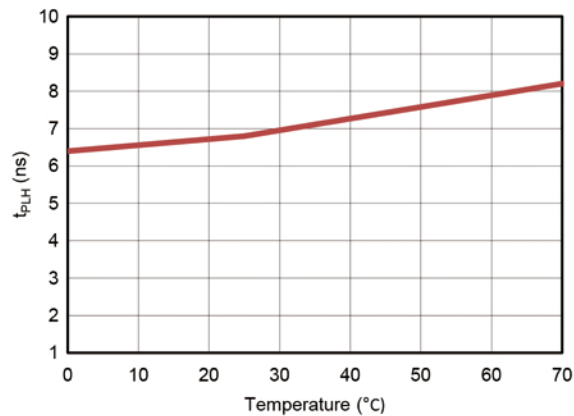
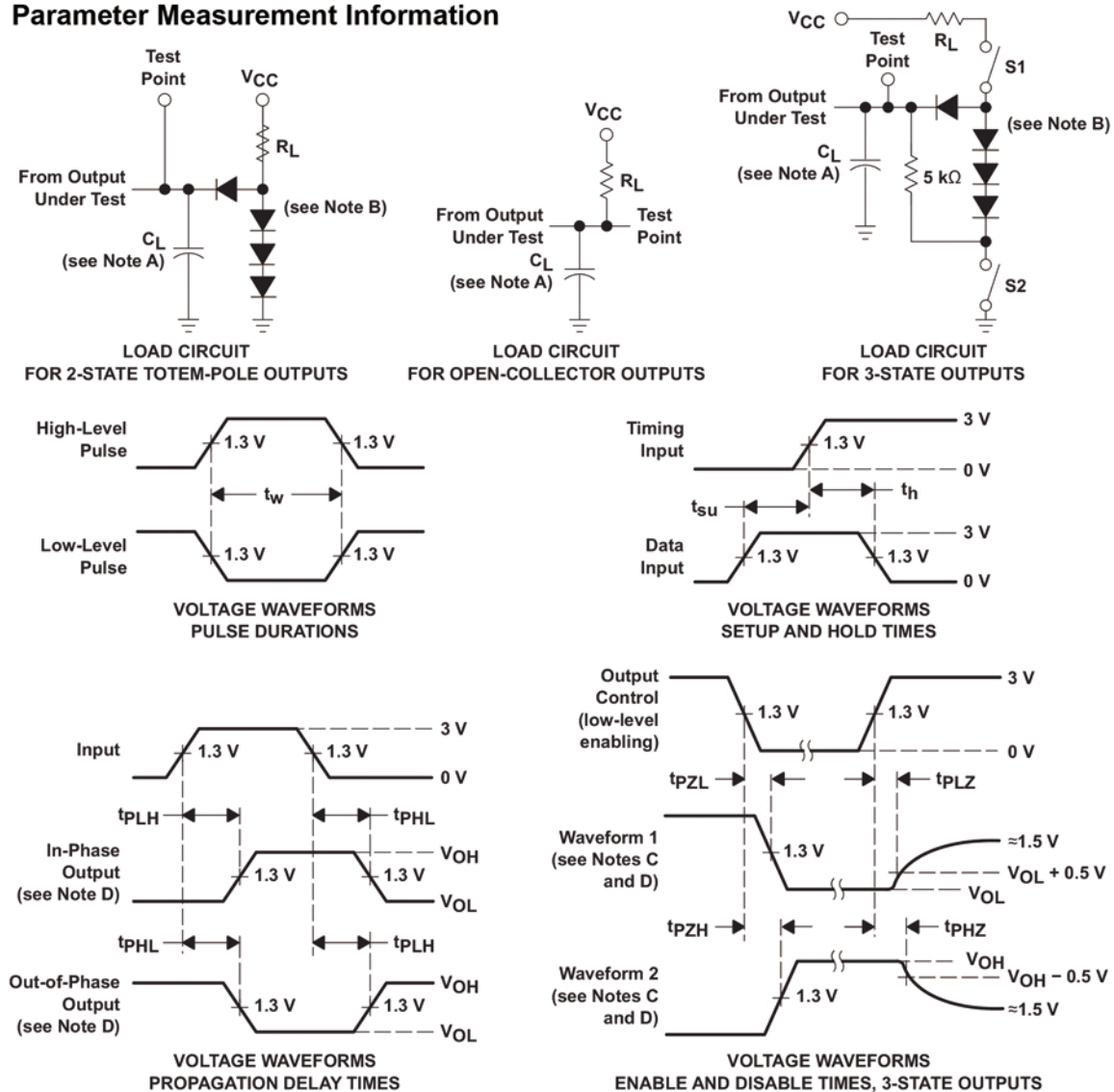


Figure 1.  $t_{PLH}$  vs. Temperature



## 7 Parameter Measurement Information



- $C_L$  includes probe and jig capacitance.
- All diodes are 1N3064 or equivalent.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .
- Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 1.5 \text{ ns}$ ,  $t_f \leq 2.6 \text{ ns}$ .
- The outputs are measured one at a time, with one input transition per measurement.

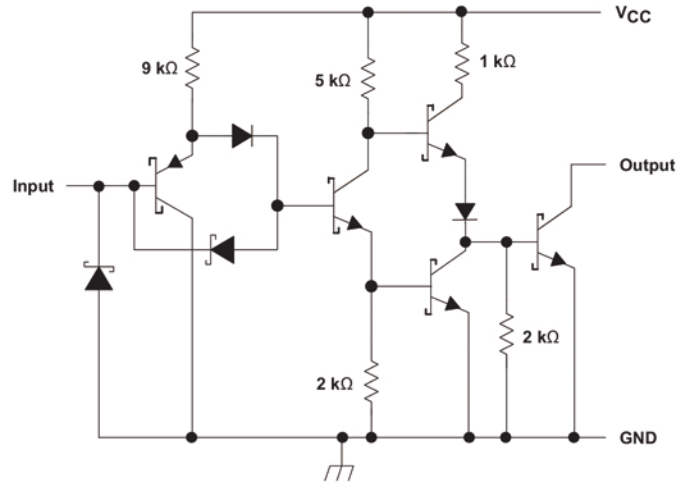
**Figure 2. Load Circuits and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The outputs of the XD74LS07 device are open-collector and can be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current for the XD74LS07 is 40 mA.

Inputs can be driven from 2.5-V, 3.3-V (LVTTL), or 5-V (CMOS) devices. This feature allows the use of this device as translators in a mixed-system environment.



Resistor values shown are nominal.

**Figure 3. Schematic (Gate)**

### 8.2 Functional Block Diagram



### 8.3 Feature Description

- Allows for up translation
  - Inputs accept voltages to 5.25 V
  - Outputs accept voltages to 30 V
- High Sink-Current Capability
  - Up to 40 mA

### 8.4 Device Functional Modes

Table 1 lists the functions of this device.

**Table 1. Function Table**

| INPUT A | OUTPUT Y |
|---------|----------|
| H       | Hi-Z     |
| L       | L        |

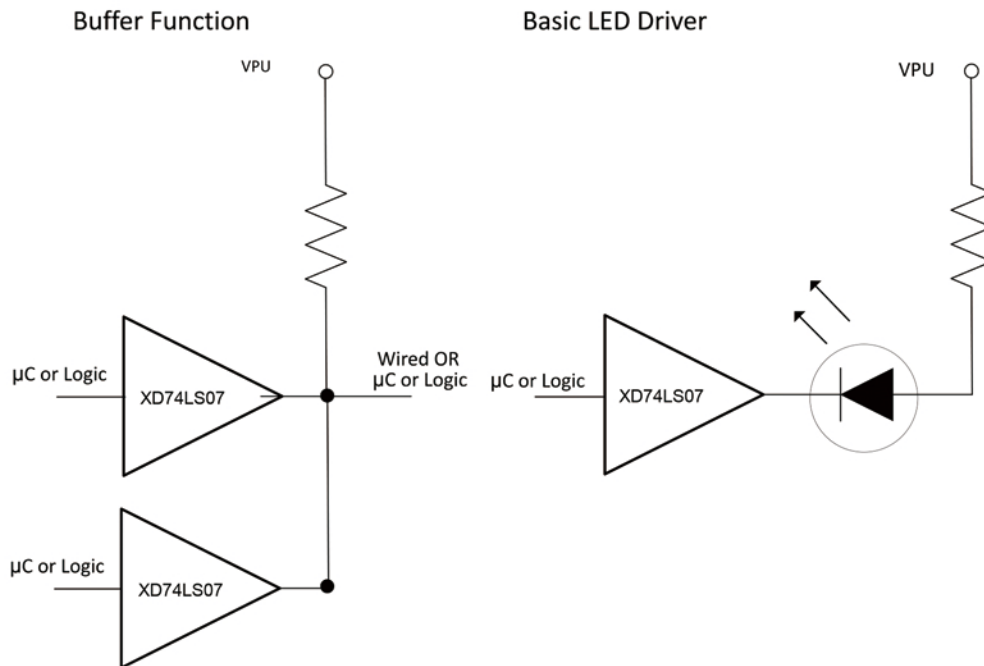
## 9 Application and Implementation

### 9.1 Application Information

The XD74LS07 device is a high-drive, open-drain CMOS device that can be used for a multitude of buffer-type functions. It can produce 40 mA of drive current at 5 V. Therefore, this device is ideal for driving multiple inputs. The inputs are 5.25-V tolerant and outputs are 30-V tolerant.

### 9.2 Typical Application

Multiple channels of the XD74LS07 device can be used to create a positive AND logic function, as shown in [Figure 4](#). Additionally, the XD74LS07 device can be used to drive an LED by sinking up to 40 mA, which may be more than the previous stage can sink.



**Figure 4. Typical Application Diagram**

#### 9.2.1 Design Requirements

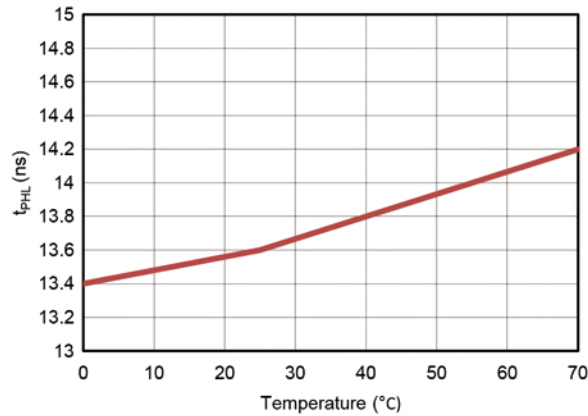
Ensure that the inputs are in a known state as defined by  $V_{IH}$  and  $V_{IL}$  in [Recommended Operating Conditions](#), or else the outputs may be in an unknown state.

#### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - For specified high and low level, see  $V_{IH}$  and  $V_{IL}$  in [Recommended Operating Conditions](#).
  - Inputs are overvoltage tolerant allowing them to go as high as 5.25 V.
2. Recommend Output Conditions
  - Load currents must not exceed 40 mA per output.
  - Outputs must not be pulled above 30 V.

## Typical Application (continued)

### 9.2.3 Application Curve



**Figure 5.  $t_{PHL}$  vs Temperature**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating indicated in [Recommended Operating Conditions](#).

Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu$ F capacitor; if there are multiple  $V_{CC}$  pins, then TI recommends either a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1- $\mu$ F and a 1- $\mu$ F capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

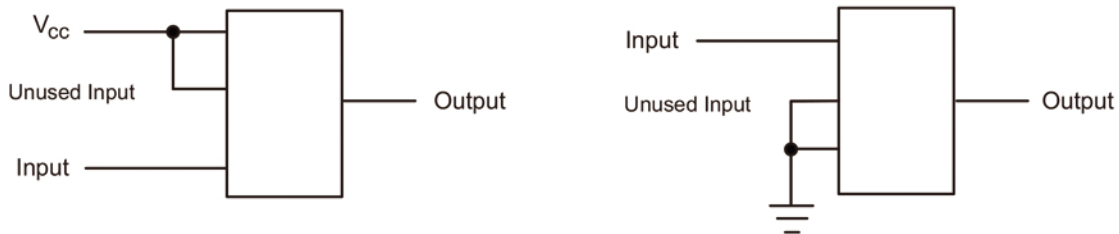
## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

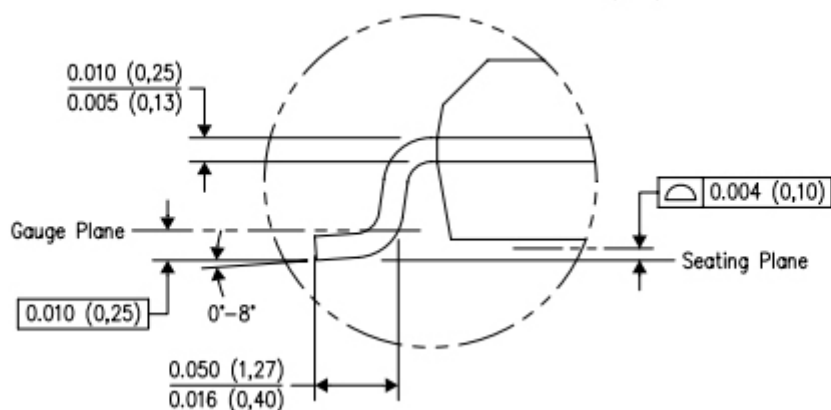
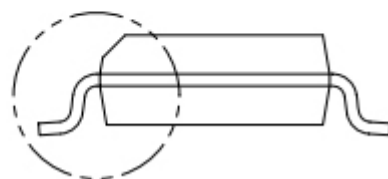
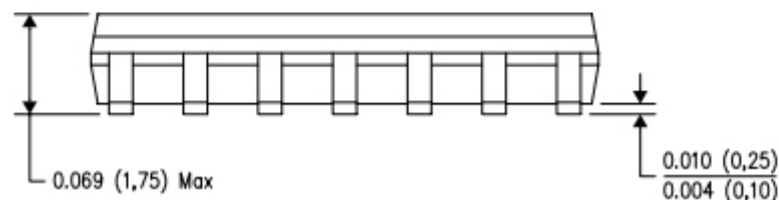
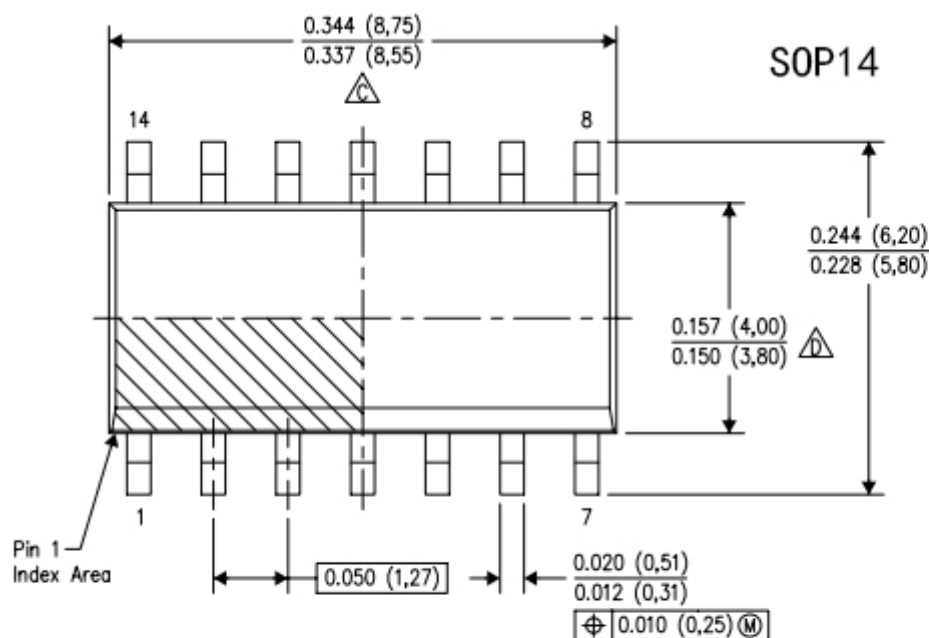
In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 6](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

### 11.2 Layout Example



**Figure 6. Layout Diagram**

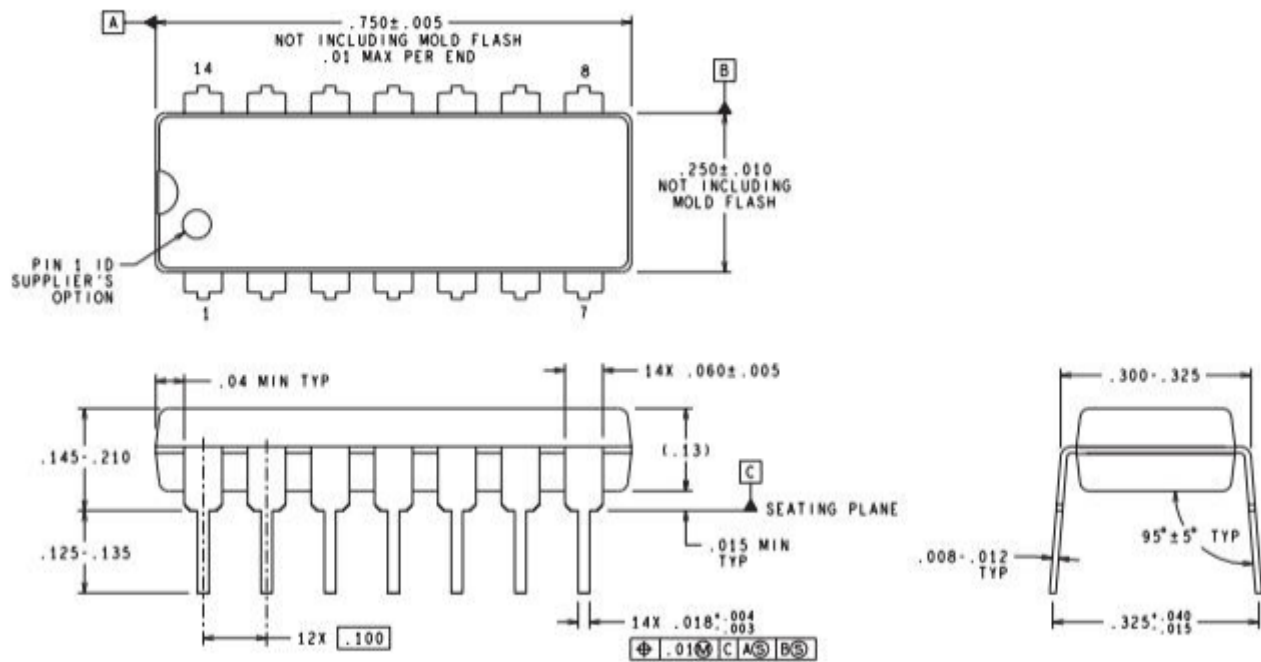
**XD74LS07 DIP14**  
**XL74LS07 SOP14**





# XL74LS07 SOP14

## DIP14



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DIMENSIONS IN ( ) FOR REFERENCE ONLY

以上信息仅供参考,如需帮助联系客服人员。谢谢 XINLUDA