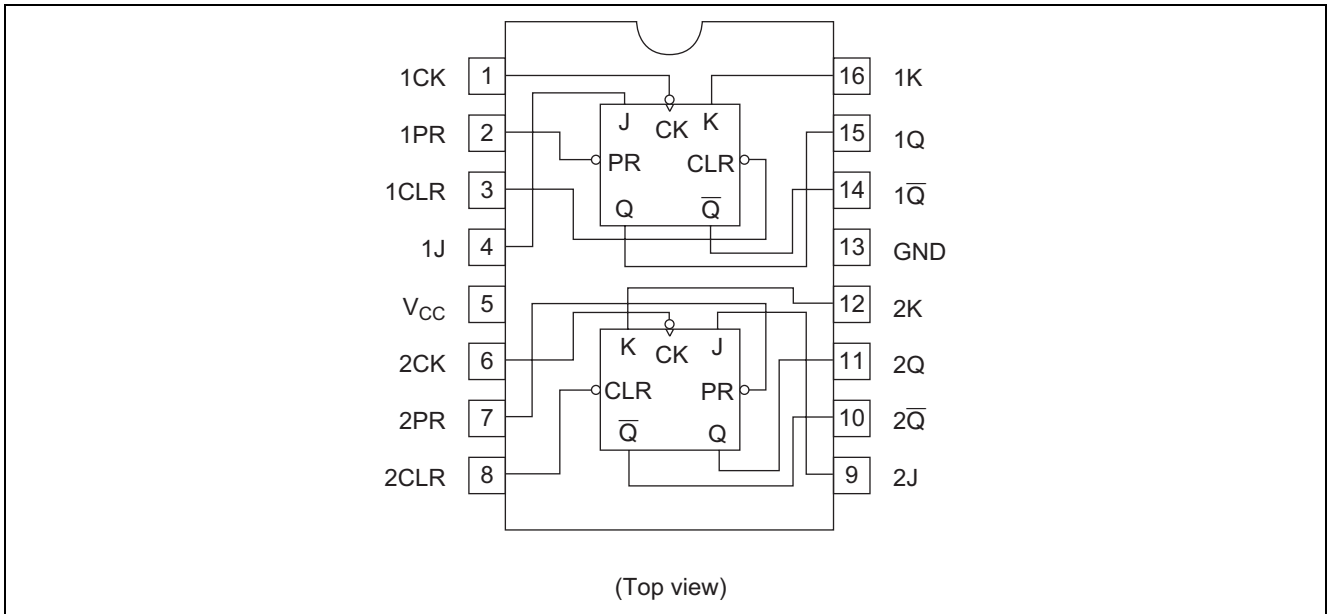


Pin Arrangement



Function Table

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q ₀	\bar{Q}_0

H; high level, L; low level, X; irrelevant, ↓; transition from high to low level,

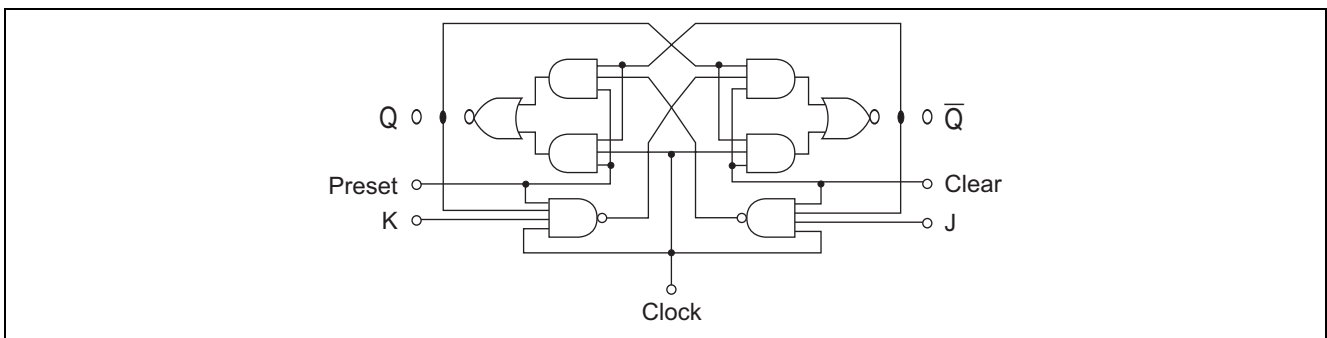
Q₀; level of Q before the indicated steady-state input conditions were established.

\bar{Q}_0 ; complement of \bar{Q}_0 or level of Q before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Block Diagram (1/2)



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Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	-400	μ A
	I_{OL}	—	—	8	mA
Operating temperature	T_{opr}	-20	25	75	°C
Clock frequency	f_{clock}	0	—	30	MHz
Pulse width	Clock High	t_w	20	—	ns
	Clear Preset Low	t_w	25	—	
Setup time	"H" Data	t_{su}	20↓	—	ns
	"L" Data	t_{su}	20↓	—	
Hold time	t_h	0↓	—	—	ns

Electrical Characteristics

($T_a = -20$ to $+75$ °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition		
Input voltage	V_{IH}	2.0	—	—	V			
	V_{IL}	—	—	0.8	V			
Output voltage	V_{OH}	2.7	—	—	V	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OH} = -400$ μ A		
	V_{OL}	—	—	0.5	V		$I_{OL} = 8$ mA $V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V	
Input current	J, K	I_{IH}	—	—		20		μ A
			Clear	—	—	60		
			Preset	—	—	60		
			Clock	—	—	80		
	J, K	I_{IL}^{**}	—	—	-0.4	mA	$V_{CC} = 5.25$ V, $V_I = 0.4$ V	
			Clear	—	—			-0.8
			Preset	—	—			-0.8
			Clock	—	—			-0.8
	J, K	I_I	—	—	0.1	mA	$V_{CC} = 5.25$ V, $V_I = 7$ V	
			Clear	—	—			0.3
			Preset	—	—			0.3
			Clock	—	—			0.4
Short-circuit output current	I_{OS}	-20	—	-100	mA	$V_{CC} = 5.25$ V		
Supply current***	I_{CC}	—	4	6	mA	$V_{CC} = 5.25$ V		
Input clamp voltage	V_{IK}	—	—	-1.5	V	$V_{CC} = 4.75$ V, $I_{IN} = -18$ mA		

Notes: * $V_{CC} = 5$ V, $T_a = 25$ °C

** I_{IL} should not be measured when preset and clear inputs are low at same time.

*** With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn.

At the time of measurement, the clock input is grounded.

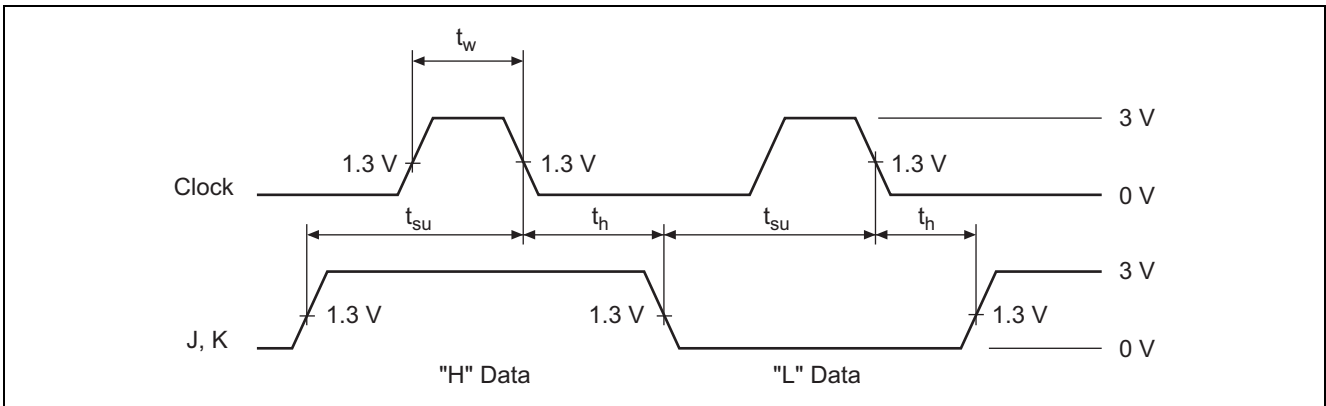
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Switching Characteristics

($V_{CC} = 5\text{ V}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{\max}			30	45		MHz	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$
Propagation delay time	t_{PLH}	Clear Preset Clock	Q, \bar{Q}	—	15	20	ns	
	t_{PHL}			—	15	20	ns	

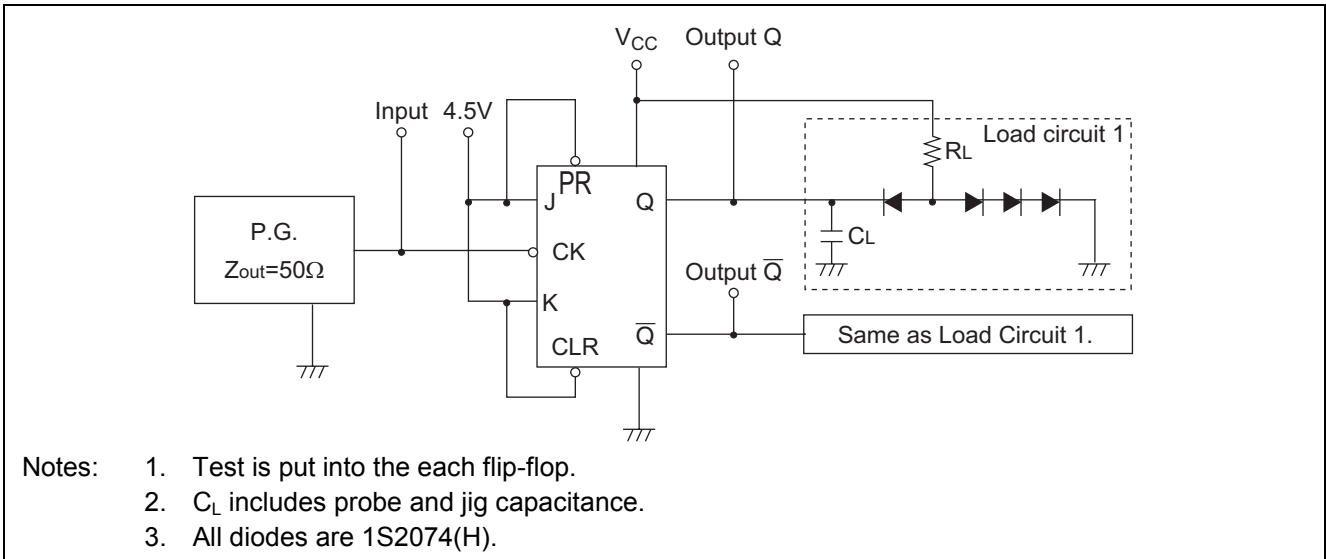
Timing Definition



Testing Method

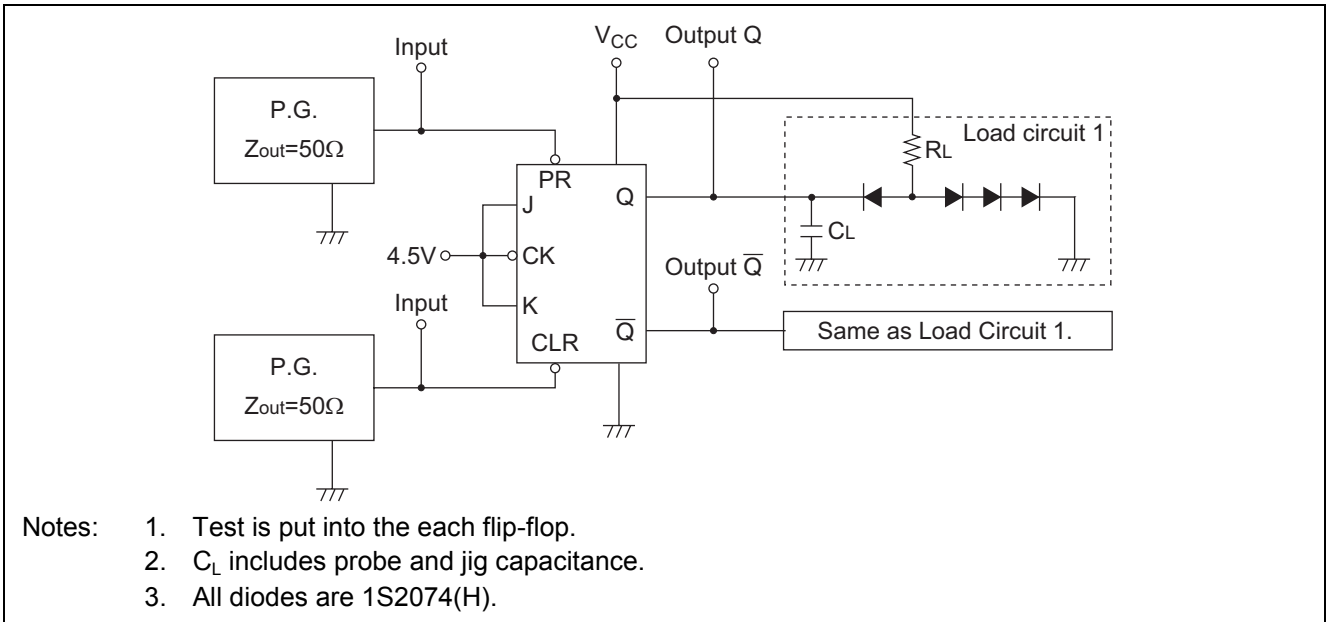
Test Circuit

1. f_{\max} , t_{PLH} , t_{PHL} , (Clock \rightarrow Q, \bar{Q})

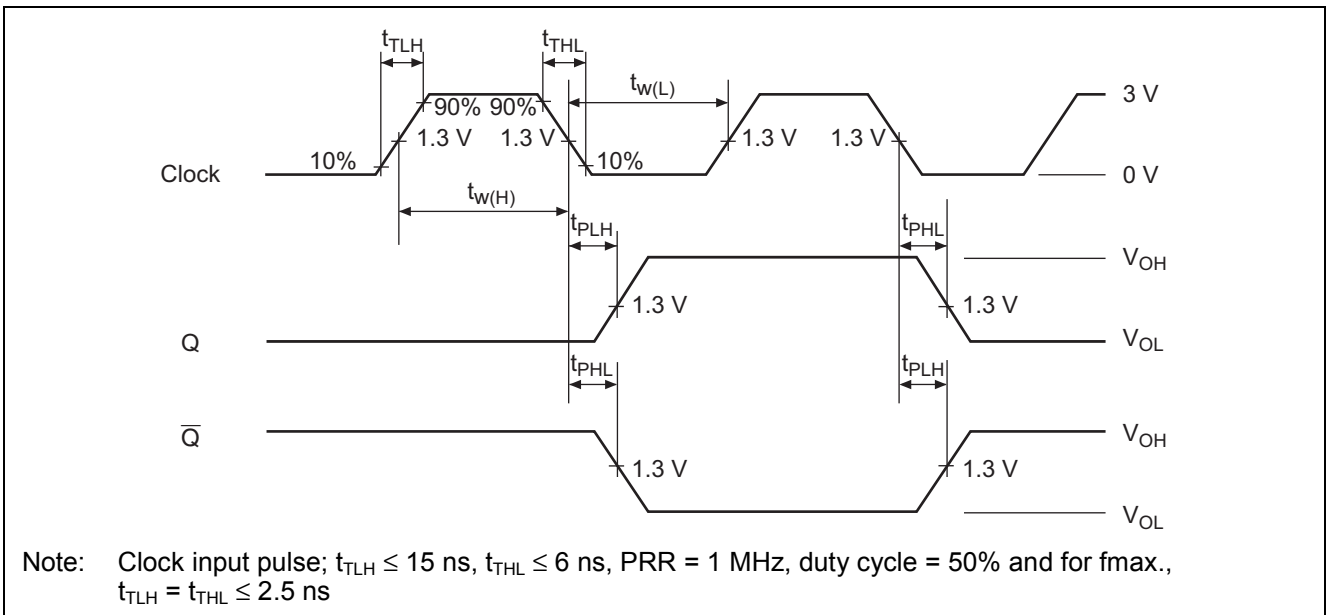


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2. t_{PHL} , t_{PLH} (Clear, Preset \rightarrow Q, \bar{Q})

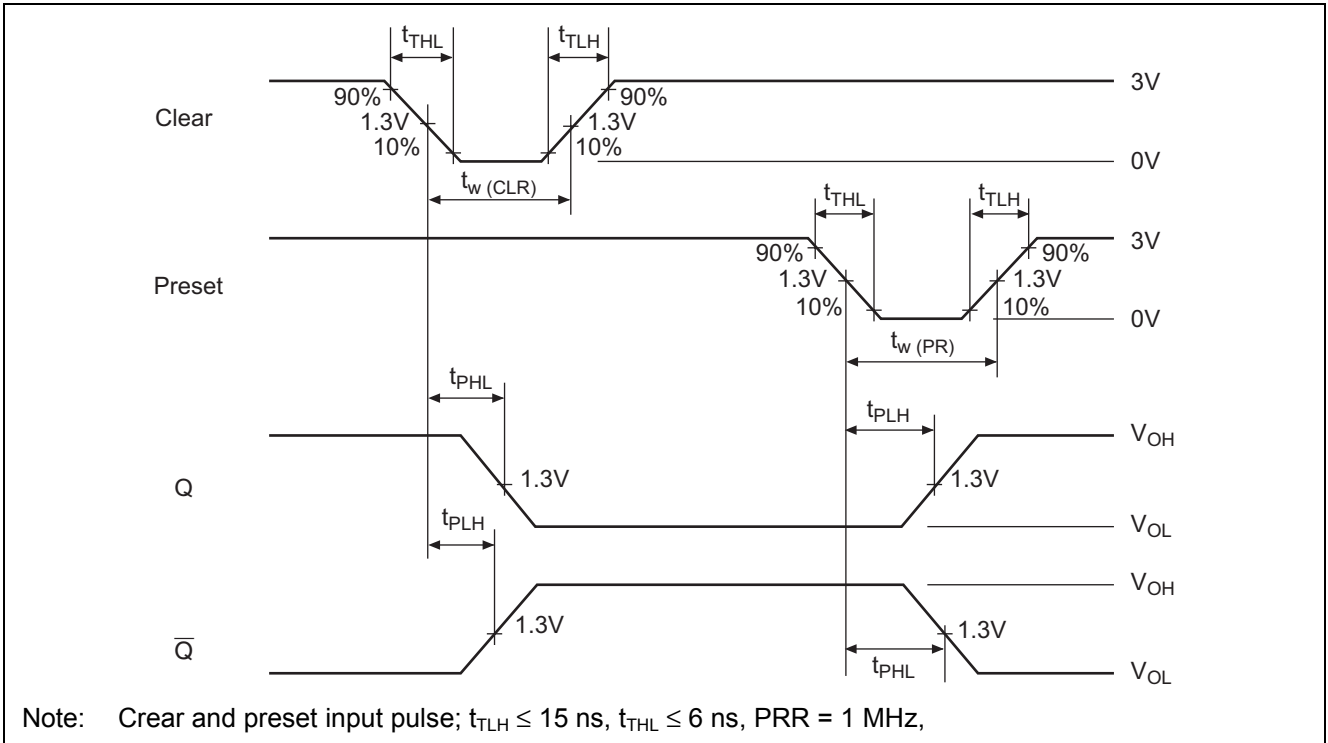


Waveforms 1

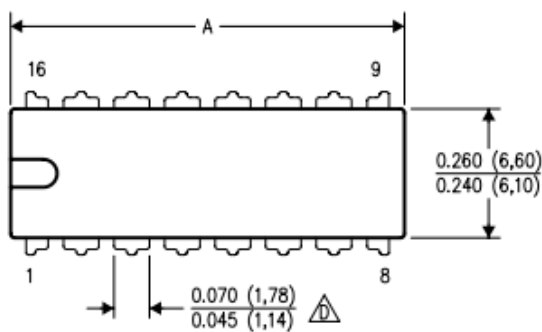


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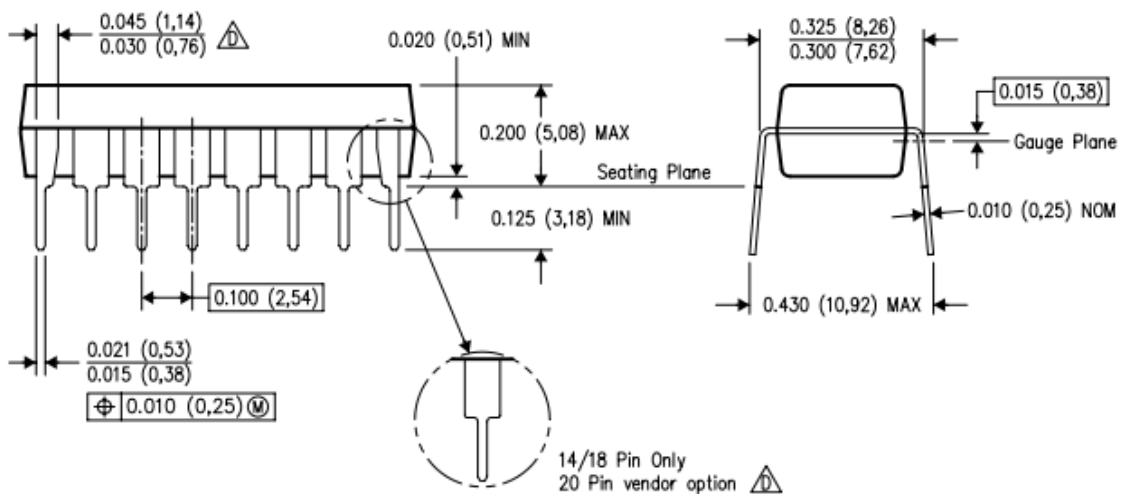
Waveforms 2



DIP



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



以上信息仅供参考. 如需帮助联系客服人员. 谢谢 XINLU DA