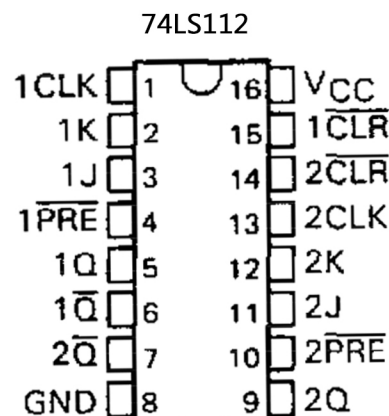


description

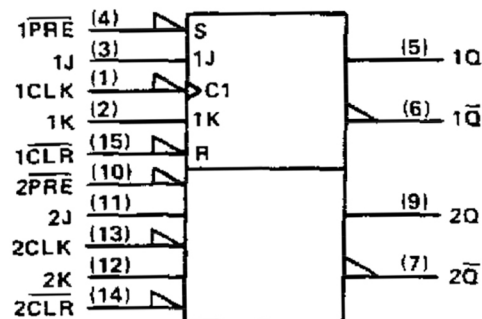
The two dividers contain two independent J-K flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage transition and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the level at the outputs. These versatile flip-flops can perform a toggle flip-flop by tying J and K high.



FUNCTION TABLE (each flip-flop)

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H↑	H↑
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q ₀	Q̄ ₀

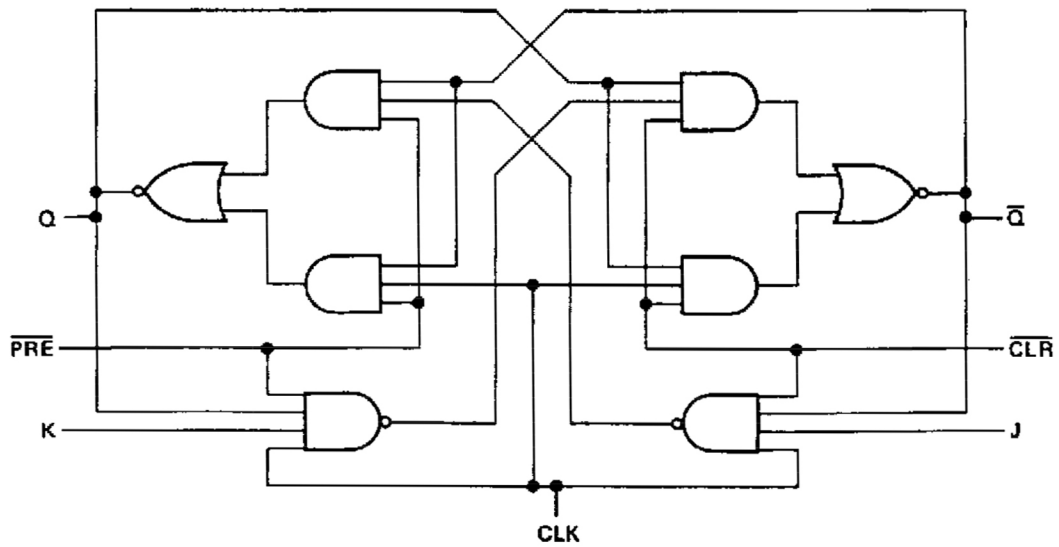
logic symbol



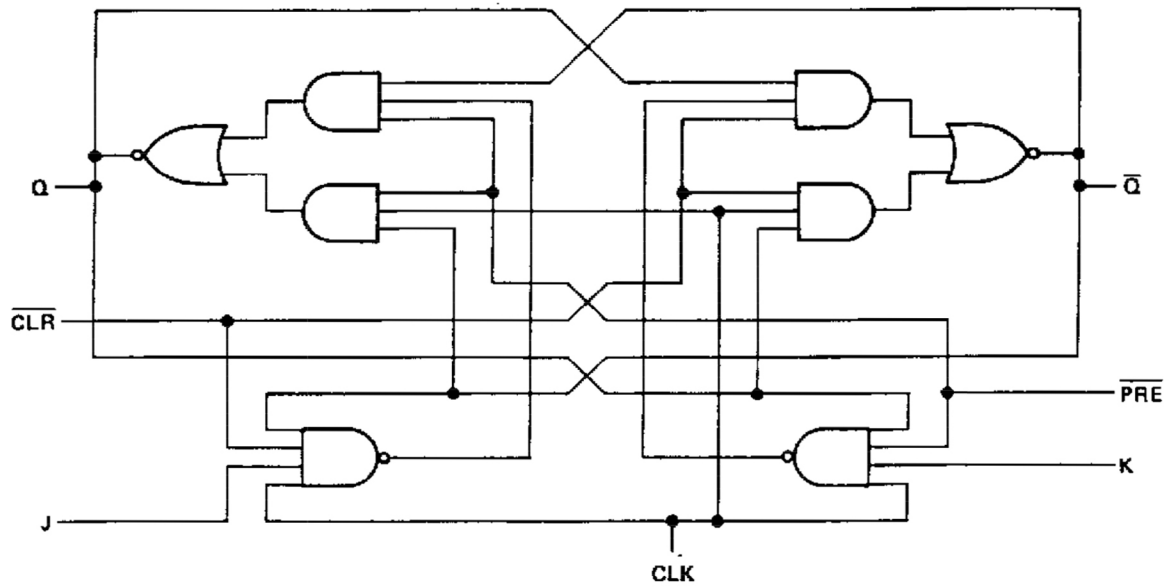
The output in configuration on or not guaranteed to meet minimum levels for V_{oh} if the loads are not specified and V_{om} are near V_{ih} minimum. Furthermore, this configuration is not recommended for use as a toggle flip-flop when either preset or clear is active (high) level.

logic diagrams (positive logic)

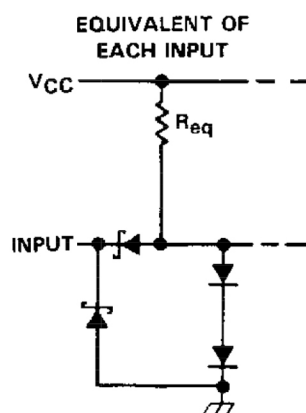
74LS112



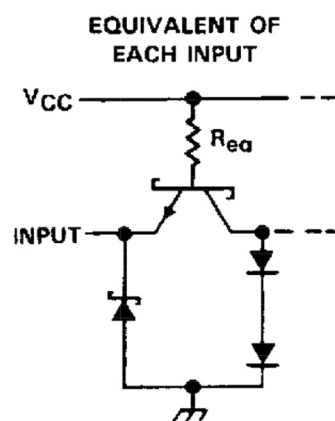
74LS112



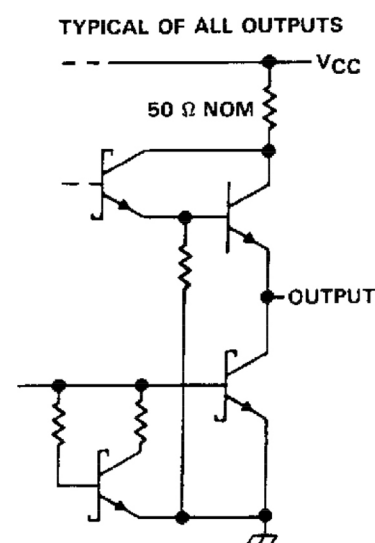
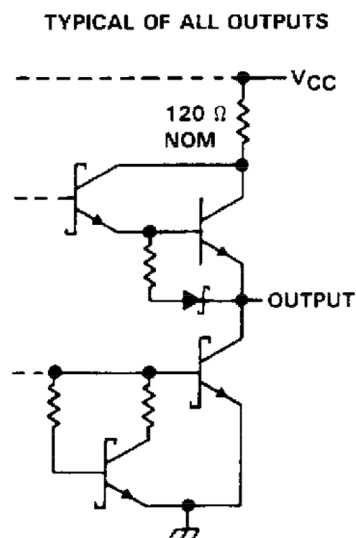
schematics of inputs and outputs



I_{IL} MAX	R_{eq} NOM
-0.4 mA	30 k Ω
-0.8 mA	8.25 k Ω



I_{IL} MAX	R_{eq} NOM
-1.6 mA	4 k Ω
-4 mA	1.4 k Ω
-7 mA	900 Ω



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 74LS112	7 V
74LS112	5.5 V
Operating free-air temperature range: 74LS112	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

XD74LS112 DIP-16

recommended operating conditions

		XD74LS112			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{OH}	High-level output current			-0.4	mA
I _{OL}	Low-level output current			8	mA
f _{clock}	Clock frequency	0		30	MHz
t _w	Pulse duration	CLK high	20		ns
		PRE or CLR low	25		
t _{su}	Set up time-before CLK↓	Data high or low	20		ns
		CLR inactive	25		
		PRE inactive	20		
t _h	Hold time-data after CLK↓	0			ns
T _A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	XD74LS112			UNIT
			MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA			-1.5	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.7	3.4		V
V _{OL}		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA	0.25		0.4	V
		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA	0.35		0.5	
I _I	J or K	V _{CC} = MAX, V _I = 7 V			0.1	mA
	CLR or PRE				0.3	
	CLK				0.4	
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.7 V			20	μA
	CLR or PRE				60	
	CLK				80	
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.4 V			-0.4	mA
	All other				-0.8	
I _{OS} §		V _{CC} = MAX, see Note 2	-20		-100	mA
I _{CC} (Total)		V _{CC} = MAX, see Note 3		4	6	mA

For ^nditiona abown at MIN or MAX. s the sppropriitti vduet specified urtder rweoiwhtdtdt o^wattng conditions.

*All typical vbluob m st *cc ■ 5 V, Ta - 25fC.

Not more thee one ouWE X RfwvrM ar x He. am rM durMmn of uhrur^ircitiT AhntUd net Exceed cne secerxt NOTES:

2. Por certain device whor» cUtacommotatfin con bo 8uaad by «ho«ting ai output to ground, s teei may ba pvformeaa with Vq — 2.25 V Md 2.12SV for tfio *M family ond the '7, family, roepMtivefy. with tt» minimum and maximum Hmit® reduced to ww hdr uf the, maied valuoee,

3. with all cinpim open, is masured wim itift a and B ntirptm high in nim. at The time of m*Mr^ent, g dock input le ggr»d

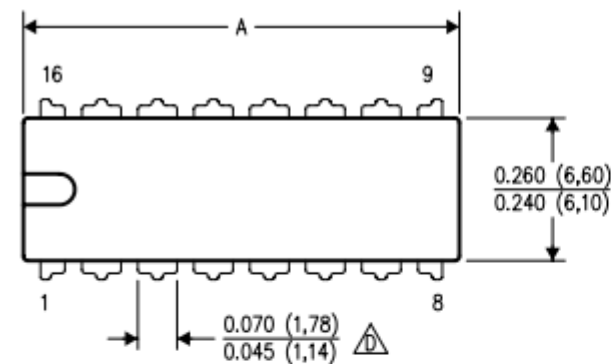
XD74LS112 DIP-16

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Note 4)

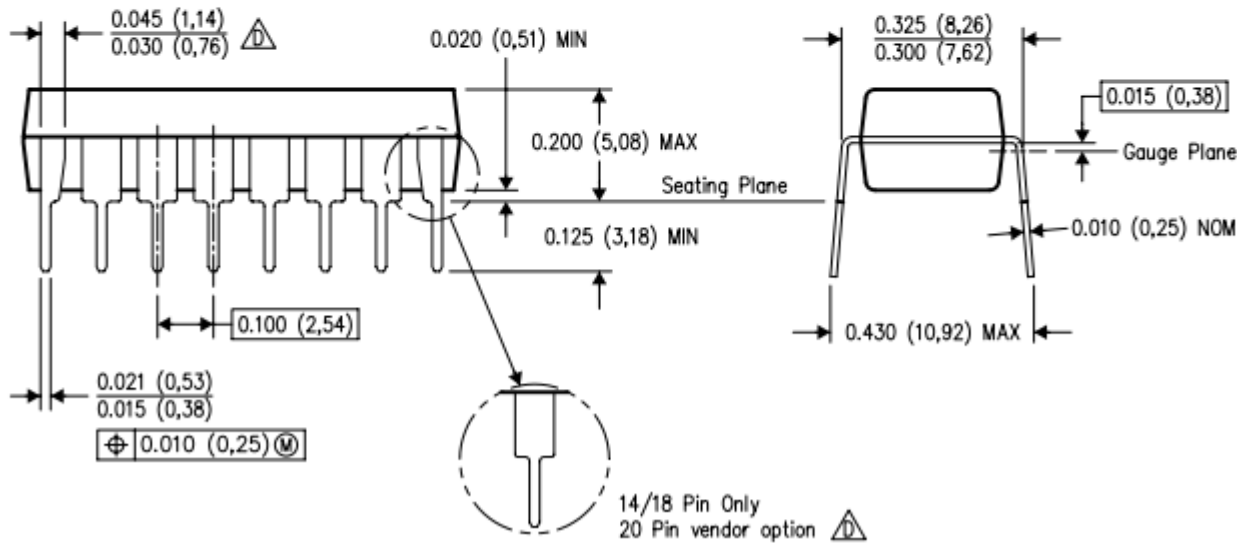
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\max}$			$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$	30	45		MHz
t_{PLH}	$\overline{CLR}$, $\overline{PRE}$ or CLK	Q or $\overline{Q}$			15	20	ns
t_{PHL}					15	20	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

DIP



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



以上信息仅供参考. 如需帮助联系客服人员。谢谢 XINLUDA