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XD7555 DIP8 / XL7555 SOP8

The XD/XL7555 and 7556 are CMOS RC timers providing significantly improved performance over the standard 555NE and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low Threshold, Trigger and Reset currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple Control Voltage for stable operation.

Specifically, the XD/XL7555 and 7556 are stable controllers capable of producing accurate time delays or frequencies. The 7556 is a dual XD/XL7555, with the two timers operating independently of each other, sharing only V+ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555NE devices, the Cont rol Voltage terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

Features

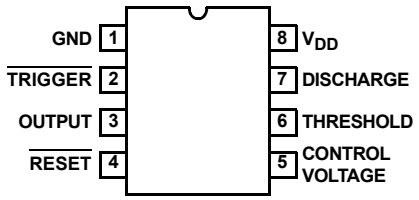
- Exact equivalent in most cases for 555NE or XD555
- Low supply current
  - XD/XL7555 . . . . . 60µA
  - 7556 . . . . . 120µA
- Extremely low input currents 20pA
- High speed operation 1MHz
- Guaranteed supply voltage range . . . . . 2V to 18V
- Temperature stability . . . . . 0.005%/°C at +25°C
- Normal reset function - no crowbarring of supply during output transition
- Can be used with higher impedance timing elements than regular 555/556 for longer RC time constants
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- High output source/sink driver can drive TTL/CMOS
- Outputs have very low offsets, HIGH and LOW
- Pb-free (RoHS Compliant)

Applications

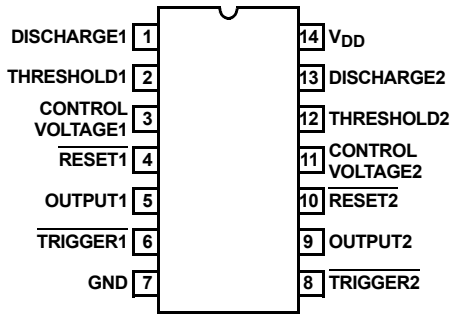
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

Pin Configurations

XD/XL7555
(8 LD PDIP, SOIC)
TOP VIEW



7556
(14 LD PDIP, CERDIP)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage . . . . . +18V
Input Voltage
Trigger, Control Voltage, Threshold,
Reset (Note 4) . . . . . V+ +0.3V to GND -0.3V
Output Current 100mA

Operating Conditions

Temperature Range
XD/XL7555 . . . . . 0°C to +70°C
XD/XL7555 . . . . . - 25°C to +85°C
7555 . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical, Notes 5, 6)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld CERDIP Package	80	24
14 Ld PDIP Package*	115	46
8 Ld PDIP Package*	130	69
8 Ld SOIC Package	170	67

Maximum Junction Temperature (Hermetic Package) . . . . . +175°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
* Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V+ +0.3V or less than V- -0.3V may cause destructive latch-up. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple supply systems, the supply of the XD/XL7555 and 7556 must be turned on first.
5. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		T_A = +25°C			(Note 8) -55°C TO +125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Static Supply Current	I_{DD}	XD/XL7555	V_{DD} = 5V		40	200			300	µA
			V_{DD} = 15V		60	300			300	µA
		7556	V_{DD} = 5V		80	400			600	µA
			V_{DD} = 15V		120	600			600	µA
Monostable Timing Accuracy		R_A = 10k, C = 0.1µF, V_{DD} = 5V			2					%
							858		1161	µs
Drift with Temperature (Note 7)		V_{DD} = 5V						150		ppm/°C
		V_{DD} = 10V						200		ppm/°C
		V_{DD} = 15V						250		ppm/°C
Drift with Supply (Note 7)		V_{DD} = 5V to 15V			0.5			0.5		%/V
Astable Timing Accuracy		R_A = R_B = 10k, C = 0.1µF, V_{DD} = 5V			2					%
							1717		2323	µs
Drift with Temperature (Note 7)		V_{DD} = 5V						150		ppm/°C
		V_{DD} = 10V						200		ppm/°C
		V_{DD} = 15V						250		ppm/°C
Drift with Supply (Note 7)		V_{DD} = 5V to 15V			0.5			0.5		%/V
Threshold Voltage	V_{TH}	V_{DD} = 15V		62	67	71	61		72	% V_{DD}
Trigger Voltage	V_{TRIG}	V_{DD} = 15V		28	32	36	27		37	% V_{DD}
Trigger Current	I_{TRIG}	V_{DD} = 15V				10			50	nA
Threshold Current	I_{TH}	V_{DD} = 15V				10			50	nA
Control Voltage	V_{CV}	V_{DD} = 15V		62	67	71	61		72	% V_{DD}

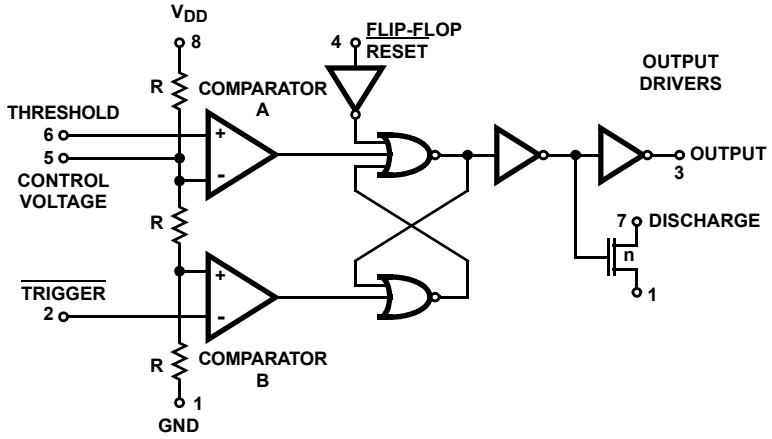
Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	T_A = +25°C			(Note 8) -55°C TO +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Reset Voltage	V_{RST}	V_{DD} = 2V to 15V	0.4		1.0	0.2		1.2	V
Reset Current	I_{RST}	V_{DD} = 15V			10			50	nA
Discharge Leakage	I_{DIS}	V_{DD} = 15V			10			50	nA
Output Voltage	V_{OL}	V_{DD} = 15V, I_{SINK} = 20mA		0.4	1.0			1.25	V
		V_{DD} = 5V, I_{SINK} = 3.2mA		0.2	0.4			0.5	V
	V_{OH}	V_{DD} = 15V, I_{SOURCE} = 0.8mA	14.3	14.6		14.2			V
		V_{DD} = 5V, I_{SOURCE} = 0.8mA	4.0	4.3		3.8			V
Discharge Output Voltage	V_{DIS}	V_{DD} = 5V, I_{SINK} = 15mA		0.2	0.4			0.6	V
		V_{DD} = 15V, I_{SINK} = 15mA						0.4	V
Supply Voltage (Note 7)	V_{DD}	Functional Operation	2.0		18.0	3.0		16.0	V
Output Rise Time (Note 7)	t_R	R_L = 10M, C_L = 10pF, V_{DD} = 5V		75					ns
Output Fall Time (Note 7)	t_F	R_L = 10M, C_L = 10pF, V_{DD} = 5V		75					ns
Oscillator Frequency (Note 7)	f_{MAX}	V_{DD} = 5V, R_A = 470Ω, R_B = 270Ω, C = 200pF		1					MHz

NOTES:

7. These parameters are based upon characterization data and are not tested.
8. Applies only to military temperature range product (M suffix).

Functional Diagram



NOTE: This functional diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs.

FIGURE 1. FUNCTIONAL DIAGRAM

TRUTH TABLE

THRESHOLD VOLTAGE	$\overline{\text{TRIGGER}}$ VOLTAGE	$\overline{\text{RESET}}$	OUTPUT	DISCHARGE SWITCH
Don't Care	Don't Care	Low	Low	On
$>^2/_3$(V+)	$>^1/_3$(V+)	High	Low	On
$<^2/_3$(V+)	$>^1/_3$(V+)	High	Stable	Stable
Don't Care	$<^1/_3$(V+)	High	High	Off

NOTE: $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

Schematic Diagram

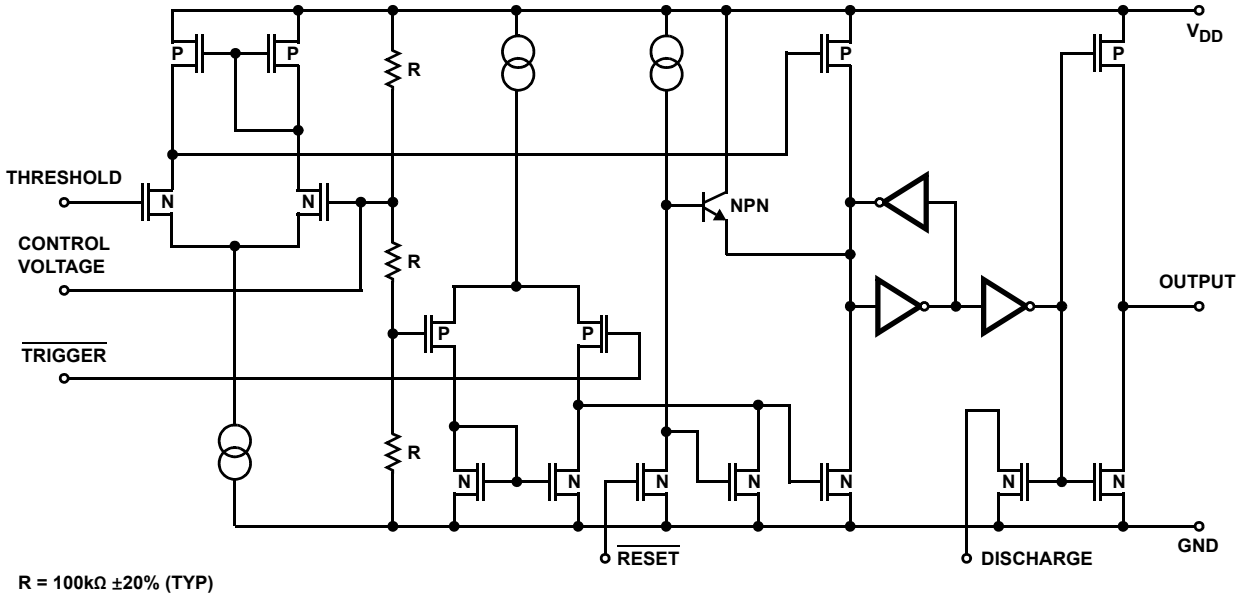


FIGURE 2. SCHEMATIC DIAGRAM

Application Information

General

The XD/XL7555 and 7556 devices are, in most instances, direct replacements for the 555NE devices. However, it is possible to effect economies in the external component count using the XD/XL7555 and 7556. Because the bipolar 555NE devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The XD/XL7555 and 7556 devices produce no such transients (see Figure 3).

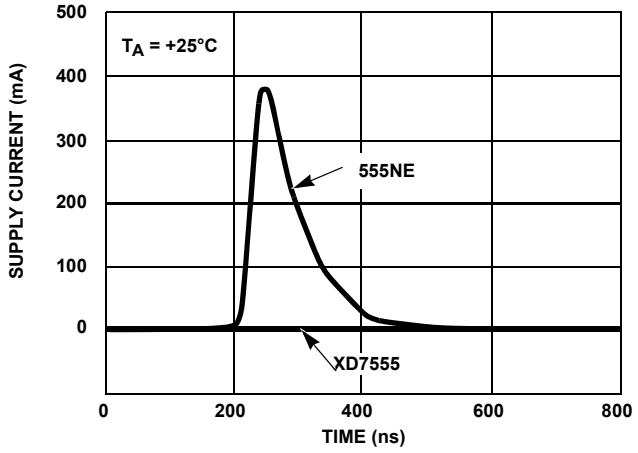


FIGURE 3. SUPPLY CURRENT TRANSIENT COMPARED WITH A STANDARD BIPOLAR 555 DURING AN OUTPUT TRANSITION

The XD/XL7555 and 7556 produce supply current spikes of only 2mA to 3mA instead of 300mA to 400mA and supply decoupling is normally not necessary. Also, in most instances, the Control Voltage decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications, two capacitors can be saved using an XD/XL7555 and three capacitors with an 7556.

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the XD/XL7555 and 7556 devices is very low, the total system supply current can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 4, 5, and 6.

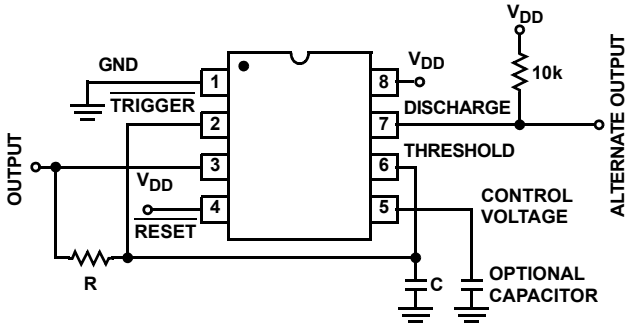


FIGURE 4. ASTABLE OPERATION

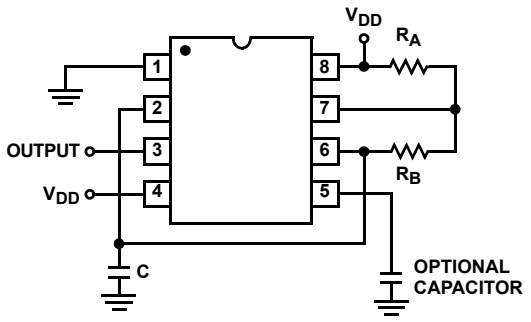


FIGURE 5. ALTERNATE ASTABLE CONFIGURATION

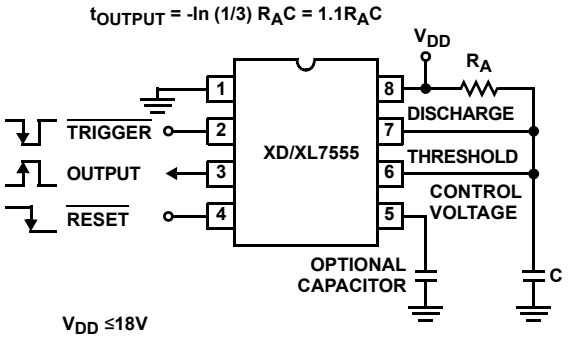


FIGURE 6. MONOSTABLE OPERATION

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5V or more, the XD/XL7555 and 7556 will drive at least two standard TTL loads.

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 4. The output swings from rail-to-rail, and is a true 50% duty cycle square wave. Trip points and output swings are symmetrical. Less than a 1% frequency variation is observed over a voltage range of +5V to +15V.

$$f = \frac{1}{1.4\ RC} \qquad \text{(EQ. 1)}$$

The timer can also be connected as shown in Figure 5. In this circuit, the frequency is as shown by Equation 2:

$$f = 1.44/(R_A + 2R_B)C \qquad \text{(EQ. 2)}$$

The duty cycle is controlled by the values of R_A and R_B, by Equation 3:

$$D = (R_A + R_B)/(R_A + 2R_B) \qquad \text{(EQ. 3)}$$

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (see Figure 6). Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{Trigger}}$ pulse to pin 2, the internal flip-flop is set, which releases the short-circuit across the external capacitor and drives the Output high. The voltage across the capacitor now increases exponentially with a time constant t = R_AC. When the voltage across the capacitor equals $^2/_3$ V+, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{Trigger}}$ must return to a high state before the OUTPUT can return to a low state.

CONTROL VOLTAGE

The Control Voltage terminal permits the two trip voltages for the Threshold and $\overline{\text{Trigger}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the Control Voltage pin.

$\overline{\text{RESET}}$

The $\overline{\text{Reset}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555/556, i.e., 0.6V to 0.7V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{Reset}}$ function is, however, much improved over the standard bipolar 555NE in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the Output and Discharge pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

Typical Performance Curves

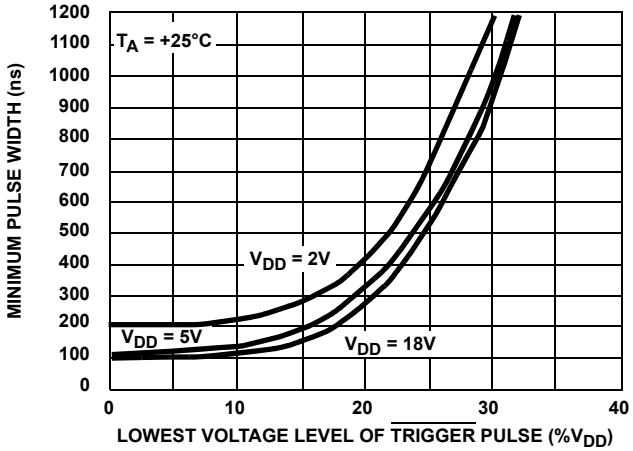


FIGURE 7. MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING

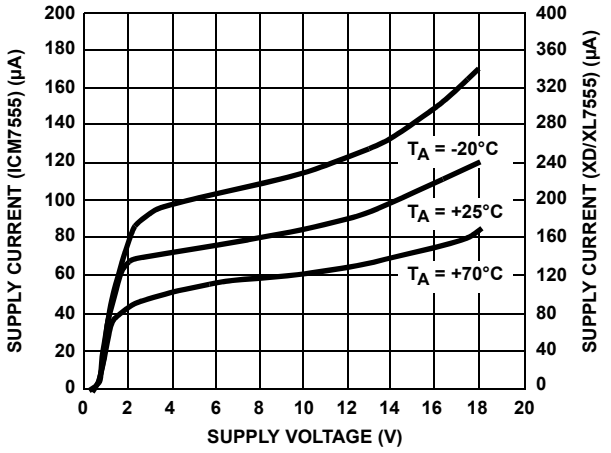


FIGURE 8. SUPPLY CURRENT vs SUPPLY VOLTAGE

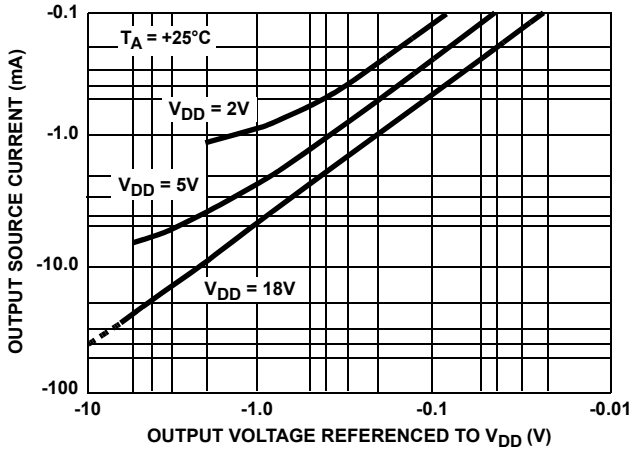


FIGURE 9. OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

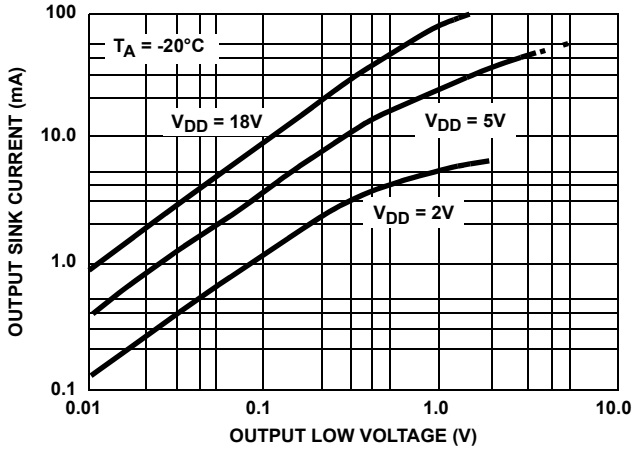


FIGURE 10. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

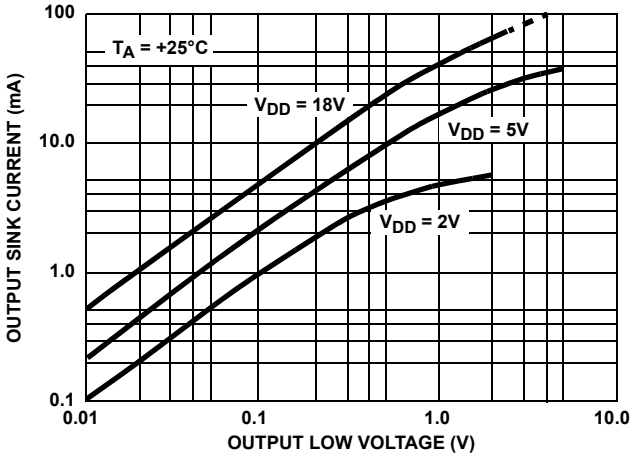


FIGURE 11. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

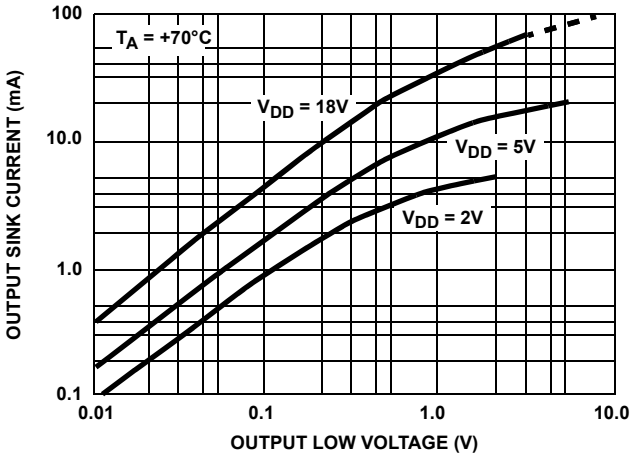


FIGURE 12. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

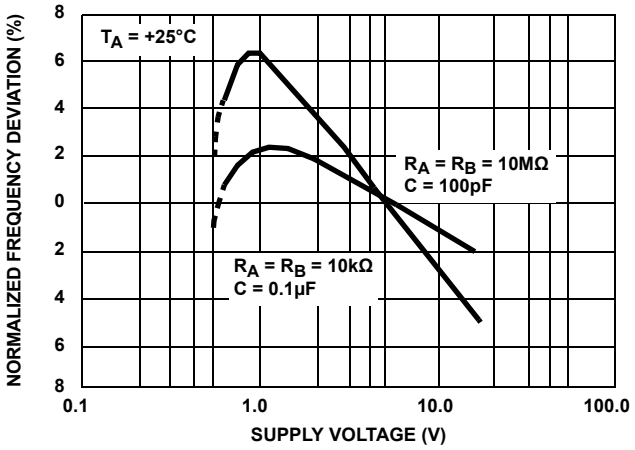


FIGURE 13. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE vs SUPPLY VOLTAGE

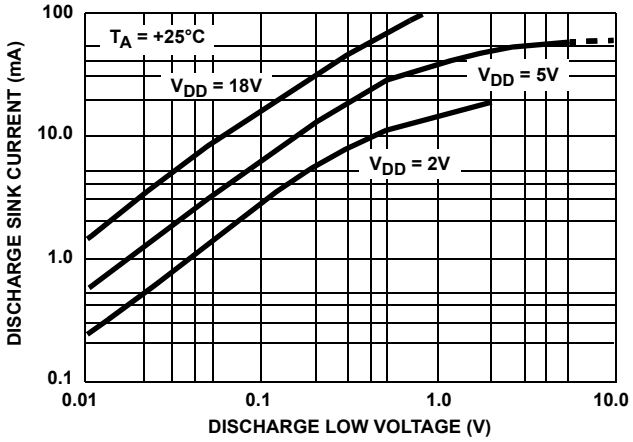


FIGURE 14. DISCHARGE OUTPUT CURRENT vs DISCHARGE OUTPUT VOLTAGE

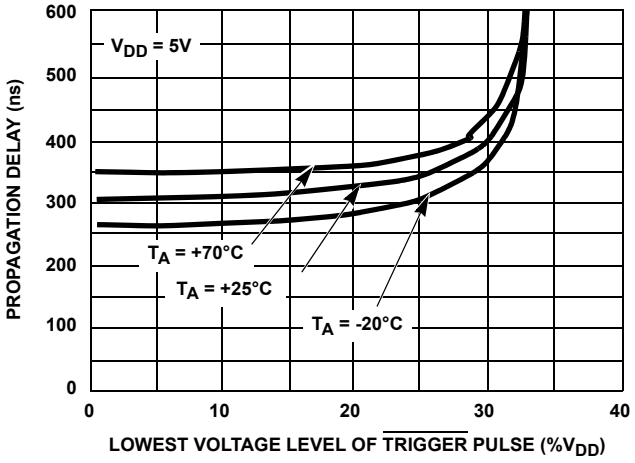


FIGURE 15. PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE

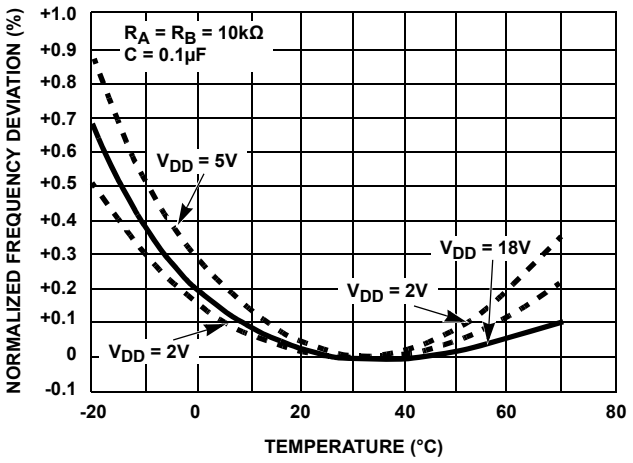


FIGURE 16. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE vs TEMPERATURE

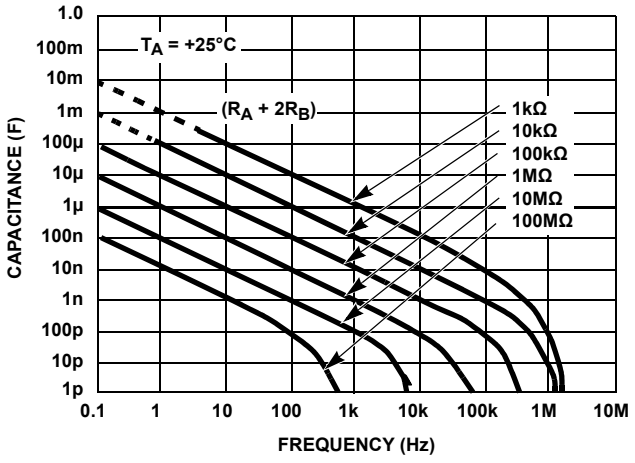


FIGURE 17. FREE RUNNING FREQUENCY vs R_A, R_B AND C

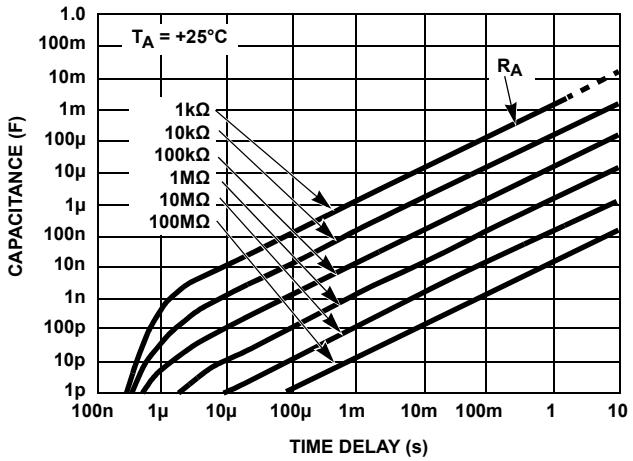
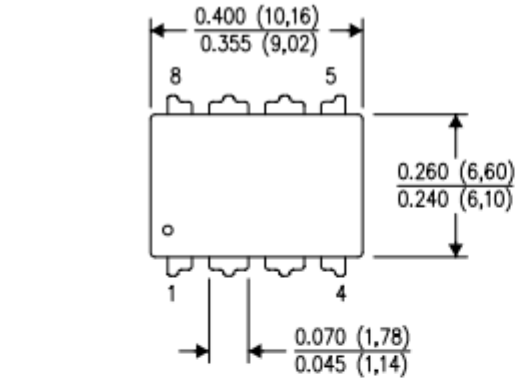
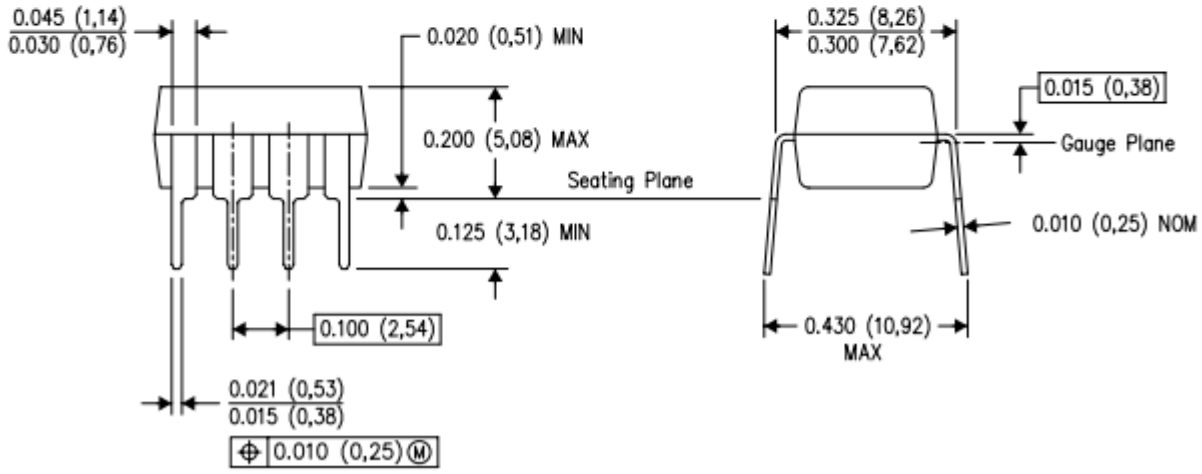
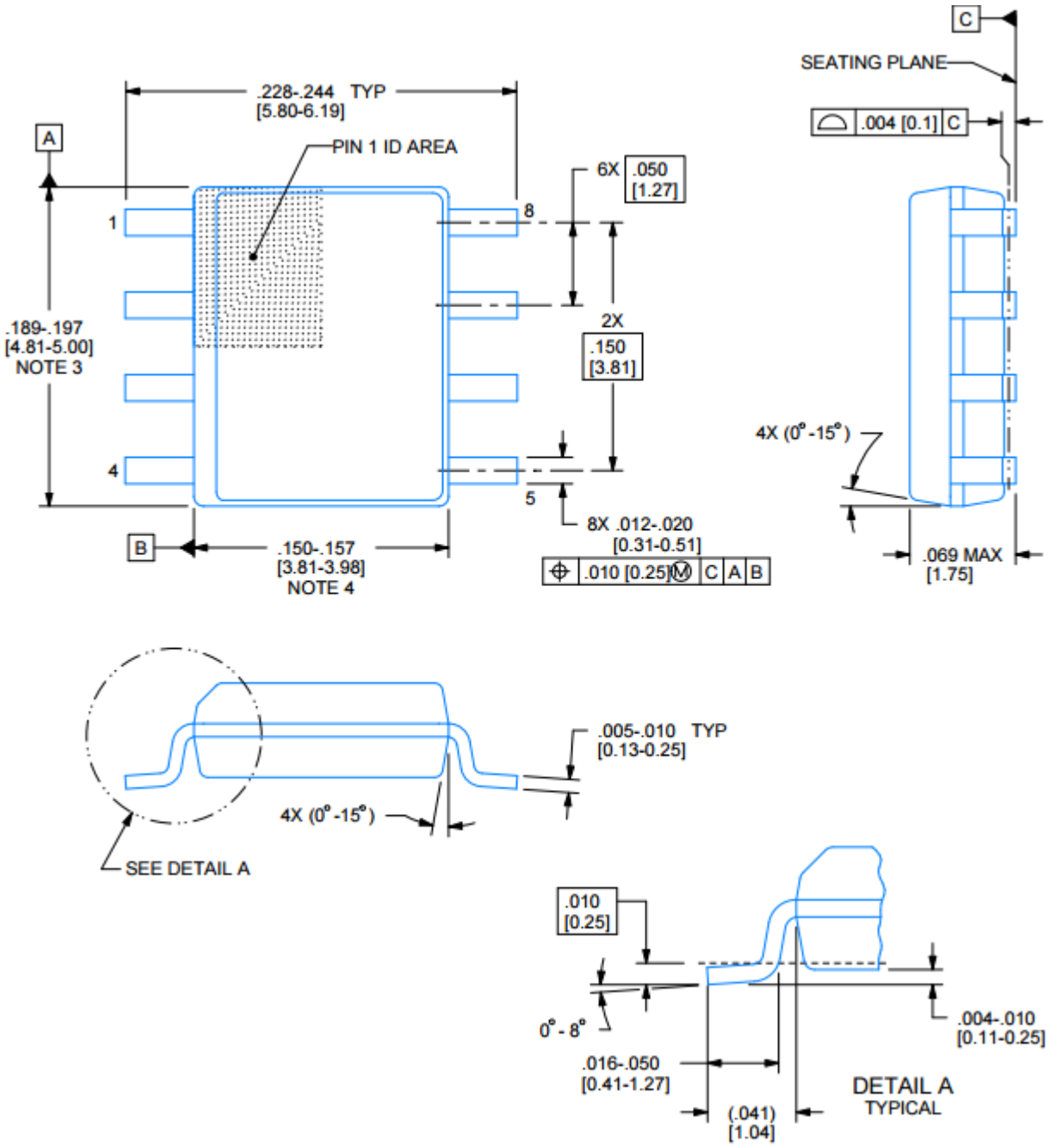


FIGURE 18. TIME DELAY IN THE MONOSTABLE MODE vs R_A AND C


0.400 (10,16)
0.355 (9,02)
8
5
0.260 (6,60)
0.240 (6,10)
1
4
0.070 (1,78)
0.045 (1,14)


0.045 (1,14)
0.030 (0,76)
0.020 (0,51) MIN
0.200 (5,08) MAX
Seating Plane
0.125 (3,18) MIN
0.100 (2,54)
0.021 (0,53)
0.015 (0,38)
0.010 (0,25) M
0.325 (8,26)
0.300 (7,62)
0.015 (0,38)
Gauge Plane
0.010 (0,25) NOM
0.430 (10,92)
MAX



以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA