

### General Description

The WSD3069DN56 is the highest performance trench N-ch and P-ch MOSFET with extreme high cell density, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications.

The WSD3069DN56 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

### Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

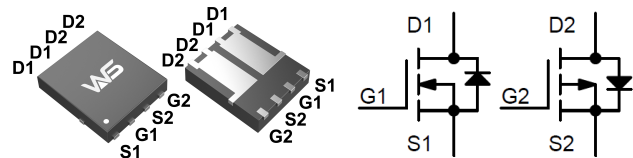
### Product Summary

BVDSS	RDS(on)	ID
30V	15mΩ	16A
-30V	15mΩ	-16A

### Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- CCFL Back-light Inverter

### DFN5X6C-8 Pin Configuration



### Absolute Maximum Ratings (TA= 25°C unless otherwise noted)

Symbol	Parameter	N Channl	P Channl	Unit	
V <sub>DSS</sub>	Drain-Source Voltage	30	-30	V	
V <sub>GSS</sub>	Gate-Source Voltage	±20	±20		
I <sub>D</sub>	Continuous Drain Current c	T <sub>C</sub> =25°C	16	-16	A
		T <sub>C</sub> =100°C	10.5	-12.5	
I <sub>DM</sub>	Pulsed Drain Current c	35	-65	A	
I <sub>DSM</sub>	Continuous Drain Current	T <sub>A</sub> =25°C	9.5	-11	A
		T <sub>A</sub> =70°C	7.5	-8.5	
P <sub>D</sub>	Maximum Power Dissipation B	T <sub>C</sub> =25°C	10	20	W
		T <sub>C</sub> =100°C	4	8	
P <sub>DSM</sub>	Maximum Power Dissipation A	T <sub>C</sub> =25°C	3.1	4.1	W
		T <sub>C</sub> =100°C	2	2.6	
I <sub>S</sub>	Diode Continuous Forward Current	T <sub>C</sub> =25°C	10	-16	A
E <sub>AS</sub>	Single pulsed avalanche energy c	L=0.5mH	7	-36	mJ
I <sub>AS</sub>	Single pulsed avalanche Current	L=0.5mH	12	-27	A
T <sub>J</sub>	Maximum Junction Temperature	150	150	°C	
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	-55 to 150		
R <sub>θJA</sub>	Thermal Resistance-Junction to Ambient	t≤10S	40	30	°C/W
		Steady Statec	70	65	°C/W
R <sub>θJC</sub>	Thermal Resistance-Junction to Case	21	6	°C/W	

**N-Channl Electrical Characteristics** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=24V, V_{GS}=0V$	-	-	1	$\mu A$
		$T_J=55^\circ C$	-	-	5	$\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1	1.5	2	V
$I_{GSS}$	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
$R_{DS(ON)}$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=10A$	-	15	19.5	m $\Omega$
		$V_{GS}=4.5V, I_{DS}=5A$	-	18	24	
$R_G$	Gate Resistance	$F=1MHz, V_{GS}=0V, V_{DS}=0V$	-	-	2.8	$\Omega$
$C_{iss}$	Input Capacitance	$V_{GS}=0V, V_{DS}=15V,$ Frequency=1.0MHz	-	373	-	pF
$C_{oss}$	Output Capacitance		-	67	-	
$C_{riss}$	Reverse transfer capacitance		-	41	-	
$t_{d(ON)}$	Turn-on delay Time	$V_{GEN}=10V, V_{DD}=15V, R_G=3\Omega,$ $RL=1.5\Omega$	-	4.3	-	nS
$t_r$	Turn-on rise Time		-	2.8	-	
$t_{d(OFF)}$	Turn-off delay Time		-	15.8	-	
$t_f$	Turn-off rise Time		-	3	-	
$Q_g$	Total Gate Charge (10V)	$V_{DS}=15V, V_{GS}=10V, I_{DS}=10A$	-	7.1	-	nC
$Q_g$	Total Gate Charge (4.5V)		-	3.5	-	
$Q_{gs}$	Gate-Source Charge		-	1.2	-	
$Q_{gd}$	Gate-Drain Charge		-	1.6	-	
$V_{SD}$	Diode Forward Voltage	$I_{SD}=1A, V_{GS}=0V$	-	0.75	1	V
$t_{rr}$	Reverse Recovery Time	$I_{DS}=10A,$ $dI_{SD}/dt=500A/\mu s$	-	6	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	6.6	-	nC

A. The value of  $R_{\theta JA}$  is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ C$ . The Power dissipation  $P_{DSM}$  is based on  $R_{\theta JA} t \leq 10s$  and the maximum allowed junction temperature of  $150^\circ C$ . The value in any given application depends on the user's specific board design.

B. The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^\circ C$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ C$ .

D. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using  $<300\mu s$  pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, rating, assuming a maximum junction temperature of  $T_{J(MAX)}=150^\circ C$ . The SOA curve provides a single pulse

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ C$ .

**P-Channl Electrical Characteristics** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=-250A$	-30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-24V, V_{GS}=0V$	-	-	-1	$\mu A$
		$T_J=55^\circ C$	-	-	-5	$\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=-250A$	1	1.5	2	V
$I_{GSS}$	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
$R_{DS(ON)}$	Drain-Source On-state Resistance	$V_{GS}=-10V, I_{DS}=-9.7A$	-	15	20	m $\Omega$
		$V_{GS}=-4.5V, I_{DS}=-7A$	-	20	27	
$R_G$	Gate Resistance	$F=1MHz, V_{GS}=0V, V_{DS}=0V$	-	4	-	$\Omega$
$C_{iss}$	Input Capacitance	$V_{GS}=0V, V_{DS}=-15V,$ Frequency=1.0MHz	-	1040	-	pF
$C_{oss}$	Output Capacitance		-	180	-	
$C_{rss}$	Reverse transfer capacitance		-	125	-	
$t_{d(ON)}$	Turn-on delay Time	$V_{GEN}=-10V, V_{DD}=-15V, R_G=3\Omega,$ $RL=1.5\Omega$	-	10	-	nS
$t_r$	Turn-on rise Time		-	5.5	-	
$t_{d(OFF)}$	Turn-off delay Time		-	26	-	
$t_f$	Turn-off rise Time		-	9	-	
$Q_g$	Total Gate Charge	$V_{DS}=-15V, V_{GS}=-10V, I_{DS}=-$ $9.7A$	-	19	-	nC
$Q_g$	Total Gate Charge		-	9.6	-	
$Q_{gs}$	Gate-Source Charge		-	3.6	-	
$Q_{gd}$	Gate-Drain Charge		-	4.6	-	
$V_{SD}$	Diode Forward Voltage	$I_{SD}=-1A, V_{GS}=0V$	-	-0.75	-1.1	V
$t_{rr}$	Reverse Recovery Time	$I_{DS}=-9.7A,$ $dI_{SD}/dt=500A/\mu s$	-	11.5	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	25	-	nC

N-Channl TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

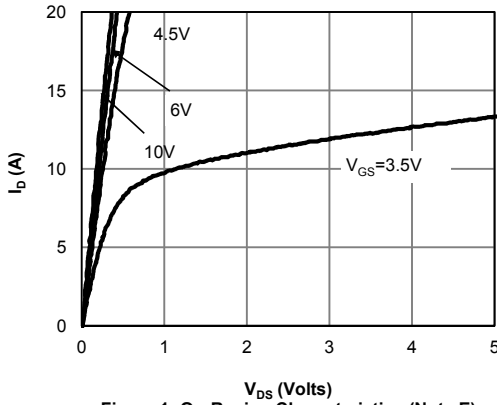


Figure 1: On-Region Characteristics (Note E)

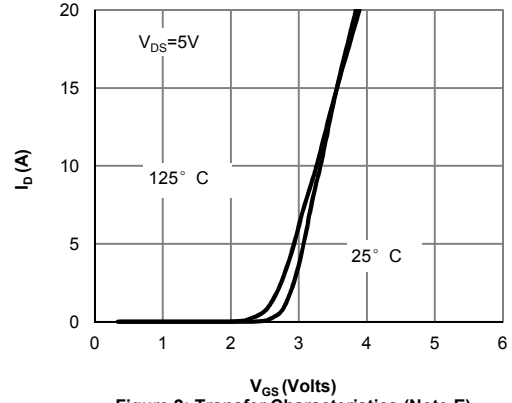


Figure 2: Transfer Characteristics (Note E)

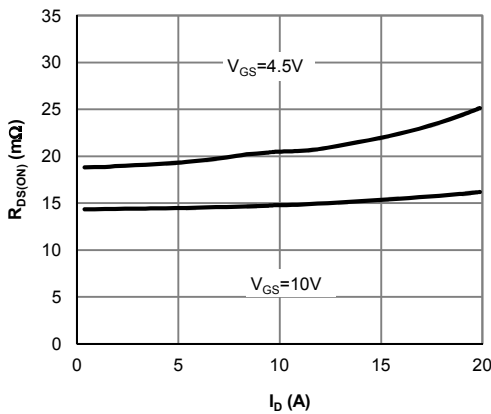


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

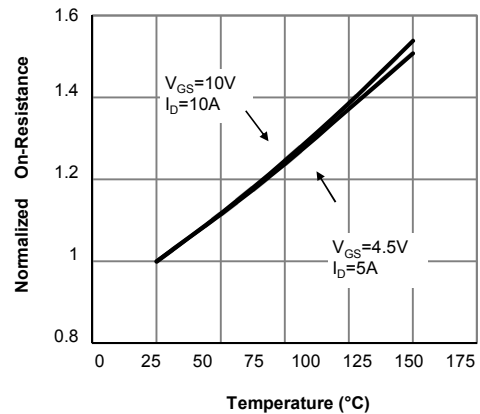


Figure 4: On-Resistance vs. Junction Temperature (Note E)

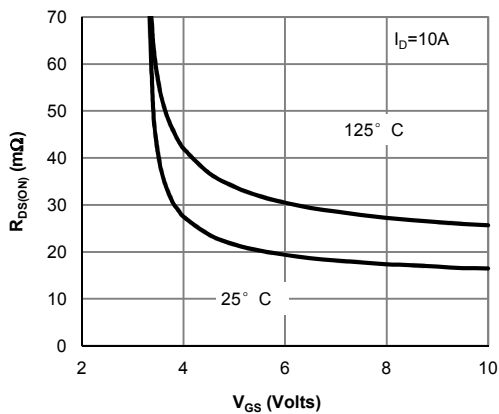


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

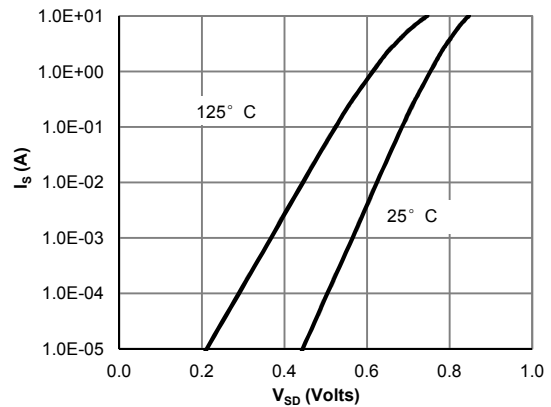


Figure 6: Body-Diode Characteristics (Note E)

N-Channl TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

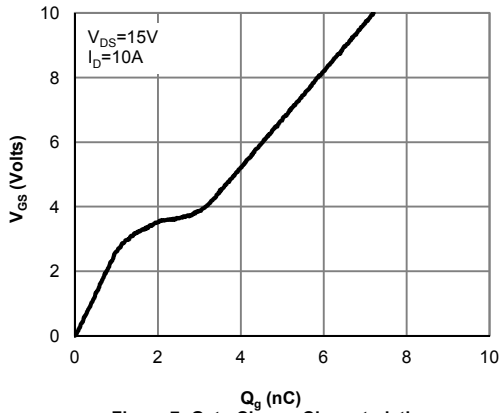


Figure 7: Gate-Charge Characteristics

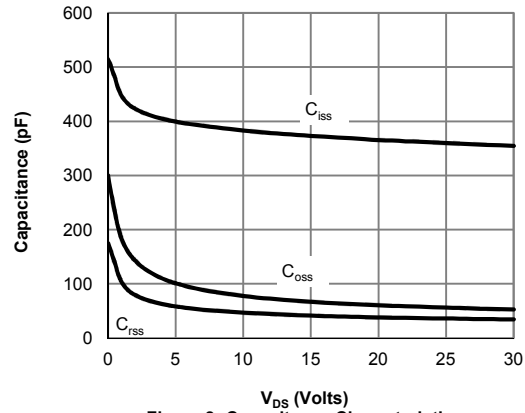


Figure 8: Capacitance Characteristics

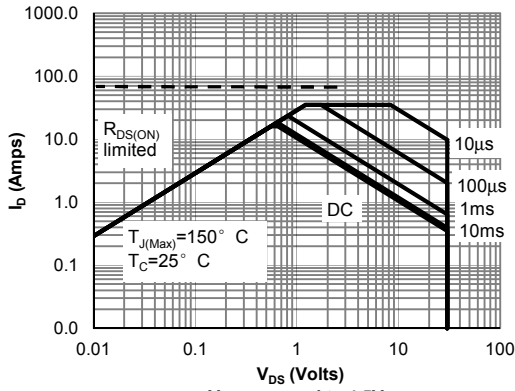


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

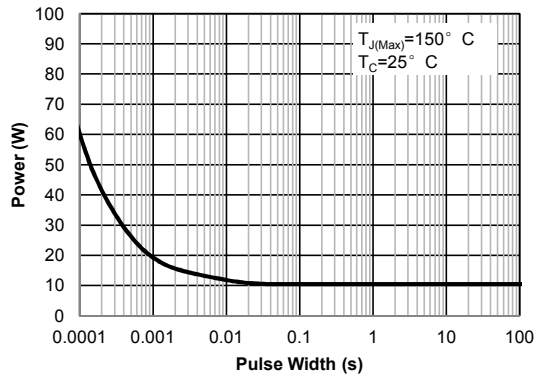


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

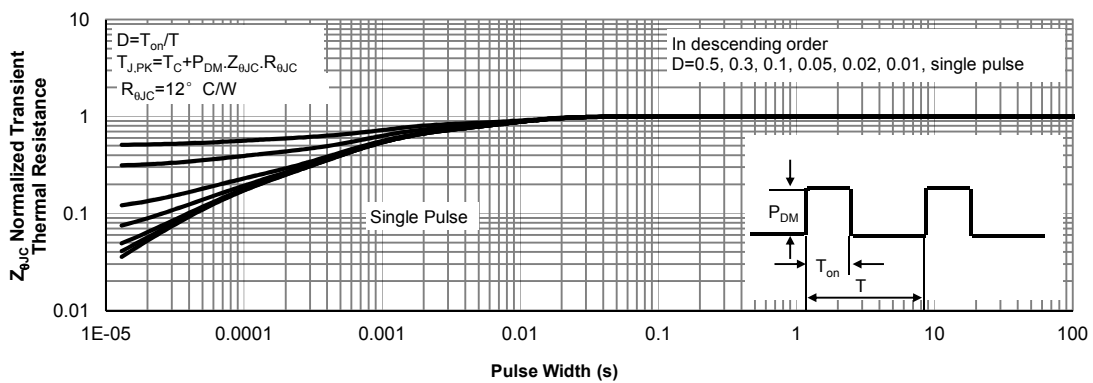


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

**N-Channl TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

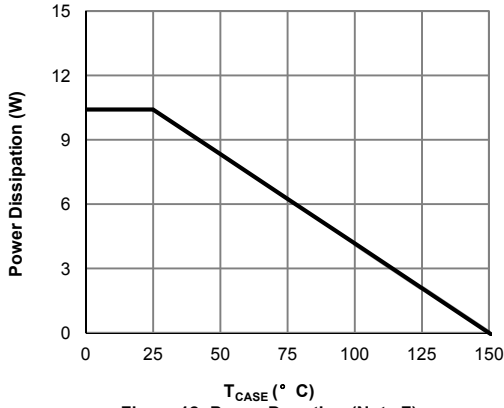


Figure 12: Power De-rating (Note F)

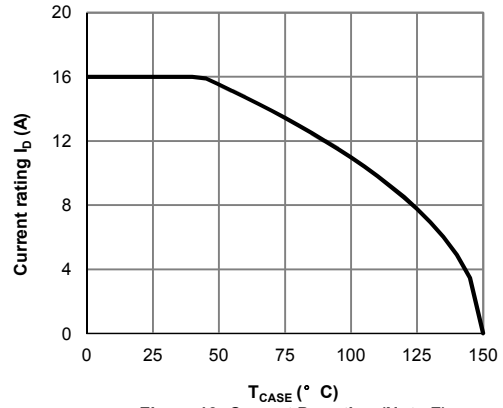


Figure 13: Current De-rating (Note F)

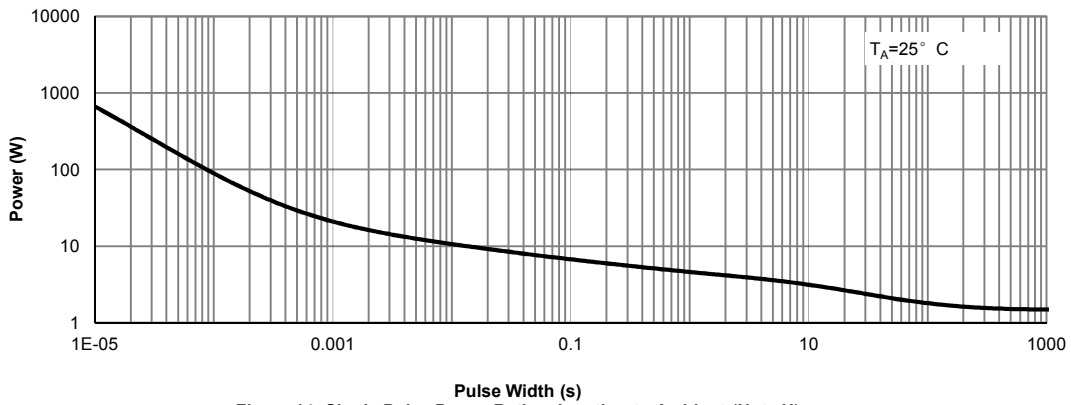


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

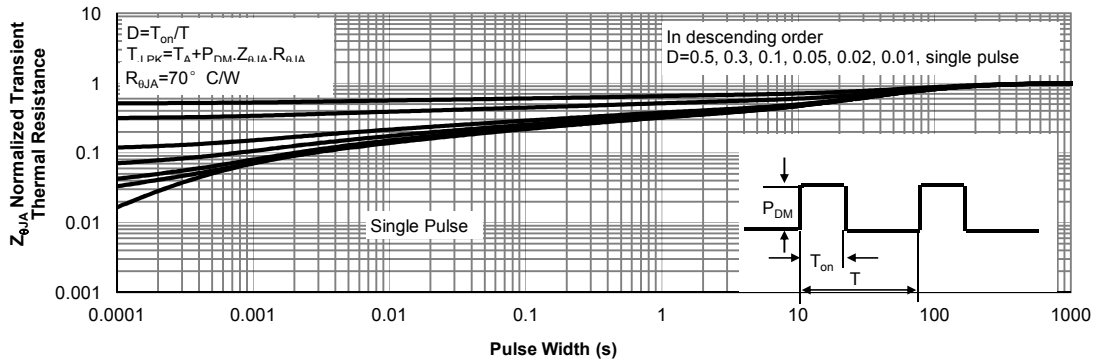


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

**P-Channl TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

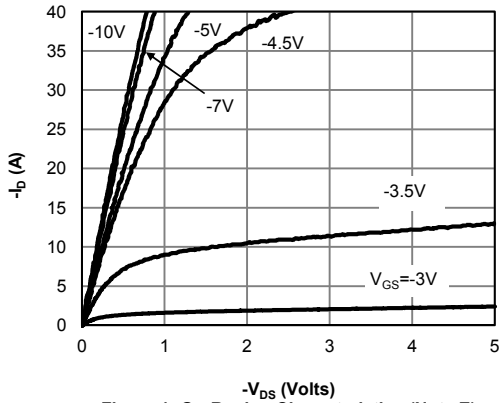


Figure 1: On-Region Characteristics (Note E)

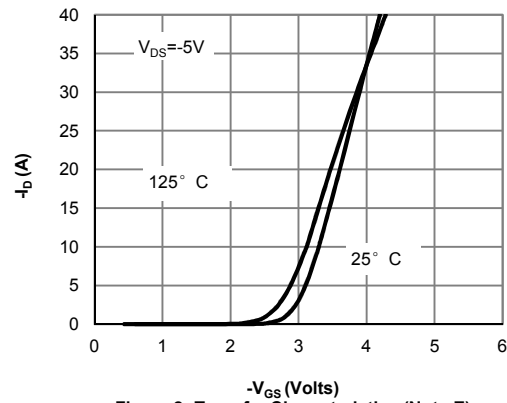


Figure 2: Transfer Characteristics (Note E)

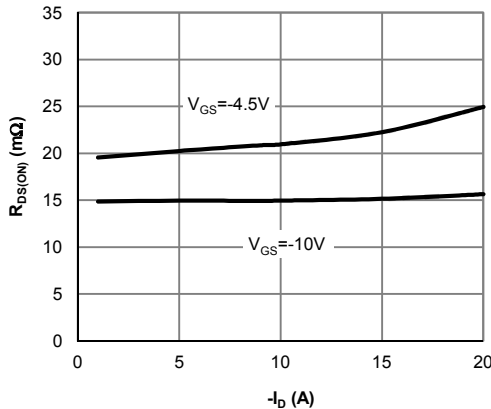


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

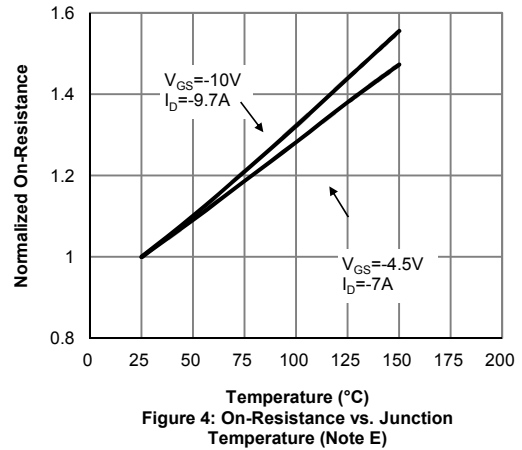


Figure 4: On-Resistance vs. Junction Temperature (Note E)

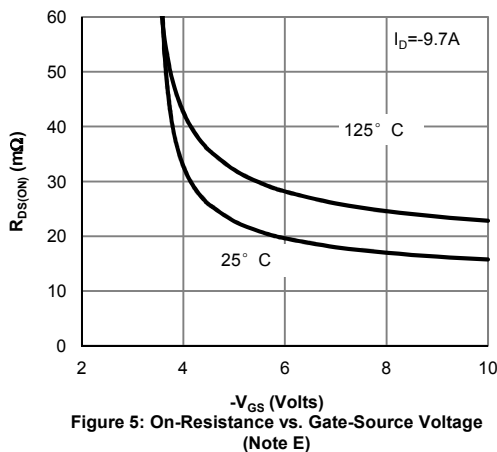


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

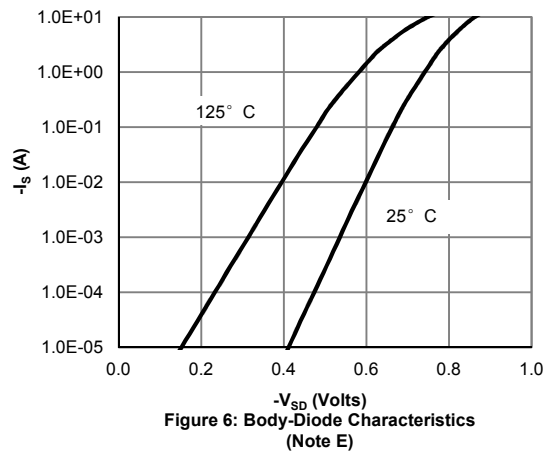


Figure 6: Body-Diode Characteristics (Note E)

**P-Channl TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

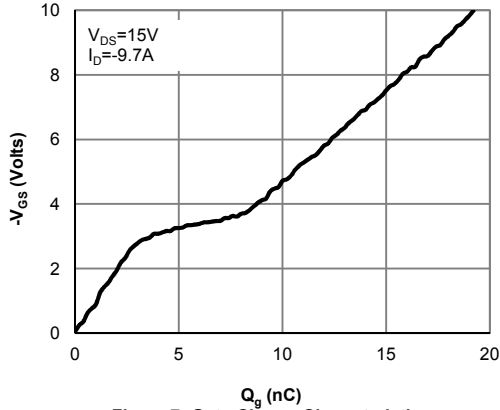


Figure 7: Gate-Charge Characteristics

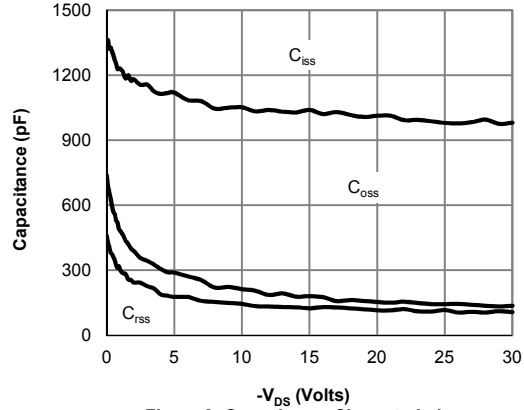


Figure 8: Capacitance Characteristics

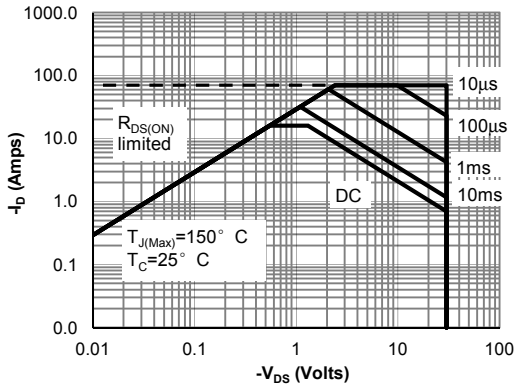


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

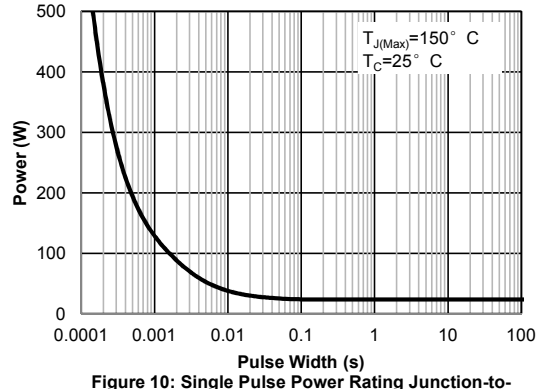


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

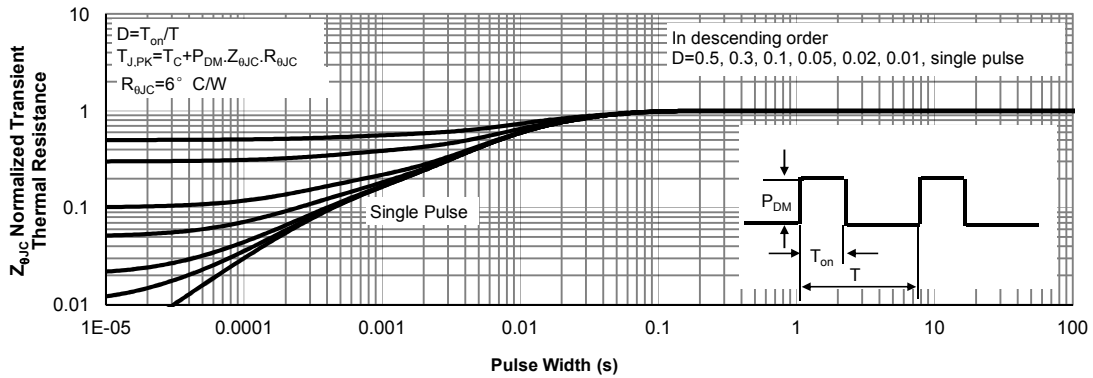


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



P-Channl TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

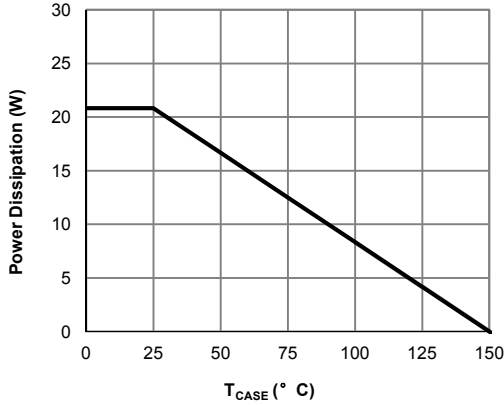


Figure 12: Power De-rating (Note F)

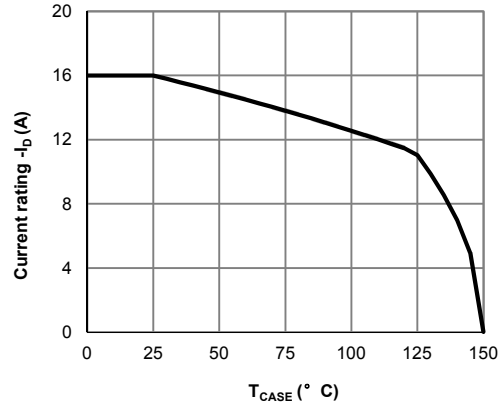


Figure 13: Current De-rating (Note F)

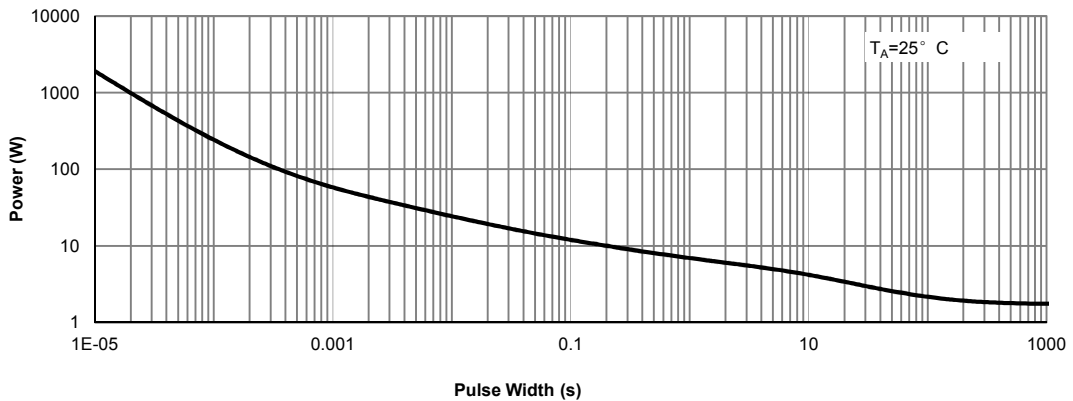


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

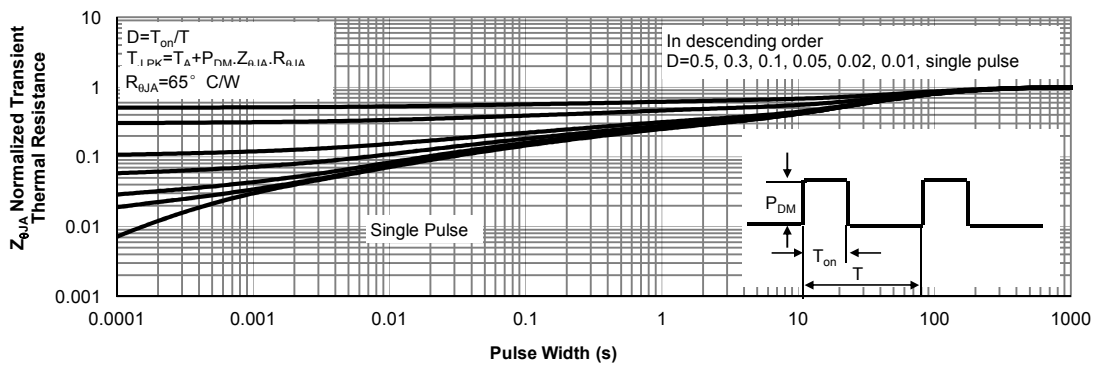


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)



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