

General Description

The WSD6056DN56 is the highest performance trench Dual N-Ch MOSFET with extreme high cell density, which provide excellent R_{DS(on)} and gate charge for most of the synchronous buck converter applications.

The WSD6056DN56 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

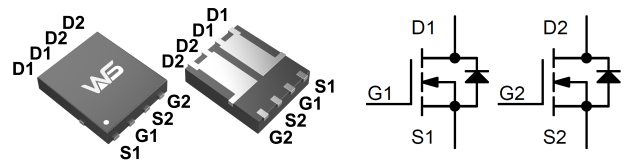
Product Summary

BVDSS	R _{DS(on)}	I _D
60V	16mΩ	45A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Fast switching
- Load Switch

DFN5X6C-8-EP2 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit	
Common Ratings				
V _{DSS}	Drain-Source Voltage	60	V	
V _{GSS}	Gate-Source Voltage	±20	V	
T _J	Maximum Junction Temperature	150	°C	
T _{STG}	Storage Temperature Range	-55 to 150	°C	
I _S	Diode Continuous Forward Current	T _c =25°C	45	A
I _D	Continuous Drain Current	T _c =25°C	45	A
		T _c =70°C	28.5	
I _{DM} ^b	Pulse Drain Current Tested	T _c =25°C	180	A
P _D	Maximum Power Dissipation	T _c =25°C	67	W
		T _c =70°C	45	
R _{θJL}	Thermal Resistance-Junction to Lead	Steady State	5	°C/W
R _{θJA}	Thermal Resistance-Junction to Ambient	t ≤ 10s	45	°C/W
		Steady State ^b	90	
I _{AS} ^d	Avalanche Current, Single pulse	L=0.5mH	20	A
E _{AS} ^d	Avalanche Energy, Single pulse	L=0.5mH	20	mJ

Note a : Max. continuous current is limited by bonding wire.

Note b : Pulse width limited by max. junction temperature.

Note c : Surface mounted on 1in² pad area, steady state t = 999s.

Note d : UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature T_J=25°C).

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	60	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V T _J =85°C	-	-	1	μA
			-	-	30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	1.2	1.5	2.5	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ³	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =20A	-	16	20	mΩ
		V _{GS} =4.5V, I _{DS} =15A	-	20	25	
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} =1A, V _{GS} =0V	-	0.75	1.2	V
t _{rr}	Reverse Recovery Time	I _{SD} =20A, dI _{SD} /dt=100A/μs	-	26	-	ns
Q _{rr}	Reverse Recovery Charge		-	30	-	nC
Dynamic Characteristics ^{3,4}						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz	-	0.9	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, F=1.0MHz	-	945	-	pF
C _{oss}	Output Capacitance		-	275	-	
C _{rss}	Reverse Transfer Capacitance		-	26	-	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =30V, I _{DS} =1A, V _{GEN} =10V, R _G =3.3Ω.	-	10	-	ns
t _r	Turn-on Rise Time		-	13.5	-	
t _{d(OFF)}	Turn-off Delay Time		-	28	-	
t _f	Turn-off Fall Time		-	20	-	
Gate Charge Characteristics ^{3,4}						
Q _g	Total Gate Charge	V _{DS} =30V, V _{GS} =10V, I _{DS} =20A	-	28	-	nC
Q _g	Total Gate Charge	V _{DS} =30V, V _{GS} =10V, I _{DS} =20A	-	17.6	-	
Q _{gth}	Threshold Gate Charge		-	3.5	-	
Q _{gs}	Gate-Source Charge		-	2.7	-	
Q _{gd}	Gate-Drain Charge		-	6.3	-	

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=48V, V_{GS}=10V, L=0.1mH, I_{AS}=20A., R_G=25Ω Starting T_J=25
3. The data tested by pulsed , pulse width<=300us , duty cycle<=2%.
4. Essentially independent of operating temperature.

Typical Operating Characteristics

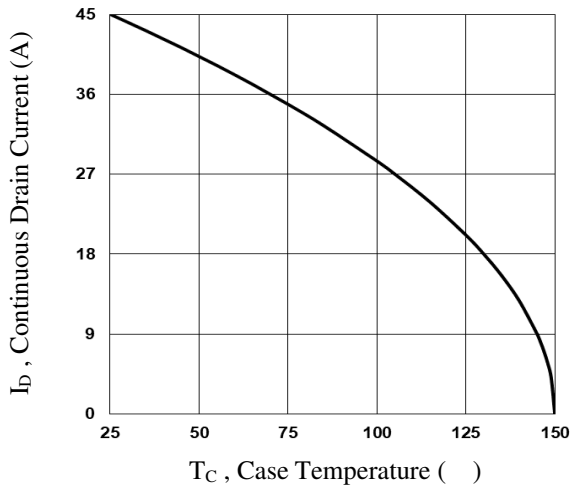


Fig.1 Continuous Drain Current vs. T_c

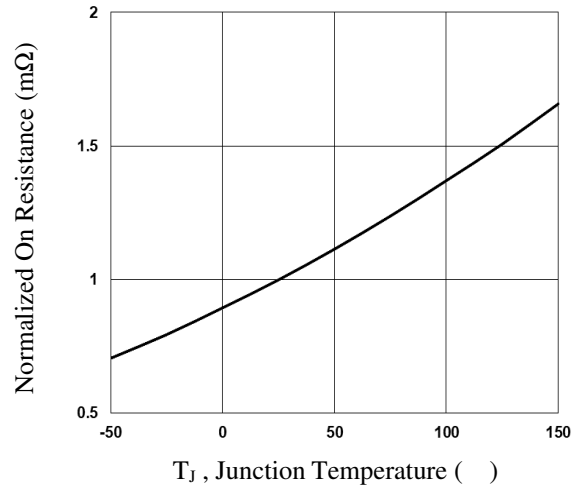


Fig.2 Normalized $R_{DS(on)}$ vs. T_j

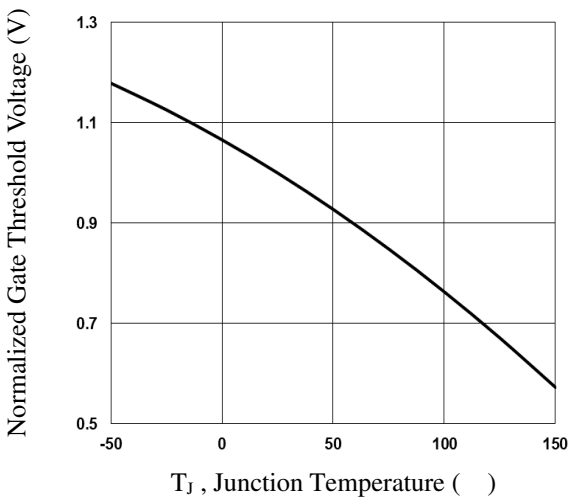


Fig.3 Normalized V_{th} vs. T_j

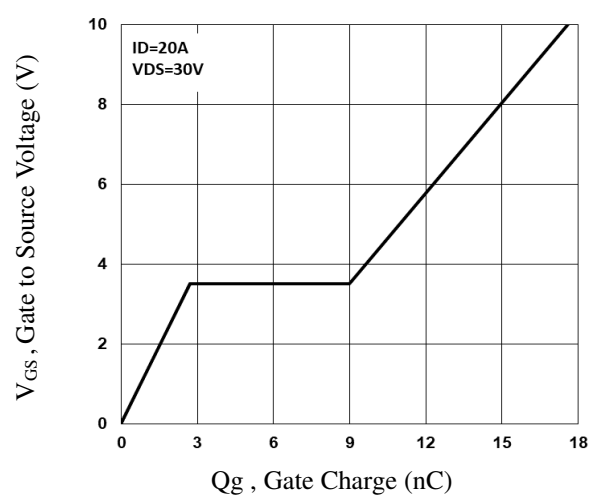


Fig.4 Gate Charge Waveform

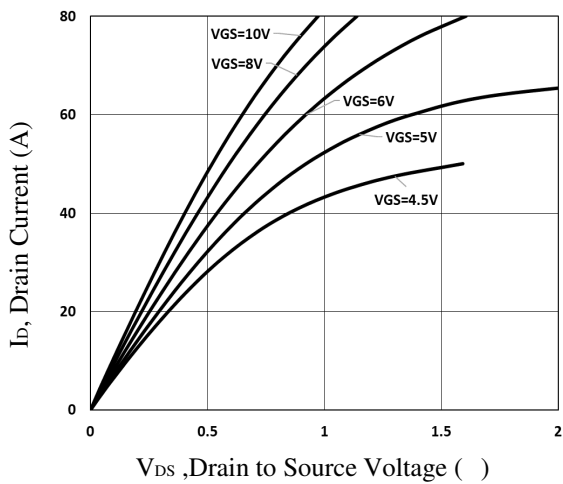


Fig.5 Typical Output Characteristics

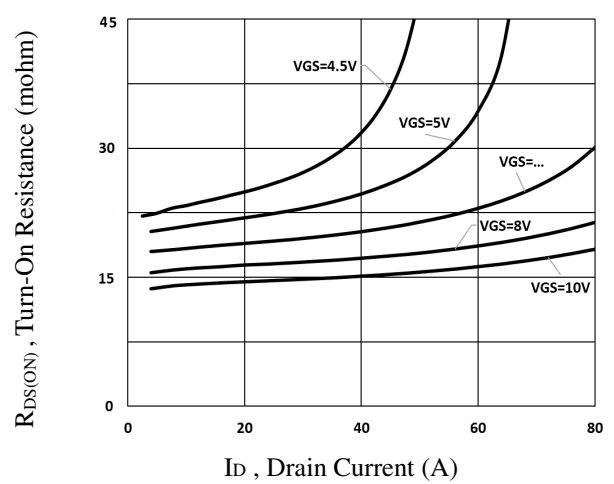


Fig.6 Turn-On Resistance vs. I_D

Typical Operating Characteristics(Cont.)

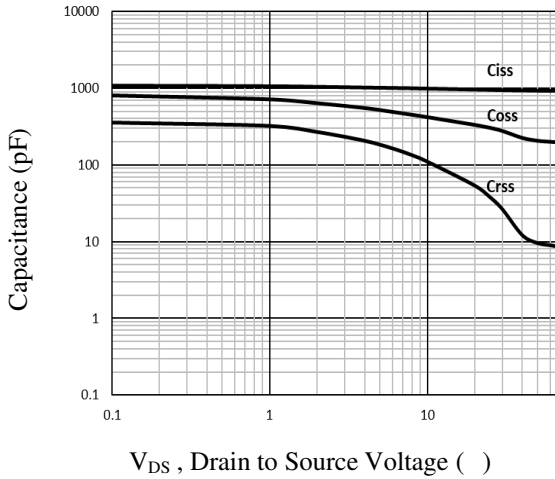


Fig.7 Capacitance Characteristics

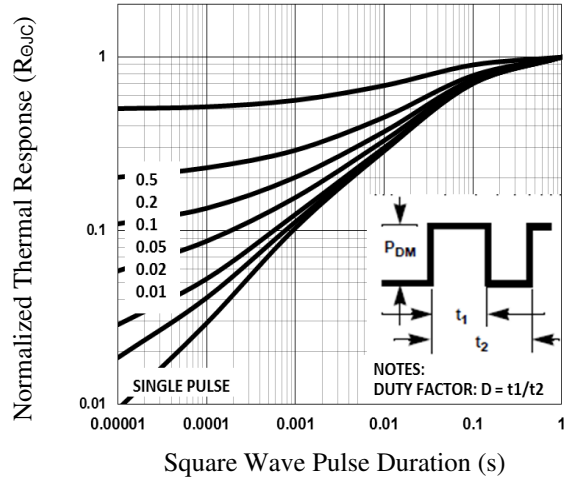


Fig.8 Normalized Transient Response

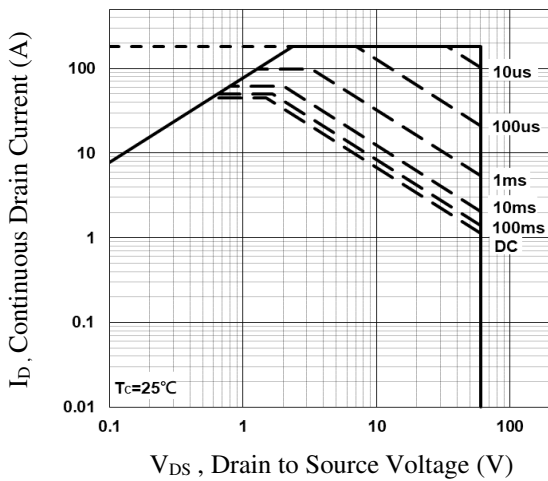


Fig.9 Maximum Safe Operation Area

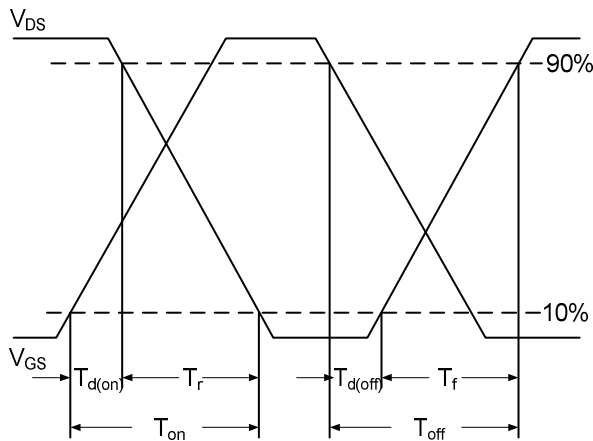


Fig.10 Switching Time Waveform

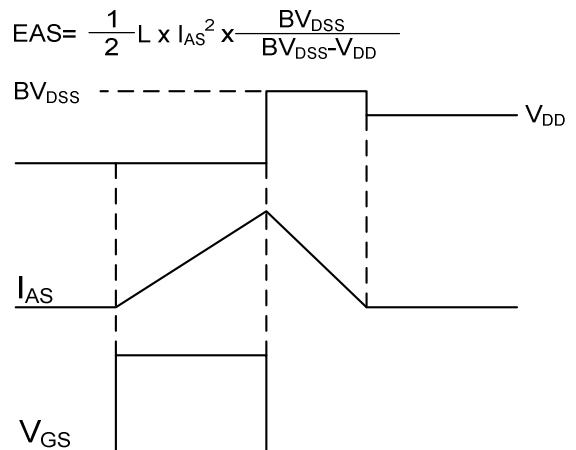


Fig.11 EAS Waveform



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