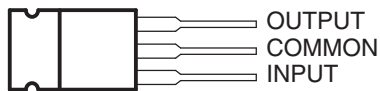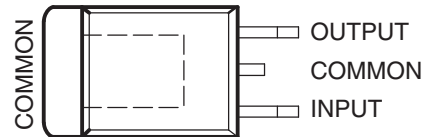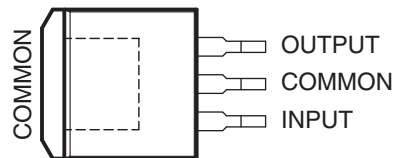# LOW-DROPOUT VOLTAGE REGULATORS

Check for Samples: TL750M SERIES

FEATURES

- **Low Dropout Voltage, Less Than 0.6 V at 750 mA**
- **Low Quiescent Current**
- **60-V Load-Dump Protection**
- **Overvoltage Protection**
- **Internal Thermal-Overload Protection**
- **Internal Overcurrent-Limiting Circuitry**

KCS PACKAGE[1]
(TOP VIEW)

OUTPUT
COMMON
INPUT

KVU PACKAGE[1]
(TOP VIEW)

COMMON

OUTPUT
COMMON
INPUT

KTT PACKAGE[1]
(TOP VIEW)

COMMON

OUTPUT
COMMON
INPUT

(1) The common terminal is in electrical contact with the mounting base.

DESCRIPTION/ORDERING INFORMATION

The TL750M series devices are low-dropout positive voltage regulators specifically designed for battery-powered systems. The TL750M devices incorporate onboard overvoltage and current-limiting protection circuitry to protect the devices and the regulated system. The devices are fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current, even during full-load conditions, makes the TL750M series ideal for standby power systems.

The TL750M offers 5-V, 8-V, 10-V, and 12-V options. The devices are characterized for operation over the virtual junction temperature range 0°C to 125°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION[1]

T_J	V_O TYP	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	5 V	PowerFLEX™ – KVU	Reel of 3000	TL750M05CKVUR	750M05C
		TO-220 – KCS	Tube of 50	TL750M05CKCS	TL750M05C
		TO-263 – KTT	Reel of 500	TL750M05CKTTR	TL750M05C
	8 V	TO-220 – KCS	Tube of 50	TL750M08CKCS	TL750M08C
		PowerFLEX – KVU	Reel of 3000	TL750M08CKVUR	750M08C
	10 V	TO-220 – KCS	Tube of 50	TL750M10CKCS	TL750M10C
		PowerFLEX – KVU	Reel of 3000	TL750M10CKVUR	750M10C
	12 V	TO-220 – KCS	Tube of 50	TL750M12CKCS	TL750M12C
		PowerFLEX – KVU	Reel of 3000	TL750M12CKVUR	750M12C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM
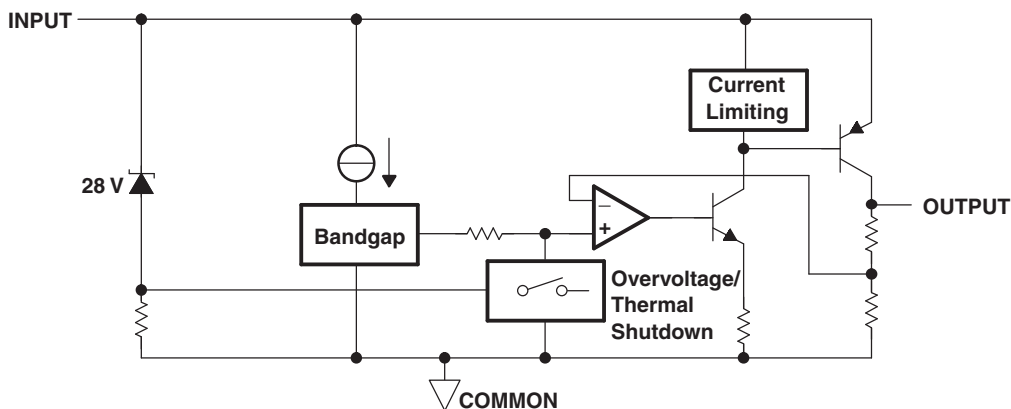
ABSOLUTE MAXIMUM RATINGS[(1)]

over virtual junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Continuous input voltage			26	V
	Transient input voltage (see Figure 3)			60	V
	Continuous reverse input voltage			−15	V
	Transient reverse input voltage	t = 100 ms		−50	V
θ_{JA}	Package thermal impedance [(2)] [(3)]	KCS package		22	°C/W
		KTT package		25.3	
		KVU package		28	
T_J	Virtual-junction temperature range		0	150	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal-overload protection may be activated at power levels slightly above or below the rated dissipation.
(3) The package thermal impedance is calculated in accordance with JESD 51.

THERMAL INFORMATION

THERMAL METRIC[(1)][(2)]		TL750M			UNITS
		KCS (3 PINS)	KVU (3 PINS)	KTT (3 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	28.7	50.9	27.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	59.8	57.9	43.2	
θ_{JB}	Junction-to-board thermal resistance	0.5	34.8	17.3	
ψ_{JT}	Junction-to-top characterization parameter	5.3	6	2.8	
ψ_{JB}	Junction-to-board characterization parameter	0.4	23.7	9.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.1	0.4	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_I	Input voltage	TL750M05	6	26	V
		TL750M08	9	26	
		TL750M10	11	26	
		TL750M12	13	26	
I_O	Output current			750	mA
T_J	Operating virtual-junction temperature		0	125	°C

TL750M05 ELECTRICAL CHARACTERISTICS[1]

V_I = 14 V, I_O = 300 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750M05			UNIT
		MIN	TYP	MAX	
Output voltage		4.95	5	5.05	V
	T_J = 0°C to 125°C	4.9		5.1	
Input voltage regulation	V_I = 9 V to 16 V, I_O = 250 mA		10	25	mV
	V_I = 6 V to 26 V, I_O = 250 mA		12	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	50	55		dB
Output regulation voltage	I_O = 5 mA to 750 mA		20	50	mV
Dropout voltage	I_O = 500 mA			0.5	V
	I_O = 750 mA			0.6	
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Bias current	I_O = 750 mA		60	75	mA
	I_O = 10 mA			5	

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 1.

TL750M08 ELECTRICAL CHARACTERISTICS[1]

V_I = 14 V, I_O = 300 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750M08			UNIT
		MIN	TYP	MAX	
Output voltage		7.92	8	8.08	V
	T_J = 0°C to 125°C	7.84		8.16	
Input voltage regulation	V_I = 10 V to 17 V, I_O = 250 mA		12	40	mV
	V_I = 9 V to 26 V, I_O = 250 mA		15	68	
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz	50	55		dB
Output regulation voltage	I_O = 5 mA to 750 mA		24	80	mV
Dropout voltage	I_O = 500 mA			0.5	V
	I_O = 750 mA			0.6	
Output noise voltage	f = 10 Hz to 100 kHz		500		μV
Bias current	I_O = 750 mA		60	75	mA
	I_O = 10 mA			5	

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 1.

TL750M10 ELECTRICAL CHARACTERISTICS[1]

V_I = 14 V, I_O = 300 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750M10			UNIT
		MIN	TYP	MAX	
Output voltage		9.9	10	10.1	V
	T_J = 0°C to 125°C	9.8		10.2	
Input voltage regulation	V_I = 12 V to 18 V, I_O = 250 mA		15	43	mV
	V_I = 11 V to 26 V, I_O = 250 mA		20	75	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	50	55		dB
Output regulation voltage	I_O = 5 mA to 750 mA		30	100	mV
Dropout voltage	I_O = 500 mA			0.5	V
	I_O = 750 mA			0.6	
Output noise voltage	f = 10 Hz to 100 kHz		1000		μV
Bias current	I_O = 750 mA		60	75	mA
	I_O = 10 mA			5	

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 1.

TL750M12 ELECTRICAL CHARACTERISTICS[1]

V_I = 14 V, I_O = 300 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TL750M12			UNIT
		MIN	TYP	MAX	
Output voltage		11.88	12	12.12	V
	T_J = 0°C to 125°C	11.76		12.24	
Input voltage regulation	V_I = 14 V to 19 V, I_O = 250 mA		15	43	mV
	V_I = 13 V to 26 V, I_O = 250 mA		20	78	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	50	55		dB
Output regulation voltage	I_O = 5 mA to 750 mA		30	120	mV
Dropout voltage	I_O = 500 mA			0.5	V
	I_O = 750 mA			0.6	
Output noise voltage	f = 10 Hz to 100 kHz		1000		μV
Bias current	I_O = 750 mA		60	75	mA
	I_O = 10 mA			5	

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 1.

PARAMETER MEASUREMENT INFORMATION

The TL750Mxx is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figure 1 and Figure 2 can establish the capacitance value and ESR range for the best regulator performance.
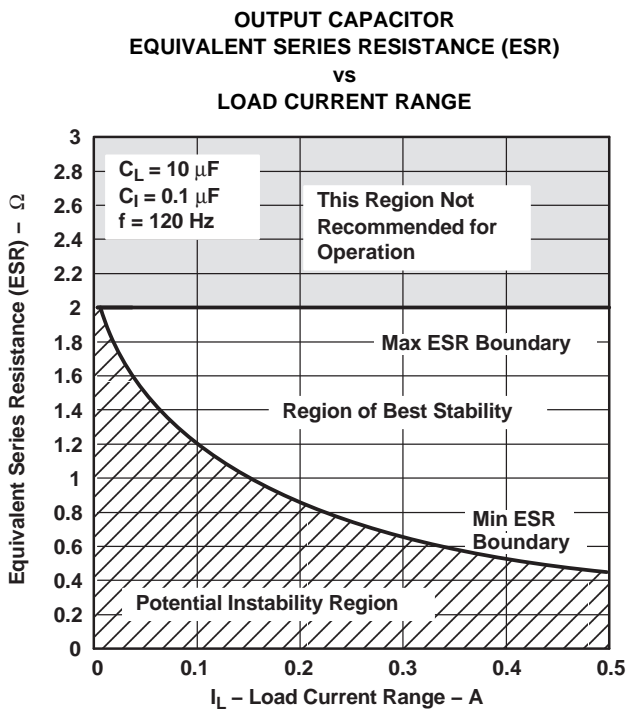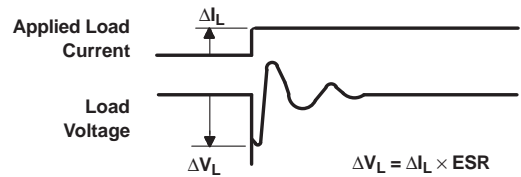
Figure 1 shows the recommended range of ESR for a given load with a 10-μF capacitor on the output. This figure also shows a maximum ESR limit of 2 Ω and a load-dependent minimum ESR limit.

For applications with varying loads, the lightest load condition should be chosen because it is the worst case. Figure 2 shows the relationship of the reciprocal of ESR to the square root of the capacitance with a minimum capacitance limit of 10 μF and a maximum ESR limit of 2 Ω. This figure establishes the amount that the minimum ESR limit shown in Figure 1 can be adjusted for different capacitor values.
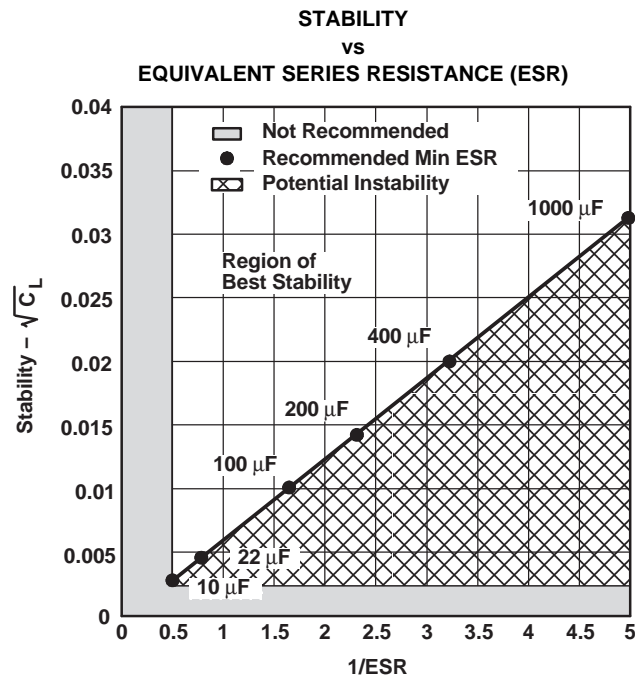
For example, where the minimum load needed is 200 mA, Figure 1 suggests an ESR range of 0.8 Ω to 2 Ω for 10 μF. Figure 2 shows that changing the capacitor from 10 μF to 400 μF can change the ESR minimum by greater than 3/0.5 (or 6). Therefore, the new minimum ESR value is 0.8/6 (or 0.13 Ω). This allows an ESR range of 0.13 Ω to 2 Ω , achieving an expanded ESR range by using a larger capacitor at the output. For better stability in low-current applications, a small resistance placed in series with the capacitor (see Table 1) is recommended, so that ESRs better approximate those shown in Figure 1 and Figure 2.

Table 1. Compensation for Increased Stability at Low Currents

MANUFACTURER	CAPACITANCE	ESR TYP	PART NUMBER	ADDITIONAL RESISTANCE		
AVX	15 μF	0.9 Ω	TAJB156M010S	1 Ω	Applied Load Current	ΔI_L
KEMET	33 μF	0.6 Ω	T491D336M010AS	0.5 Ω	Load Voltage	ΔV_L $\Delta V_L = \Delta I_L \times ESR$

OUTPUT CAPACITOR
EQUIVALENT SERIES RESISTANCE (ESR)
vs
LOAD CURRENT RANGE

Figure 1.

STABILITY
vs
EQUIVALENT SERIES RESISTANCE (ESR)

Figure 2.

TYPICAL CHARACTERISTICS

Table 2. Table of Graphs

		FIGURE
Transient input voltage vs Time		3
Output voltage vs Input voltage		4
Input current vs Input voltage	I_O = 10 mA	5
	I_O = 100 mA	6
Dropout voltage vs Output current		7
Quiescent voltage vs Output current		8
Load transient response		9
Line transient response		10

TRANSIENT INPUT VOLTAGE
vs
TIME
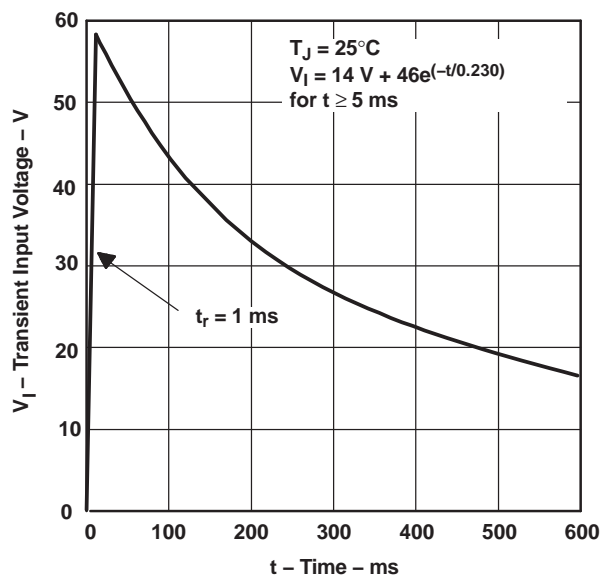
T_J = 25°C
V_I = 14 V + 46e$^{(-t/0.230)}$
for t ≥ 5 ms

t_r = 1 ms

Figure 3.

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

I_O = 10 mA
T_J = 25°C

TL750M12
TL750M10
TL750M08
TL750M05

Figure 4.

INPUT CURRENT
vs
INPUT VOLTAGE

Figure 5.

INPUT CURRENT
vs
INPUT VOLTAGE

Figure 6.

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

Figure 7.

QUIESCENT CURRENT
vs
OUTPUT CURRENT

Figure 8.

LOAD TRANSIENT RESPONSE

Figure 9.

LINE TRANSIENT RESPONSE
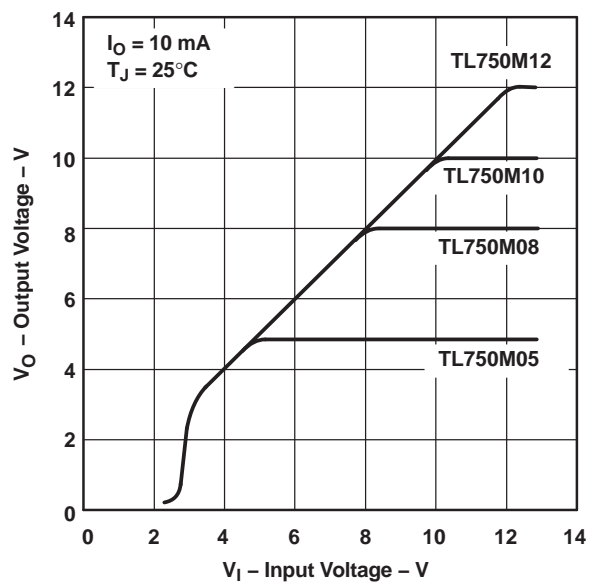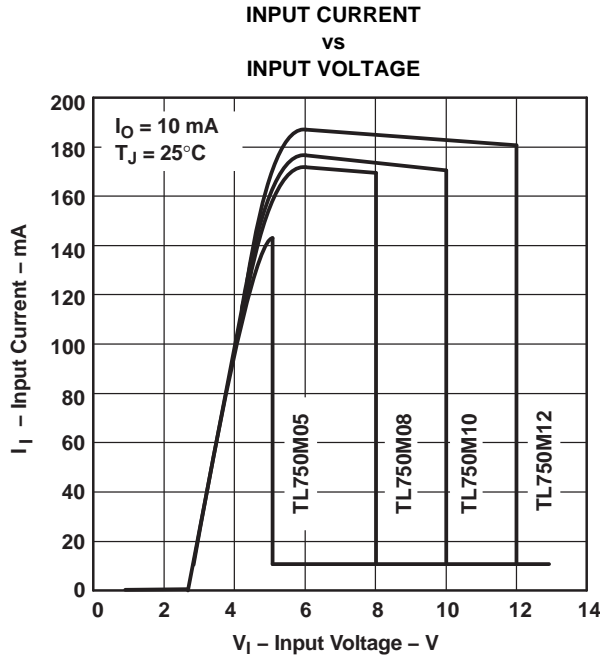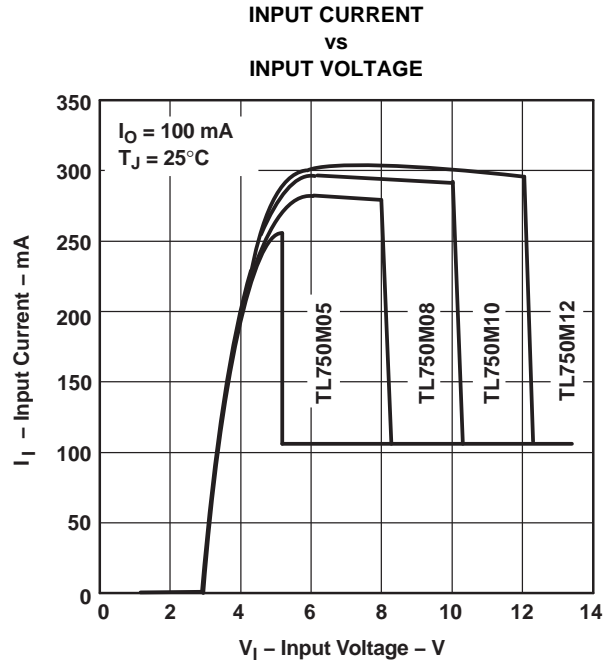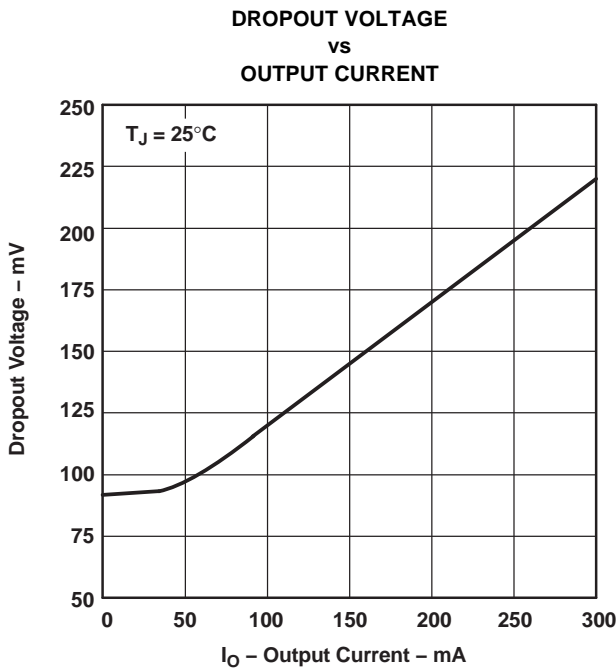
Figure 10.

PACKAGING INFORMATION

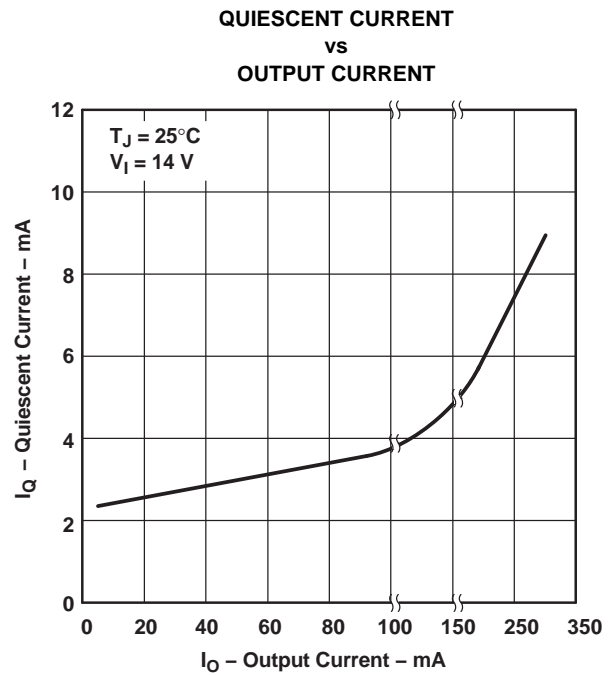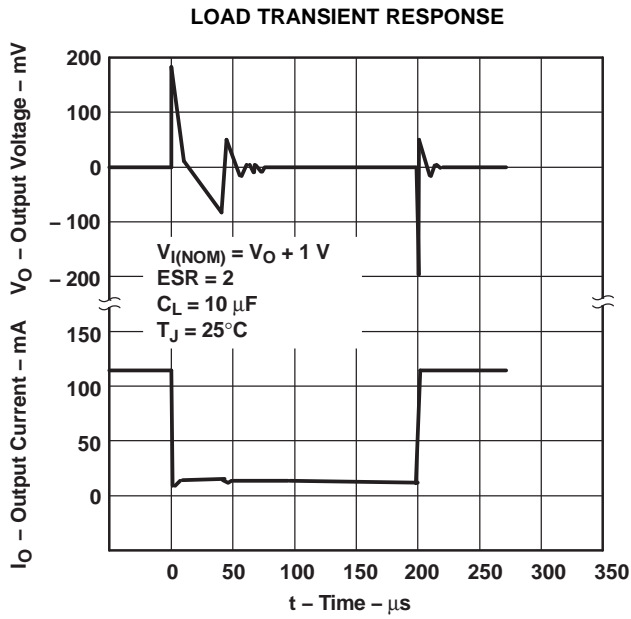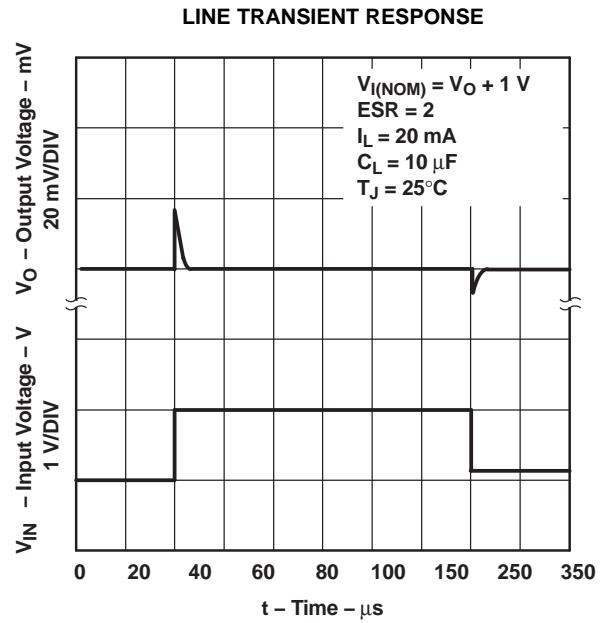| Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL750M05CKCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TL750M05C	Samples
TL750M05CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS & Green	SN	Level-3-245C-168 HR	0 to 125	TL750M05C	Samples
TL750M05CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	50M05C	Samples
TL750M08CKCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TL750M08C	Samples
TL750M08CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	50M08C	Samples
TL750M10CKCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TL750M10C	Samples
TL750M10CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	50M10C	Samples
TL750M12CKCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TL750M12C	Samples
TL750M12CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	50M12C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL750M :

- Automotive: TL750M-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

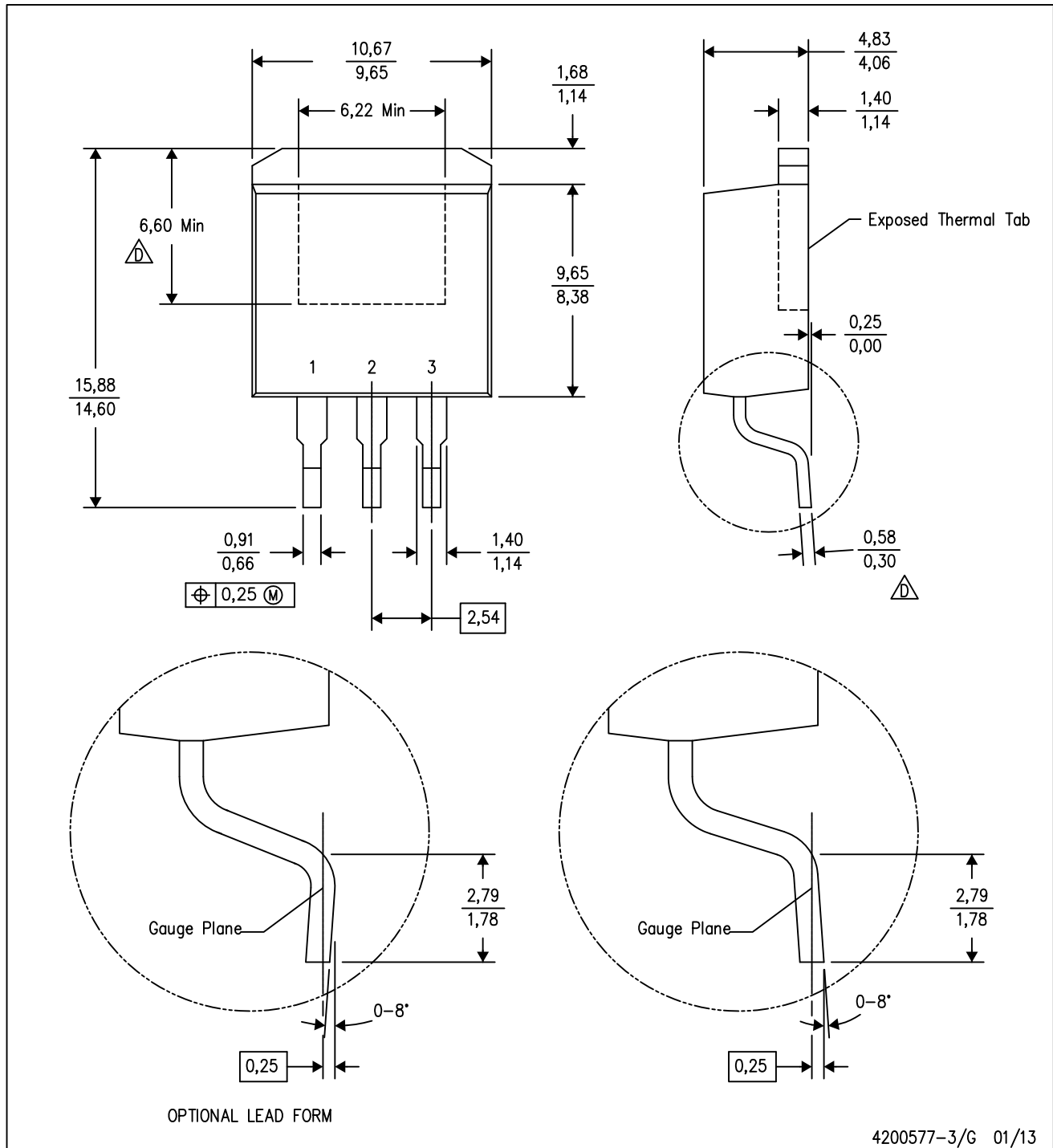| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL750M05CKTTR	DDPAK/TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TL750M05CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750M08CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750M10CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750M12CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL750M05CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TL750M05CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TL750M08CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TL750M10CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TL750M12CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0

KTT (R−PSFM−G3)   PLASTIC FLANGE−MOUNT PACKAGE

10,67
9,65

1,68
1,14

6,22 Min

4,83
4,06

1,40
1,14

6,60 Min

⚠ D

Exposed Thermal Tab

9,65
8,38

15,88
14,60

1   2   3

0,25
0,00

0,91
0,66

1,40
1,14

⊕ | 0,25 Ⓜ

2,54

0,58
0,30

⚠ D

Gauge Plane

2,79
1,78

Gauge Plane

2,79
1,78

0−8°

0−8°

0,25

0,25

OPTIONAL LEAD FORM
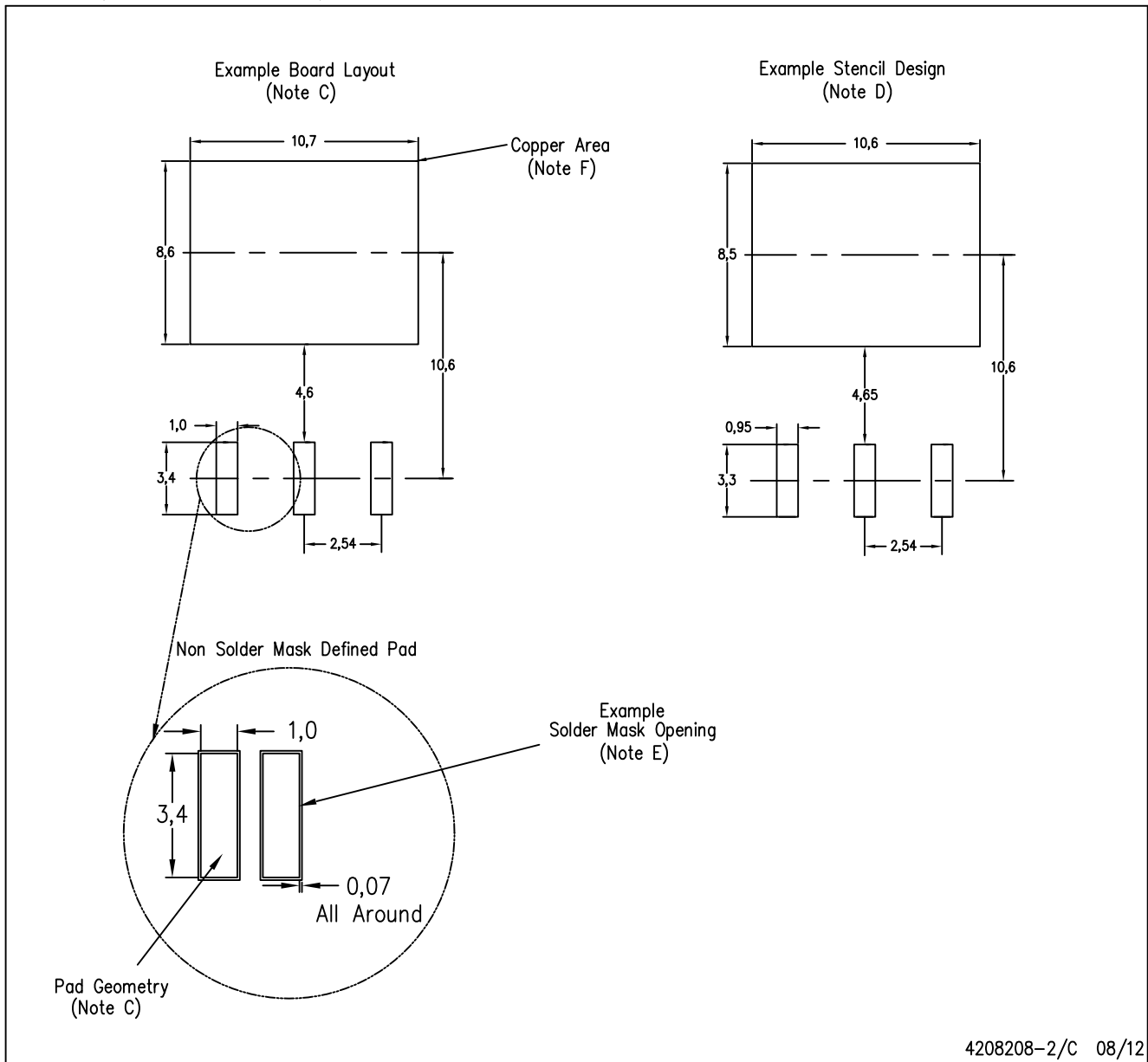
4200577−3/G 01/13

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
         ⚠ D Falls within JEDEC TO−263 variation AA, except minimum lead thickness and minimum exposed pad length.
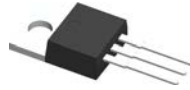
KTT (R−PSFM−G3)   PLASTIC FLANGE−MOUNT PACKAGE

Example Board Layout
(Note C)

10,7

8,6

10,6

Copper Area
(Note F)

4,6

1,0

3,4

2,54

Example Stencil Design
(Note D)

10,6

8,5

10,6

0,95

3,3

4,65

2,54

Non Solder Mask Defined Pad

1,0

3,4

0,07
All Around

Example
Solder Mask Opening
(Note E)

Pad Geometry
(Note C)

4208208−2/C 08/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−SM−782 is recommended for alternate designs.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.
            Customers should contact their board assembly site for stencil design recommendations. Refer to IPC−7525.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around
            signal pads.
        F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet
            for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad
            sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable
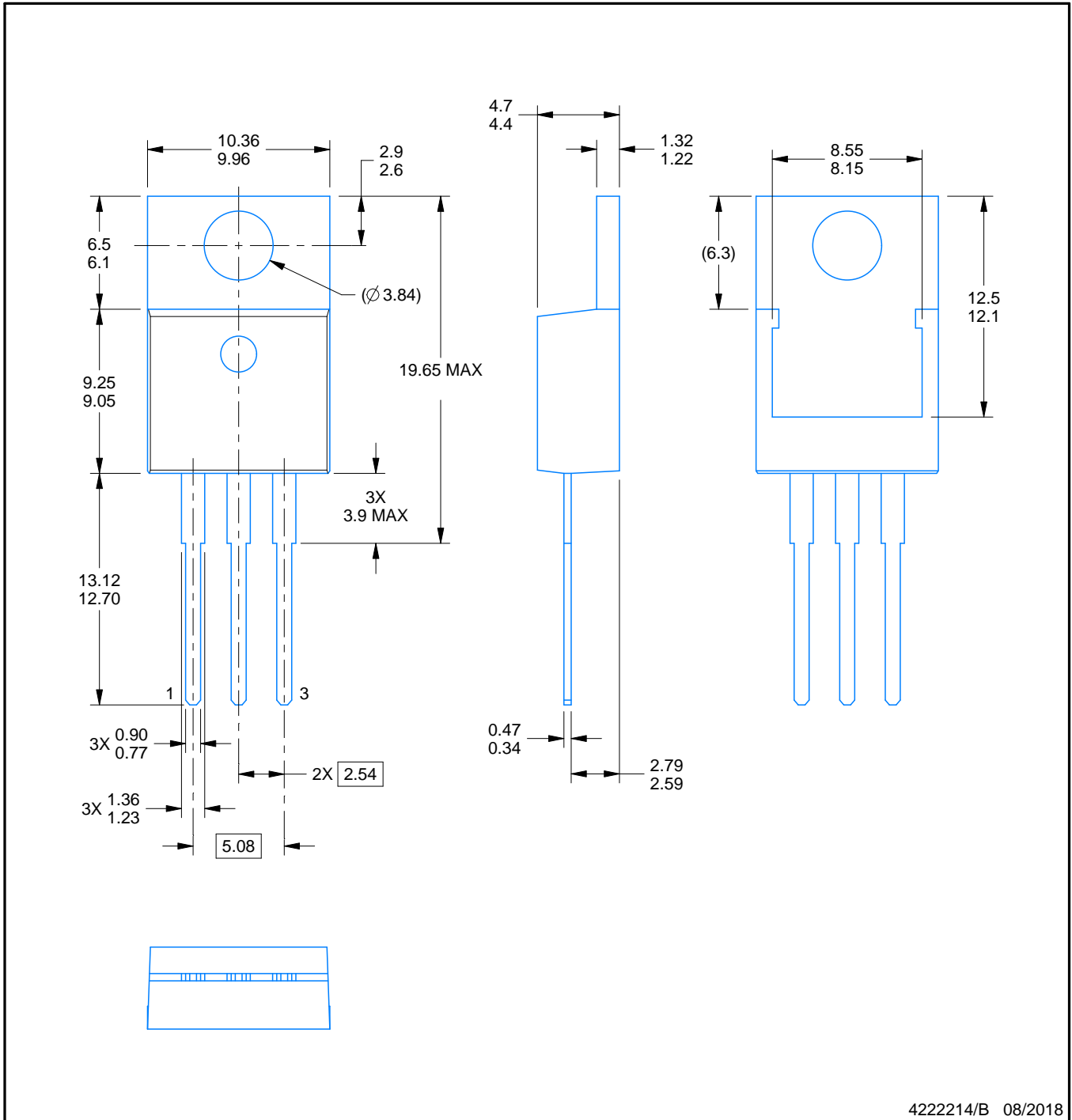   pad geometry while increasing copper area.

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10.36
9.96

2.9
2.6

6.5
6.1

(⌀ 3.84)

9.25
9.05

19.65 MAX

3X
3.9 MAX

13.12
12.70

1   3

3X 0.90
   0.77

2X [2.54]

3X 1.36
   1.23

[5.08]

4.7
4.4

1.32
1.22

0.47
0.34

2.79
2.59

8.55
8.15

(6.3)

12.5
12.1

4222214/B   08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
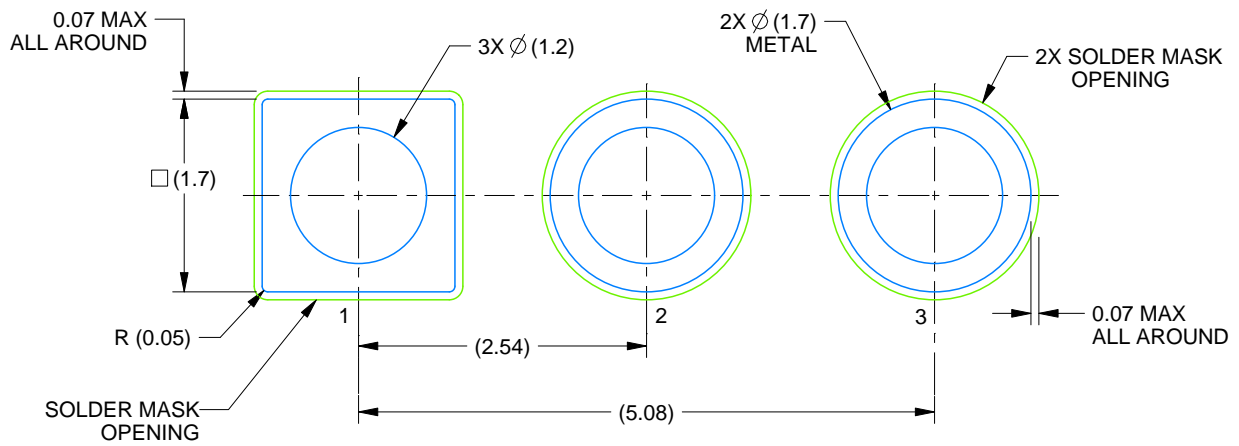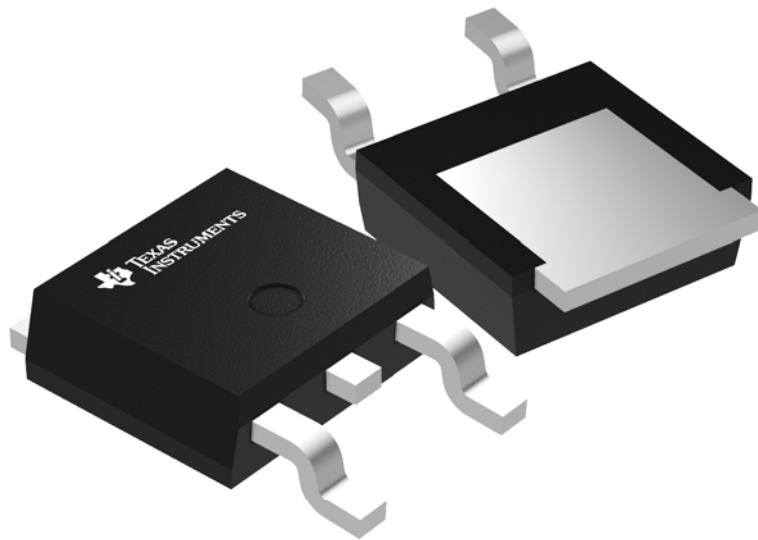3. Reference JEDEC registration TO-220.

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0.07 MAX
ALL AROUND

3X ⌀ (1.2)

2X ⌀ (1.7)
METAL

2X SOLDER MASK
OPENING

☐ (1.7)

R (0.05)

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

1   2   3

(2.54)

(5.08)

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B   08/2018

TRANSISTOR OUTLINE

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4205521-2/E
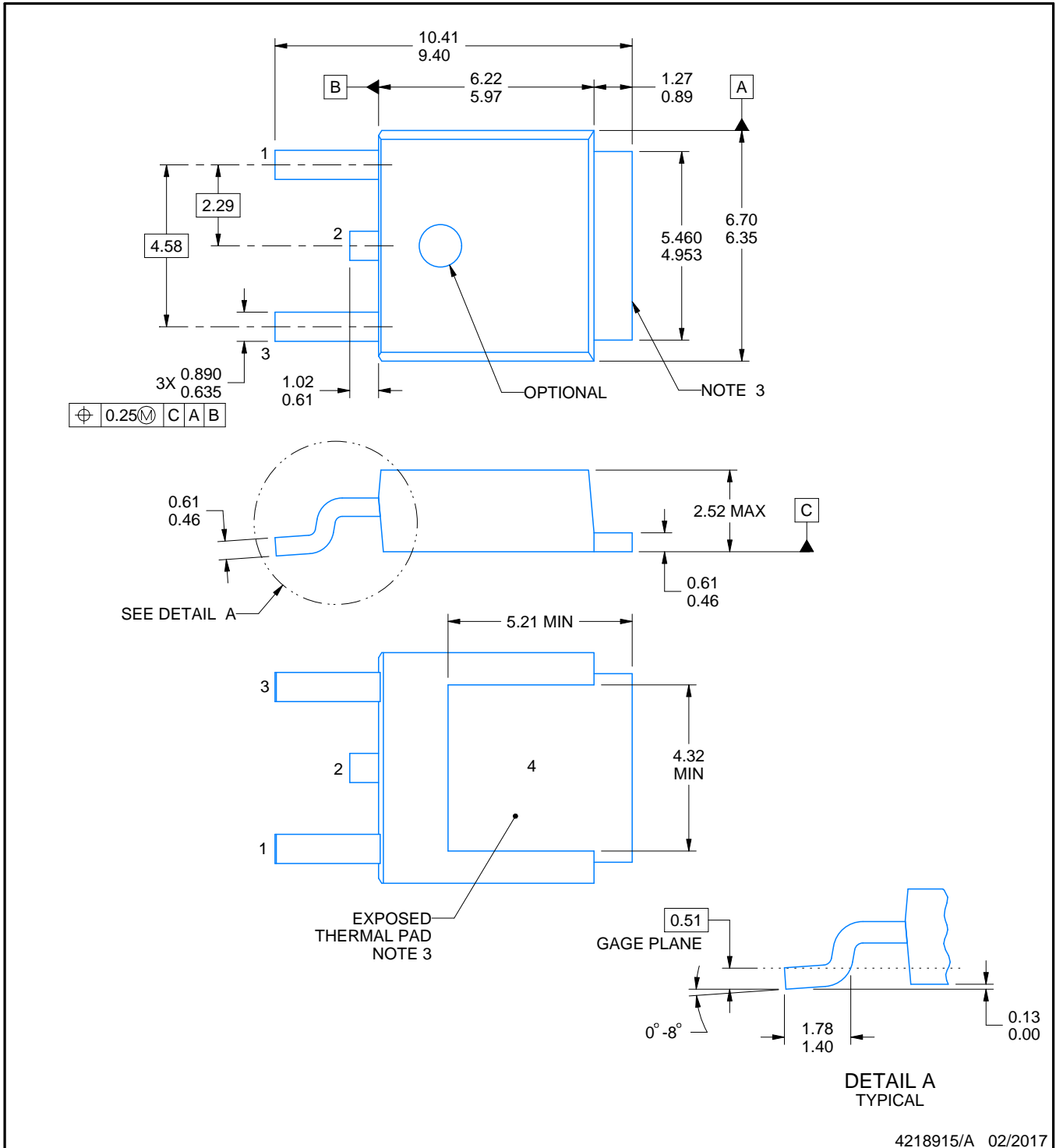
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10.41
9.40

B

6.22
5.97

1.27
0.89

A

1

2.29

4.58

2

2

6.70
6.35

5.460
4.953

3

3X 0.890
0.635

1.02
0.61

OPTIONAL

NOTE 3

⊕ 0.25Ⓜ C A B

0.61
0.46

2.52 MAX

C

0.61
0.46

SEE DETAIL A

5.21 MIN

3

2

4

4.32
MIN

1

EXPOSED
THERMAL PAD
NOTE 3

0.51

GAGE PLANE
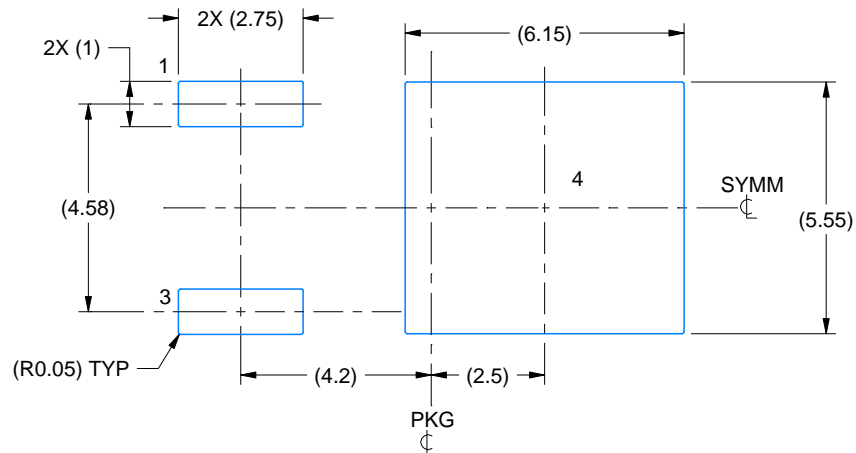
0° -8°

1.78
1.40

0.13
0.00

DETAIL A
TYPICAL

4218915/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
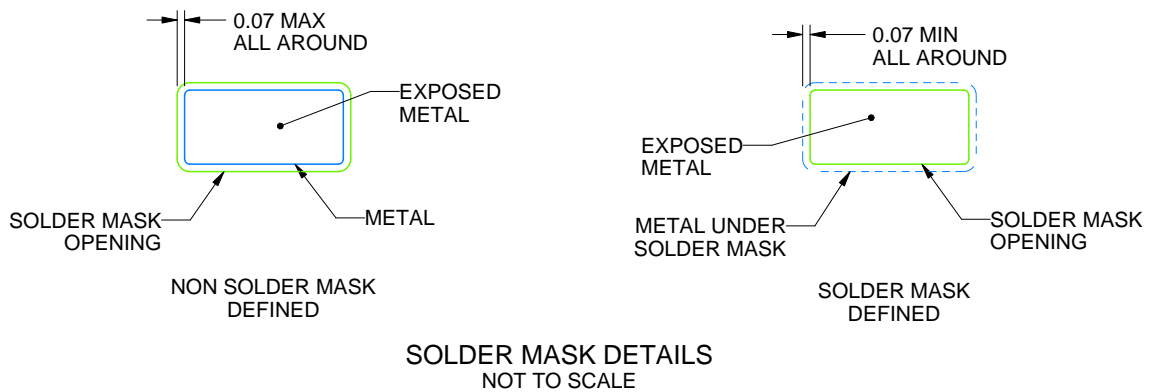4. Reference JEDEC registration TO-252.

2X (2.75)

2X (1)

1

(4.58)

(6.15)

4

SYMM

(5.55)

3

(R0.05) TYP

(4.2)

(2.5)

PKG

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

0.07 MAX
ALL AROUND

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

**NON SOLDER MASK
DEFINED**

0.07 MIN
ALL AROUND

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**

SOLDER MASK DETAILS
NOT TO SCALE

4218915/A   02/2017

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers
SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
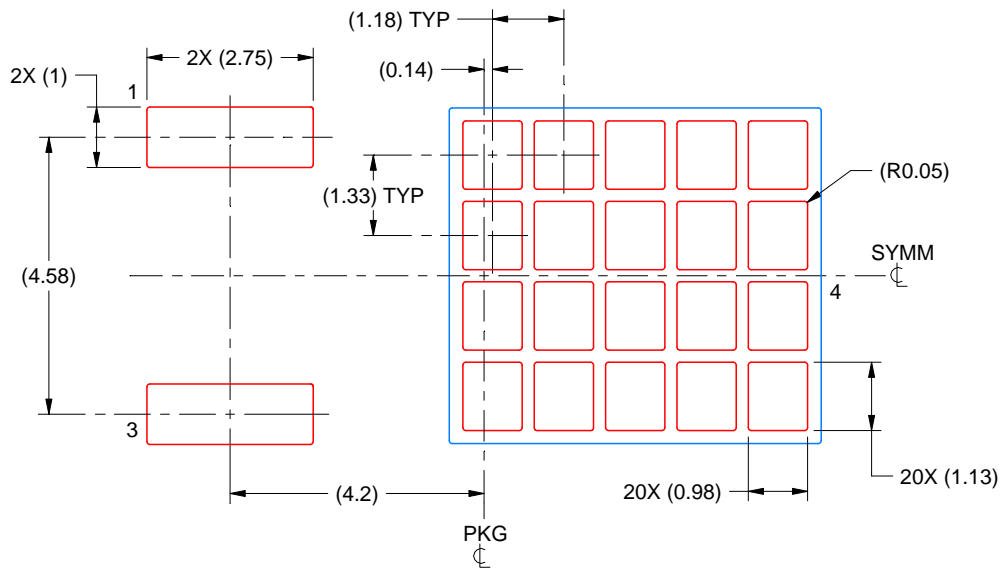
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A   02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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