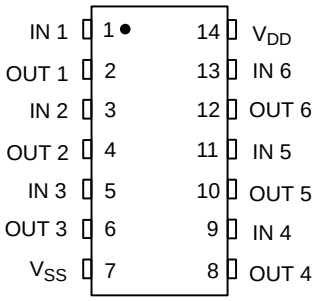
The XD14069 hex inverter is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.



Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs
- Pin−for−Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Packages: –7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

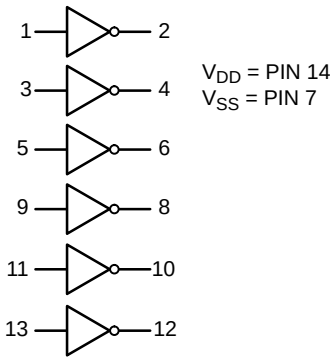
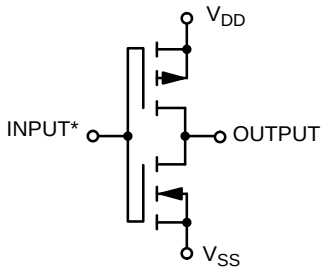


Figure 1. Logic Diagram



*Double diode protection on all inputs not shown

(1/6 of circuit shown)

Figure 2. Circuit Schematic

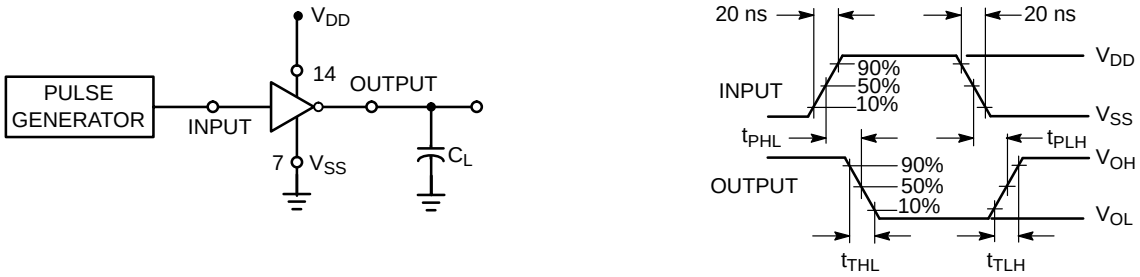


Figure 3. Switching Time Test Circuit and Waveforms

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level	V_{OL}	5.0	−	0.05	−	0	0.05	−	0.05	Vdc
V_{in} = V_{DD}		10	−	0.05	−	0	0.05	−	0.05	
		15	−	0.05	−	0	0.05	−	0.05	
V_{in} = 0 “1” Level	V_{OH}	5.0	4.95	−	4.95	5.0	−	4.95	−	Vdc
		10	9.95	−	9.95	10	−	9.95	−	
		15	14.95	−	14.95	15	−	14.95	−	
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	−	1.0	−	2.25	1.0	−	1.0	
(V_O = 9.0 Vdc)		10	−	2.0	−	4.50	2.0	−	2.0	
(V_O = 13.5 Vdc)		15	−	2.5	−	6.75	2.5	−	2.5	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 Vdc)		5.0	4.0	−	4.0	2.75	−	4.0	−	
(V_O = 1.0 Vdc)		10	8.0	−	8.0	5.50	−	8.0	−	
(V_O = 1.5 Vdc)		15	12.5	−	12.5	8.25	−	12.5	−	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–3.0	−	–2.4	–4.2	−	–1.7	−	
(V_{OH} = 4.6 Vdc)		5.0	–0.64	−	–0.51	–0.88	−	–0.36	−	
(V_{OH} = 9.5 Vdc)		10	–1.6	−	–1.3	–2.25	−	–0.9	−	
(V_{OH} = 13.5 Vdc)		15	–4.2	−	–3.4	–8.8	−	–2.4	−	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	−	0.51	0.88	−	0.36	−	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	−	1.3	2.25	−	0.9	−	
(V_{OL} = 1.5 Vdc)		15	4.2	−	3.4	8.8	−	2.4	−	
Input Current	I_{in}	15	−	±0.1	−	±0.00001	±0.1	−	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current	I_{DD}	5.0	−	0.25	−	0.0005	0.25	−	7.5	μAdc
(Per Package)		10	−	0.5	−	0.0010	0.5	−	15	
		15	−	1.0	−	0.0015	1.0	−	30	
Total Supply Current (Notes 3 and 4)	I_T	5.0	I_T = (0.3 μA/kHz) f + I_{DD}/6							μAdc
(Dynamic plus Quiescent,		10	I_T = (0.6 μA/kHz) f + I_{DD}/6							
Per Gate) (C_L = 50 pF)		15	I_T = (0.9 μA/kHz) f + I_{DD}/6							
Output Rise and Fall Times (Note 3)	t_{TLH},									ns
(C_L = 50 pF)	t_{THL}	5.0	−	−	−	100	200	−	−	
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns		10	−	−	−	50	100	−	−	
t_{TLH}, t_{THL} = (0.60 ns/pF) C_L + 20 ns		15	−	−	−	40	80	−	−	
t_{TLH}, t_{THL} = (0.40 ns/pF) C_L + 20 ns										
Propagation Delay Times (Note 3)	t_{PLH},									ns
(C_L = 50 pF)	t_{PHL}									
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 20 ns		5.0	−	−	−	65	125	−	−	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 22 ns		10	−	−	−	40	75	−	−	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 17 ns		15	−	−	−	30	55	−	−	

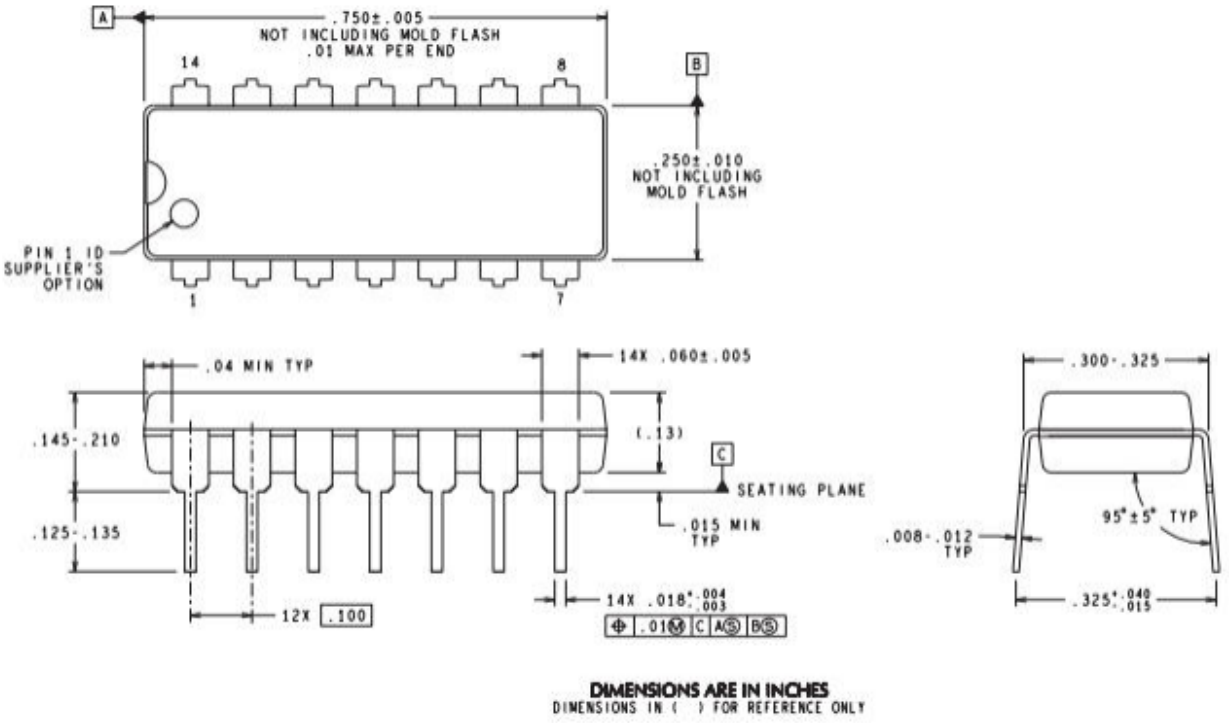
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

DIP14



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA